

74LV4053

Triple single-pole double-throw analog switch

Rev. 9 — 2 April 2024

Product data sheet

1. General description

The 74LV4053 is a triple single-pole double-throw (SPDT) analog switch, suitable for use in 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input (S_n), two independent inputs/outputs (Y_0 and Y_1) and a common input/output (Z). A digital enable input (E) is common to all switches. When E is HIGH, the switches are turned off.

Digital inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC} .

2. Features and benefits

- Wide supply voltage range from 1.0 V to 6.0 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- CMOS low power dissipation
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low ON resistance:
 - 180 Ω (typical) at $V_{CC} - V_{EE} = 2.0$ V
 - 100 Ω (typical) at $V_{CC} - V_{EE} = 3.0$ V
 - 75 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
- Logic level translation:
 - To enable 3 V logic to communicate with ± 3 V analog signals
- Typical 'break before make' built in
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.6 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4053D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4053PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4053BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

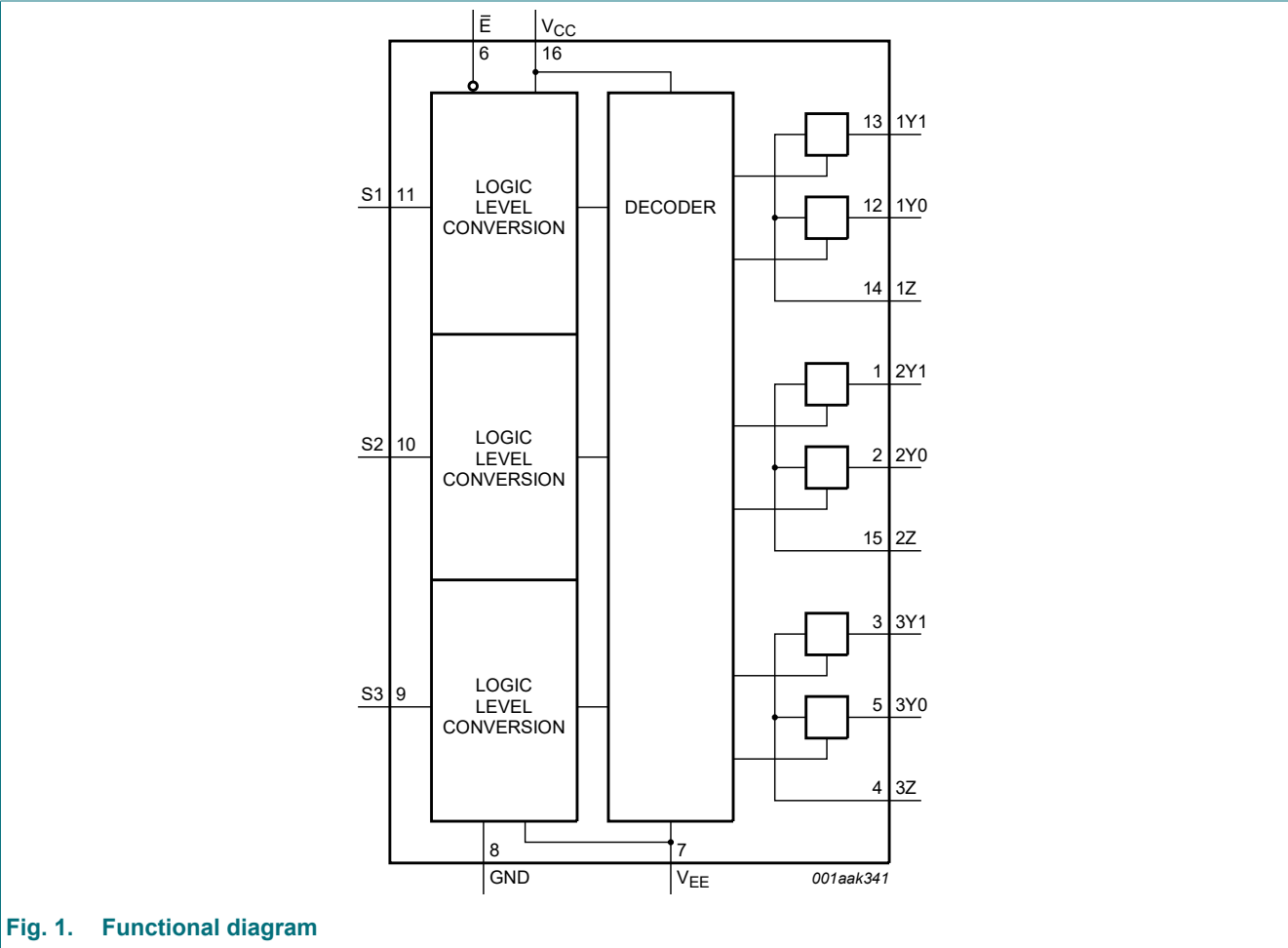
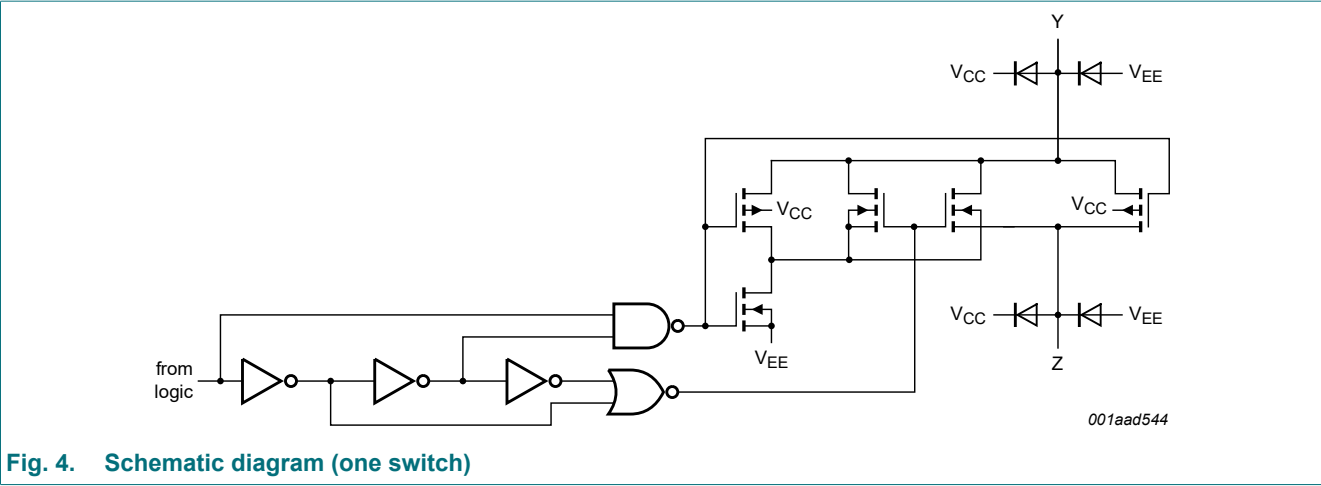
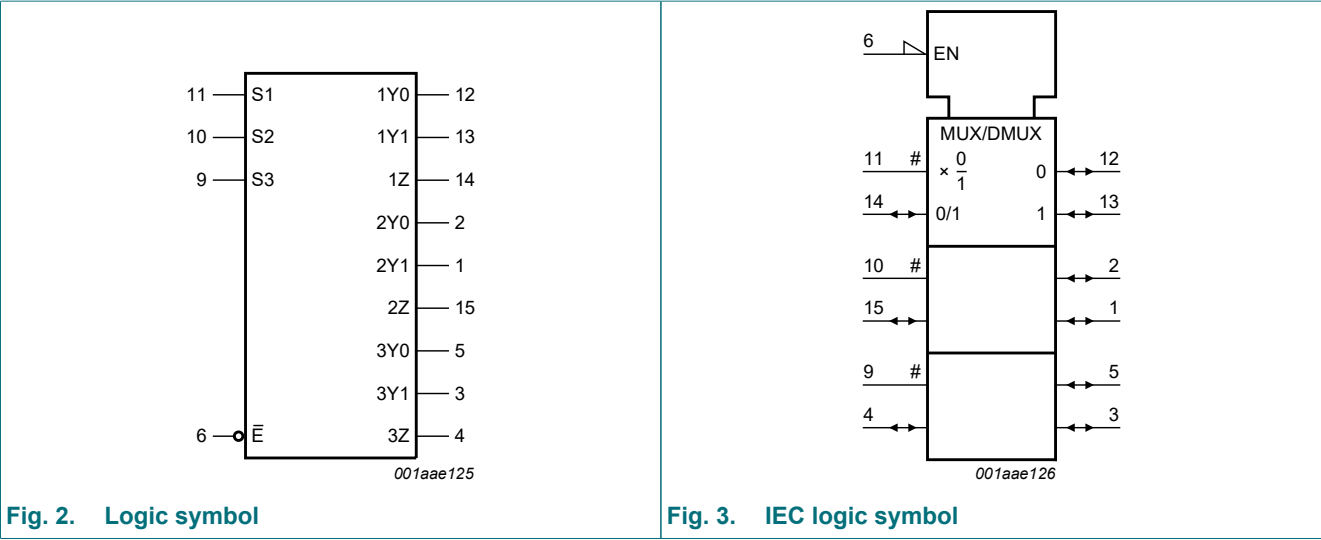
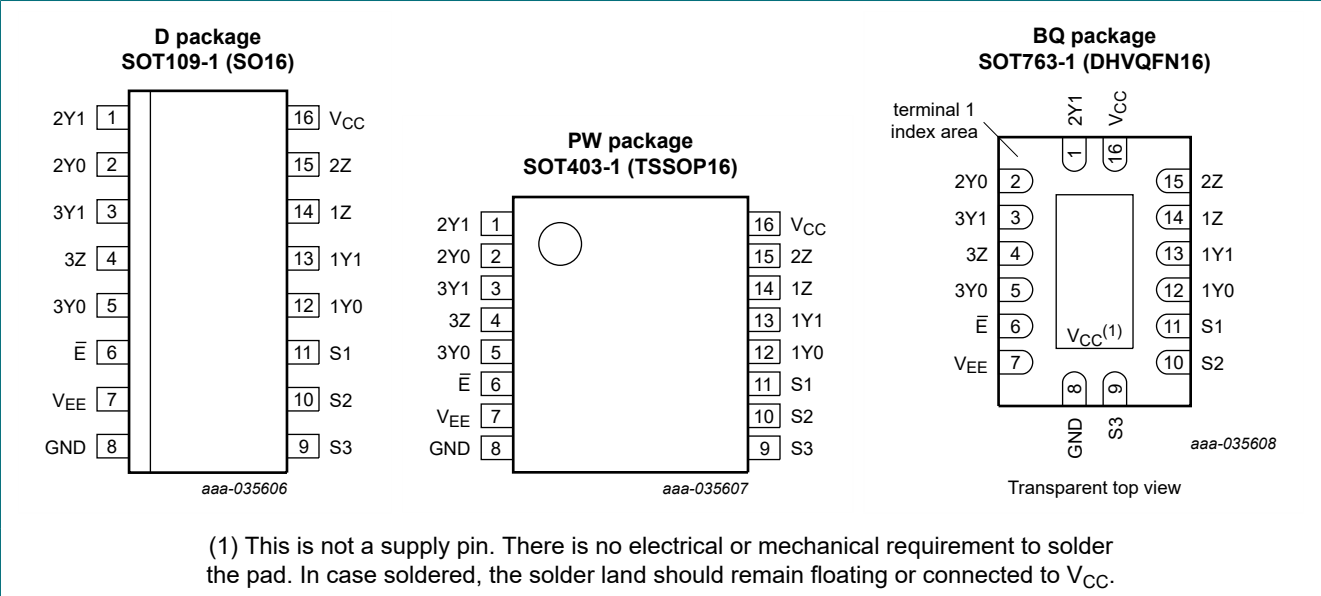


Fig. 1. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	common output or input
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Channel on
$\overline{E}$	S _n	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [2]	-	± 20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$ [2]	-	± 20	mA
I_{SW}	switch current	$V_{SW} > -0.5\text{ V}$ or $V_{SW} < V_{CC} + 0.5\text{ V}$ [2] V;source or sink current	-	± 25	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [3]	-	500	mW

- [1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE} .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	see Fig. 5	1	3.3	6	V
V_I	input voltage		0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	100	ns/V

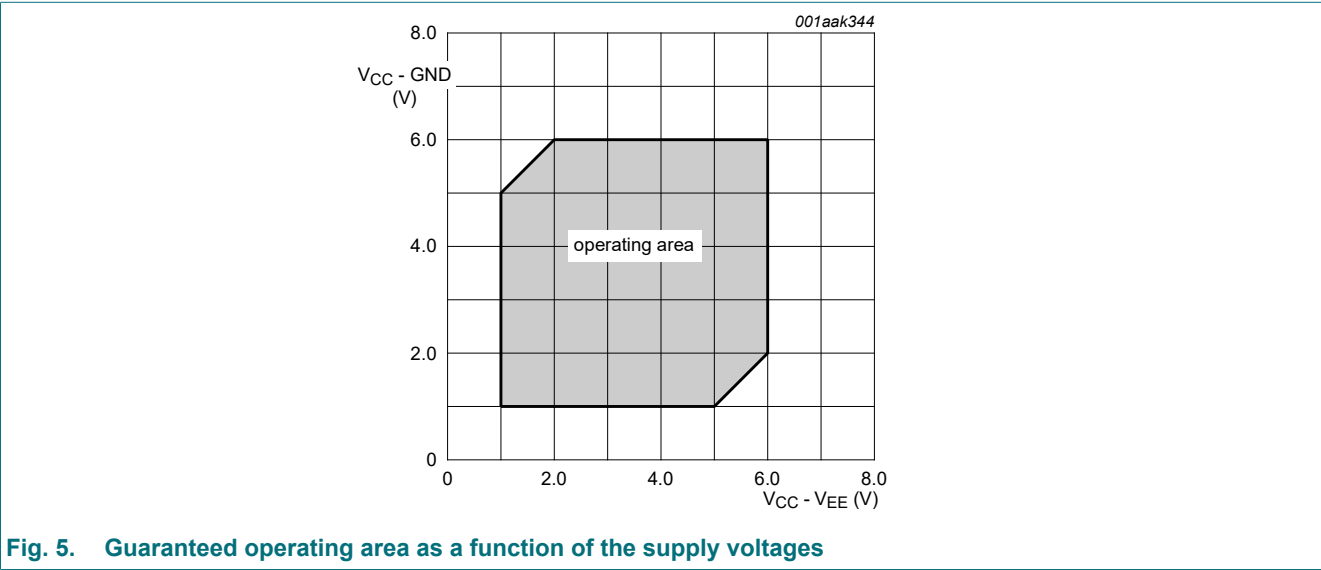


Fig. 5. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

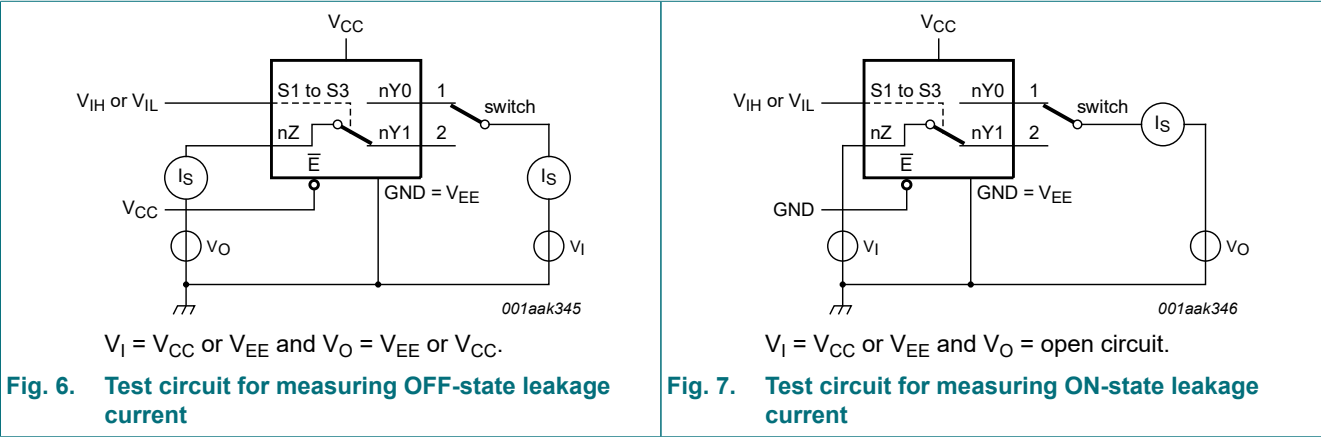
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V _{CC} = 6.0 V	4.20	-	-	4.20	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	-	1.80	V
I _I	input leakage current	V _I = V _{CC} or GND						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(OFF)}	OFF-state leakage current	V _I = V _{IH} or V _{IL} ; see Fig. 6						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; see Fig. 7						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A						
		V _{CC} = 3.6 V	-	-	20	-	40	μA
		V _{CC} = 6.0 V	-	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{sw}	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	8	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

9.1. Test circuits



9.2. ON resistance

Table 7. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Fig. 8 and Fig. 9.

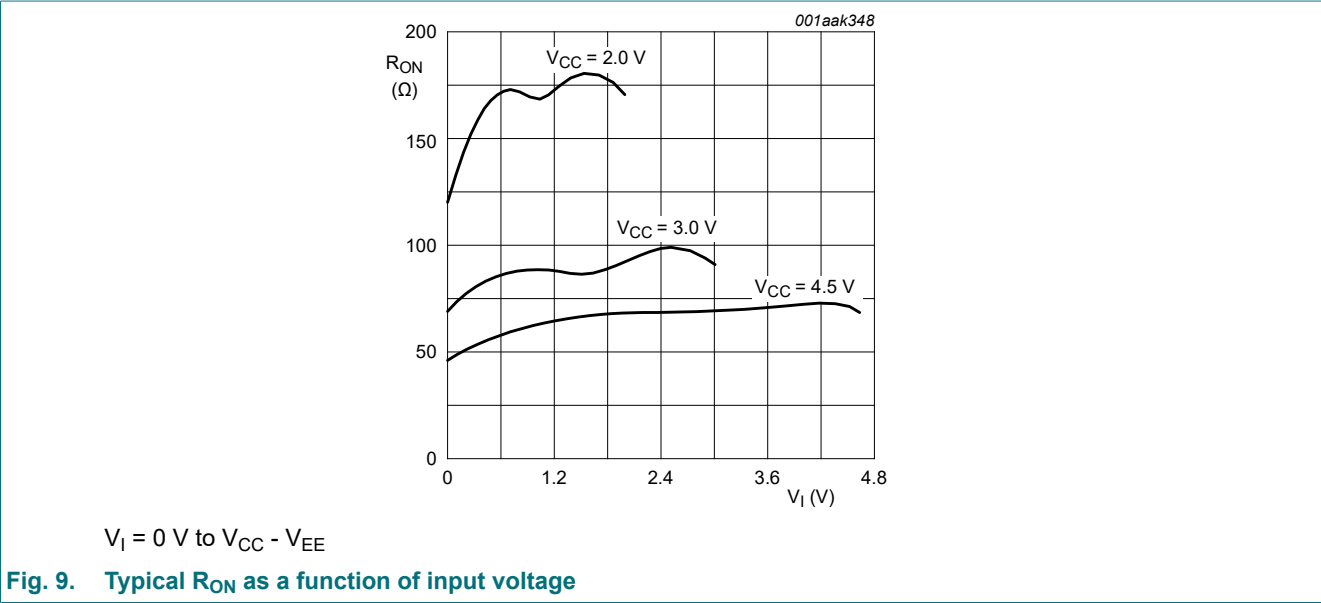
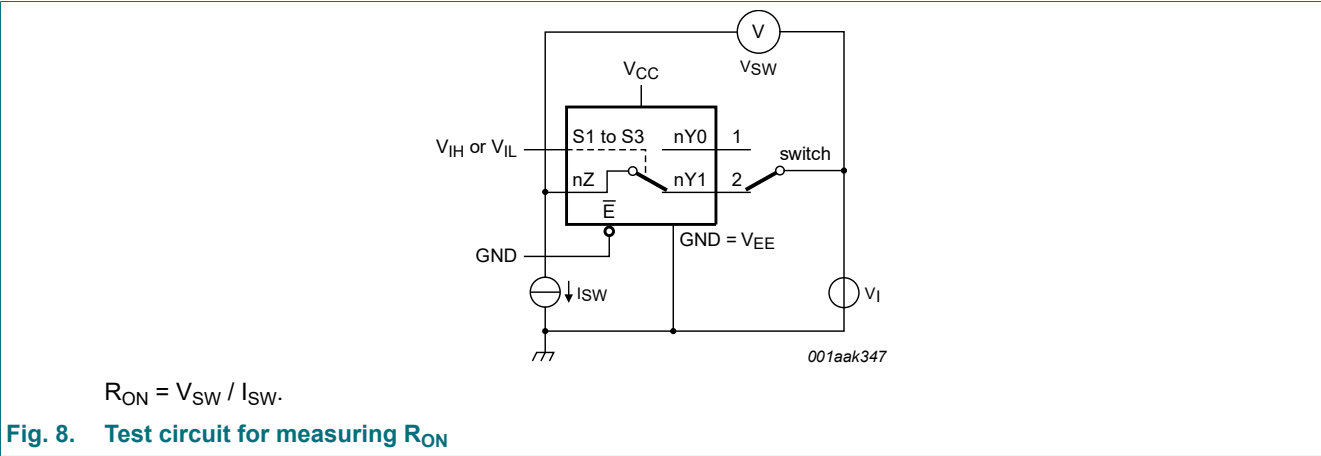
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0\text{ V to }V_{CC} - V_{EE}$						
		$V_{CC} = 1.2\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [2]	-	-	-	-	-	Ω
		$V_{CC} = 2.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	180	365	-	435	Ω
		$V_{CC} = 2.7\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	115	225	-	270	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	100	200	-	245	Ω
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	75	150	-	180	Ω
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	70	140	-	165	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0\text{ V to }V_{CC} - V_{EE}$						
		$V_{CC} = 1.2\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [2]	-	-	-	-	-	Ω
		$V_{CC} = 2.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	5	-	-	-	Ω
		$V_{CC} = 2.7\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	3	-	-	-	Ω
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	2	-	-	-	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_I = \text{GND}$						
		$V_{CC} = 1.2\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [2]	-	250	-	-	-	Ω
		$V_{CC} = 2.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	120	280	-	325	Ω
		$V_{CC} = 2.7\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	75	170	-	195	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	70	155	-	180	Ω
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	50	120	-	135	Ω
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$	-	45	105	-	120	Ω

Triple single-pole double-throw analog switch

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R _{ON(rail)}	ON resistance (rail)	V _I = V _{CC} - V _{EE}						
		V _{CC} = 1.2 V; I _{SW} = 100 µA [2]	-	350	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA	-	170	340	-	400	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA	-	105	210	-	250	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA	-	95	190	-	225	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA	-	70	140	-	165	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA	-	65	125	-	150	Ω

- [1] Typical values are measured at T_{amb} = 25 °C.
- [2] When supply voltages (V_{CC} - V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3. On resistance waveform and test circuit



10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nYn, nZ to nZ, nYn; see Fig. 10 [2]						
		$V_{CC} = 1.2\text{ V}$	-	25	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	9	17	-	20	ns
		$V_{CC} = 2.7\text{ V}$	-	6	13	-	15	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	5	10	-	12	ns
		$V_{CC} = 4.5\text{ V}$	-	4	9	-	10	ns
		$V_{CC} = 6.0\text{ V}$	-	3	7	-	8	ns
t_{en}	enable time	$\bar{E}$ to nYn, nZ; see Fig. 11 [2]						
		$V_{CC} = 1.2\text{ V}$	-	100	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	34	65	-	77	ns
		$V_{CC} = 2.7\text{ V}$	-	25	48	-	56	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ [3]	-	16	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	19	38	-	45	ns
		$V_{CC} = 4.5\text{ V}$	-	17	32	-	38	ns
		$V_{CC} = 6.0\text{ V}$	-	13	25	-	29	ns
		Sn to nYn, nZ; see Fig. 11 [2]						
		$V_{CC} = 1.2\text{ V}$	-	125	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	43	82	-	97	ns
		$V_{CC} = 2.7\text{ V}$	-	31	60	-	71	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ [3]	-	20	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	24	48	-	57	ns
		$V_{CC} = 4.5\text{ V}$	-	21	41	-	48	ns
		$V_{CC} = 6.0\text{ V}$	-	16	31	-	37	ns
t_{dis}	disable time	$\bar{E}$ to nYn, nZ; see Fig. 11 [2]						
		$V_{CC} = 1.2\text{ V}$	-	95	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	34	61	-	73	ns
		$V_{CC} = 2.7\text{ V}$	-	26	46	-	54	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ [3]	-	17	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	20	37	-	44	ns
		$V_{CC} = 4.5\text{ V}$	-	18	32	-	38	ns
		$V_{CC} = 6.0\text{ V}$	-	15	25	-	30	ns
		Sn to nYn, nZ; see Fig. 11 [2]						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	32	59	-	70	ns
		$V_{CC} = 2.7\text{ V}$	-	24	44	-	52	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ [3]	-	16	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	19	36	-	42	ns
		$V_{CC} = 4.5\text{ V}$	-	17	31	-	36	ns
		$V_{CC} = 6.0\text{ V}$	-	14	24	-	28	ns

Triple single-pole double-throw analog switch

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [4]	-	36	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz, f_o = output frequency in MHz
C_L = output load capacitance in pF
C_{SW} = maximum switch capacitance in pF;
V_{CC} = supply voltage in Volts
N = number of inputs switching
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit

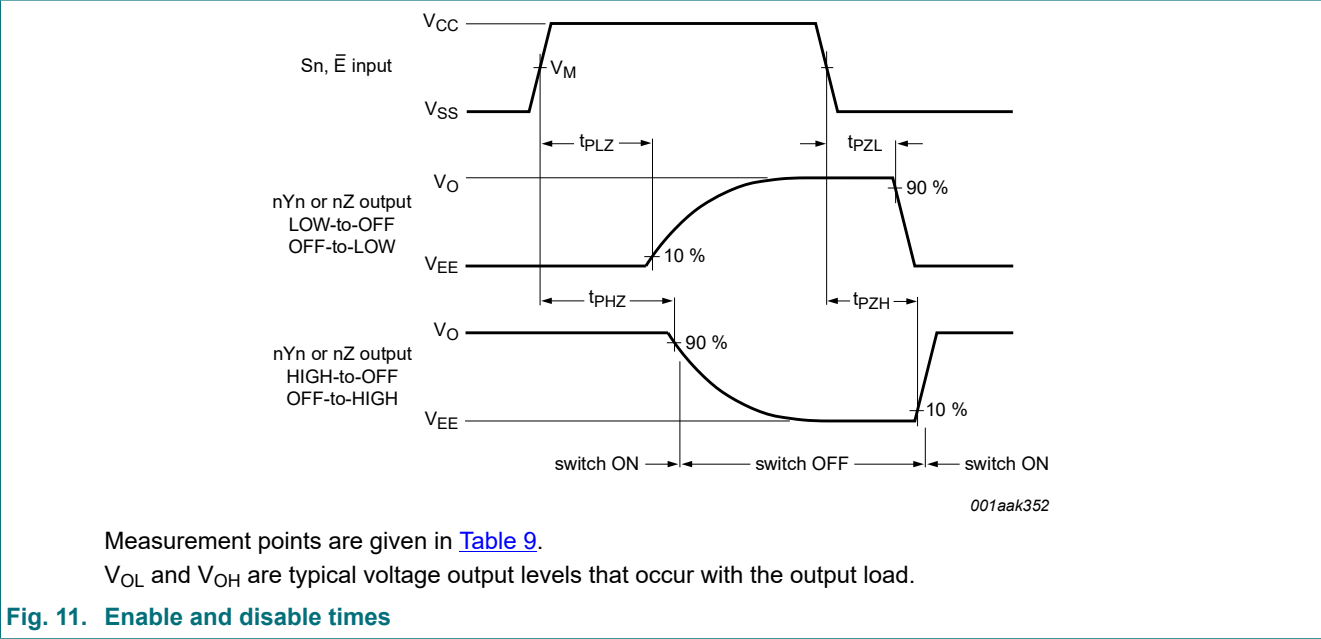
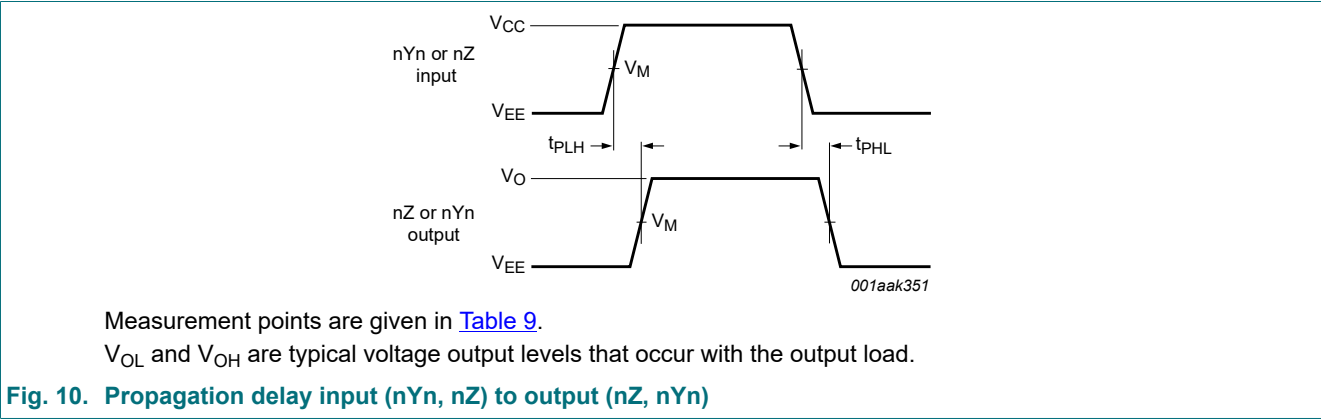


Table 9. Measurement points

Supply voltage	Input	Output		
V _{CC}	V _M	V _M	V _X	V _Y
< 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.1V _{CC}	V _{OH} - 0.1V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
> 3.6 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.1V _{CC}	V _{OH} - 0.1V _{CC}

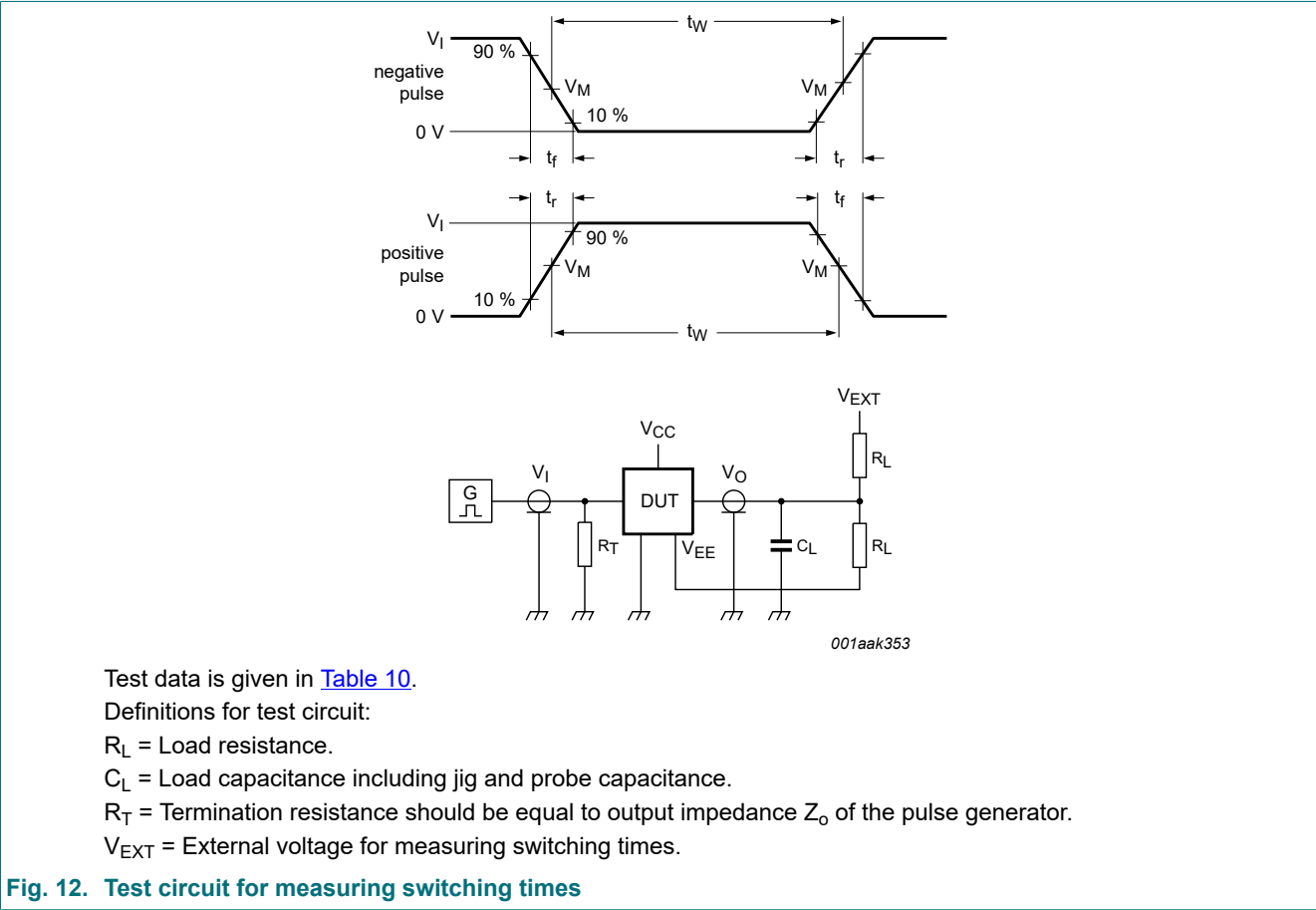


Table 10. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
< 2.7 V	V _{CC}	≤ 6 ns	50 pF	1 kΩ	open	V _{EE}	2V _{CC}
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	V _{EE}	2V _{CC}
> 3.6 V	V _{CC}	≤ 6 ns	50 pF	1 kΩ	open	V _{EE}	2V _{CC}

10.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0 \text{ ns}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Fig. 13				
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$	-	0.8	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$	-	0.4	-	%
		$f_i = 10 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Fig. 13				
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$	-	2.4	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$	-	1.2	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$C_L = 50 \text{ pF}$; $R_L = 50 \text{ }\Omega$; see Fig. 14 [1]				
		$V_{CC} = 3.0 \text{ V}$	-	180	-	MHz
		$V_{CC} = 6.0 \text{ V}$	-	200	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 16 [2]				
		$V_{CC} = 3.0 \text{ V}$	-	-50	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 18 [2]				
		$V_{CC} = 3.0 \text{ V}$	-	0.11	-	V
		$V_{CC} = 6.0 \text{ V}$	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 19				
		$V_{CC} = 3.0 \text{ V}$	-	-60	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).
[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.2.1. Test circuits

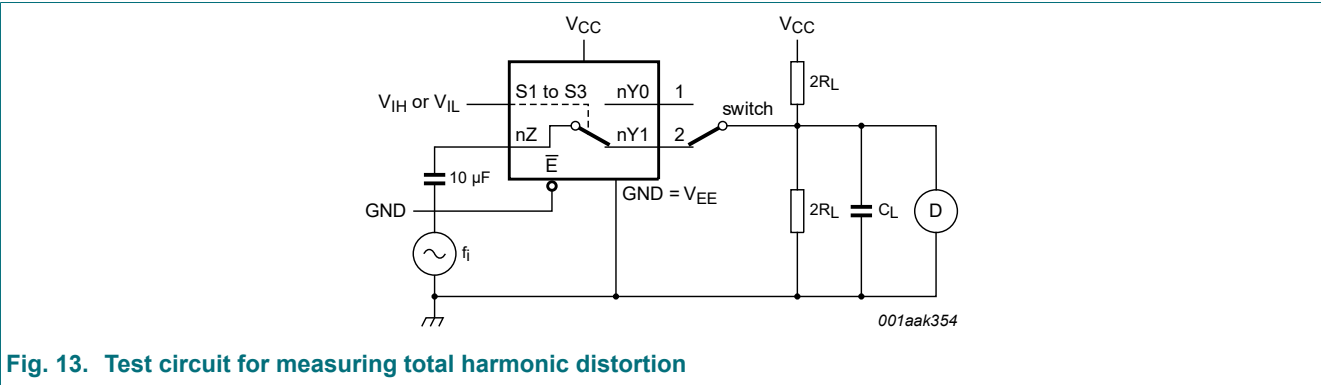


Fig. 13. Test circuit for measuring total harmonic distortion

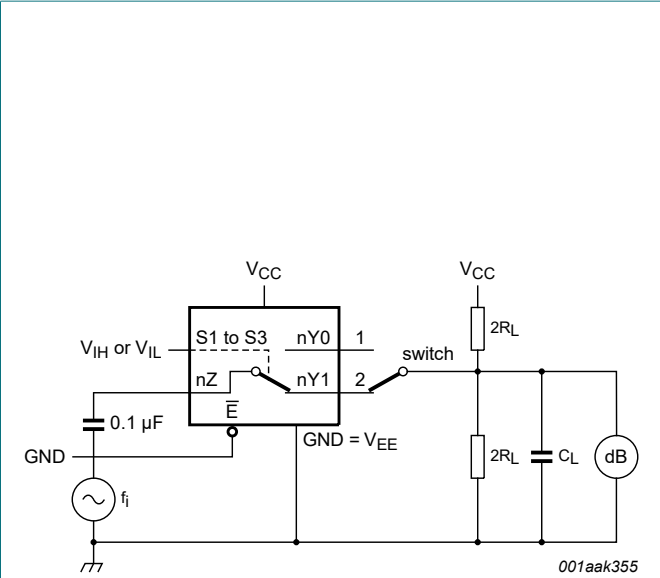


Fig. 14. Test circuit for measuring frequency response

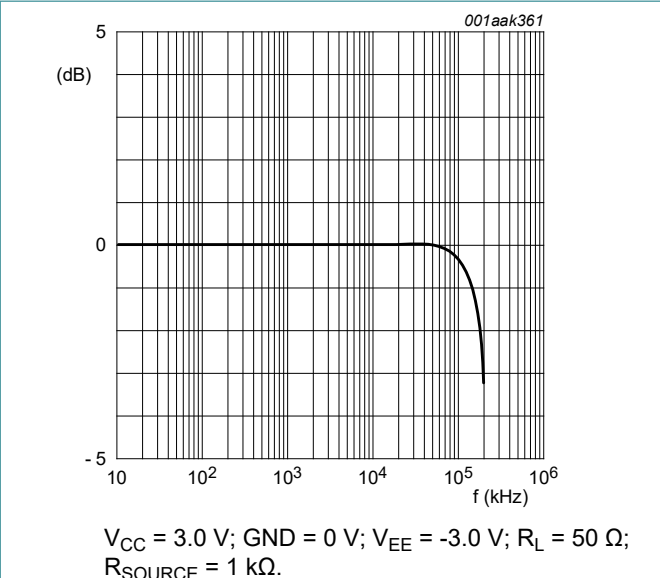


Fig. 15. Typical frequency response

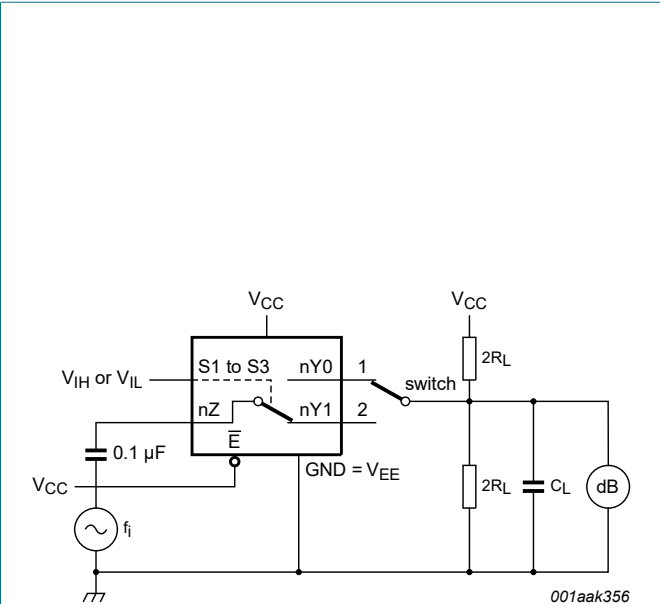


Fig. 16. Test circuit for measuring isolation (OFF-state)

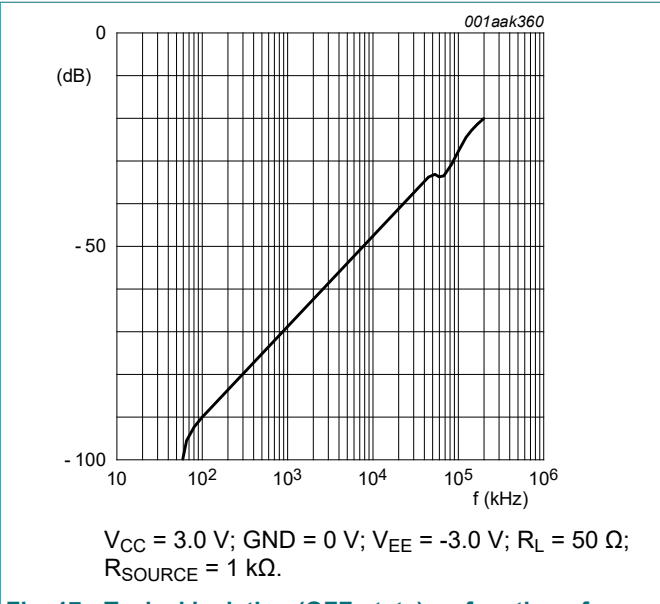
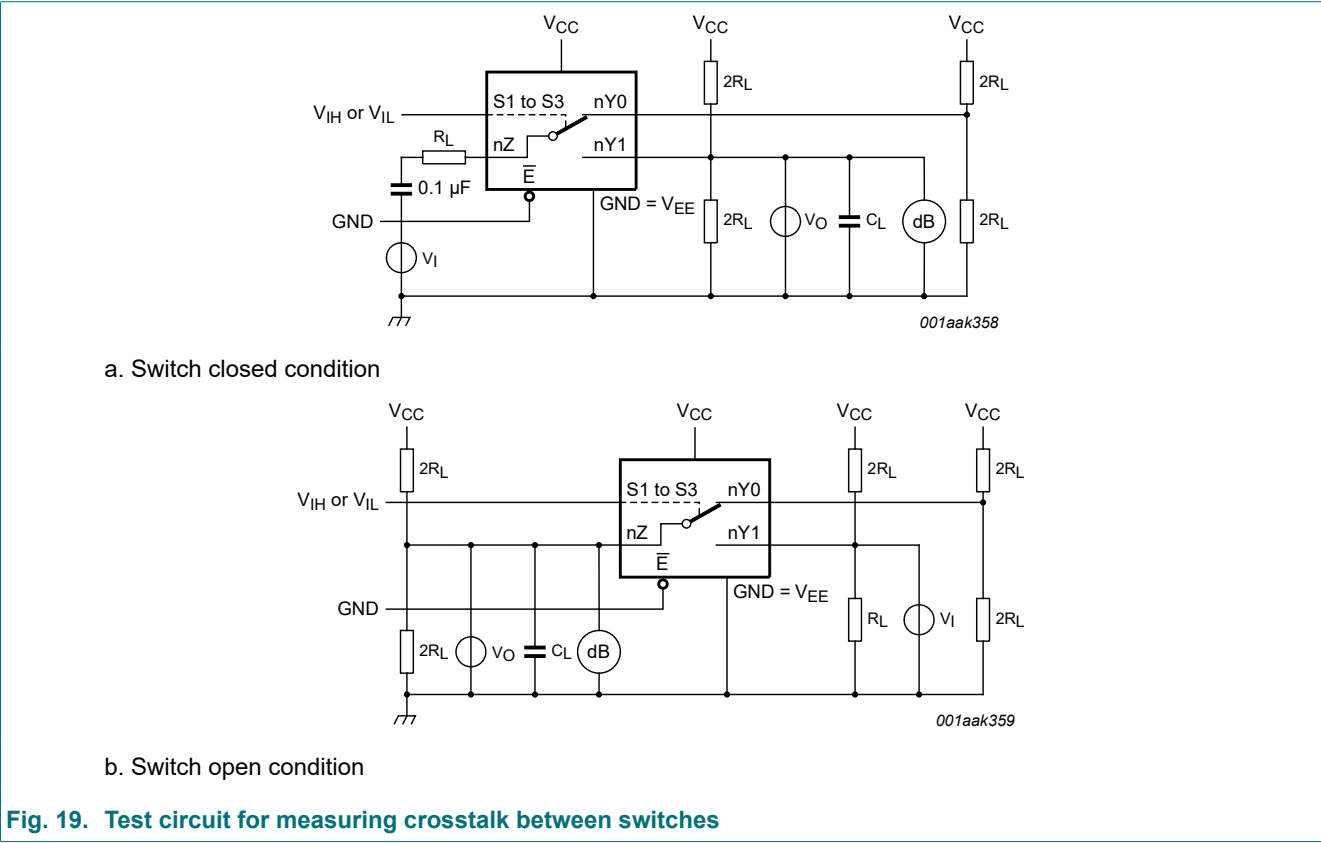
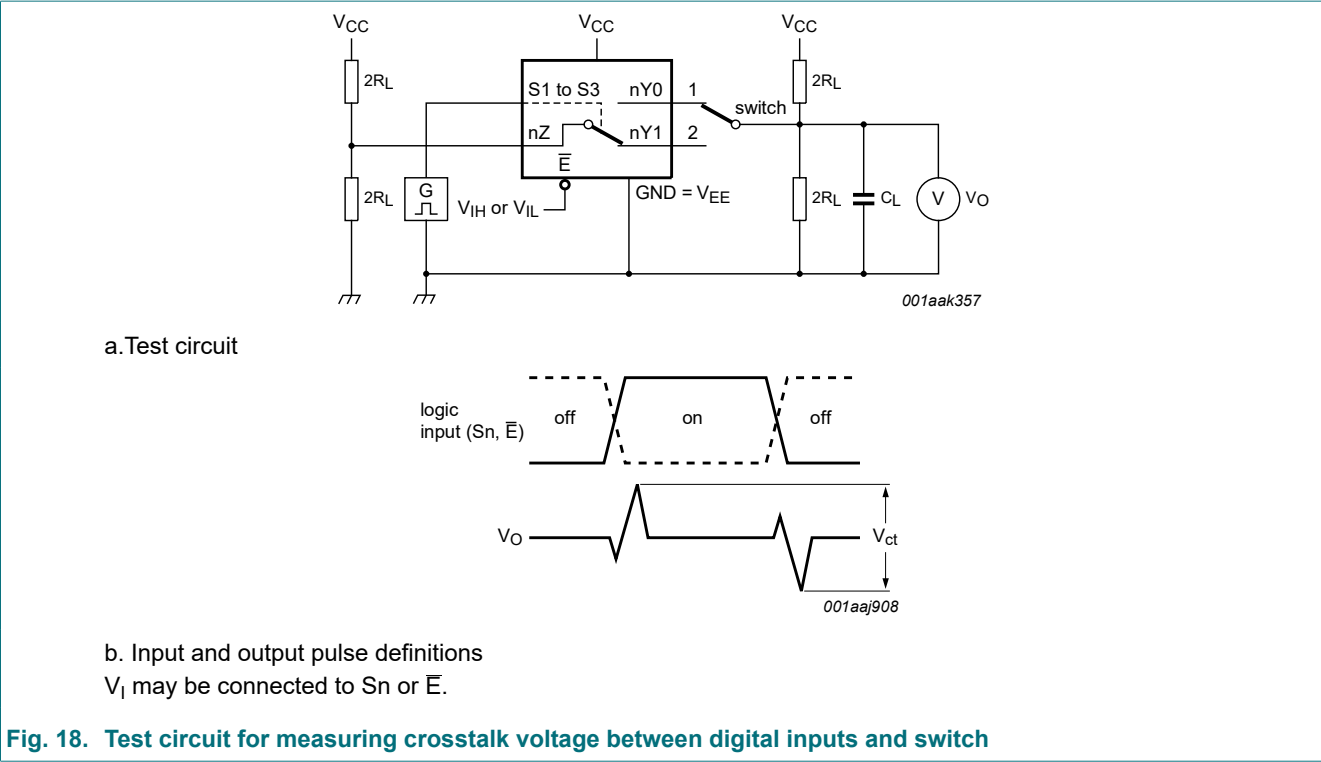


Fig. 17. Typical isolation (OFF-state) as function of frequency



11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

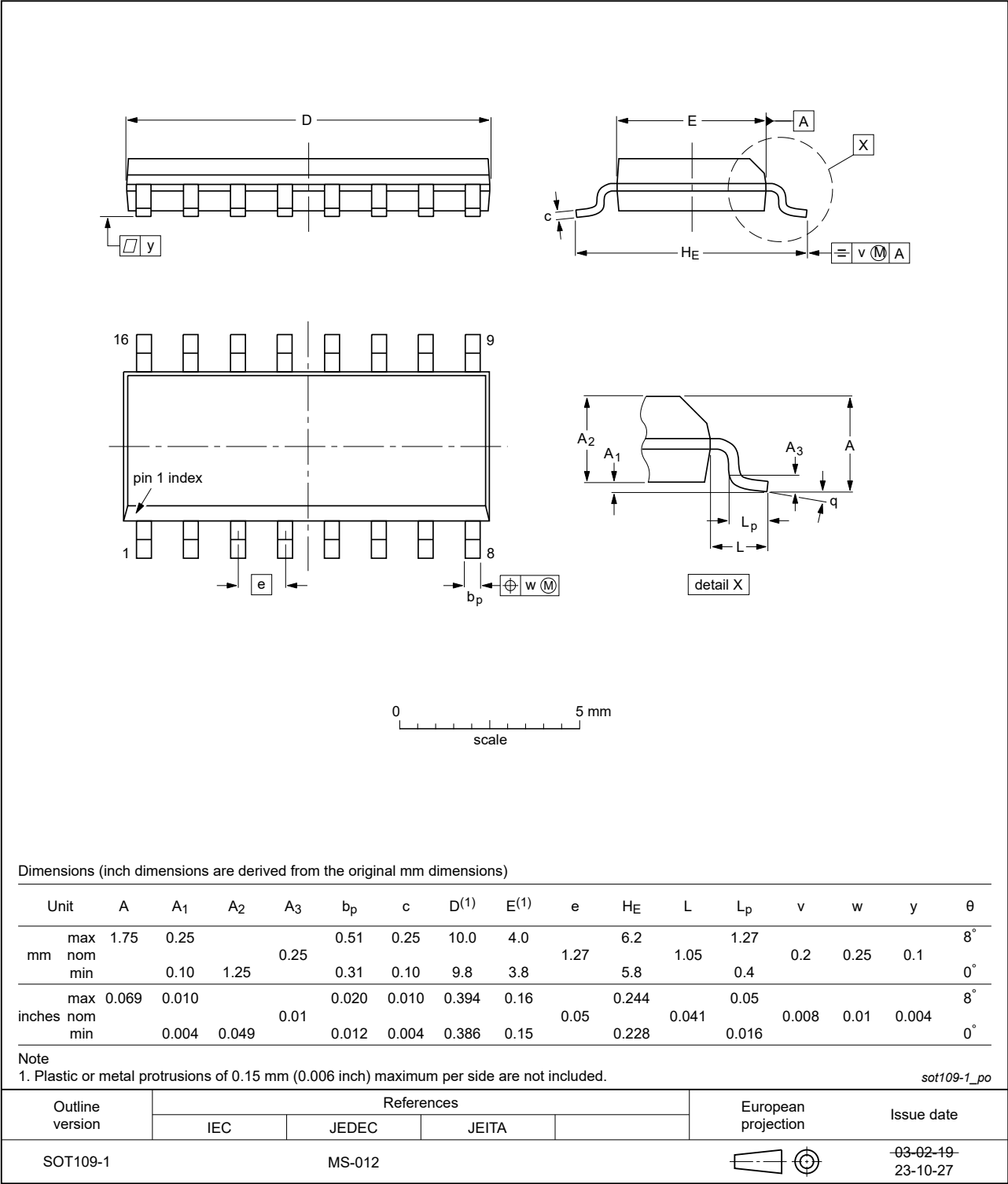


Fig. 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

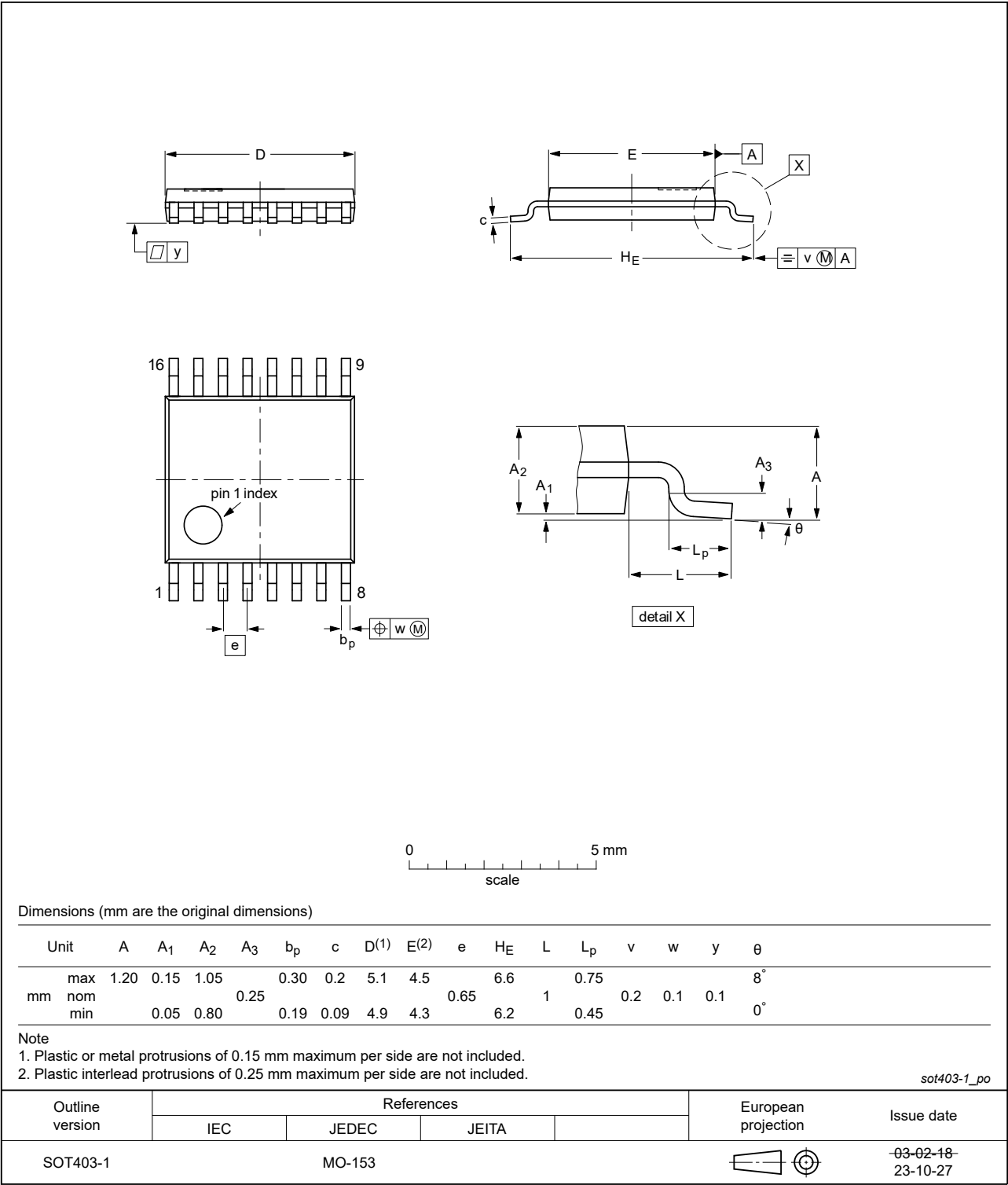


Fig. 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

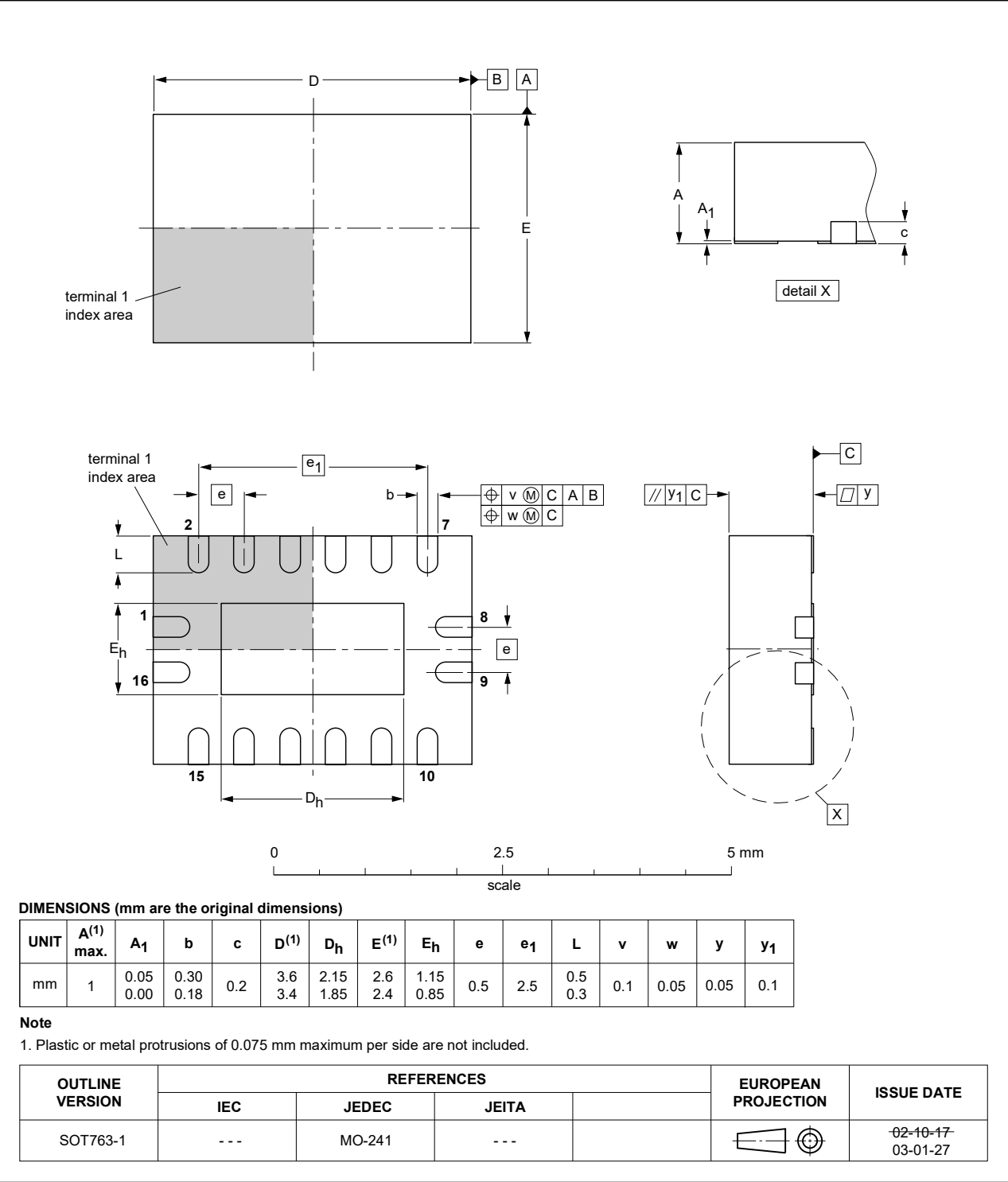


Fig. 22. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4053 v.9	20240402	Product data sheet	-	74LV4053 v.8
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 20 and Fig. 21: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LV4053 v.8	20210915	Product data sheet	-	74LV4053 v.7
Modifications:	- Type number 74LV4053DB (SOT338-1/SSOP16) removed. - Section 1 and Section 2 updated.			
74LV4053 v.7	20200923	Product data sheet	-	74LV4053 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Table 4: Derating values for P_{tot} total power dissipation updated.			
74LV4053 v.6	20160317	Product data sheet	-	74LV4053 v.5
Modifications:	Type number 74LV4053N (SOT38-4) removed.			
74LV4053 v.5	20140918	Product data sheet	-	74LV4053 v.4
Modifications:	Section 5.1: Figure note added for DHVQFN16 package.			
74LV4053 v.4	20090810	Product data sheet	-	74LV4053 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Added type number 74LV4053BQ (DHVQFN16 package) - R_{ON} values changed in Section 2. - Package version SOT38-1 changed to SOT38-4 in Section 5, and Section 11.			
74LV4053 v.3	19980623	Product specification	-	74LV4053 v.2
74LV4053 v.2	19970715	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information.....2

4. Functional diagram.....2

5. Pinning information.....4

5.1. Pinning..... 4

5.2. Pin description..... 4

6. Functional description..... 4

7. Limiting values..... 5

8. Recommended operating conditions.....5

9. Static characteristics.....6

9.1. Test circuits..... 7

9.2. ON resistance..... 7

9.3. On resistance waveform and test circuit..... 8

10. Dynamic characteristics..... 9

10.1. Waveforms and test circuit..... 10

10.2. Additional dynamic parameters..... 12

10.2.1. Test circuits..... 12

11. Package outline..... 15

12. Abbreviations..... 18

13. Revision history..... 18

14. Legal information.....19

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 2 April 2024