



BUK9K5R6-30E

Dual N-channel 30 V, 5.8 mΩ logic level MOSFET

2 September 2015

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	30	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	-	40	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$		-	-	64	W
Static characteristics FET1 and FET2							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$		-	4.7	5.8	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 24\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$		-	9.2	-	nC

[1] Continuous current is limited by package

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 <i>mbk725</i>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K5R6-30E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K5R6-30E	95E630

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	30	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC		-10	10	V
		$T_j \leq 175\text{ °C}$; Pulsed	[1][2]	-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	64	W
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	-	40	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	-	40	A

Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3		-	305	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I_S	source current	$T_{mb} = 25\text{ °C}$	[3]	-	40	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	305	A
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 40\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[4][5]	-	169	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
 [2] Significantly longer life times are achieved by lowering T_j and or V_{GS} .
 [3] Continuous current is limited by package
 [4] Refer to application note AN10273 for further information
 [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

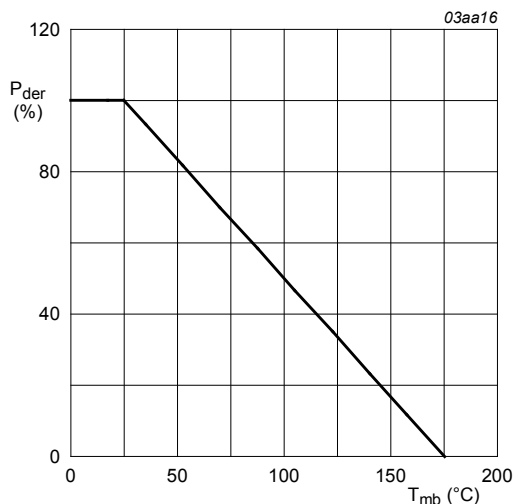
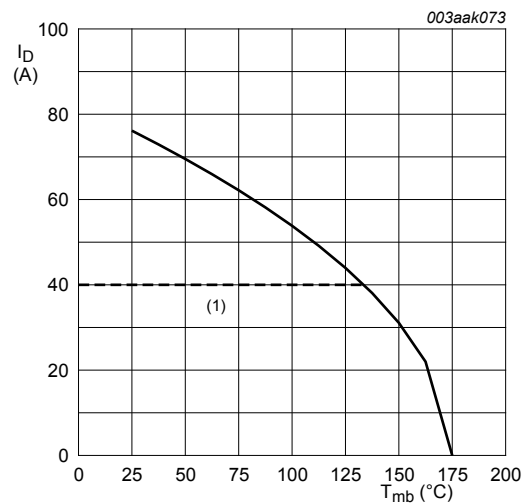


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



(1) Capped at 40A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

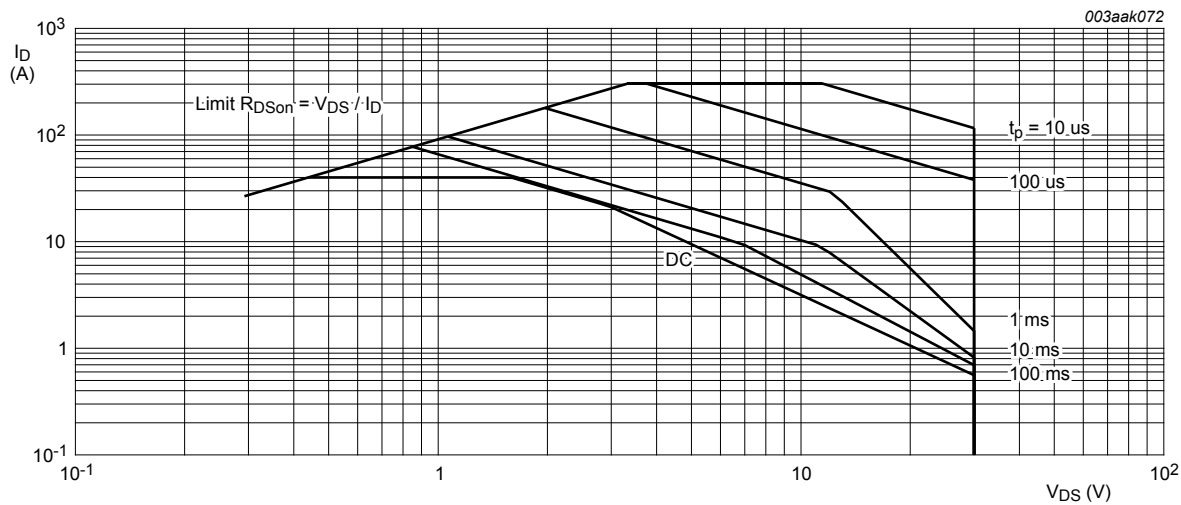


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

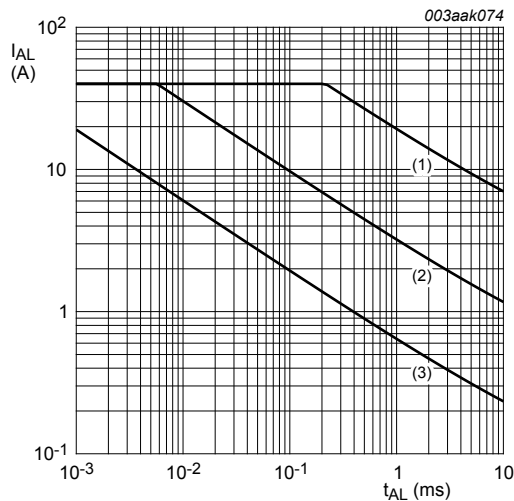


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^{\circ}\text{C}$; (2) $T_{j(init)} = 150^{\circ}\text{C}$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

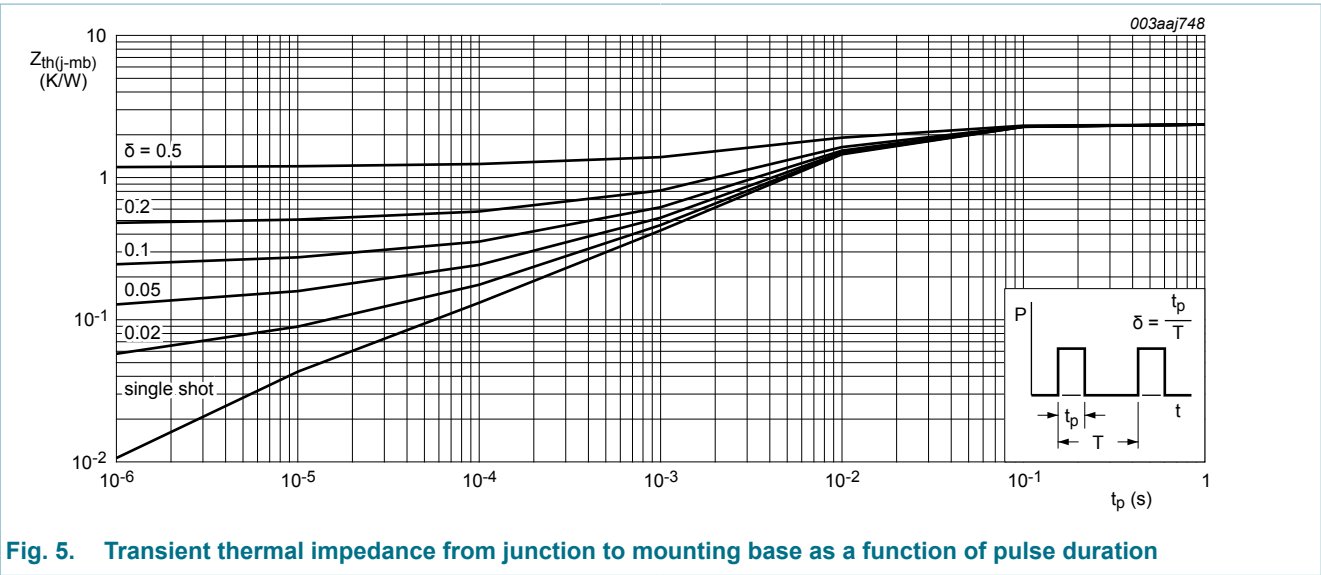


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		27	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 9		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 9		-	-	2.45	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _J = 25 °C		-	0.02	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _J = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = -10 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = 10 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; T _J = 25 °C; Fig. 11		-	4.7	5.8	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _J = 175 °C; Fig. 11 ; Fig. 12		-	8.9	11	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _J = 25 °C; Fig. 11		-	3.9	4.7	mΩ
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 24 V; V _{GS} = 5 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	22.6	-	nC
Q _{GS}	gate-source charge			-	4.4	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GD}	gate-drain charge			-	9.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	1860	2480	pF
C _{oss}	output capacitance			-	391	469	pF
C _{rss}	reverse transfer capacitance			-	231	316	pF
t _{d(on)}	turn-on delay time	V _{DS} = 24 V; R _L = 2.4 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	13.8	-	ns
t _r	rise time			-	25.2	-	ns
t _{d(off)}	turn-off delay time			-	30.1	-	ns
t _f	fall time			-	22.4	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.78	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 15 V; T _j = 25 °C		-	32.3	-	ns
Q _r	recovered charge			-	26.7	-	nC

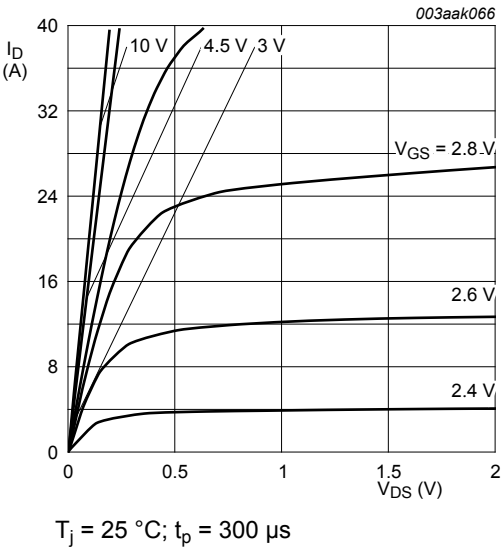


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

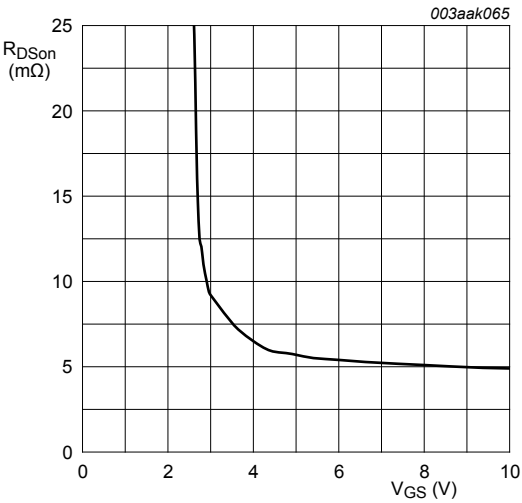


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 10\text{ A}$

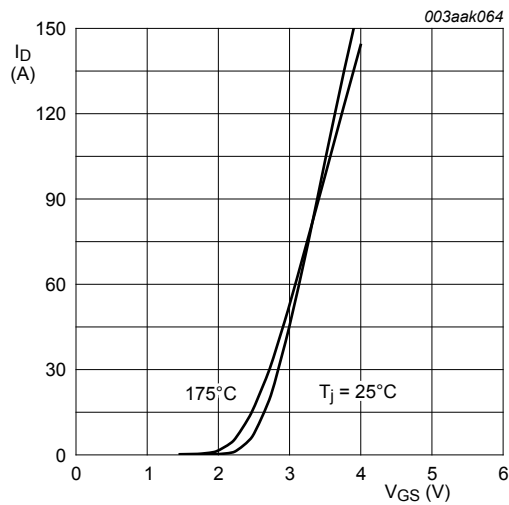


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

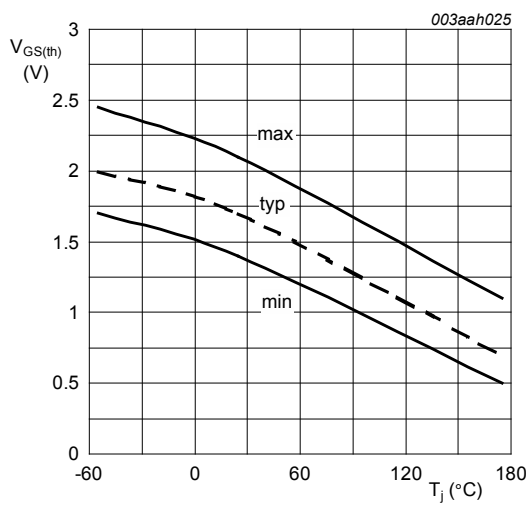


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

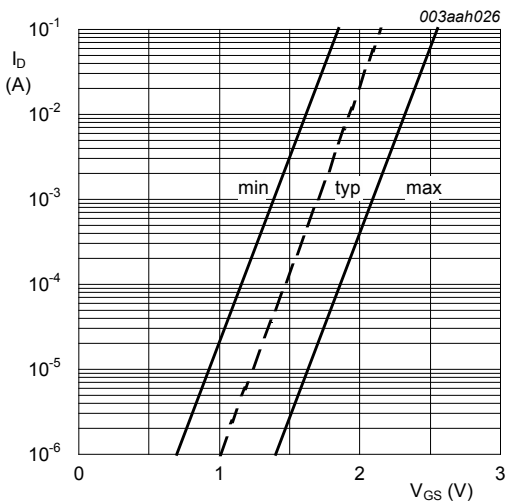


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

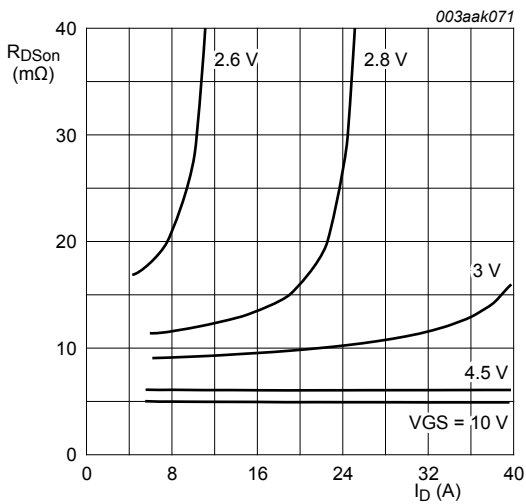


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

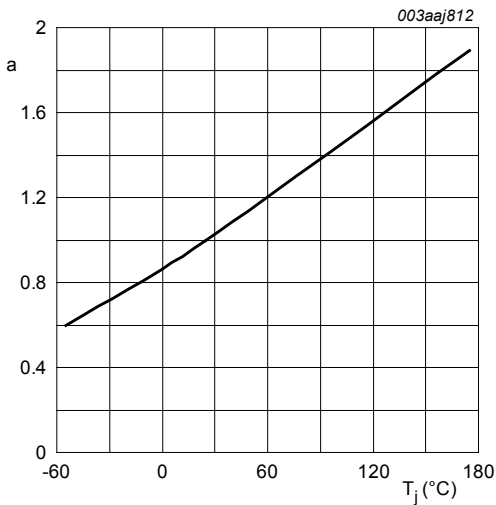


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

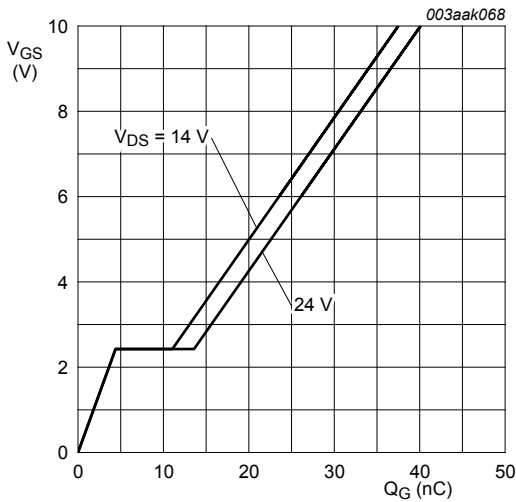


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 10\text{ A}$$

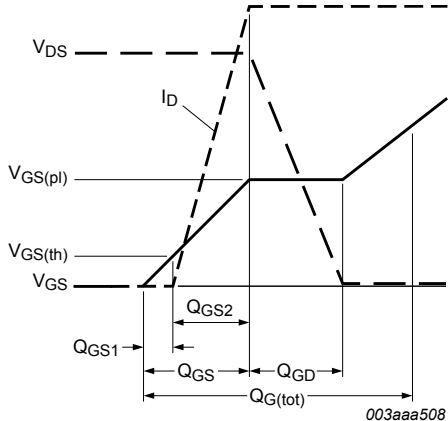


Fig. 13. Gate charge waveform definitions

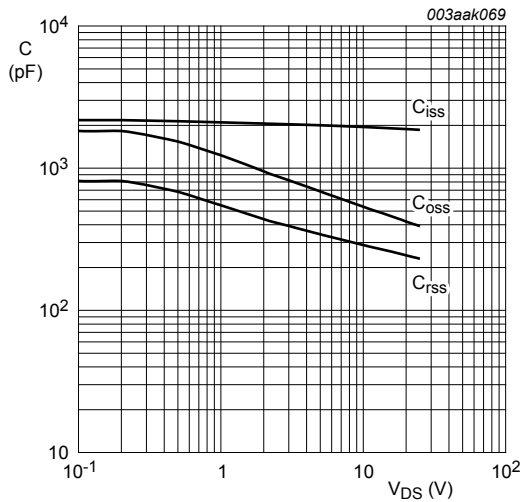


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

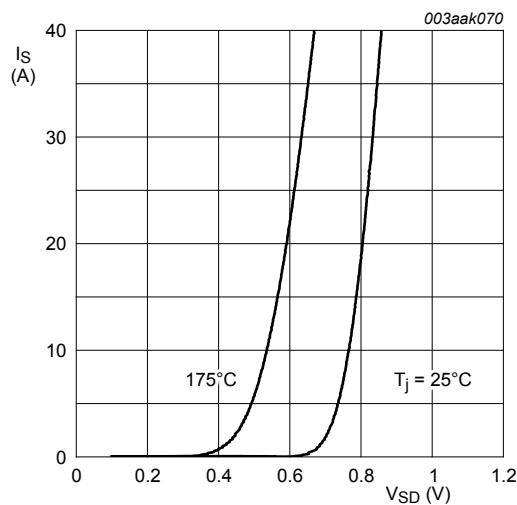


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values
 $V_{GS} = 0V$

11. Package outline

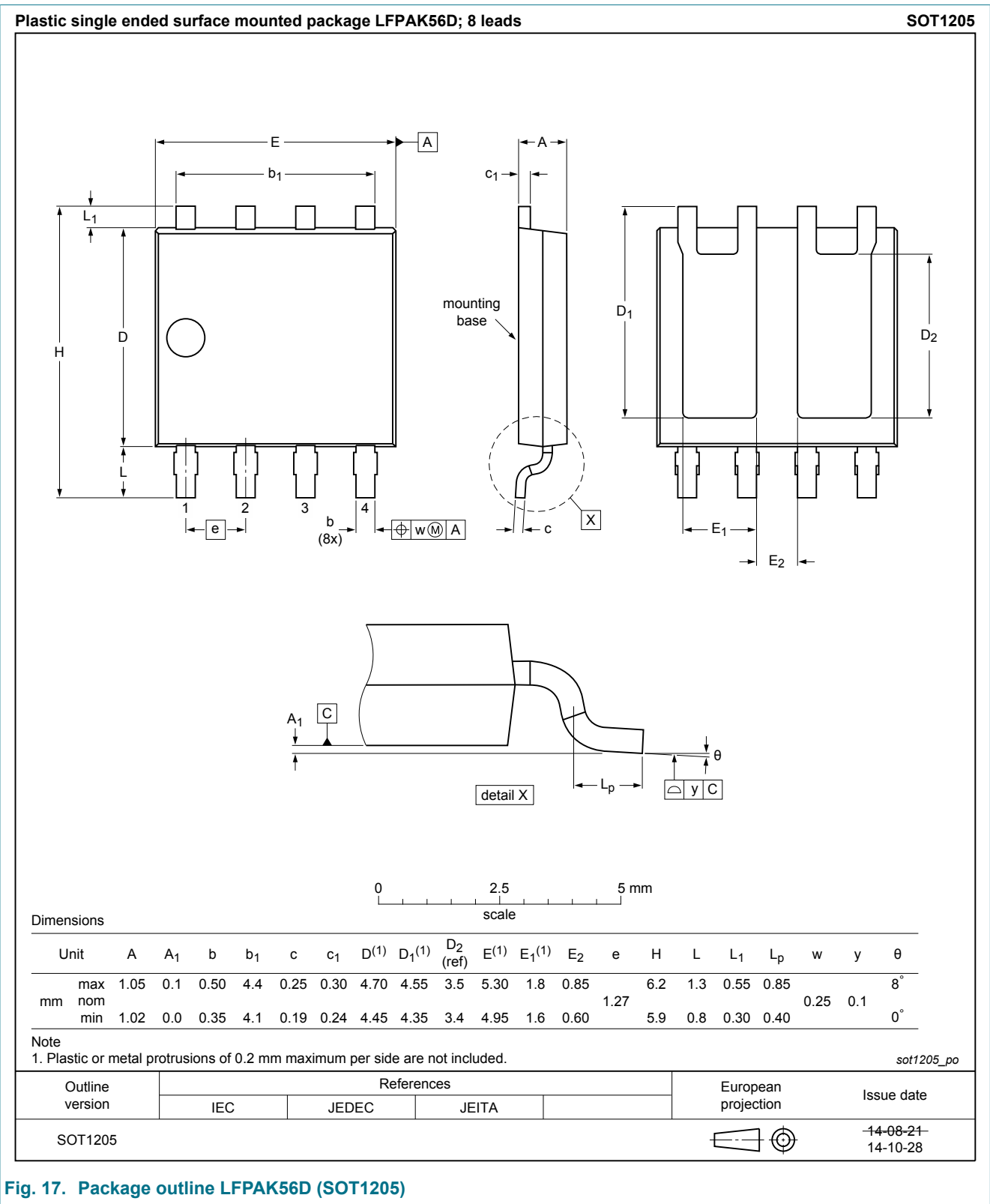


Fig. 17. Package outline LPAK56D (SOT1205)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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