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Kind regards,

Team Nexperia

# IP4059CX5

Integrated USB 2.0 and USB OTG ESD protection to  
IEC 61000-4-2 level 4

Rev. 1 — 15 September 2011

Product data sheet

## 1. Product profile

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### 1.1 General description

The IP4059CX5 is designed to protect several I/O pins of computer interfaces, such as Universal Serial Bus (USB) 2.0, USB On-The-Go (OTG), Ethernet, Digital Visual Interface (DVI) etc. The IP4059CX5 incorporates ultra-low capacity diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as  $\pm 8$  kV contact discharge according to the IEC 61000-4-2 model.

The device is fabricated using monolithic silicon technology and integrates four ultra-low capacity ESD protection diodes in a 0.5 mm pitch Wafer-Level Chip-Scale Package (WLCSP) measuring 0.96 mm by 1.34 mm only.

### 1.2 Features and benefits

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- 4 ultra-low input capacity rail-to-rail ESD protection diodes with  $C_d = 3.0$  pF
- Integrated ESD protection withstanding  $\pm 8$  kV contact discharge and  $\pm 15$  kV air discharge
- WLCSP with 0.5 mm pitch

### 1.3 Applications

General purpose ElectroMagnetic Interference (EMI) and Radio Frequency Interference (RFI) filtering and downstream ESD protection for USB ports inside:

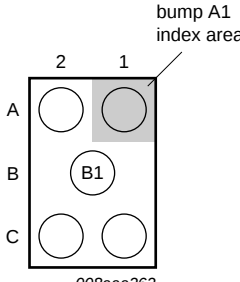
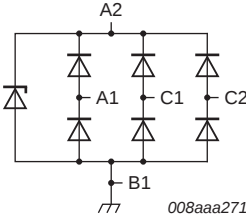
- Cellular and Personal Communication System (PCS) mobile handsets
- PC peripherals and PCs
- Cordless telephones
- Wireless data and Local Area Network (LAN) systems
- Personal Digital Assistants (PDAs)
- Digital cameras



## 2. Pinning information

**Table 1. Pinning**

Example of pin configuration for USB 2.0; other combinations for ID, D+ and D– in relation to pin A1, pin C1 and pin C2 are possible.

| Pin | Symbol           | Description               | Simplified outline                                                                                                                                            | Graphic symbol                                                                                       |
|-----|------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| A1  | D–               | USB 2.0 differential pair |  <p>008aaa262</p> <p>transparent top view,<br/>solder balls facing down</p> |  <p>008aaa271</p> |
| C1  | D+               |                           |                                                                                                                                                               |                                                                                                      |
| B1  | GND              | ground                    |                                                                                                                                                               |                                                                                                      |
| A2  | V <sub>BUS</sub> | power                     |                                                                                                                                                               |                                                                                                      |
| C2  | ID               | USB OTG ID pin            |                                                                                                                                                               |                                                                                                      |

## 3. Ordering information

**Table 2. Ordering information**

| Type number  | Package |                                                |              |
|--------------|---------|------------------------------------------------|--------------|
|              | Name    | Description                                    | Version      |
| IP4059CX5/LF | WLCSP5  | wafer level chip-size package; 5 bumps (2-1-2) | IP4059CX5/LF |

## 4. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                    | Parameter                       | Conditions            | Min     | Max                   | Unit |
|---------------------------|---------------------------------|-----------------------|---------|-----------------------|------|
| V <sub>CC</sub>           | supply voltage                  |                       | 0       | 5                     | V    |
| V <sub>I</sub>            | input voltage                   |                       | –0.5    | V <sub>CC</sub> + 0.5 | V    |
| V <sub>ESD</sub>          | electrostatic discharge voltage | contact discharge     | [1] –15 | +15                   | kV   |
|                           |                                 | air discharge         | [1] –15 | +15                   | kV   |
|                           |                                 | IEC 61000-4-2 level 4 |         |                       |      |
|                           |                                 | contact discharge     | –8      | +8                    | kV   |
|                           |                                 | air discharge         | –15     | +15                   | kV   |
| T <sub>stg</sub>          | storage temperature             |                       | –55     | +150                  | °C   |
| T <sub>reflow(peak)</sub> | peak reflow temperature         | 10 s maximum          | –       | 260                   | °C   |
| T <sub>amb</sub>          | ambient temperature             |                       | –40     | +85                   | °C   |

[1] Device is qualified with > 200 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

## 5. Characteristics

**Table 4. Electrical characteristics***T<sub>amb</sub> = 25 °C; unless otherwise specified.*

| Symbol          | Parameter               | Conditions                                                                                                  | Min | Typ | Max | Unit |
|-----------------|-------------------------|-------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| C <sub>d</sub>  | diode capacitance       | pins A1, C1 and C2; <a href="#">[1]</a><br>V <sub>bias(DC)</sub> = 0 V;<br>f = 1 MHz; V <sub>A2</sub> = 0 V | -   | 3.0 | 4.0 | pF   |
| I <sub>LR</sub> | reverse leakage current | V <sub>I</sub> = 3.0 V                                                                                      | -   | -   | 100 | nA   |
| V <sub>BR</sub> | breakdown voltage       | I <sub>test</sub> = 1 mA                                                                                    | 6   | -   | 9   | V    |
| V <sub>F</sub>  | forward voltage         |                                                                                                             | -   | 0.7 | -   | V    |

[1] Guaranteed by design.

## 6. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)

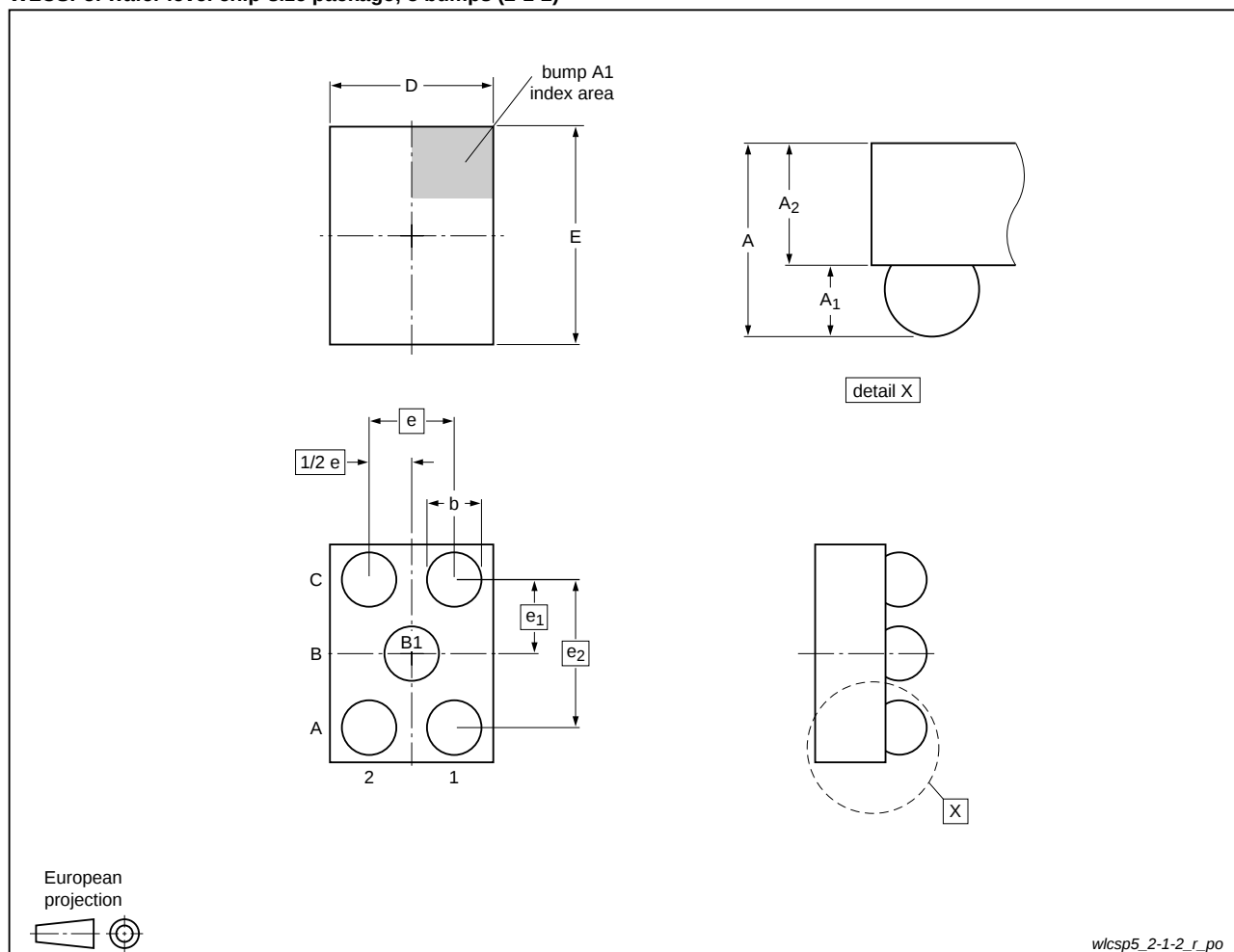


Fig 1. Package outline IP4059CX5/LF (WLCSP5)

Table 5. Dimensions for [Figure 1](#)

| Symbol         | Min  | Typ   | Max  | Unit |
|----------------|------|-------|------|------|
| A              | 0.61 | 0.65  | 0.69 | mm   |
| A <sub>1</sub> | 0.22 | 0.24  | 0.26 | mm   |
| A <sub>2</sub> | 0.39 | 0.41  | 0.43 | mm   |
| b              | 0.27 | 0.32  | 0.37 | mm   |
| D              | 0.91 | 0.96  | 1.01 | mm   |
| E              | 1.29 | 1.34  | 1.39 | mm   |
| e              | -    | 0.5   | -    | mm   |
| e <sub>1</sub> | -    | 0.435 | -    | mm   |
| e <sub>2</sub> | -    | 0.87  | -    | mm   |

## 7. Design and assembly recommendations

### 7.1 PCB design guidelines

For optimum performance it is recommended to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to [Table 6](#) for the recommended PCB design parameters.

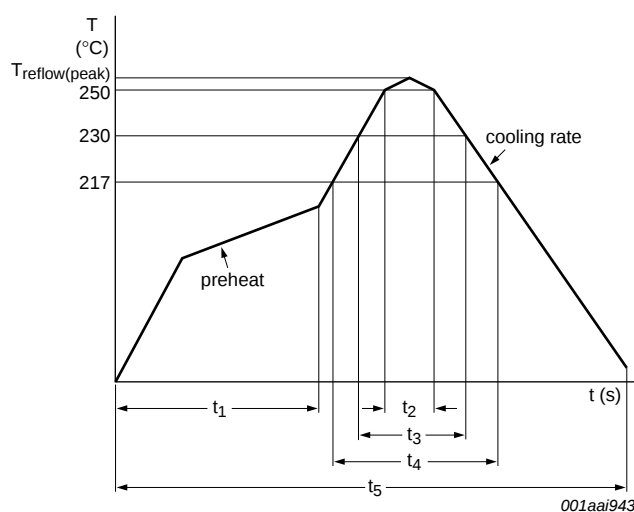
**Table 6. Recommended PCB design parameters**

| Parameter                     | Value or specification               |
|-------------------------------|--------------------------------------|
| PCB pad diameter              | 275 $\mu\text{m}$                    |
| Micro-via diameter            | 100 $\mu\text{m}$ (0.004 inch)       |
| Solder mask aperture diameter | 375 $\mu\text{m}$                    |
| Copper thickness              | 20 $\mu\text{m}$ to 40 $\mu\text{m}$ |
| Copper finish                 | AuNi                                 |
| PCB material                  | FR4                                  |

### 7.2 PCB assembly guidelines for Pb-free soldering

**Table 7. Assembly recommendations**

| Parameter                       | Value or specification                |
|---------------------------------|---------------------------------------|
| Solder screen aperture diameter | 330 $\mu\text{m}$                     |
| Solder screen thickness         | 100 $\mu\text{m}$ (0.004 inch)        |
| Solder paste: Pb-free           | SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %) |
| Solder to flux ratio            | 50 : 50                               |
| Solder reflow profile           | see <a href="#">Figure 2</a>          |



The device is capable of withstanding at least three reflows with this profile.

**Fig 2. Pb-free solder reflow profile**

Table 8. Characteristics

| Symbol                    | Parameter                     | Conditions                  | Min | Typ | Max | Unit |
|---------------------------|-------------------------------|-----------------------------|-----|-----|-----|------|
| $T_{\text{reflow(peak)}}$ | peak reflow temperature       |                             | 230 | -   | 260 | °C   |
| $t_1$                     | time 1                        | soak time                   | 60  | -   | 180 | s    |
| $t_2$                     | time 2                        | time during $T \geq 250$ °C | -   | -   | 30  | s    |
| $t_3$                     | time 3                        | time during $T \geq 230$ °C | 10  | -   | 50  | s    |
| $t_4$                     | time 4                        | time during $T > 217$ °C    | 30  | -   | 150 | s    |
| $t_5$                     | time 5                        |                             | -   | -   | 540 | s    |
| dT/dt                     | rate of change of temperature | cooling rate                | -   | -   | -6  | °C/s |
|                           |                               | preheat                     | 2.5 | -   | 4.0 | °C/s |

## 8. Abbreviations

Table 9. Abbreviations

| Acronym | Description                               |
|---------|-------------------------------------------|
| DVI     | Digital Visual Interface                  |
| EMI     | ElectroMagnetic Interference              |
| ESD     | ElectroStatic Discharge                   |
| FR4     | Flame Retard 4                            |
| IEC     | International Electrotechnical Commission |
| I/O     | Input/Output                              |
| LAN     | Local Area Network                        |
| NSMD    | Non-Solder Mask Defined                   |
| OTG     | On-The-Go                                 |
| PCB     | Printed-Circuit Board                     |
| PCS     | Personal Communication System             |
| PDA     | Personal Digital Assistant                |
| RFI     | Radio Frequency Interference              |
| RoHS    | Restriction of Hazardous Substances       |
| USB     | Universal Serial Bus                      |
| WLCSP   | Wafer-Level Chip-Scale Package            |

## 9. Revision history

Table 10. Revision history

| Document ID   | Release date | Data sheet status  | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| IP4059CX5 v.1 | 20110915     | Product data sheet | -             | -          |

## 10. Legal information

### 10.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 15 September 2011

Document identifier: IP4059CX5