

74HC377; 74HCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 3 — 25 September 2013

Product data sheet

1. General description

The 74HC377; 74HCT377 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and data enable ($\bar{E}$) inputs. When $\bar{E}$ is LOW, the outputs Qn assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. Input $\bar{E}$ must be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC377: CMOS level
 - ◆ For 74HCT377: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC377N	–40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT377N				
74HC377D	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT377D				
74HC377DB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT377DB				
74HC377PW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT377PW				



4. Functional diagram

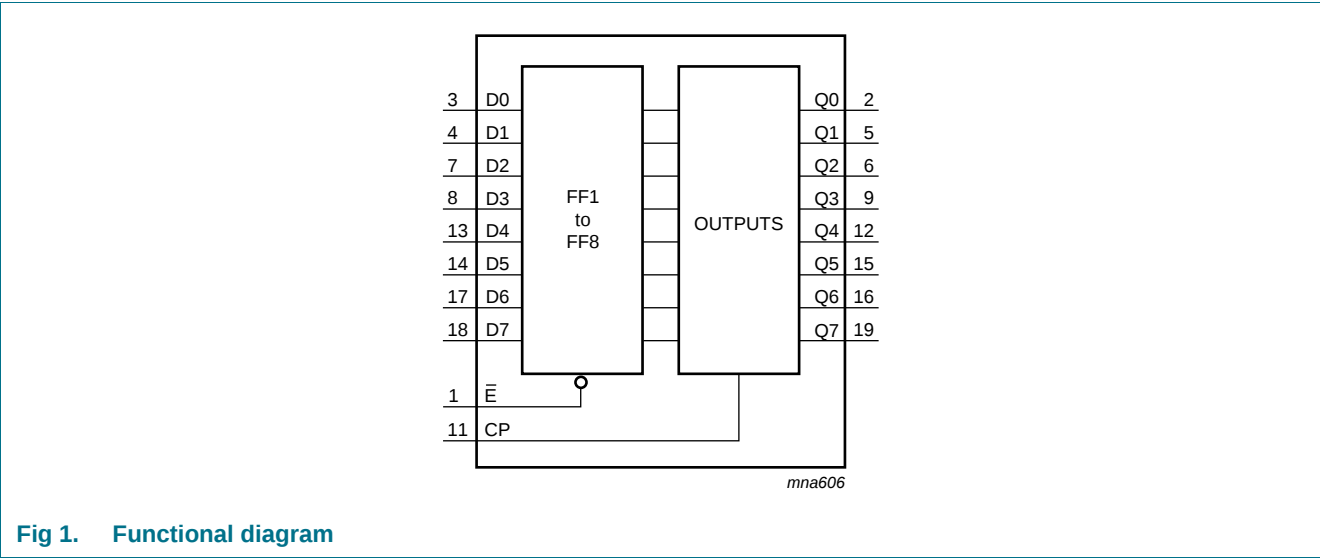


Fig 1. Functional diagram

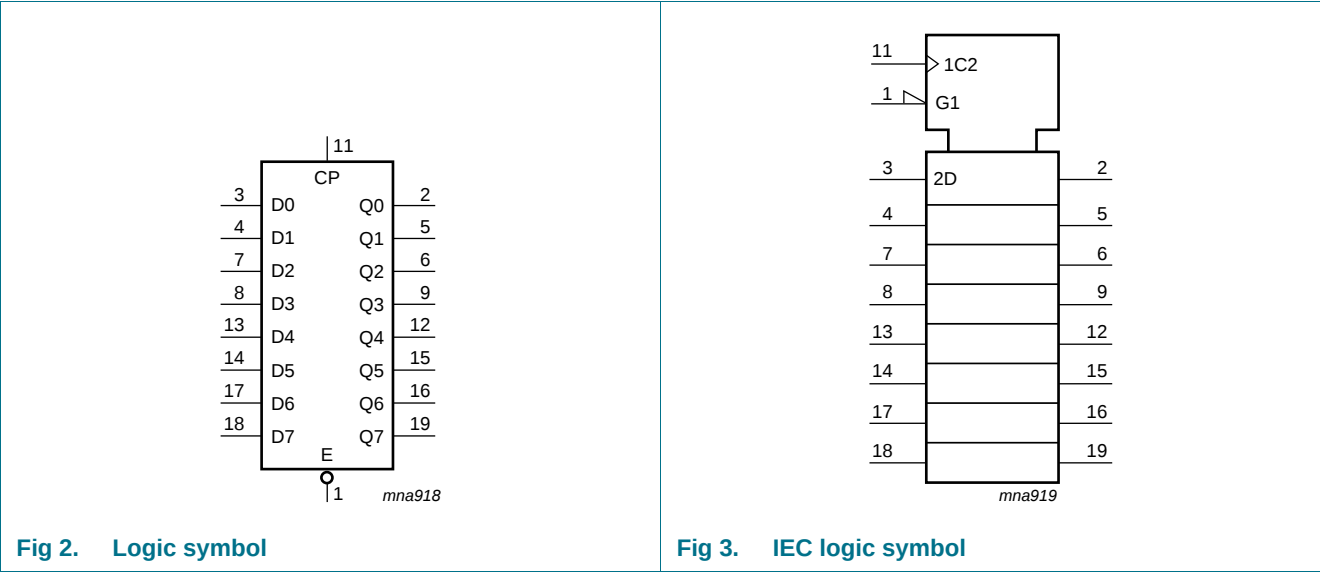


Fig 2. Logic symbol

Fig 3. IEC logic symbol

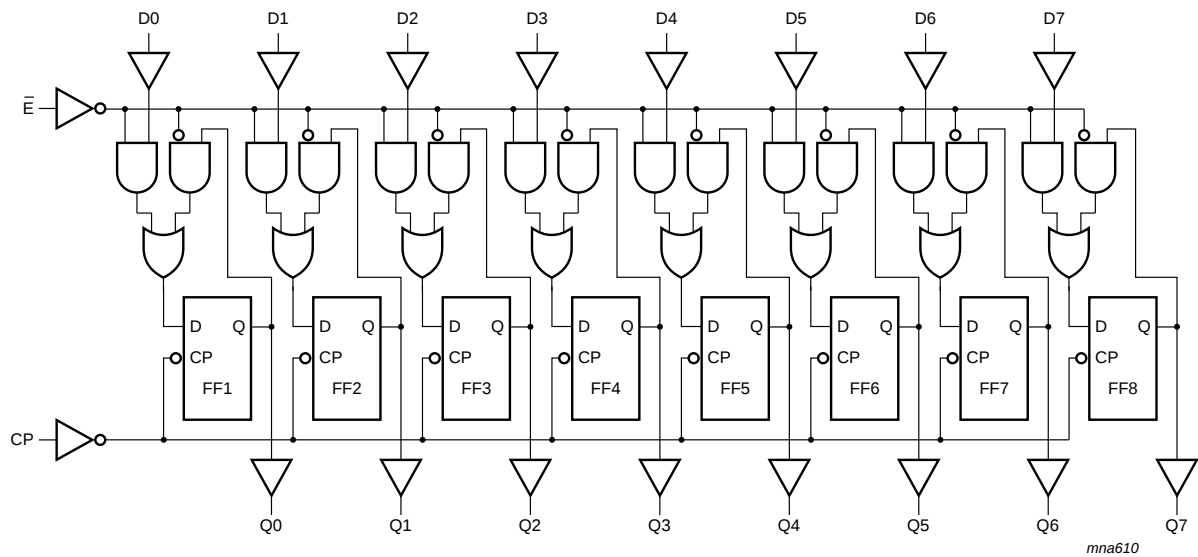


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

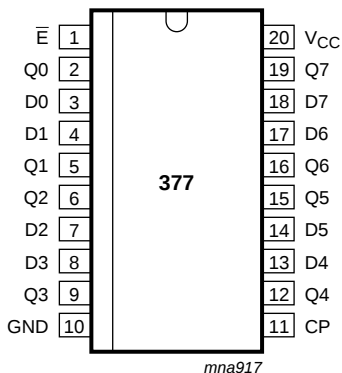


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	1	data enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating modes	Inputs			Outputs
	CP	$\overline{E}$	Dn	Qn
load "1"	↑	L	h	H
load "0"	↑	L	L	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
L = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			
		DIP20 package	[2] -	750	mW
		SO20, SSOP20, TSSOP20	[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 package: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.

[3] For SO20 package: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC377			74HCT377			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

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Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		$\overline{E}$ input	-	150	540	-	675	-	735	μA
		CP input	-	50	180	-	225	-	245	μA
		Dn input	-	20	72	-	90	-	98	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC377										
t _{pd}	propagation delay	CP to Qn; see Figure 6 ^[1]								
		V _{CC} = 2.0 V	-	44	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	16	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	-
		V _{CC} = 6.0 V	-	13	27	-	34	-	41	ns
t _t	transition time	Qn output; see Figure 6 ^[2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
		t _w	pulse width	CP input HIGH or LOW; see Figure 6						
V _{CC} = 2.0 V	80			14	-	100	-	120	-	ns
V _{CC} = 4.5 V	16			5	-	20	-	24	-	ns
V _{CC} = 6.0 V	14			4	-	17	-	20	-	ns
t _{su}	set-up time			Dn to CP; see Figure 7						
		V _{CC} = 2.0 V	60	14	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	4	-	13	-	15	-	ns
	$\overline{E}$ to CP; see Figure 7									
		V _{CC} = 2.0 V	60	6	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	Dn to CP; see Figure 7								
		$V_{CC} = 2.0$ V	3	−8	-	3	-	3	-	ns
		$V_{CC} = 4.5$ V	3	−3	-	3	-	3	-	ns
		$V_{CC} = 6.0$ V	3	−2	-	3	-	3	-	ns
		$\overline{E}$ to CP; see Figure 7								
		$V_{CC} = 2.0$ V	4	−3	-	4	-	4	-	ns
		$V_{CC} = 4.5$ V	4	−1	-	4	-	4	-	ns
f_{max}	maximum frequency	CP input; see Figure 6								
		$V_{CC} = 2.0$ V	6	23	-	5	-	4	-	MHz
		$V_{CC} = 4.5$ V	30	70	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	77	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	83	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	[3]	-	20	-	-	-	-	pF

74HCT377

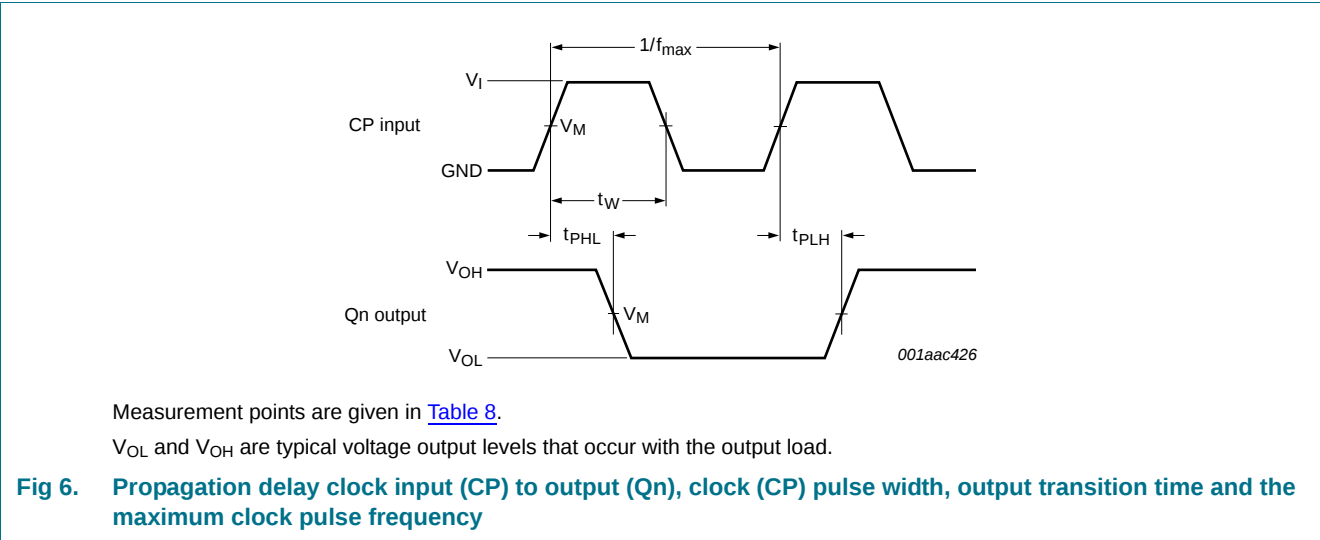
t_{pd}	propagation delay	CP to Qn; see Figure 6	[1]							
		$V_{CC} = 4.5$ V	-	17	32	-	40	-	48	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
t_t	transition time	Qn output; see Figure 6	[2]							
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP input; see Figure 6								
		$V_{CC} = 4.5$ V	20	8	-	25	-	30	-	ns
t_{su}	set-up time	Dn to CP; see Figure 7								
		$V_{CC} = 4.5$ V	12	4	-	15	-	18	-	ns
		$\overline{E}$ to CP; see Figure 7								
t_h	hold time	$V_{CC} = 4.5$ V	22	12	-	28	-	33	-	ns
		Dn to CP; see Figure 7								
		$V_{CC} = 4.5$ V	2	−4	-	2	-	2	-	ns
f_{max}	maximum frequency	$\overline{E}$ to CP; see Figure 7								
		$V_{CC} = 4.5$ V	3	−2	-	3	-	3	-	ns
		CP input; see Figure 6								
f_{max}	maximum frequency	$V_{CC} = 4.5$ V	27	48	-	22	-	18	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	53	-	-	-	-	-	MHz

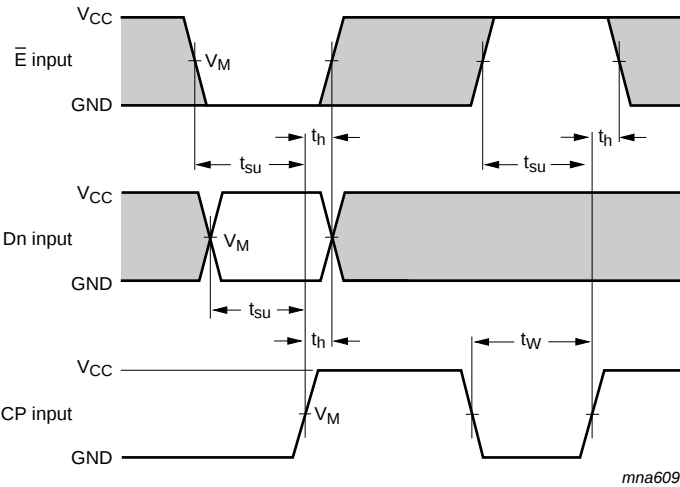
Table 7. Dynamic characteristics ...continued
GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} − 1.5 V	[3]	-	20	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
Σ (C_L × V_{CC}² × f_o) = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

11. Waveforms





Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Data set-up and hold times data input (Dn)

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC377	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT377	3 V	1.3 V	1.3 V

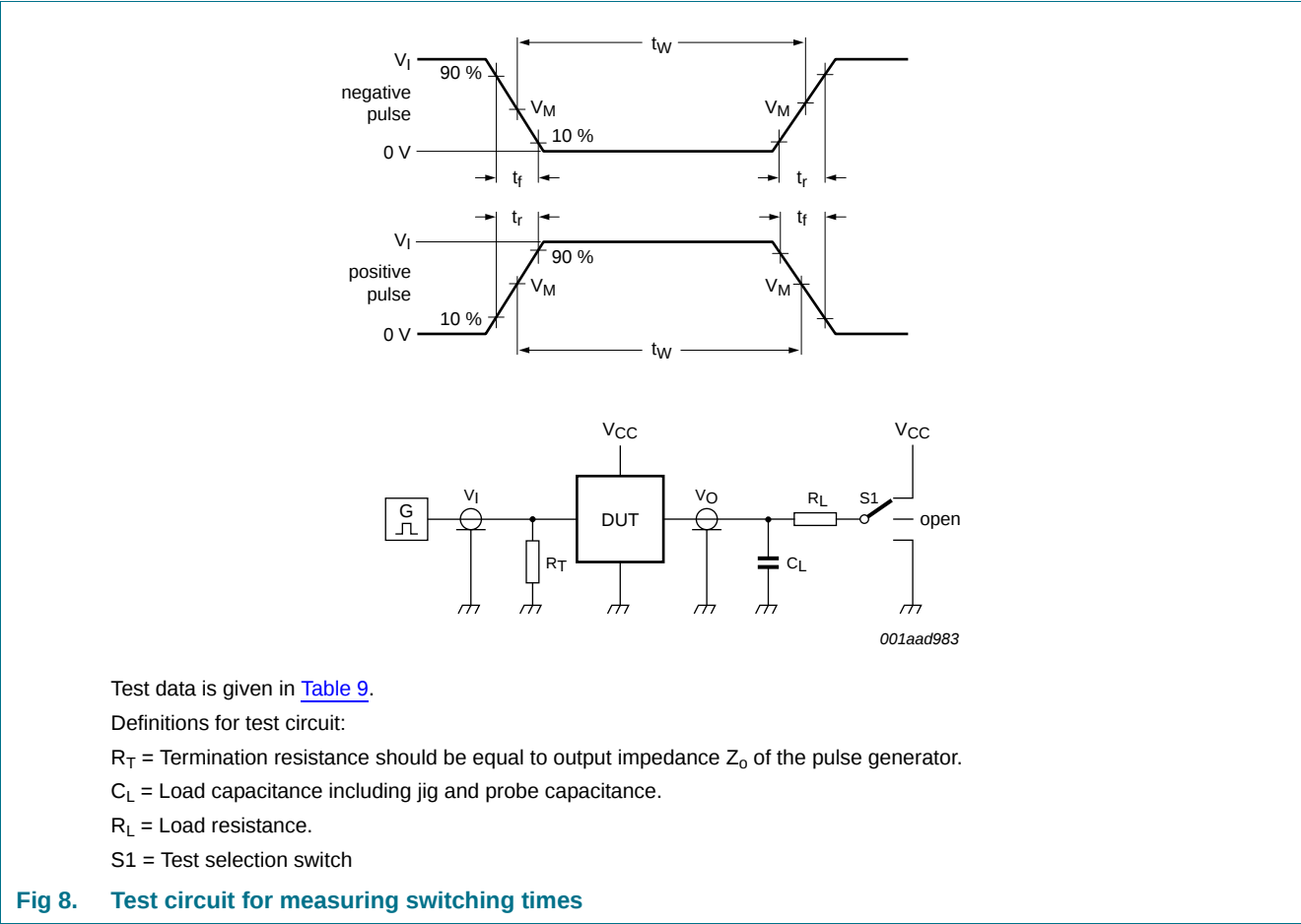


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC377	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT377	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

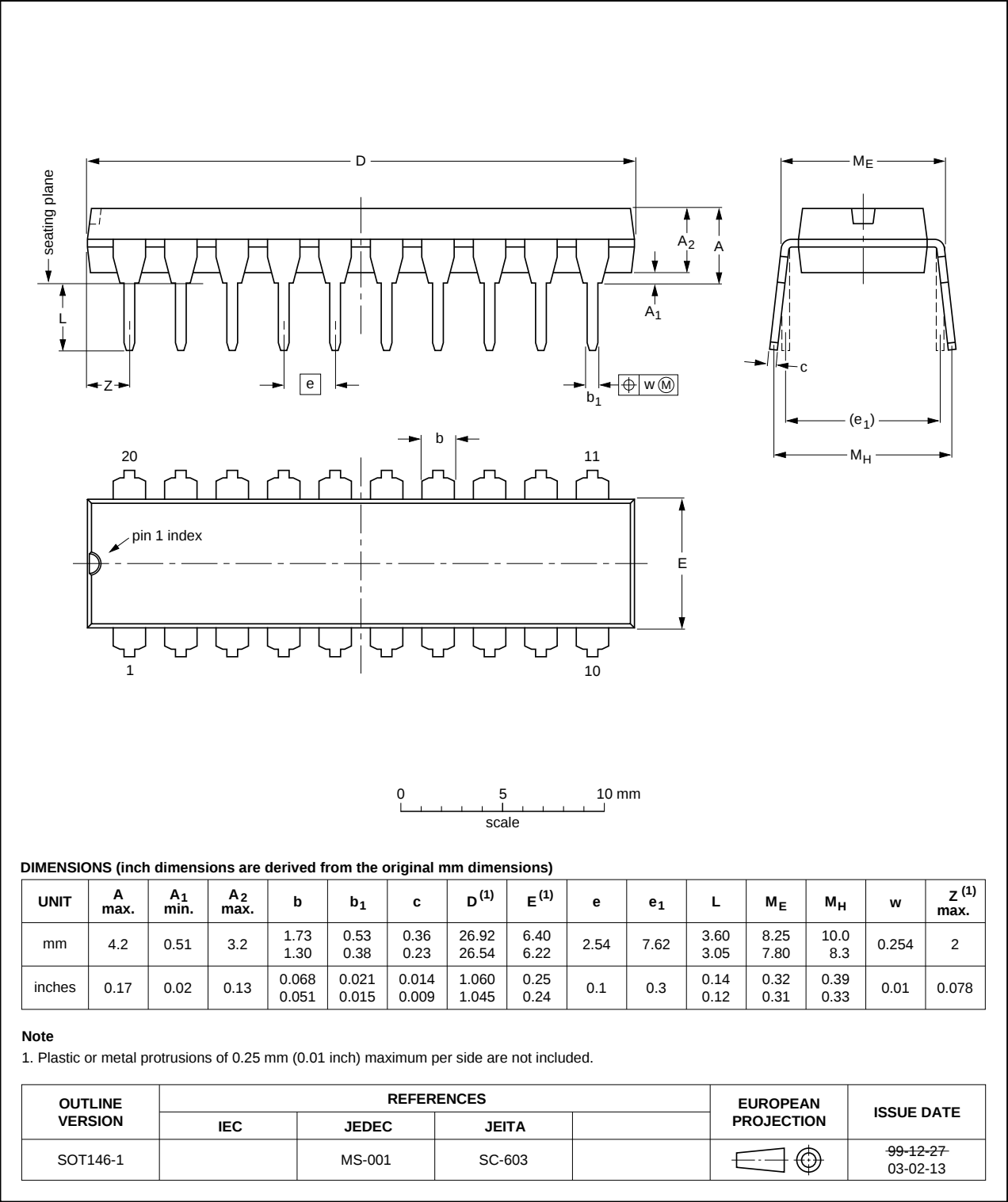
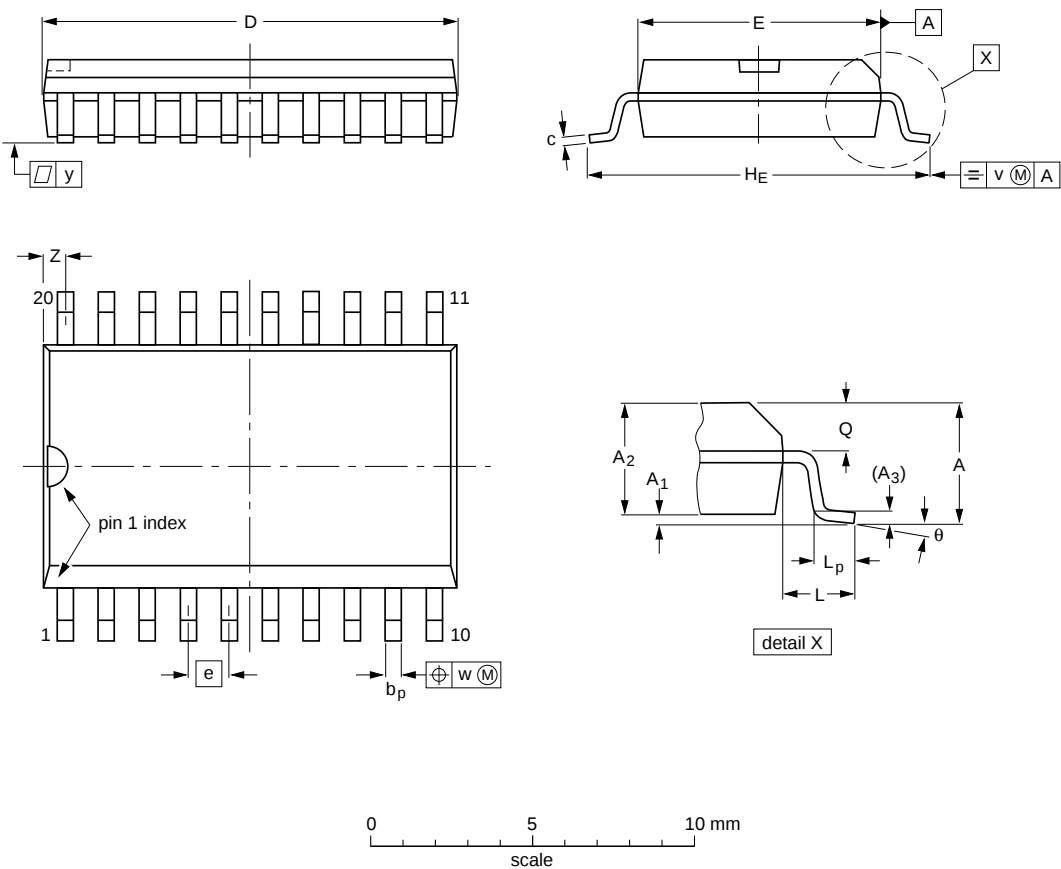


Fig 9. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

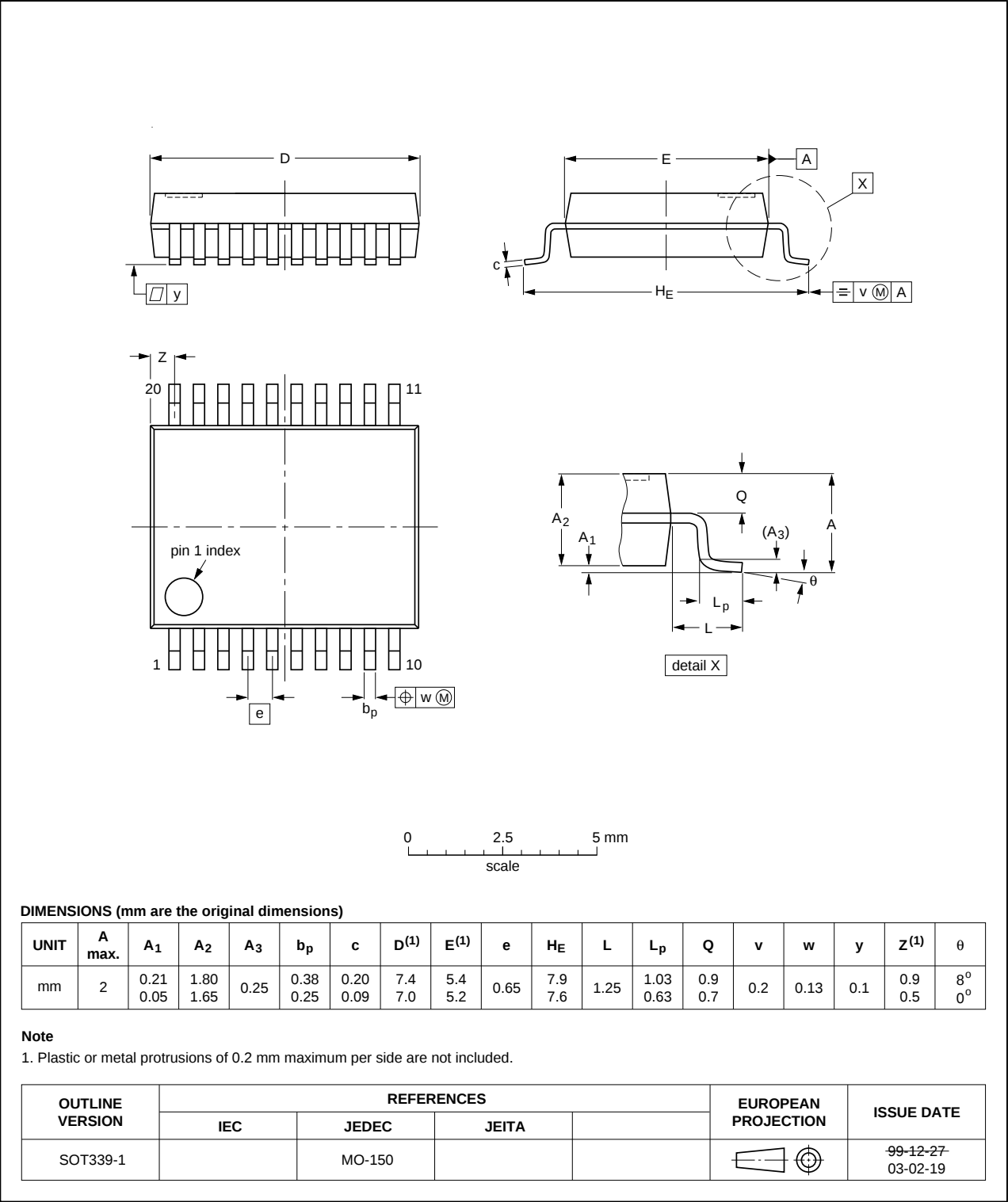


Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

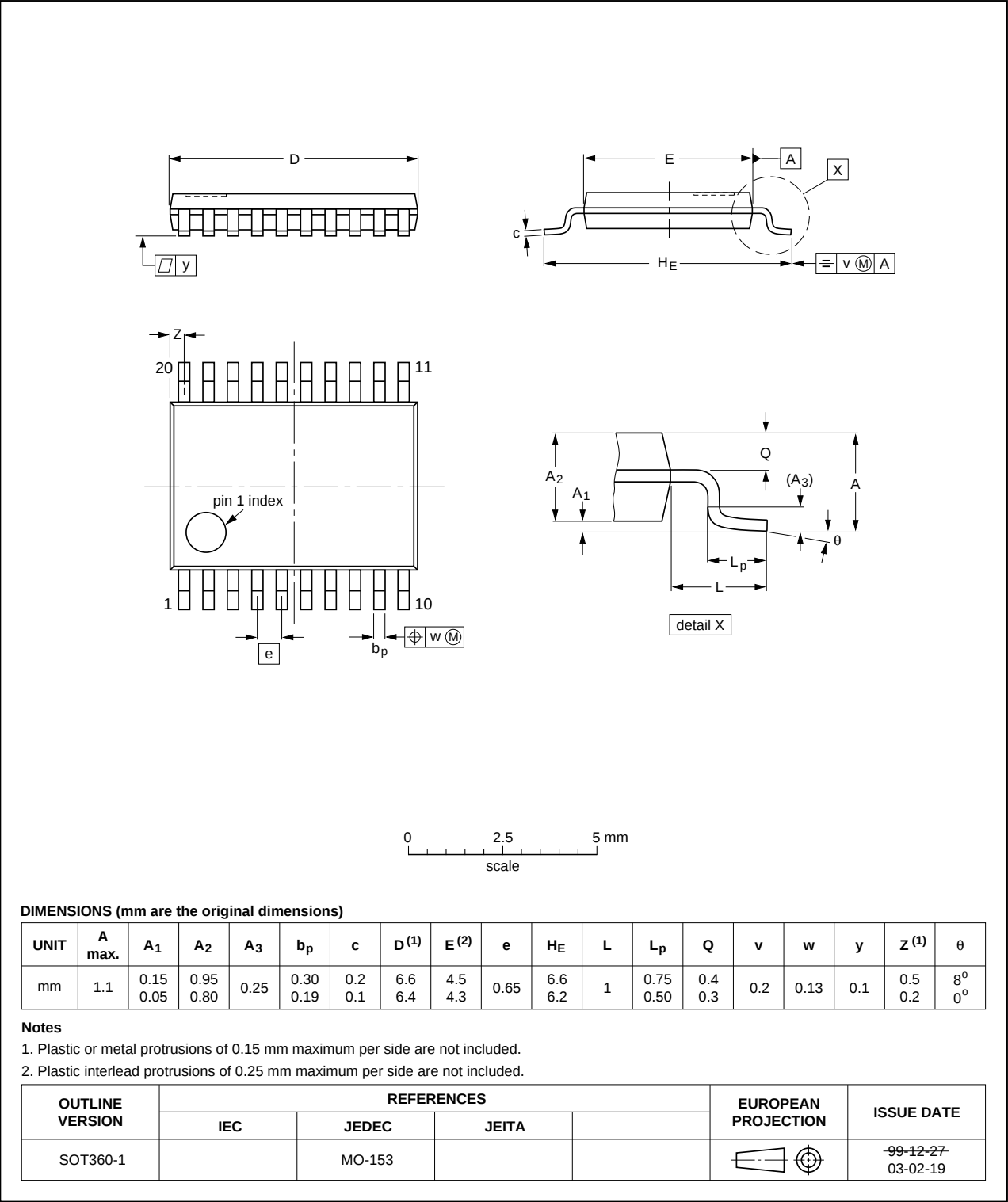


Fig 12. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT377 v.3	20130925	Product data sheet	-	74HC_HCT377_CNV v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT377_CNV v.2	19901227	Product specification	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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