

74HC4852-Q100; 74HCT4852-Q100

Dual 4-channel analog multiplexer/demultiplexer with injection-current effect control

Rev. 1 — 12 July 2012

Product data sheet

1. General description

The 74HC4852-Q100; 74HCT4852-Q100 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7A.

The 74HC4852-Q100; 74HCT4852-Q100 are dual 4-channel analog multiplexers/demultiplexers with common select inputs (S0 and S1). Both multiplexers have a common active LOW enable input ($\overline{E}$), four independent inputs/outputs (nY0 to nY3) and two common inputs/outputs (1Z, 2Z). The devices feature injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With $\overline{E}$ LOW, two of the eight switches are selected (low impedance ON-state) by S0 and S1. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 and S1.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Injection-current cross coupling $< 1\text{ mV/mA}$
- Wide supply voltage range from 2.0 V to 6.0 V for 74HC4852-Q100
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pf}$, $R = 0\text{ }\Omega$)
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- Low ON-state resistance:
 - ◆ $400\text{ }\Omega$ (typical) at $V_{CC} = 2.0\text{ V}$
 - ◆ $215\text{ }\Omega$ (typical) at $V_{CC} = 3.0\text{ V}$
 - ◆ $120\text{ }\Omega$ (typical) at $V_{CC} = 3.3\text{ V}$
 - ◆ $76\text{ }\Omega$ (typical) at $V_{CC} = 4.5\text{ V}$
 - ◆ $59\text{ }\Omega$ (typical) at $V_{CC} = 6.0\text{ V}$



3. Applications

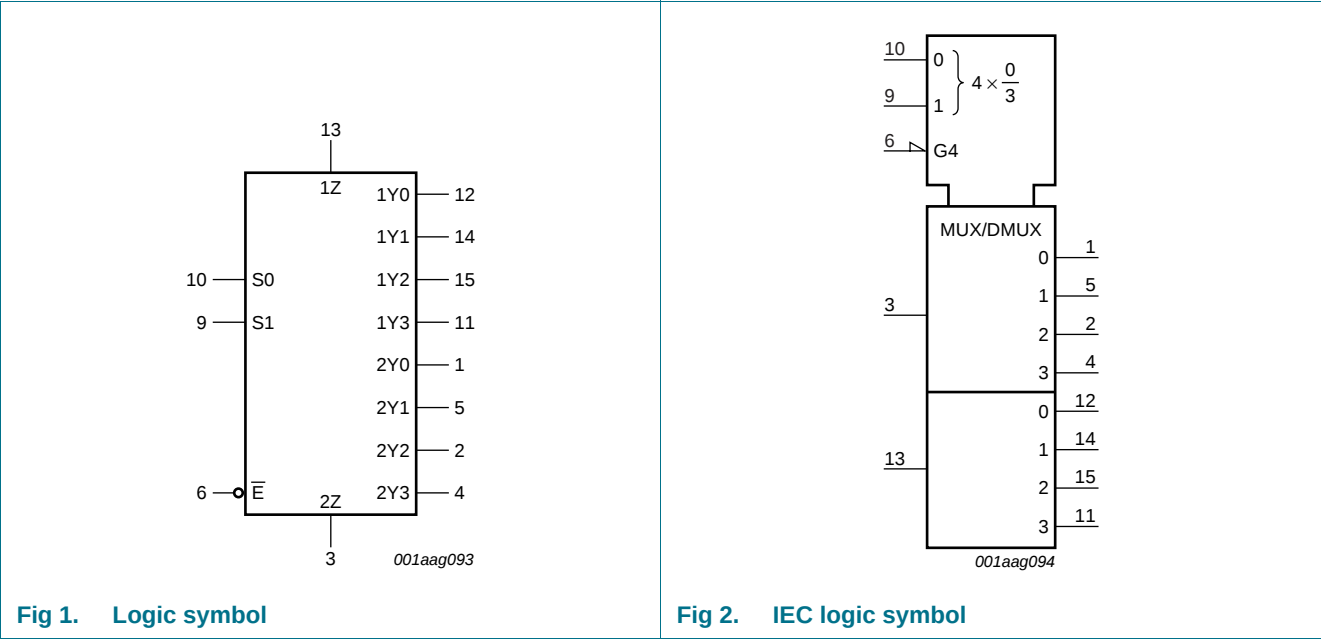
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Automotive application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4852D-Q100 74HCT4852D-Q100	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4852PW-Q100 74HCT4852PW-Q100	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4852BQ-Q100 74HCT4852BQ-Q100	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram



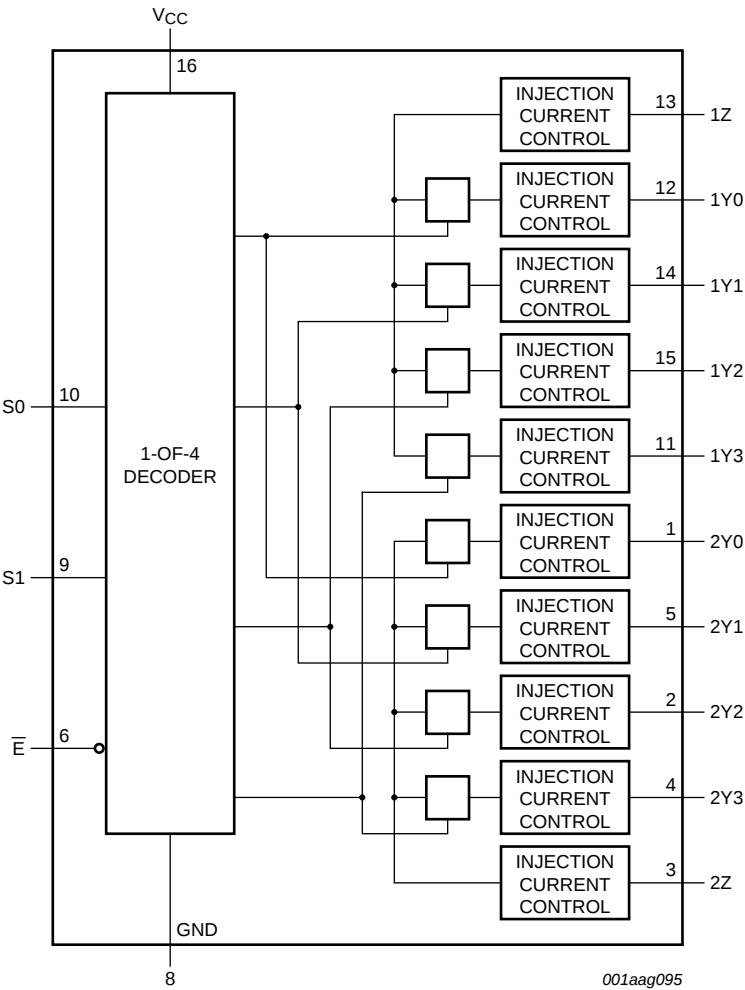


Fig 3. Functional diagram

6. Pinning information

6.1 Pinning

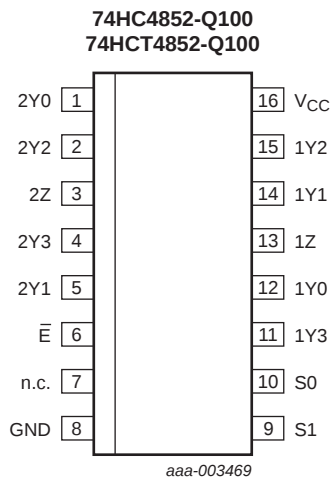
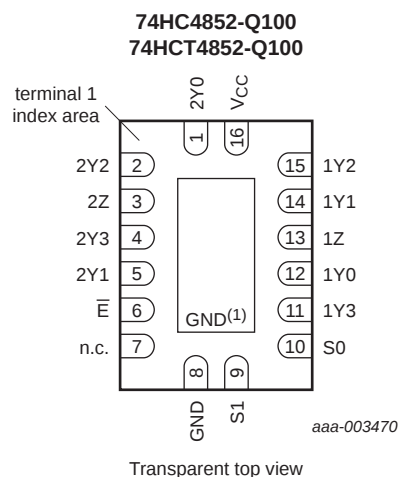


Fig 4. Pin configuration SO16 and TSSOP16



- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input/output
2Y2	2	independent input/output
2Z	3	common input/output
2Y3	4	independent input/output
2Y1	5	independent input/output
$\bar{E}$	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S1	9	select input
S0	10	select input
1Y3	11	independent input/output
1Y0	12	independent input/output
1Z	13	common input/output
1Y1	14	independent input/output
1Y2	15	independent input/output
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Input			Channel ON
$\overline{E}$	S1	S0	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	-

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		^[1] -0.5	$V_{CC} + 0.5$	V
V_{SW}	switch voltage		^[2] -0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5 \text{ V}$ or $V_{SW} > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_{SW}	switch current	$V_{SW} > -0.5 \text{ V}$ or $V_{SW} < V_{CC} + 0.5 \text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$	^[3] -	500	mW

- [1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.
 [2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.
 [3] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4852-Q100			74HCT4852-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	-	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	6.0	1000	-	-	-	ns/V
		$V_{CC} = 3.0\text{ V}$	-	6.0	800	-	-	-	ns/V
		$V_{CC} = 3.3\text{ V}$	-	6.0	800	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	-	6.0	500	ns/V
		$V_{CC} = 6.0\text{ V}$	-	6.0	400	-	-	-	ns/V

10. Static characteristics

Table 6. R_{ON} resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	

74HC4852-Q100

$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\bar{E} = V_{IL}$								
		$V_{CC} = 2.0\text{ V}; I_{SW} = 2\text{ mA}$	-	400	650	-	670	-	700	Ω
		$V_{CC} = 3.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	215	330	-	360	-	380	Ω
		$V_{CC} = 3.3\text{ V}; I_{SW} \leq 2\text{ mA}$	-	120	270	-	305	-	345	Ω
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	76	210	-	240	-	270	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}; \bar{E} = V_{IL}$								
		$V_{CC} = 2.0\text{ V}; I_{SW} = 2\text{ mA}$	-	4	10	-	15	-	20	Ω
		$V_{CC} = 3.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	-	12	-	16	Ω
		$V_{CC} = 3.3\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	-	12	-	16	Ω
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	-	12	-	16	Ω
		$V_{CC} = 6.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	3	9	-	13	-	18	Ω

74HCT4852-Q100

$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\bar{E} = V_{IL}$								
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	76	210	-	240	-	270	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}; \bar{E} = V_{IL}$								
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	-	12	-	16	Ω

Table 7. Injection current couplingAt recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	74HC4852/Q100			74HCT4852/Q100			Unit
			Min	Typ ^[1]	Max	Min	Typ ^[1]	Max	
T _{amb} = −40 °C to +125 °C									
ΔV _O	output voltage variation	I _{SW} ≤ 1 mA; R _S ≤ 3.9 kΩ [2][3]							
		V _{CC} = 3.3 V	-	0.05	1	-	-	-	mV
		V _{CC} = 5.0 V	-	0.03	1	-	0.03	1	mV
		I _{SW} ≤ 10 mA; R _S ≤ 3.9 kΩ							
		V _{CC} = 3.3 V	-	0.55	5	-	-	-	mV
		V _{CC} = 5.0 V	-	0.27	5	-	0.27	5	mV
		I _{SW} ≤ 1 mA; R _S ≤ 20 kΩ							
		V _{CC} = 3.3 V	-	0.04	2	-	-	-	mV
		V _{CC} = 5.0 V	-	0.03	2	-	0.03	2	mV
		I _{SW} ≤ 10 mA; R _S ≤ 20 kΩ							
		V _{CC} = 3.3 V	-	0.56	20	-	-	-	mV
		V _{CC} = 5.0 V	-	0.48	20	-	0.48	20	mV

[1] Typical values are measured at T_{amb} = 25 °C.[2] ΔV_O here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.[3] I_{SW} = total current injected into all disabled channels.**Table 8. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol Parameter Conditions			25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4852-Q100										
V _{IH}	HIGH-level input voltage	control inputs								
		V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 3.3 V	2.3	-	-	2.3	-	2.3	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	-	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	control inputs								
		V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 3.3 V	-	-	1.0	-	1.0	-	1.0	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	-	1.8	-	1.8	V
I _I	input leakage current	control inputs; V _I = GND or V _{CC}								
		V _{CC} = 6.0 V	-	-	±0.1	-	±0.1	-	±1.0	μA

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{S(OFF)}	OFF-state leakage current	$\bar{E} = V_{IH}$; V _I = GND or V _{CC} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V; see Figure 6								
		nYn; per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		nZ; all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
I _{S(ON)}	ON-state leakage current	$\bar{E} = V_{IL}$; V _I = GND or V _{CC} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V; see Figure 7	-	-	±0.1	-	±0.5	-	±1.0	μA
I _{CC}	supply current	V _I = GND or V _{CC}								
		V _{CC} = 6.0 V	-	-	2.0	-	5.0	-	20.0	μA
C _I	input capacitance	S0, S1, S2 and $\bar{E}$	-	2	10	-	10	-	10	pF
C _{SW}	switch capacitance	nZ; OFF-state	-	15	40	-	40	-	40	pF
		nYn; OFF-state	-	3	15	-	15	-	15	pF
74HCT4852-Q100										
V _{IH}	HIGH-level input voltage	control inputs								
		V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	control inputs								
		V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
I _I	input leakage current	control inputs; V _I = GND or V _{CC}								
		V _{CC} = 5.5 V	-	-	±0.1	-	±0.1	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	$\bar{E} = V_{IH}$; V _I = GND or V _{CC} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V; see Figure 6								
		per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
I _{S(ON)}	ON-state leakage current	$\bar{E} = V_{IL}$; V _I = GND or V _{CC} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V; see Figure 7	-	-	±0.1	-	±0.5	-	±1.0	μA
I _{CC}	supply current	V _I = GND or V _{CC}								
		V _{CC} = 5.5 V	-	-	2.0	-	5.0	-	20.0	μA
ΔI _{CC}	additional supply current	control inputs; V _I = V _{CC} − 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A	-	-	300	-	370	-	370	μA
C _I	input capacitance	S0, S1, S2 and $\bar{E}$	-	2	10	-	10	-	10	pF
C _{SW}	switch capacitance	nZ; OFF-state	-	9	40	-	40	-	40	pF
		nYn; OFF-state	-	3	15	-	15	-	15	pF

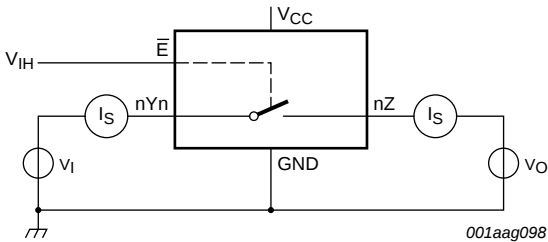


Fig 6. Test circuit for measuring OFF-state leakage current

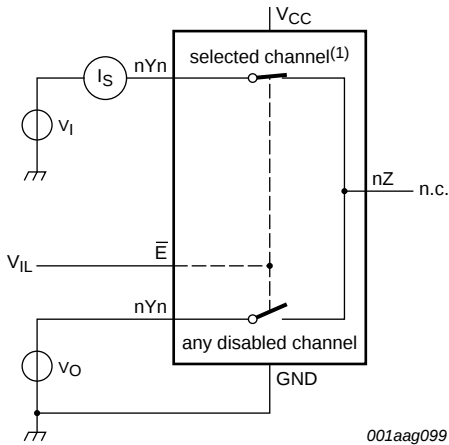
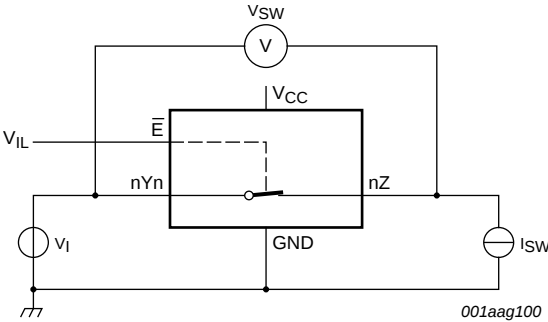
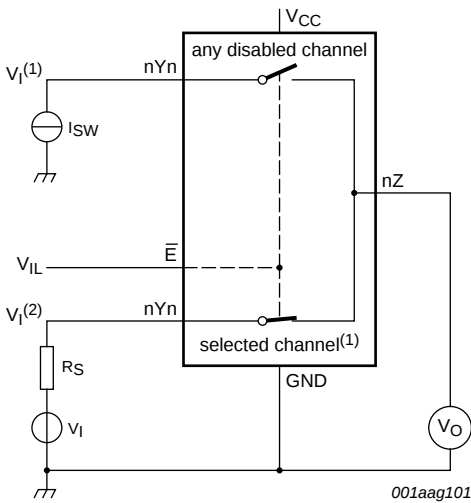


Fig 7. Test circuit for measuring ON-state leakage current



$$R_{ON} = V_{SW} / I_{SW}.$$

Fig 8. Test circuit for measuring ON resistance



(1) Channel is selected by S0 and S1.
 $V_i^{(1)} < GND$ or $V_i^{(1)} > V_{CC}$.
 $GND < V_i^{(2)} < V_{CC}$.

Fig 9. Test circuit for injection current coupling

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for load circuit see [Figure 14](#).

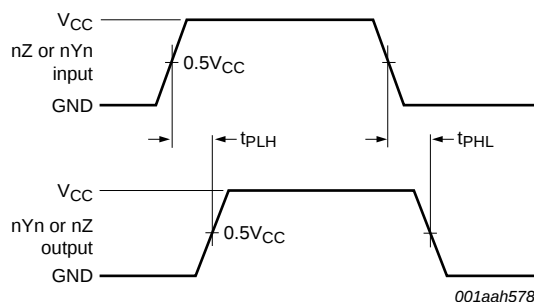
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4852-Q100										
t _{pd}	propagation delay	nZ, nYn to nYn, nZ; see Figure 10 [1]								
		V _{CC} = 2.0 V	2.2	9.3	33	2.2	34	2.2	35	ns
		V _{CC} = 3.0 V	2.2	4.9	16.5	1.9	18	1.9	19.5	ns
		V _{CC} = 3.3 V	2.0	4.4	15.0	1.6	16.5	1.6	18.5	ns
		V _{CC} = 4.5 V	1.6	3.2	11.6	1.1	12.5	1.1	13.5	ns
		V _{CC} = 6.0 V	1.5	2.5	10.2	0.9	11	0.9	12	ns
		Sn to nZ, nYn; see Figure 11 [1]								
		V _{CC} = 2.0 V	7.7	16.8	38	6.3	40	6.3	42	ns
		V _{CC} = 3.0 V	4.9	8.8	20	3.9	21.5	3.9	23	ns
		V _{CC} = 3.3 V	4.4	7.9	17.5	3.4	19	3.4	22	ns
		V _{CC} = 4.5 V	3.2	5.8	14	2.3	15	2.3	17	ns
		V _{CC} = 6.0 V	2.4	4.8	12.6	1.6	14.5	1.6	16.5	ns
t _{en}	enable time	$\overline{E}$ to nZ, nYn; see Figure 12 [2]								
		V _{CC} = 2.0 V	10.5	20.5	47.5	8.5	52.5	8.5	57.5	ns
		V _{CC} = 3.0 V	6.2	10.6	45	5.2	50	5.2	55	ns
		V _{CC} = 3.3 V	5.6	9.4	42.5	4.6	47.5	4.6	52.5	ns
		V _{CC} = 4.5 V	4.2	6.9	40	3	45	3	50	ns
		V _{CC} = 6.0 V	3.2	5.6	39	2.2	40	2.2	40	ns
t _{dis}	disable time	$\overline{E}$ to nZ, nYn; see Figure 12 [3]								
		V _{CC} = 2.0 V	39.5	75.4	100	39.3	105	39	115	ns
		V _{CC} = 3.0 V	35.2	69.5	90	35.5	100	35	110	ns
		V _{CC} = 3.3 V	34.6	68.1	85	34.6	95	34.5	105	ns
		V _{CC} = 4.5 V	28.5	63	80	28.2	90	28	100	ns
		V _{CC} = 6.0 V	14.4	57.9	78	13.5	80	13.0	80	ns
C _{PD}	power dissipation capacitance	per channel; see Figure 13 [4]								
		V _{CC} = 3.3 V	-	42	-	-	-	-	-	pF
		V _{CC} = 5.0 V	-	47	-	-	-	-	-	pF

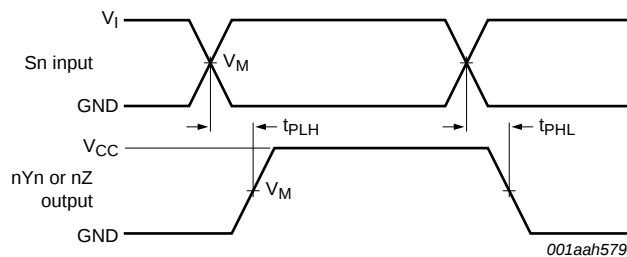
Table 9. Dynamic characteristics ...continuedAt recommended operating conditions; voltages are referenced to GND (ground 0 V); for load circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4852-Q100										
t _{pd}	propagation delay	nZ, nYn to nYn, nZ; see Figure 10 [1]								
		V _{CC} = 4.5 V	1.6	3.5	11.5	1.1	12.5	1.1	13.5	ns
		Sn to nZ, nYn; see Figure 11 [1]								
		V _{CC} = 4.5 V	3.2	7.6	13	2.3	15	1.6	17	ns
t _{en}	enable time	$\overline{E}$ to nZ, nYn; see Figure 12 [2]								
		V _{CC} = 4.5 V	4.2	8.3	25	3.0	30	3.0	35	ns
t _{dis}	disable time	$\overline{E}$ to nZ, nYn; see Figure 12 [3]								
		V _{CC} = 4.5 V	28.5	61.8	80	28.2	90	28.0	100	ns
C _{PD}	power dissipation capacitance	per channel; see Figure 13 [4]								
		V _{CC} = 5.0 V	-	47	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .[2] t_{en} is the same as t_{PZH} and t_{PZL} .[3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; $\sum \{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$ = sum of outputs; C_L = output load capacitance in pF; C_{SW} = switch capacitance in pF; V_{CC} = supply voltage in V.

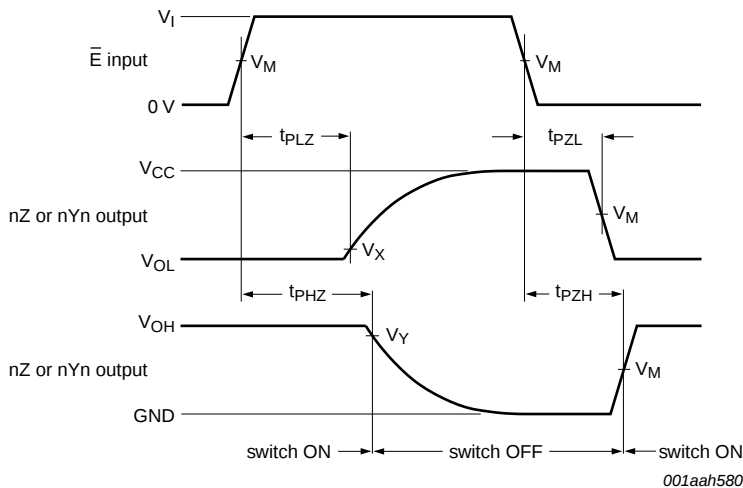
12. Waveforms

**Fig 10. Input (nZ, nYn) to output (nYn, nZ) propagation delays**



Measurement points are given in [Table 10](#).

Fig 11. Input (Sn) to output (nYn, nZ) propagation delays



Measurement points are shown in [Table 10](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Enable and disable times

Table 10. Measurement points

Type	Input		Output		
	V _M	V _I	V _M	V _X	V _Y
74HC4852-Q100	0.5V _{CC}	V _{CC}	0.5V _{CC}	V _{OL} + 0.1(V _{CC} – V _{OL})	0.9V _{OH}
74HCT4852-Q100	1.3 V	3.0 V	0.5V _{CC}	V _{OL} + 0.1(V _{CC} – V _{OL})	0.9V _{OH}

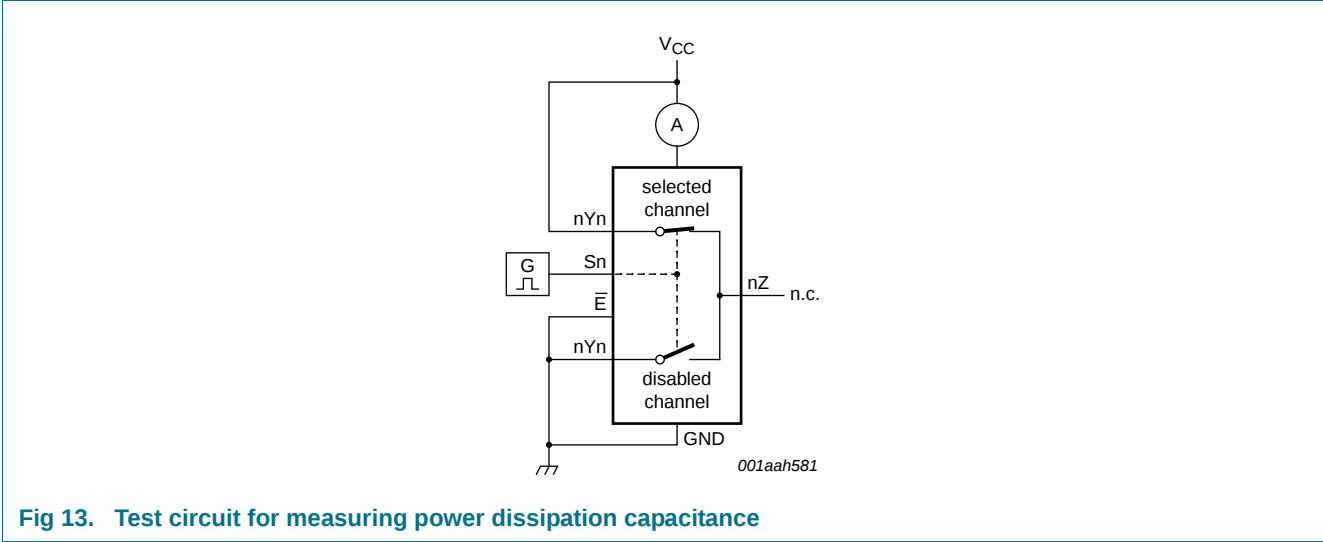
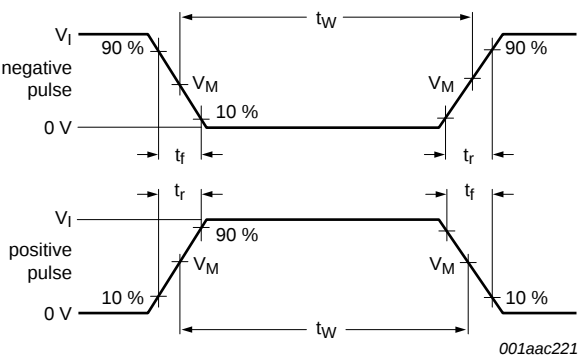
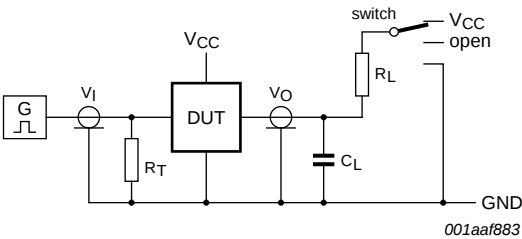


Fig 13. Test circuit for measuring power dissipation capacitance



a. Input pulse definition



Definitions for test circuit:

- R_L = load resistance.
- C_L = load capacitance including jig and probe capacitance.
- R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

b. Load circuit

Test data is given in [Table 11](#).

Fig 14. Input pulse definition and load circuit

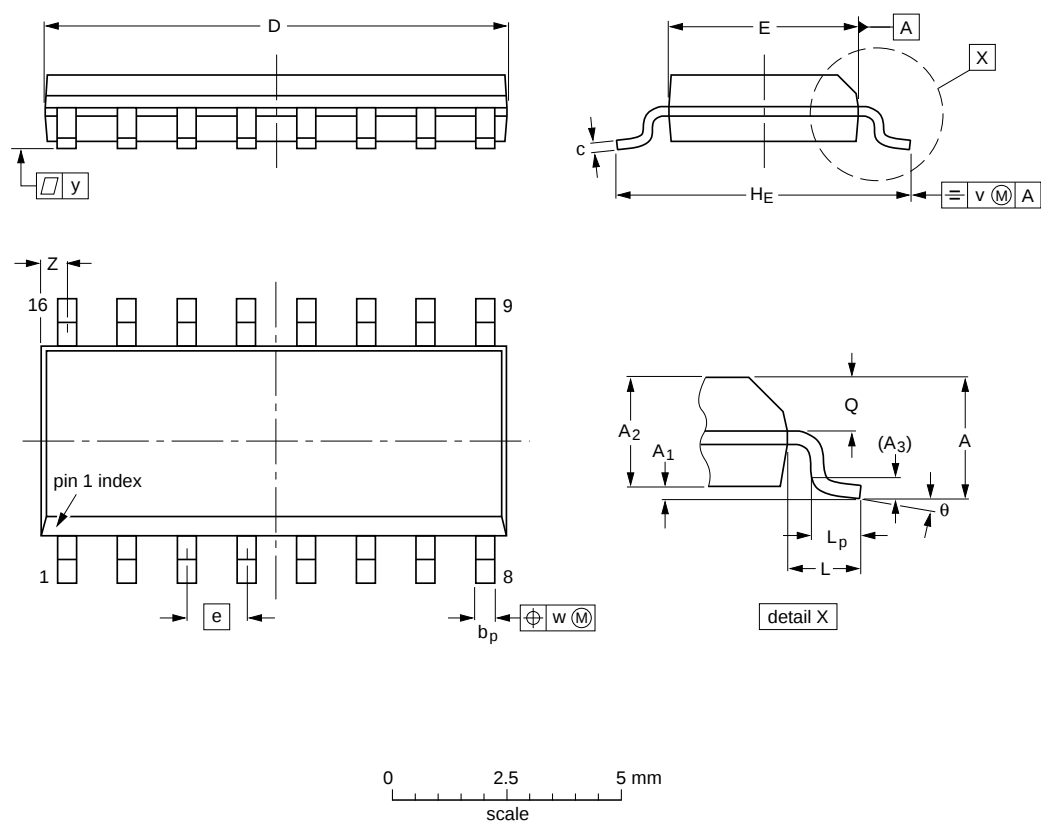
Table 11. Test data

Test	Input			Output		S1 position
	Control $\bar{E}$, Sn	Switch nYn (nZ)	t_r , t_f	Switch nZ (nYn)		
	V_I ^[1]	V_I		C_L	R_L	
t_{PHL} , t_{PLH}	V_{CC}	V_{CC}	6 ns	50 pF	-	open
t_{PHZ} , t_{PZH}	V_{CC}	V_{CC}	6 ns	50 pF	10 kΩ	GND
t_{PLZ} , t_{PZL}	V_{CC}	V_{CC}	6 ns	50 pF	10 kΩ	V_{CC}
C_{PD}	V_{CC}	V_{CC}	6 ns	0 pF	-	open

[1] For 74HCT4852-Q100: input voltage $V_I = 3.0$ V.

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

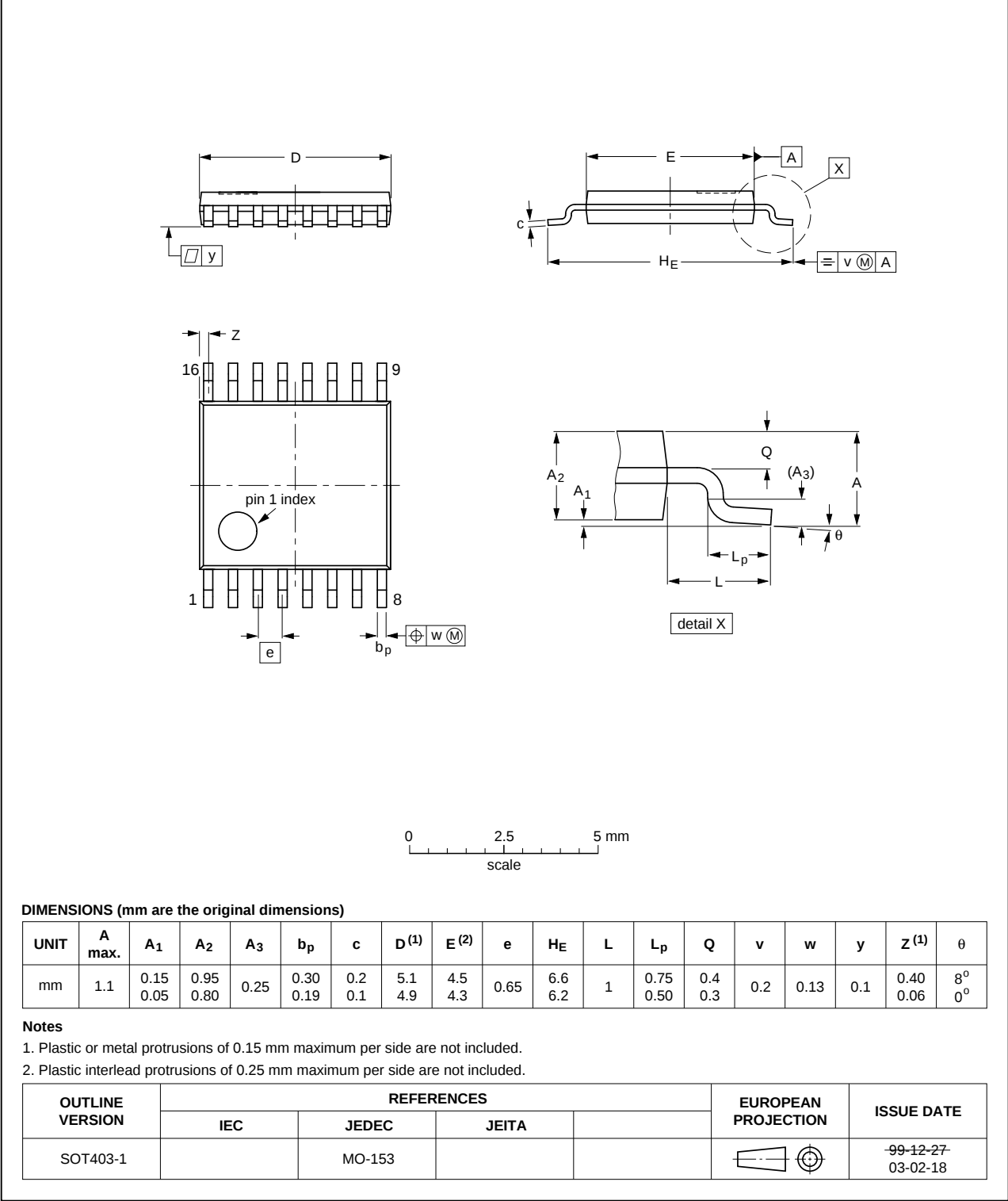


Fig 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

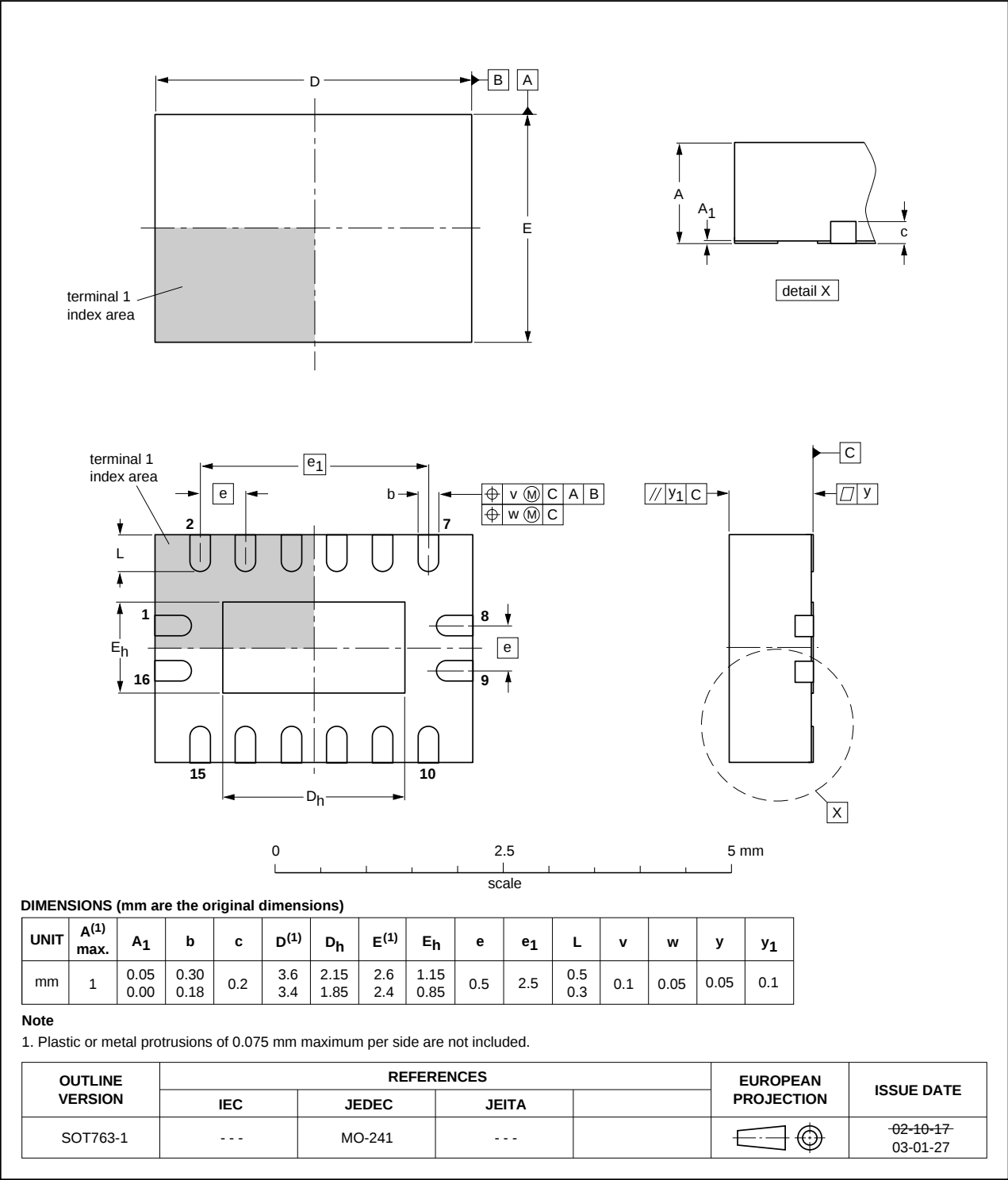


Fig 17. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4852_Q100_1	20120712	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	4
6.1	Pinning	4
6.2	Pin description	4
7	Functional description	5
8	Limiting values	5
9	Recommended operating conditions	6
10	Static characteristics	6
11	Dynamic characteristics	10
12	Waveforms	11
13	Package outline	15
14	Abbreviations	18
15	Revision history	18
16	Legal information	19
16.1	Data sheet status	19
16.2	Definitions	19
16.3	Disclaimers	19
16.4	Trademarks	20
17	Contact information	20
18	Contents	21

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 12 July 2012

Document identifier: 74HC_HCT4852_Q100