

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT688** 8-bit magnitude comparator

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit magnitude comparator

## 74HC/HCT688

## FEATURES

- Compare two 8-bit words
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words.

The output provides  $\overline{P = Q}$ .

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	P <sub>n</sub> , Q <sub>n</sub> to $\overline{P = Q}$		17	17	ns
	E to $\overline{P = Q}$		8	12	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	30	30	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \quad \text{where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

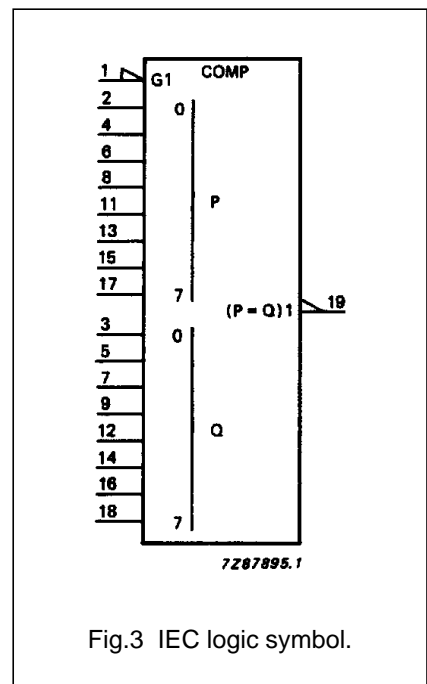
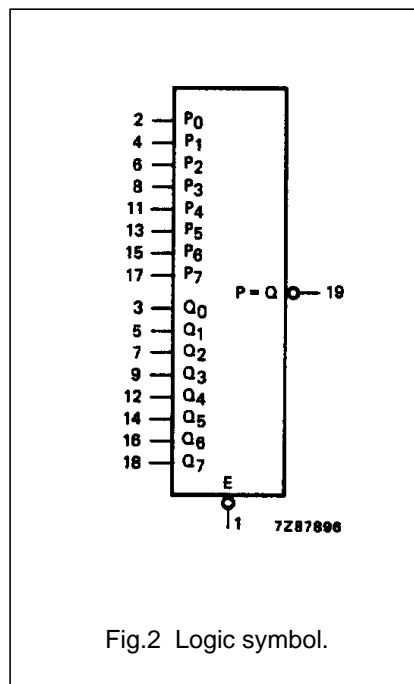
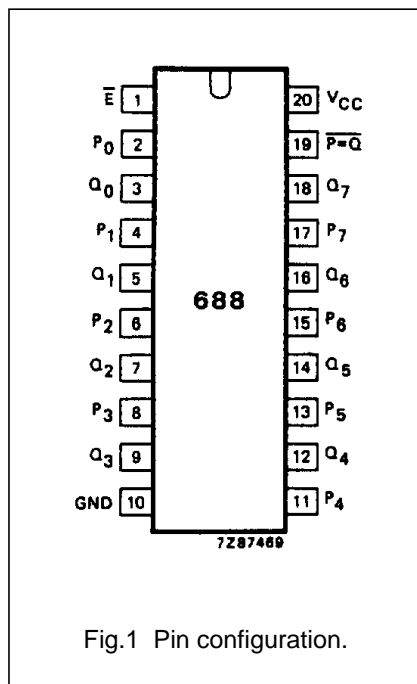
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 8-bit magnitude comparator

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	$P_0$ to $P_7$	word inputs
3, 5, 7, 9, 12, 14, 16, 18	$Q_0$ to $Q_7$	word inputs
10	GND	ground (0 V)
19	$\overline{P = Q}$	equal to output
20	$V_{CC}$	positive supply voltage



8-bit magnitude comparator

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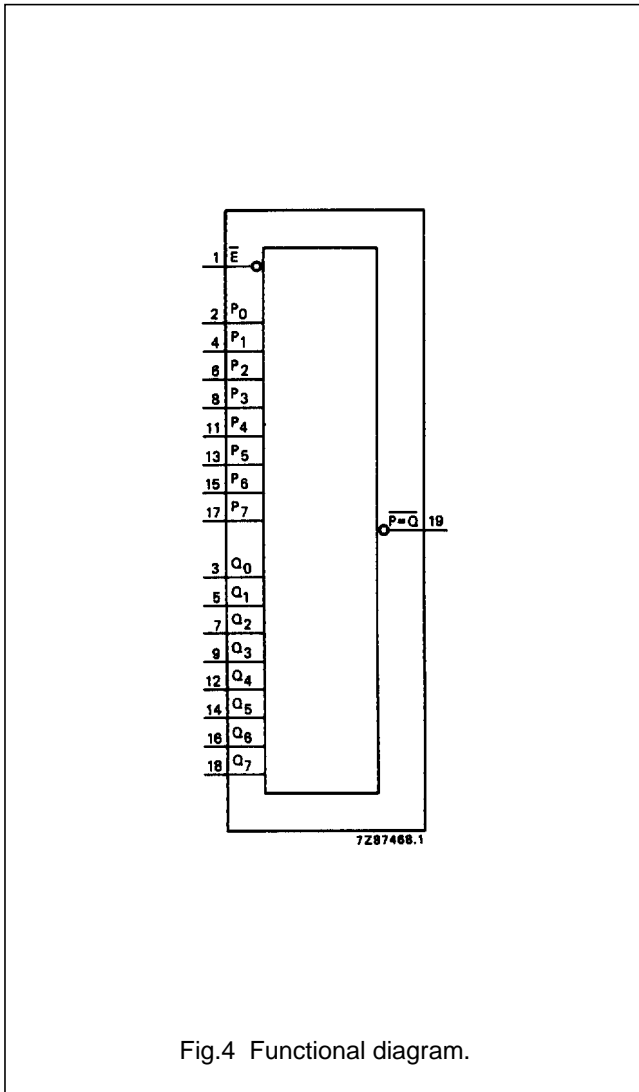


Fig.4 Functional diagram.

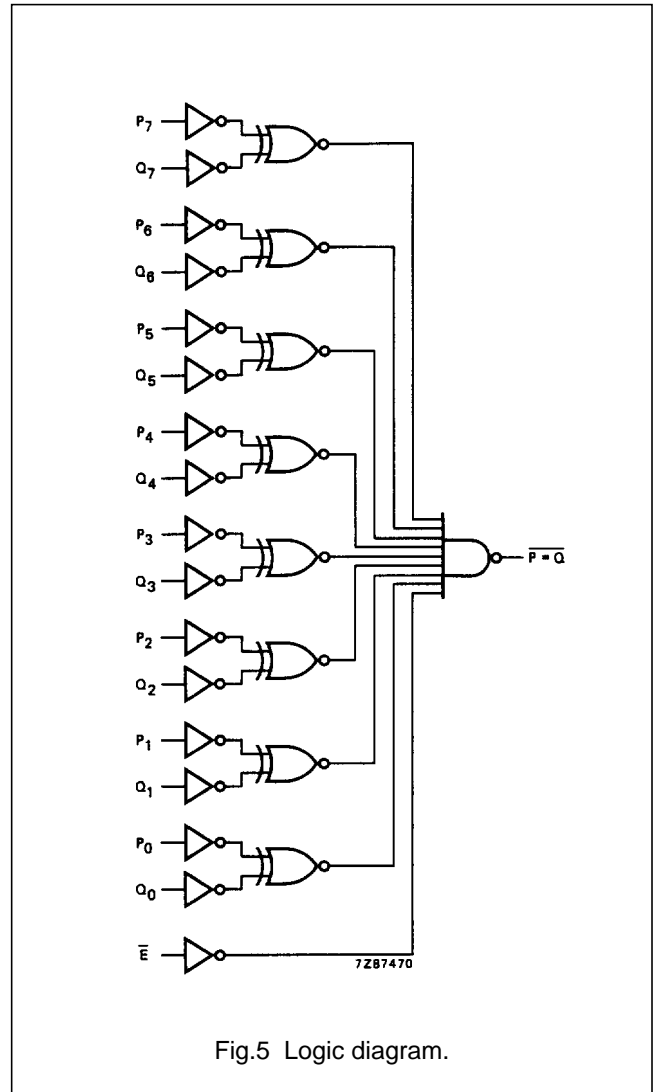


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P <sub>n</sub> , Q <sub>n</sub>	ENABLE Ē	P = Q̄
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care

## 8-bit magnitude comparator

## 74HC/HCT688

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> , Q <sub>n</sub> to $\overline{P} = \overline{Q}$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{E}$ to P = Q		28 10 8	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

## 8-bit magnitude comparator

## 74HC/HCT688

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$P_n$	0.35
$Q_n$	0.35
$\bar{E}$	0.70

**AC CHARACTERISTICS FOR 74HCT**

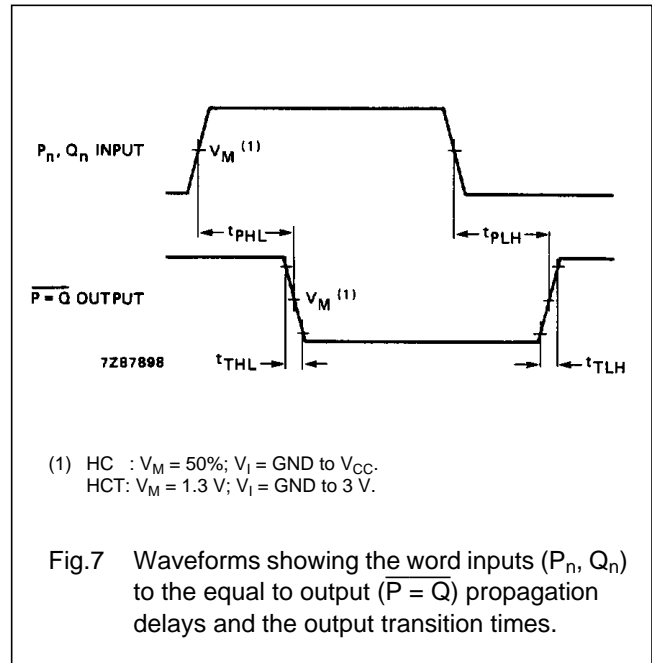
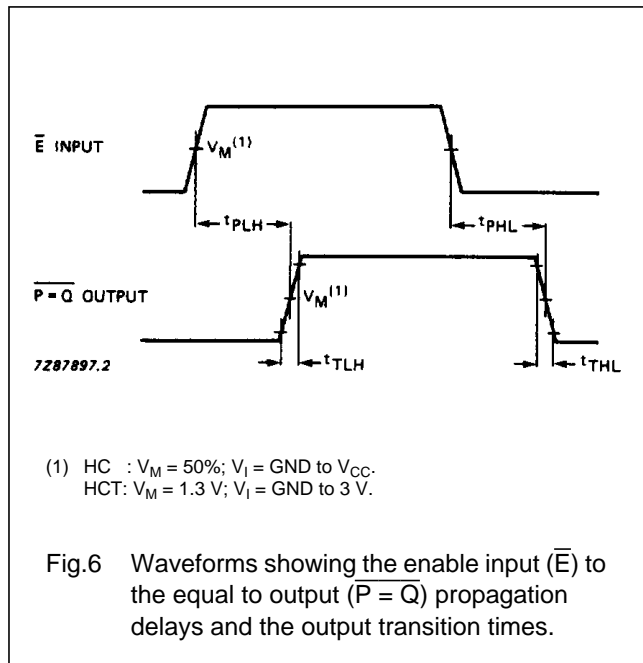
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $P_n, Q_n$ to $\bar{P} = \bar{Q}$		20	34		43		51	ns	4.5	Fig.6	
$t_{PHL}/t_{PLH}$	propagation delay $\bar{E}$ to $P = Q$		18	24		30		36	ns	4.5	Fig.7	
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

# 8-bit magnitude comparator

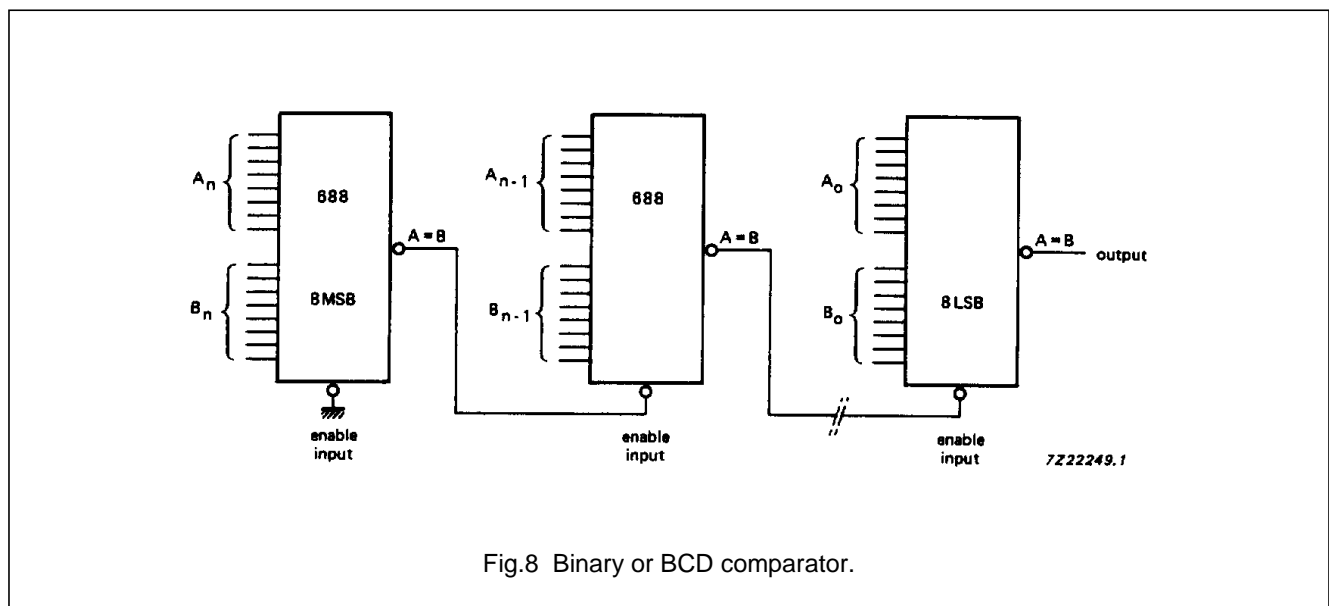
# 74HC/HCT688

## AC WAVEFORMS



## APPLICATION INFORMATION

Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits. An example is shown in Fig.8.



## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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