

74LVC162244A; 74LVCH162244A

16-bit buffer/line driver; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Rev. 6 — 16 December 2011

Product data sheet

1. General description

The 74LVC162244A; 74LVCH162244A are 16-bit non-inverting buffer/line drivers with 3-state bus compatible outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. It features four output enable inputs, ($\overline{1OE}$ to $\overline{4OE}$) each controlling four of the 3-state outputs. A HIGH on \overline{nOE} causes the outputs to assume a high-impedance OFF-state. The device is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH162244A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- All data inputs have bus hold. (74LVCH162244A only)
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

| Type number | Temperature range | Package | | Version |
|------------------|-------------------|---------|--|----------|
| | | Name | Description | |
| 74LVC162244ADL | -40 °C to +125 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74LVCH162244ADL | | | | |
| 74LVC162244ADGG | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVCH162244ADGG | | | | |

4. Functional diagram

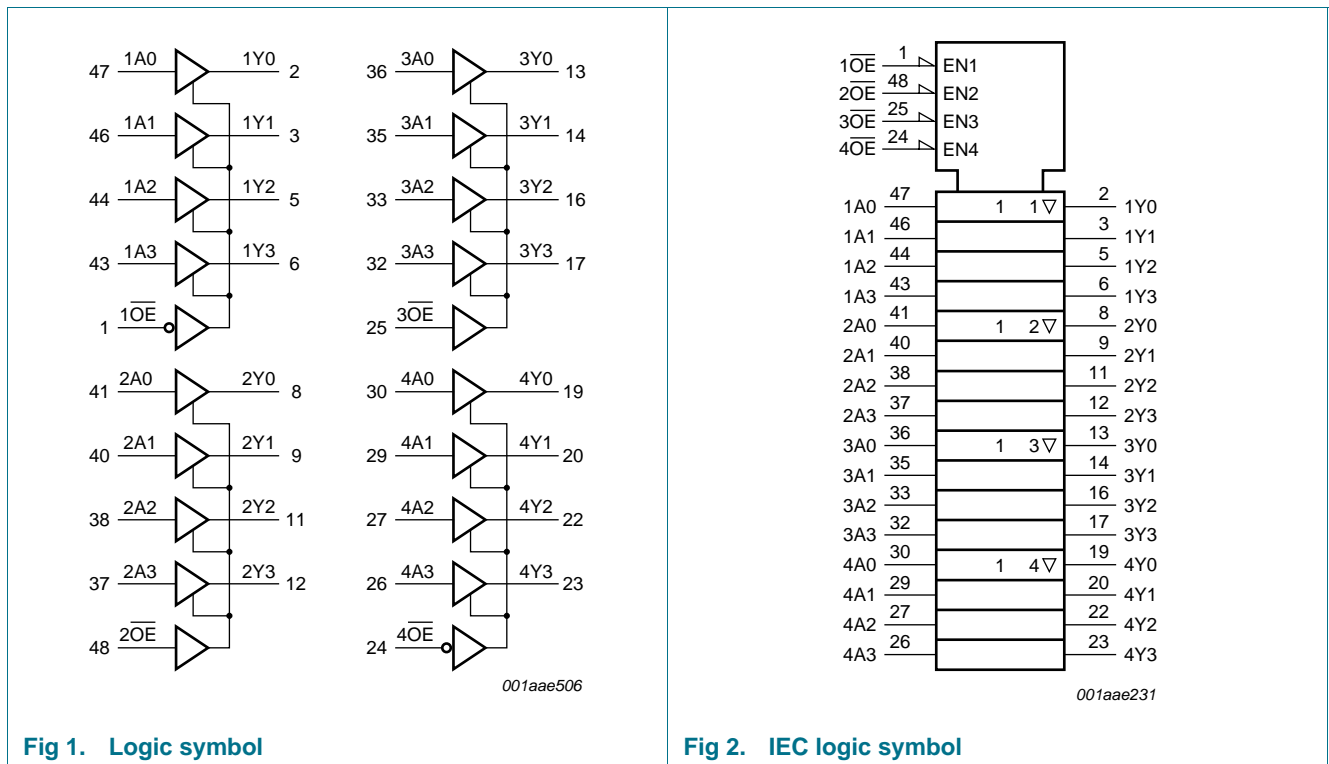


Fig 1. Logic symbol

Fig 2. IEC logic symbol

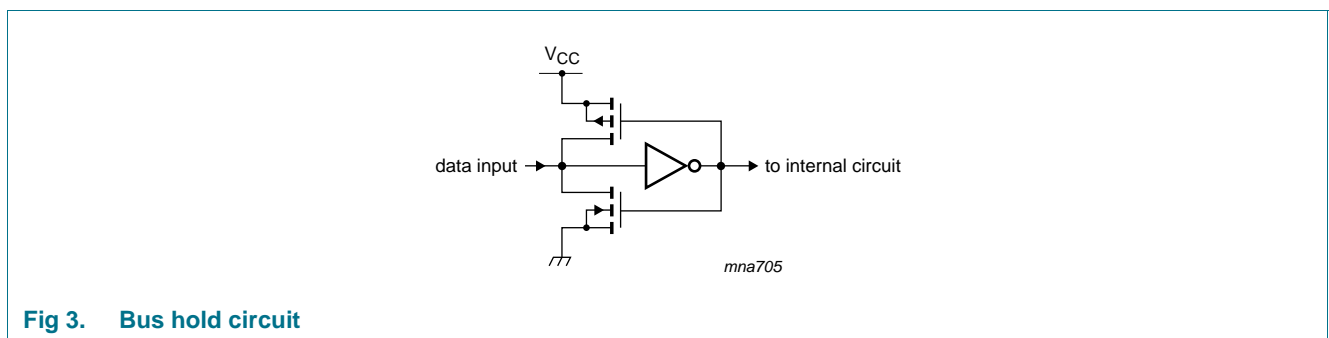


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning

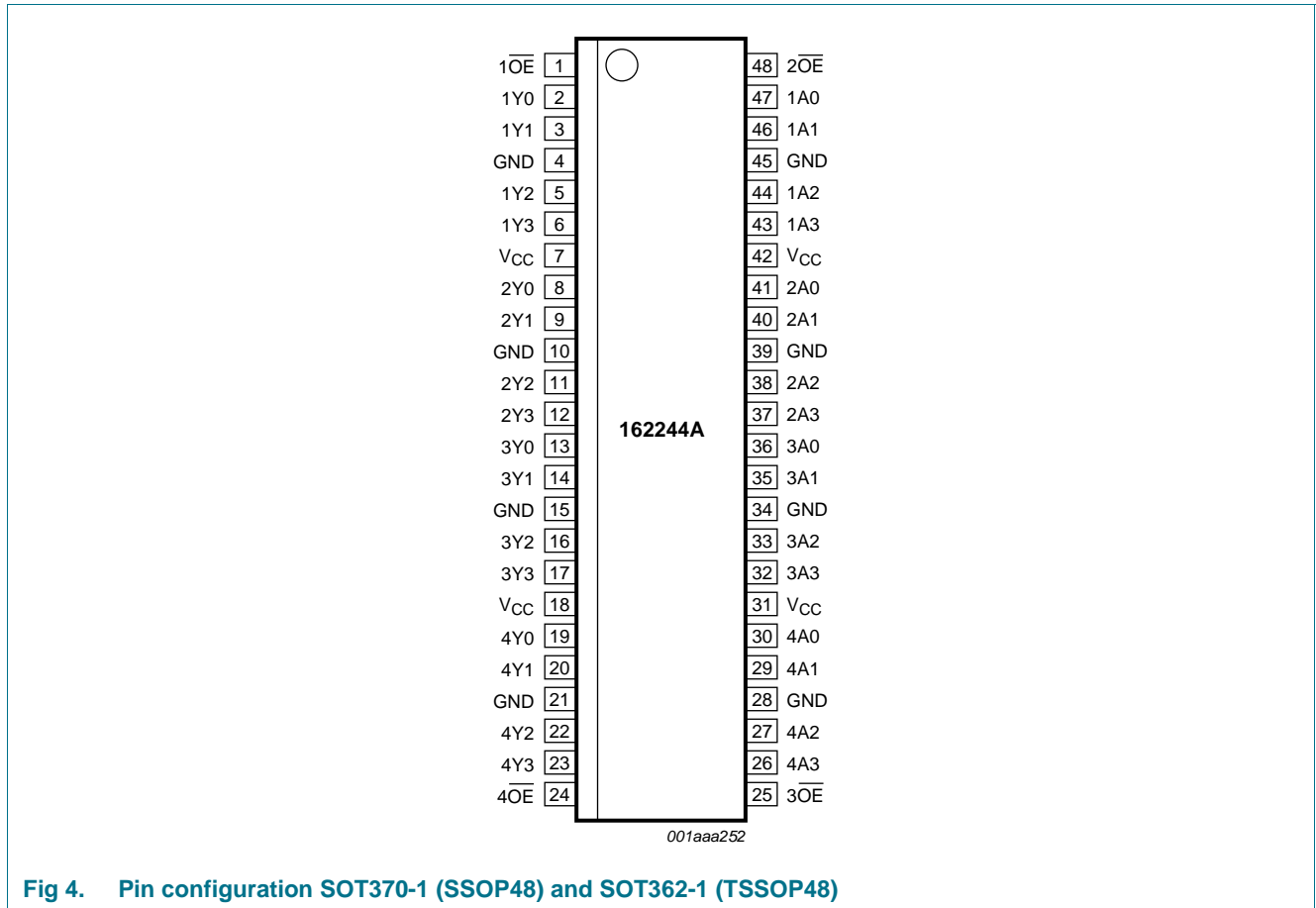


Fig 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-------------------------------|----------------------------------|
| 1OE | 1 | output enable input (active LOW) |
| 2OE | 48 | output enable input (active LOW) |
| 3OE | 25 | output enable input (active LOW) |
| 4OE | 24 | output enable input (active LOW) |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 1A[0:3] | 47, 46, 44, 43 | data input |
| 2A[0:3] | 41, 40, 38, 37 | data input |
| 3A[0:3] | 36, 35, 33, 32 | data input |
| 4A[0:3] | 30, 29, 27, 26 | data input |
| 1Y[0:3] | 2, 3, 5, 6 | data output |

Table 2. Pin description ...continued

| Symbol | Pin | Description |
|---------|----------------|-------------|
| 2Y[0:3] | 8, 9, 11, 12 | data output |
| 3Y[0:3] | 13, 14, 16, 17 | data output |
| 4Y[0:3] | 19, 20, 22, 23 | dataoutput |

6. Functional description

Table 3. Function table^[1]

| Control | Input | Output |
|---------|-------|--------|
| nOE | nAn | nYn |
| L | L | L |
| L | H | H |
| H | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|----------|----------------|--------------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ± 50 | mA |
| V_O | output voltage | output HIGH or LOW | [2] -0.5 | $V_{CC} + 0.5$ | V |
| | | output 3-state | [2] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | $^{\circ}$ C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C; | [3] - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 $^{\circ}$ C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|-----------------------------------|------|-----|-----------------|------|
| V _{CC} | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _O | output voltage | output HIGH or LOW | 0 | - | V _{CC} | V |
| | | output 3-state | 0 | - | 5.5 | V |
| T _{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | V _{CC} = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|------------------------|--------------------|------------------------|------------------------|------------------------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | 0.65 × V _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.2 | - | - | V _{CC} - 0.3 | - | V |
| | | I _O = -2 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | I _O = -4 mA; V _{CC} = 2.3 V | 1.7 | - | - | 1.55 | - | V |
| | | I _O = -6 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | I _O = -12 mA; V _{CC} = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | I _O = 2 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | I _O = 4 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | I _O = 6 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | I _O = 12 mA; V _{CC} = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| I _I | input leakage current | V _{CC} = 3.6 V; V _I = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-------------------|---------------------------------|--|------------------|--------------------|-----|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND; ^[2] | - | ±0.1 | ±5 | - | ±20 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | ±0.1 | ±10 | - | ±20 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.1 | 20 | - | 80 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 5 | 500 | - | 5000 | μA |
| C _I | input capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 5.0 | - | - | - | pF |
| I _{BHL} | bus hold LOW current | V _{CC} = 1.65 V; V _I = 0.58 V ^{[3][4]} | 10 | - | - | 10 | - | μA |
| | | V _{CC} = 2.3 V; V _I = 0.7 V | 30 | - | - | 25 | - | μA |
| | | V _{CC} = 3.0 V; V _I = 0.8 V | 75 | - | - | 60 | - | μA |
| I _{BHH} | bus hold HIGH current | V _{CC} = 1.65 V; V _I = 1.07 V ^{[3][4]} | -10 | - | - | -10 | - | μA |
| | | V _{CC} = 2.3 V; V _I = 1.7 V | -30 | - | - | -25 | - | μA |
| | | V _{CC} = 3.0 V; V _I = 2.0 V | -75 | - | - | -60 | - | μA |
| I _{BHLO} | bus hold LOW overdrive current | V _{CC} = 1.95 V ^{[3][5]} | 200 | - | - | 200 | - | μA |
| | | V _{CC} = 2.7 V | 300 | - | - | 300 | - | μA |
| | | V _{CC} = 3.6 V | 500 | - | - | 500 | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current | V _{CC} = 1.95 V ^{[3][5]} | -200 | - | - | -200 | - | μA |
| | | V _{CC} = 2.7 V | -300 | - | - | -300 | - | μA |
| | | V _{CC} = 3.6 V | -500 | - | - | -500 | - | μA |

- [1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.
- [3] Valid for data inputs only. Control inputs do not have a bus hold circuit.
- [4] The specified sustaining current at the data input holds the input below the specified V_I level.
- [5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[2] | Max | Min | Max | |
| t _{pd} | propagation delay | nAn to nYn; see Figure 5 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 11.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 6.0 | 15.0 | 1.5 | 17.2 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.2 | 7.4 | 1.0 | 8.2 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 3.3 | 6.7 | 1.0 | 8.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 5.8 | 1.0 | 7.5 | ns |
| t _{en} | enable time | nOE to nYn; see Figure 6 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 15.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.7 | 6.8 | 15.3 | 1.7 | 17.7 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.5 | 3.8 | 8.0 | 1.5 | 8.9 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 4.2 | 7.6 | 1.5 | 9.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.1 | 6.0 | 1.0 | 7.5 | ns |
| t _{dis} | disable time | nOE to nYn; see Figure 6 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 10.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 2.2 | 3.9 | 8.2 | 2.2 | 9.5 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.1 | 4.4 | 0.5 | 5.0 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.1 | 4.7 | 1.5 | 6.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 2.8 | 4.5 | 1.5 | 6.0 | ns |
| C _{PD} | power dissipation capacitance | per input; V _i = GND to V _{CC} ^[3] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | - | 4.8 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 8.3 | - | - | - | pF |
| | | V _{CC} = 3.0 V to 3.6 V | - | 11.4 | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

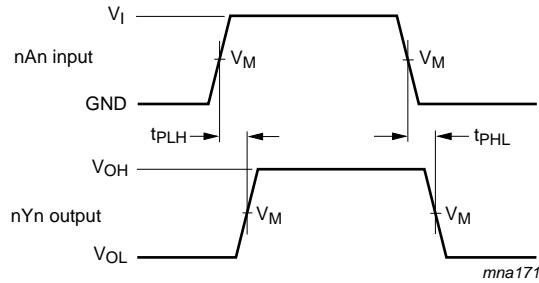
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

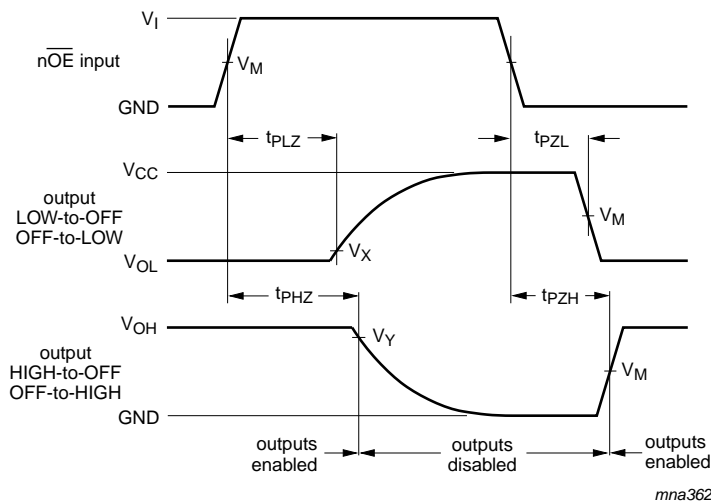
11. Waveforms



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The input (nAn) to output (nYn) propagation delays



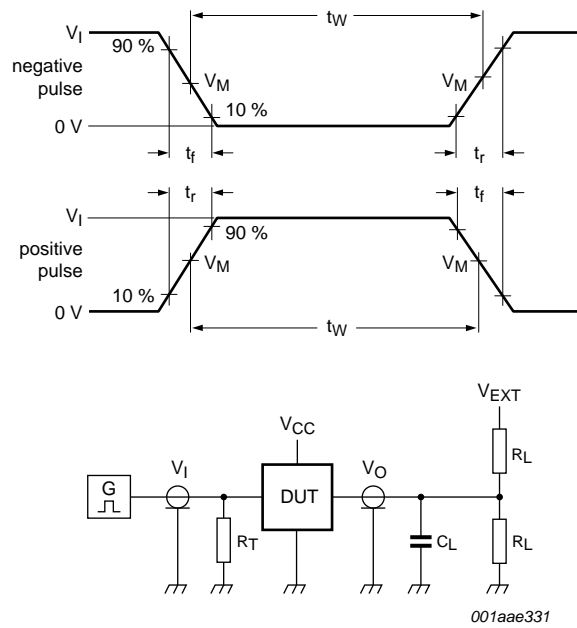
Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. 3-state enable and disable times.

Table 8. Measurement points

| Supply voltage V_{CC} | V_M | Input | | Output | |
|----------------------------|---------------------|----------|---------------|-------------------|-------------------|
| | | V_I | $t_r = t_f$ | V_X | V_Y |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |
| 3.0 V to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|-------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 1.2 V | V_{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

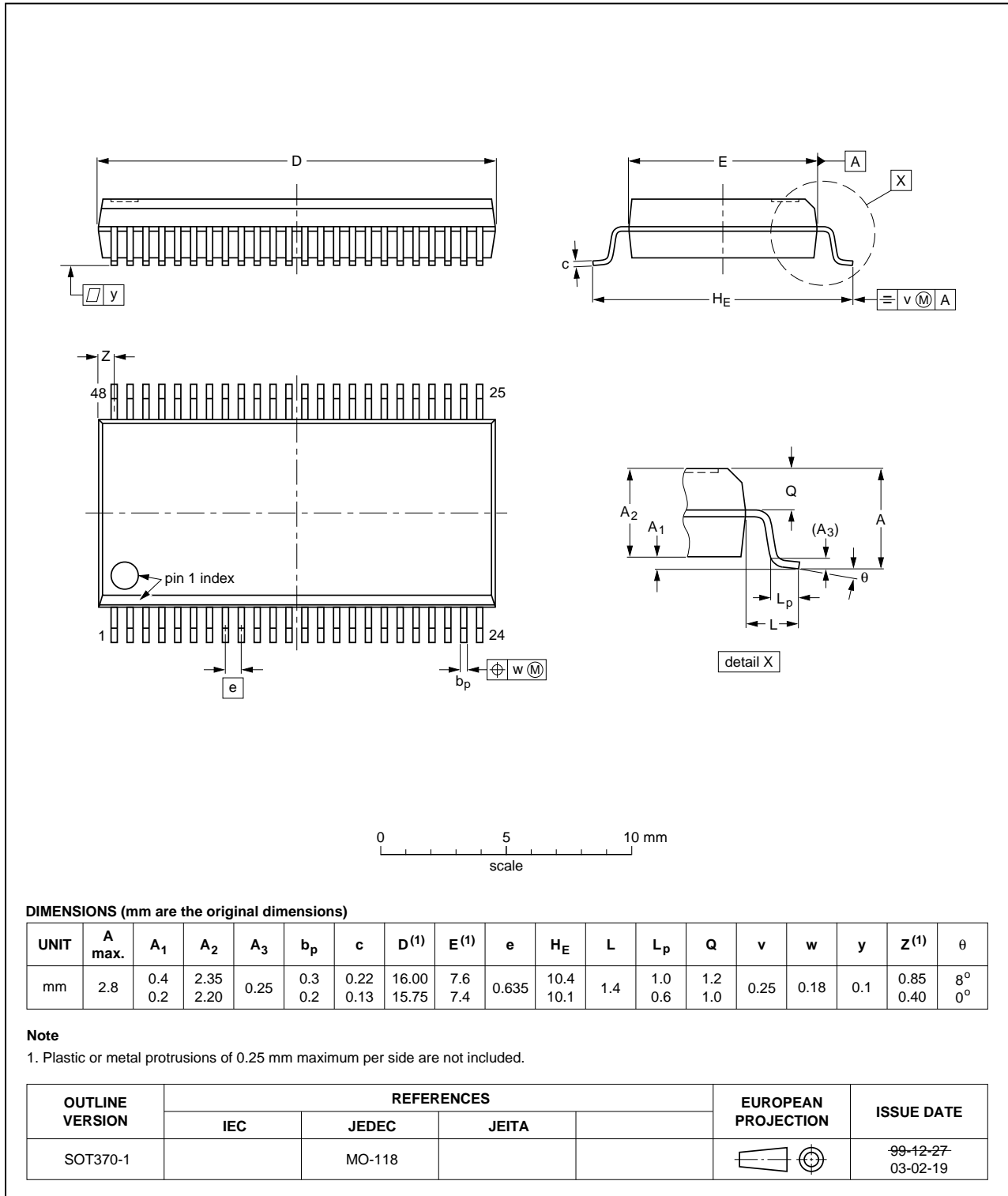


Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

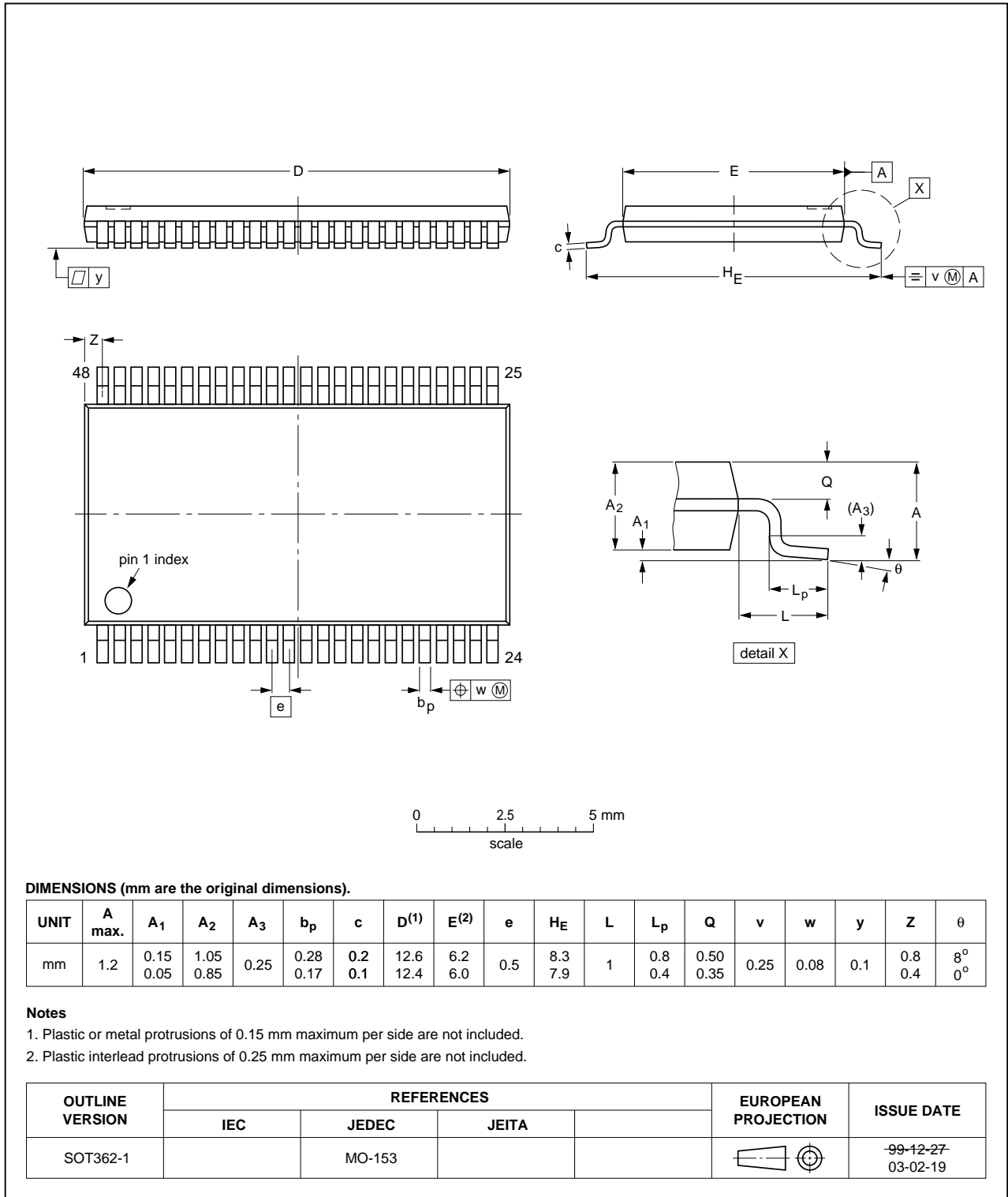


Fig 9. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------------------|--------------|--|---------------|------------------------------|
| 74LVC_LVCH162244A v.6 | 20111216 | Product data sheet | - | 74LVC_LVCH162244A v.5 |
| Modifications: | | <ul style="list-style-type: none"> Maximum propagation delay value for $V_{CC} = 1.65$ V to 1.95 V at +125 °C changed from 15.7 ns to 17.2 ns Maximum enable time value for $V_{CC} = 1.65$ V to 1.95 V at +125 °C changed from 16.1 ns to 17.7 ns Maximum disable time value for $V_{CC} = 1.65$ V to 1.95 V at +125 °C changed from 8.7 ns to 9.5 ns | | |
| 74LVC_LVCH162244A v.5 | 20111108 | Product data sheet | - | 74LVC_LVCH162244A v.4 |
| Modifications: | | <ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 5, Table 6, Table 7 and Table 9: values added for lower voltage ranges. | | |
| 74LVC_LVCH162244A v.4 | 20031212 | Product specification | - | 74LVC_H162244A v.3 |
| 74LVC_H162244A v.3 | 19980217 | Product specification | - | 74LVC162244A_LVCH162244A v.3 |
| 74LVC162244A_LVCH162244A v.3 | 19980217 | Product specification | - | 74LVC162244A v.2 |
| 74LVC162244A v.2 | 19970801 | Product specification | - | 74LVC162244A v.1 |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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