

74LVC162245A; 74LVCH162245A

16-bit transceiver with direction pin, 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Rev. 6 — 23 November 2011

Product data sheet

1. General description

The 74LVC162245A; 74LVCH162245A are 16-bit transceivers with non-inverting 3-state bus compatible outputs in both send and receive directions. Two send/receive ($\overline{\text{nDIR}}$) inputs control direction, and two output enable ($\overline{\text{nOE}}$) inputs make cascading easy. The $\overline{\text{nOE}}$ inputs control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

The 74LVCH162245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

Both HIGH and LOW output stages include 30 Ω series termination resistors to reduce line noise.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors
- High-impedance when $V_{CC} = 0$ V
- All data inputs have bus hold (74LVCH162245A only)
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

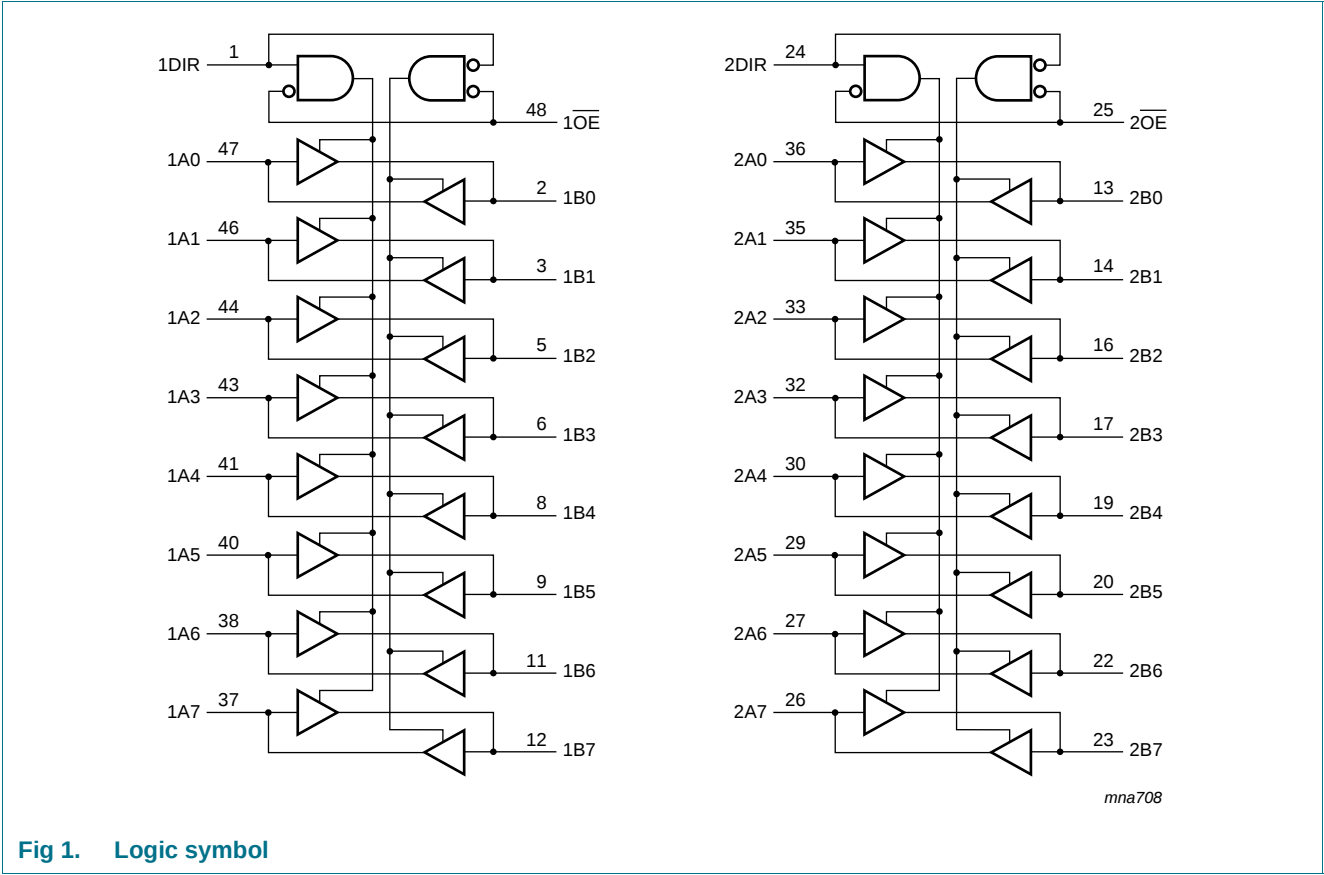


3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC162245ADL 74LVCH162245ADL	−40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVC162245ADGG 74LVCH162245ADGG	−40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram



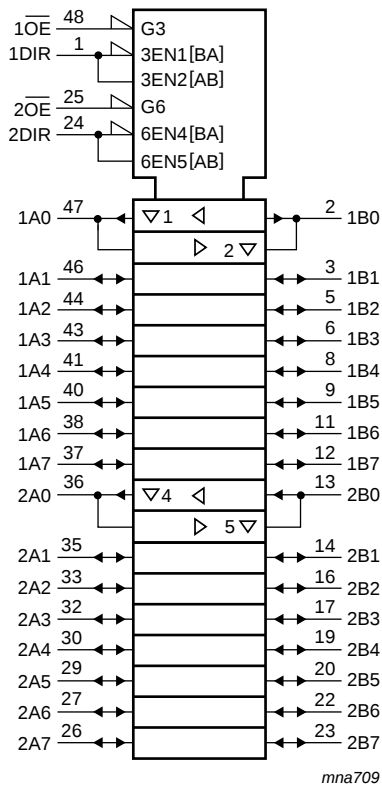


Fig 2. IEC logic symbol

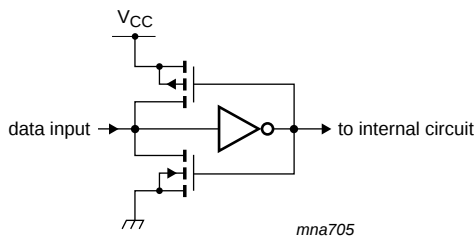
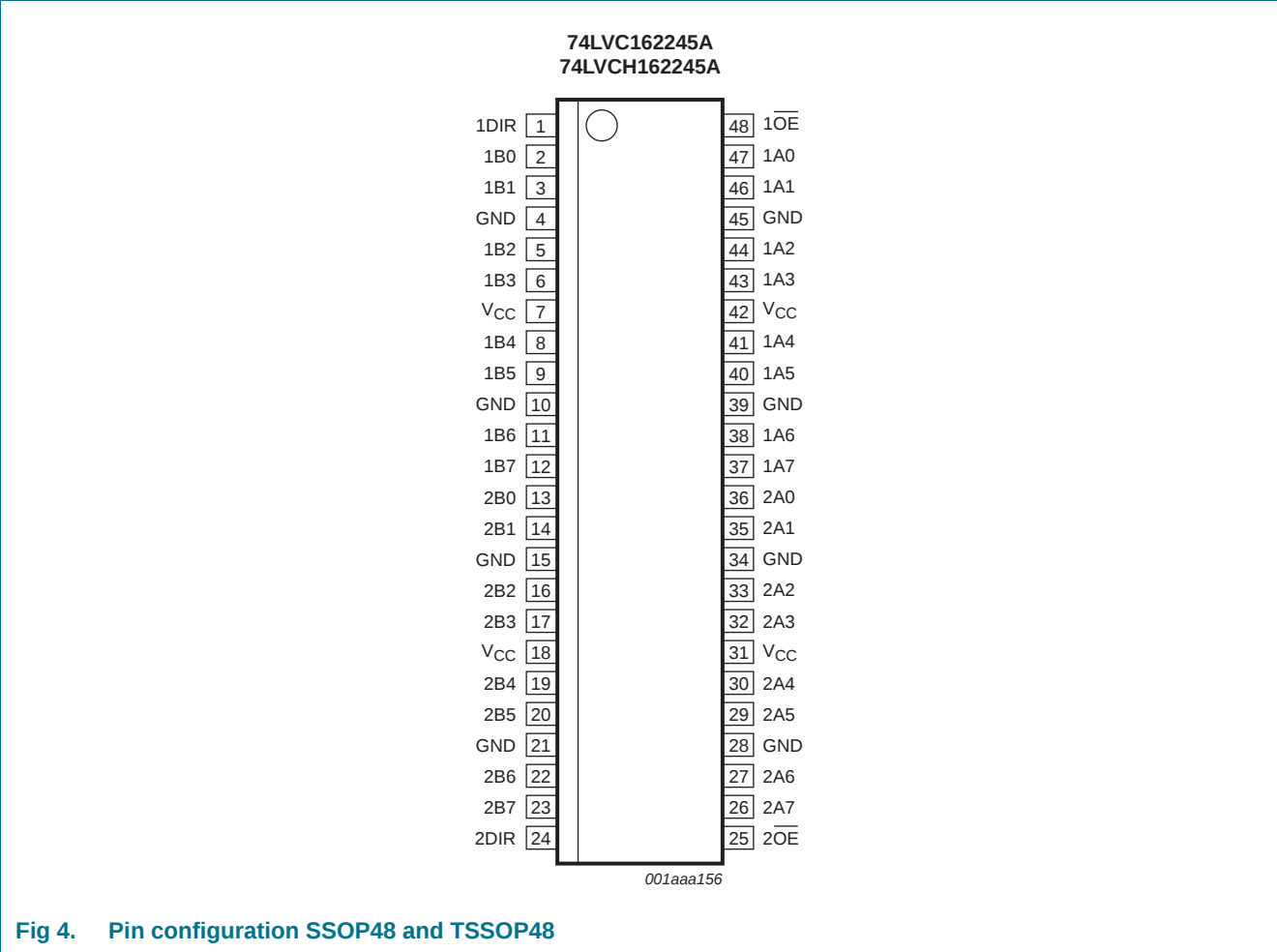


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Name	Pin	Description
1DIR	1	direction control input
2DIR	24	direction control input
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
1OE	48	output enable input (active LOW)
2OE	25	output enable input (active LOW)
1A[0:7]	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A[0:7]	36, 35, 33, 32, 30, 29, 27, 26	data input/output
1B[0:7]	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B[0:7]	13, 14, 16, 17, 19, 20, 22, 23	data input/output

6. Functional description

Table 3. Function table^[1]

Input		Output	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

- [1] H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW state	^[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	^[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3] -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.
 [3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$						
		$I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.2$	V_{CC}	-	$V_{CC} - 0.3$	-	V
		$I_O = -2 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -6 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$						
		$I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 2 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 4 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 6 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 12 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$ ^[2]	-	± 0.1	± 5	-	± 20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 3.6$ V; $V_O = 5.5$ V or GND; ^{[2][3]}	-	± 0.1	± 5	-	± 20	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 5.5$ V	-	± 0.1	± 10	-	± 20	μA
I_{CC}	supply current	$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	0.1	20	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7$ V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = \text{GND to } V_{CC}$	-	5.0	-	-	-	pF
$C_{I/O}$	input/output capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = \text{GND to } V_{CC}$	-	10.0	-	-	-	pF
I_{BHL}	bus hold LOW current	$V_{CC} = 1.65$ V; $V_I = 0.58$ V ^{[4][5]}	10	-	-	10	-	μA
		$V_{CC} = 2.3$ V; $V_I = 0.7$ V	30	-	-	25	-	μA
		$V_{CC} = 3.0$ V; $V_I = 0.8$ V	75	-	-	60	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 1.65$ V; $V_I = 1.07$ V ^{[4][5]}	-10	-	-	-10	-	μA
		$V_{CC} = 2.3$ V; $V_I = 1.7$ V	-30	-	-	-25	-	μA
		$V_{CC} = 3.0$ V; $V_I = 2.0$ V	-75	-	-	-60	-	μA
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 1.95$ V ^{[4][6]}	200	-	-	200	-	μA
		$V_{CC} = 2.7$ V	300	-	-	300	-	μA
		$V_{CC} = 3.6$ V	500	-	-	500	-	μA
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 1.95$ V ^{[4][6]}	-200	-	-	-200	-	μA
		$V_{CC} = 2.7$ V	-300	-	-	-300	-	μA
		$V_{CC} = 3.6$ V	-500	-	-	-500	-	μA

[1] All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs only. Control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nBn; nBn to nAn; see Figure 5 ^[2]						
		V _{CC} = 1.2 V	-	12	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.6	16.0	1.5	18.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.5	7.8	1.0	9.1	ns
		V _{CC} = 2.7 V	1.0	3.5	6.7	1.0	9.5	ns
t _{en}	enable time	nOE to nAn, nBn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	18	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	7.7	17.2	2.0	19.8	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.3	9.4	1.5	10.9	ns
		V _{CC} = 2.7 V	1.5	4.6	8.5	1.5	9.5	ns
t _{dis}	disable time	nOE to nAn, nBn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	10	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.8	4.6	11.0	2.8	12.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	6.3	1.0	7.3	ns
		V _{CC} = 2.7 V	1.5	3.4	7.5	1.5	11.0	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} ^[3]						
		V _{CC} = 1.65 V to 1.95 V	-	10.4	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	14.0	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	17.2	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms

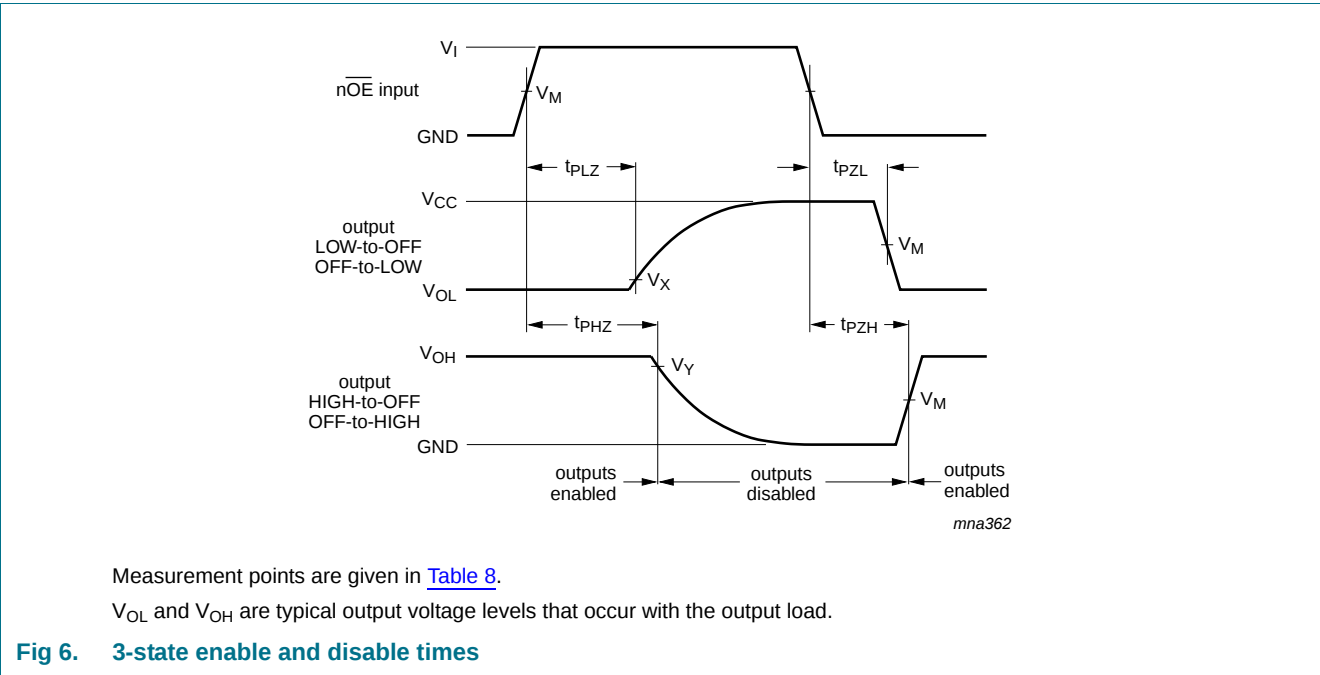
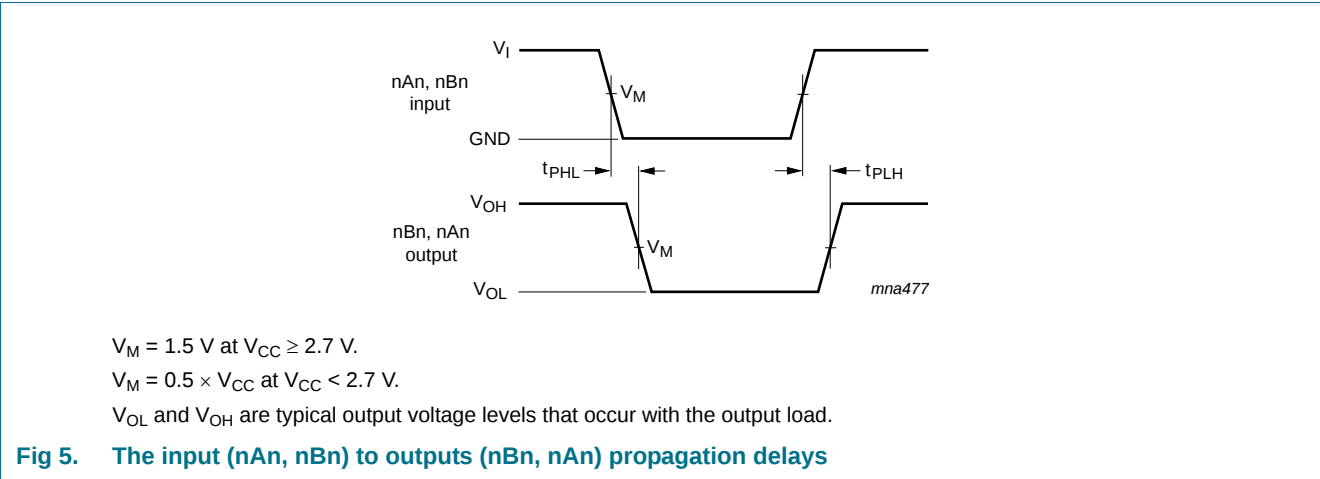
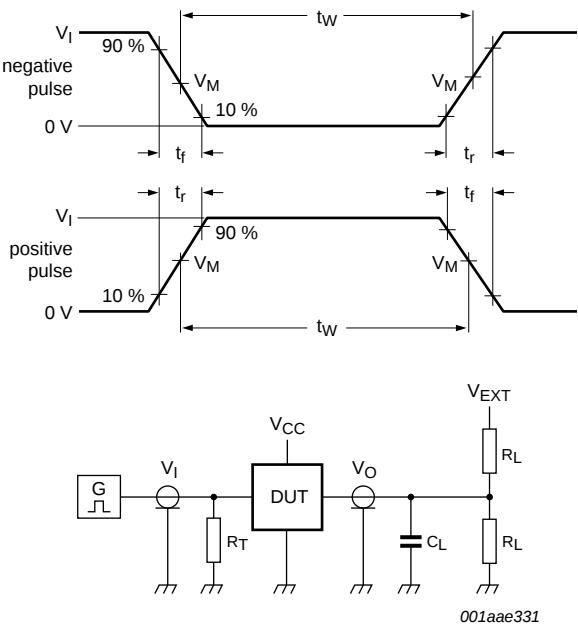


Table 8. Measurement points

Supply voltage V_{CC}	V_M	Input			
		V_I	$t_r = t_f$	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.7 V	1.5 V	2.7 V	$\leq 2.5\text{ ns}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
3.0 V to 3.6 V	1.5 V	2.7 V	$\leq 2.5\text{ ns}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

- R_L = Load resistance.
- C_L = Load capacitance including jig and probe capacitance.
- R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
- V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1

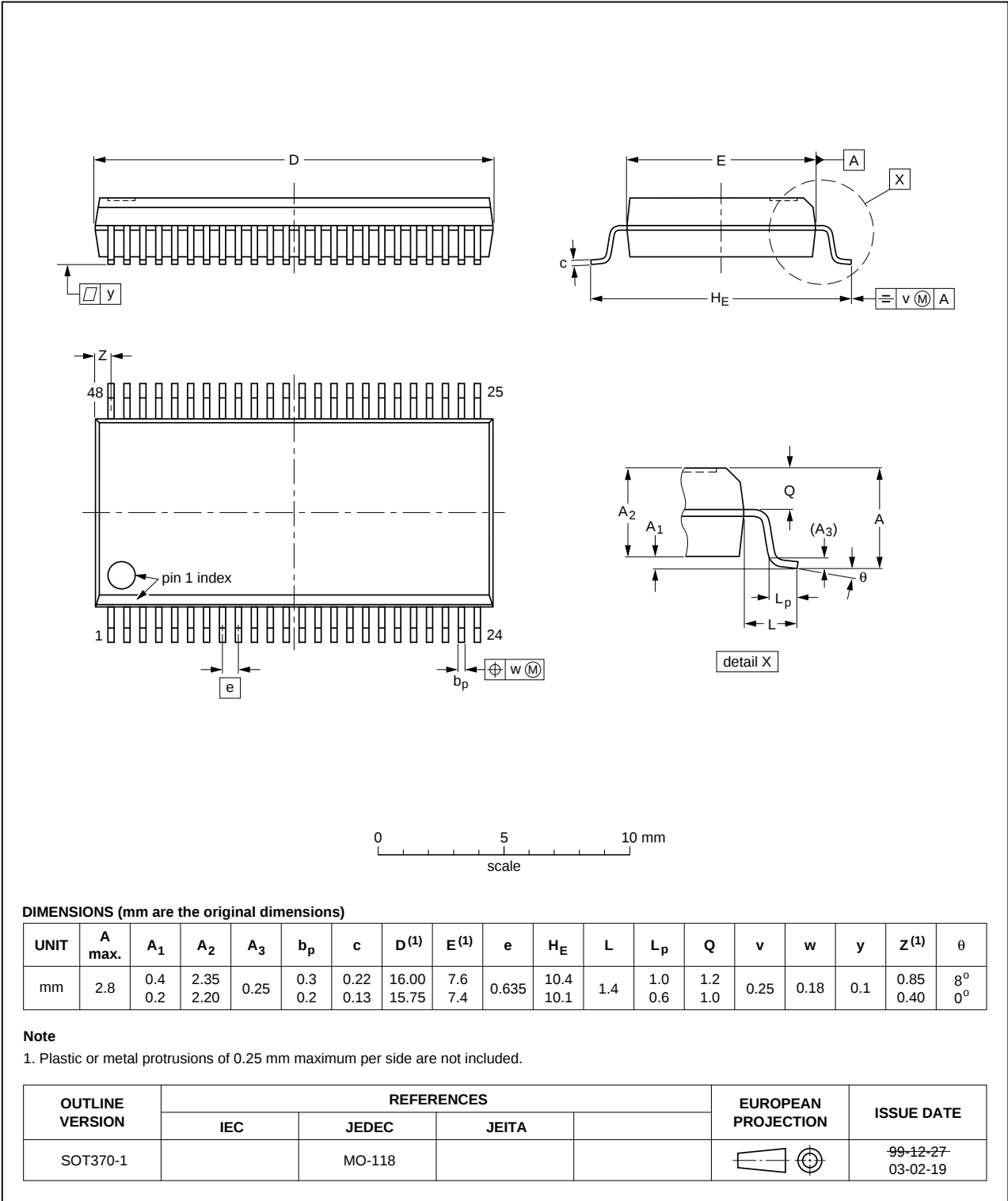


Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

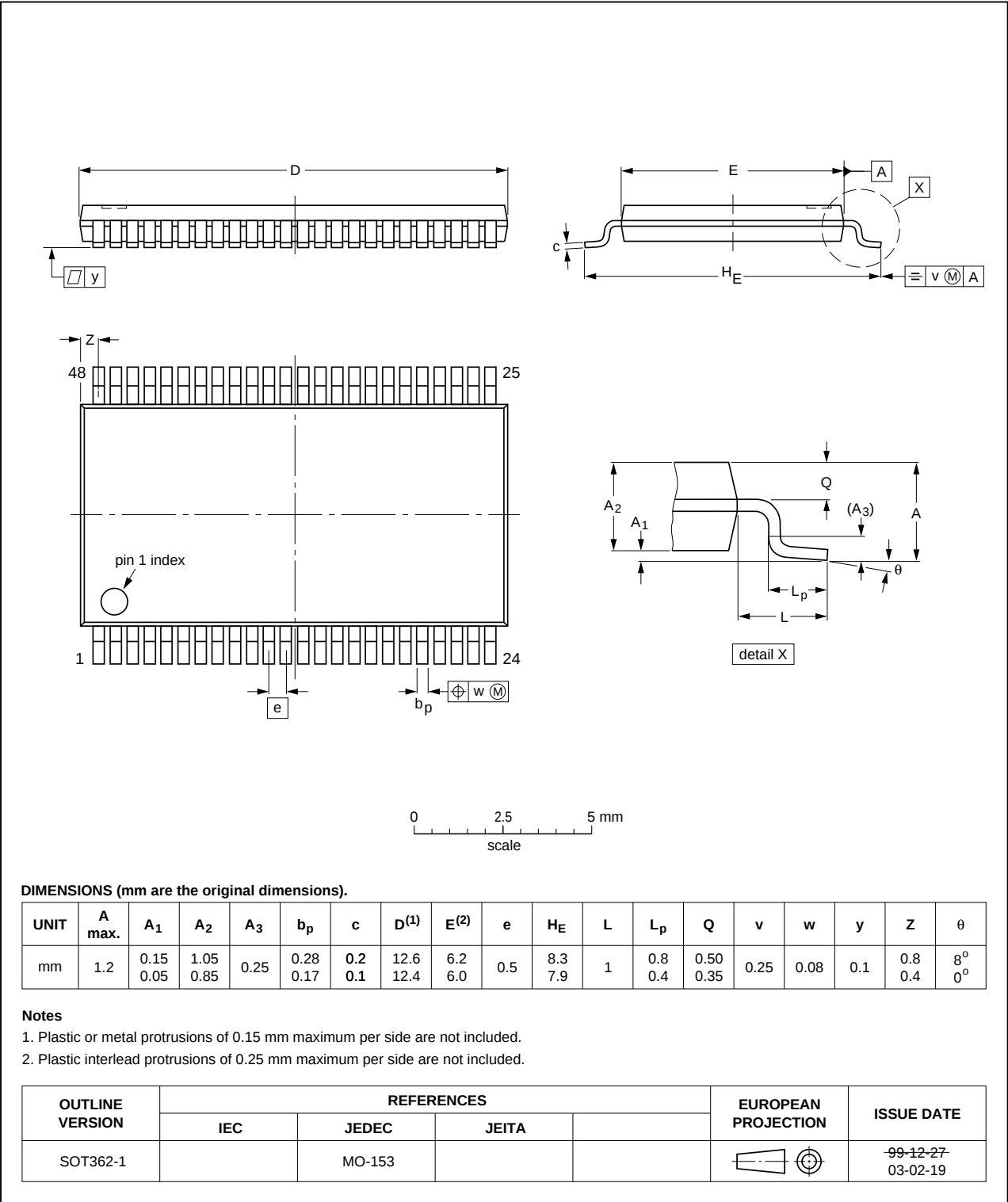


Fig 9. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH162245A v.6	20111123	Product data sheet	-	74LVC_LVCH162245A v.5
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 5, Table 6, Table 7 and Table 9: values added for lower voltage ranges.			
74LVC_LVCH162245A v.5	20031208	Product specification	-	74LVC_H162245A v.4
74LVC_H162245A v.4	19980217	Product specification	-	74LVC162245A_74LVCH162245A v.3
74LVC162245A_74LVCH162245A v.3	19980217	Product specification	-	74LVC162245A v.2
74LVC162245A v.2	19970801	Product specification	-	74LVC162245A v.1
74LVC162245A v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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