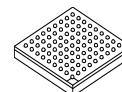


|                 |                 |
|-----------------|-----------------|
| MIMX8MN6DVTJZAA | MIMX8MN6DVTJZCA |
| MIMX8MN6DVTJZDA | MIMX8MN5DVTJZAA |
| MIMX8MN4DVTJZAA | MIMX8MN3DVTJZAA |
| MIMX8MN2DVTJZAA | MIMX8MN1DVTJZAA |
| MIMX8MN5DVPIZCA | MIMX8MN5DVPIZDA |
| MIMX8MN5DVPIZAA | MIMX8MN3DVPIZAA |
| MIMX8MN1DVPIZAA |                 |

# i.MX 8M Nano

## Applications Processor

### Datasheet for Consumer Products



#### Package Information

Plastic Package  
FCBGA 14 x 14 mm, 0.5 mm pitch  
FCBGA 11 x 11 mm, 0.5 mm pitch

#### Ordering Information

See [Table 3 on page 6](#)

## 1 i.MX 8M Nano introduction

The i.MX 8M Nano application processor represents NXP's latest graphics and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption.

The i.MX 8M Nano family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M7 running up to 750 MHz core processor is for real-time and low-power processing.

The i.MX 8M Nano family of processors provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- A wide range of audio interfaces, including I2S, AC 97, TDM, and S/PDIF
- Large set of peripherals that are commonly used in consumer/industrial market, including USB and Ethernet

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Table 1. Features

| Subsystem                   | Feature                                                                                                                                                                                                                                                                                                                                                                              |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Cortex®-A53 MPCore platform | Quad symmetric Cortex® -A53 processors <ul style="list-style-type: none"> <li>• 32 KB L1 Instruction Cache</li> <li>• 32 KB L1 Data Cache</li> <li>• Media Processing Engine (MPE) with Arm® NEON™ technology supporting the Advanced Single Instruction Multiple Data architecture:</li> <li>• Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture</li> </ul> |
|                             | Support of 64-bit Arm®v8-A architecture                                                                                                                                                                                                                                                                                                                                              |
|                             | 512 KB unified L2 cache                                                                                                                                                                                                                                                                                                                                                              |
| Cortex®-M7 core platform    | Low power microcontroller available for customer application: <ul style="list-style-type: none"> <li>• low power standby mode</li> <li>• IoT features including Weave</li> <li>• Manage IR or wireless remote</li> <li>• ML inference applications (enhanced for i.MX 8M Nano)</li> </ul>                                                                                            |
|                             | Cortex® M7 CPU: <ul style="list-style-type: none"> <li>• 256 KB tightly coupled memory (TCM)</li> </ul>                                                                                                                                                                                                                                                                              |
| Connectivity                | One USB 2.0 OTG controllers with integrated PHY interfaces: <ul style="list-style-type: none"> <li>• Spread spectrum clock support</li> </ul>                                                                                                                                                                                                                                        |
|                             | Three Ultra Secure Digital Host Controller (uSDHC) interfaces: <ul style="list-style-type: none"> <li>• MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec</li> <li>• SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec</li> <li>• Support for SDXC (extended capacity)</li> </ul>                                                  |
|                             | One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588                                                                                                                                                                                                                                                                        |
|                             | Four Universal Asynchronous Receiver/Transmitter (UART) modules                                                                                                                                                                                                                                                                                                                      |
|                             | Four I <sup>2</sup> C modules                                                                                                                                                                                                                                                                                                                                                        |
|                             | Three SPI modules                                                                                                                                                                                                                                                                                                                                                                    |
| On-chip memory              | Boot ROM (256 KB)                                                                                                                                                                                                                                                                                                                                                                    |
|                             | On-chip RAM (512 KB + 32 KB)                                                                                                                                                                                                                                                                                                                                                         |
| GPIO and pin multiplexing   | General-purpose input/output (GPIO) modules with interrupt capability                                                                                                                                                                                                                                                                                                                |
|                             | Input/output multiplexing controller (IOMUXC) to provide centralized pad control                                                                                                                                                                                                                                                                                                     |
| Power management            | Temperature sensor with programmable trip points                                                                                                                                                                                                                                                                                                                                     |
|                             | Flexible power domain partitioning with internal power switches to support efficient power management                                                                                                                                                                                                                                                                                |

Table 1. Features (continued)

| Subsystem                 | Feature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External memory interface | 16-bit DRAM interfaces: <ul style="list-style-type: none"> <li>• LPDDR4-3200</li> <li>• DDR4-2400</li> <li>• DDR3L-1600</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                           | 8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                           | eMMC 5.1 Flash (3 interfaces)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                           | SPI NOR Flash (3 interfaces)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                           | QuadSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and parallel read mode of two identical FLASH devices                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Multimedia                | Graphic Processing Unit: <ul style="list-style-type: none"> <li>• GC7000UL with OpenCL and Vulkan support</li> <li>• 2 shader</li> <li>• 99.8 million triangles/sec</li> <li>• 0.6 giga pixel/sec</li> <li>• 9.6 GFLOPs 32-bit/19.2 GFLOPs 16-bit</li> <li>• Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL</li> <li>• Core clock frequency of 600 MHz</li> <li>• Shader clock frequency of 600 MHz</li> </ul>                                                                                                                                                                                                     |
|                           | LCDIF Display Controller: <ul style="list-style-type: none"> <li>• Support up to 1080p60 display through MIPI DSI</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                           | MIPI Interfaces: <ul style="list-style-type: none"> <li>• 4-lane MIPI DSI interface</li> <li>• 4-lane MIPI CSI interface</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                           | Audio: <ul style="list-style-type: none"> <li>• S/PDIF input and output, including a raw capture input mode</li> <li>• Five external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and two SAI with 1 Tx and 1Rx lane. All ports support 49.152 MHz BCLK.</li> <li>• ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate and 1/16 to 8x sample rate conversion ratio.</li> <li>• Pulse Density Modulation (PDM) input</li> </ul> |

**Table 1. Features (continued)**

| Subsystem    | Feature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Security     | Resource Domain Controller (RDC): <ul style="list-style-type: none"> <li>• supports 4 domains and up to 8 regions of DDR</li> </ul>                                                                                                                                                                                                                                                                                                                                                    |
|              | Arm® TrustZone® (TZ) architecture: <ul style="list-style-type: none"> <li>• Arm® Cortex-A53 MPCore TrustZone support</li> </ul>                                                                                                                                                                                                                                                                                                                                                        |
|              | On-chip RAM (OCRAM) secure region protection using OCRAM controller                                                                                                                                                                                                                                                                                                                                                                                                                    |
|              | High Assurance Boot (HAB)                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|              | Cryptographic acceleration and assurance module (CAAM): <ul style="list-style-type: none"> <li>• Support Widevine and PlayReady content protection</li> <li>• Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms</li> <li>• Real-time integrity checker (RTIC)</li> <li>• DRM support for RSA, AES, 3DES, DES</li> <li>• Side channel attack resistance</li> <li>• True random number generation (RNG)</li> <li>• Manufacturing protection support</li> </ul> |
|              | Secure non-volatile storage (SNVS): <ul style="list-style-type: none"> <li>• Secure real-time clock (RTC)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                   |
|              | Secure JTAG controller (SJC)                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| System debug | Arm® CoreSight™ debug and trace technology                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|              | Trace Port Interface Unit (TPIU) to support off-chip real-time trace                                                                                                                                                                                                                                                                                                                                                                                                                   |
|              | Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering                                                                                                                                                                                                                                                                                                                                                                                                        |
|              | Unified trace capability for Quad Cortex®-A53 and Cortex®-M7 CPUs                                                                                                                                                                                                                                                                                                                                                                                                                      |
|              | Cross Triggering Interface (CTI)                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|              | Support for 4-pin (JTAG) debug interface                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**NOTE**

The actual feature set depends on the part numbers as described in [Table 3](#). Functions such as display and camera interfaces, and connectivity interfaces, may not be enabled for specific part numbers.

## 1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Nano applications processor system.

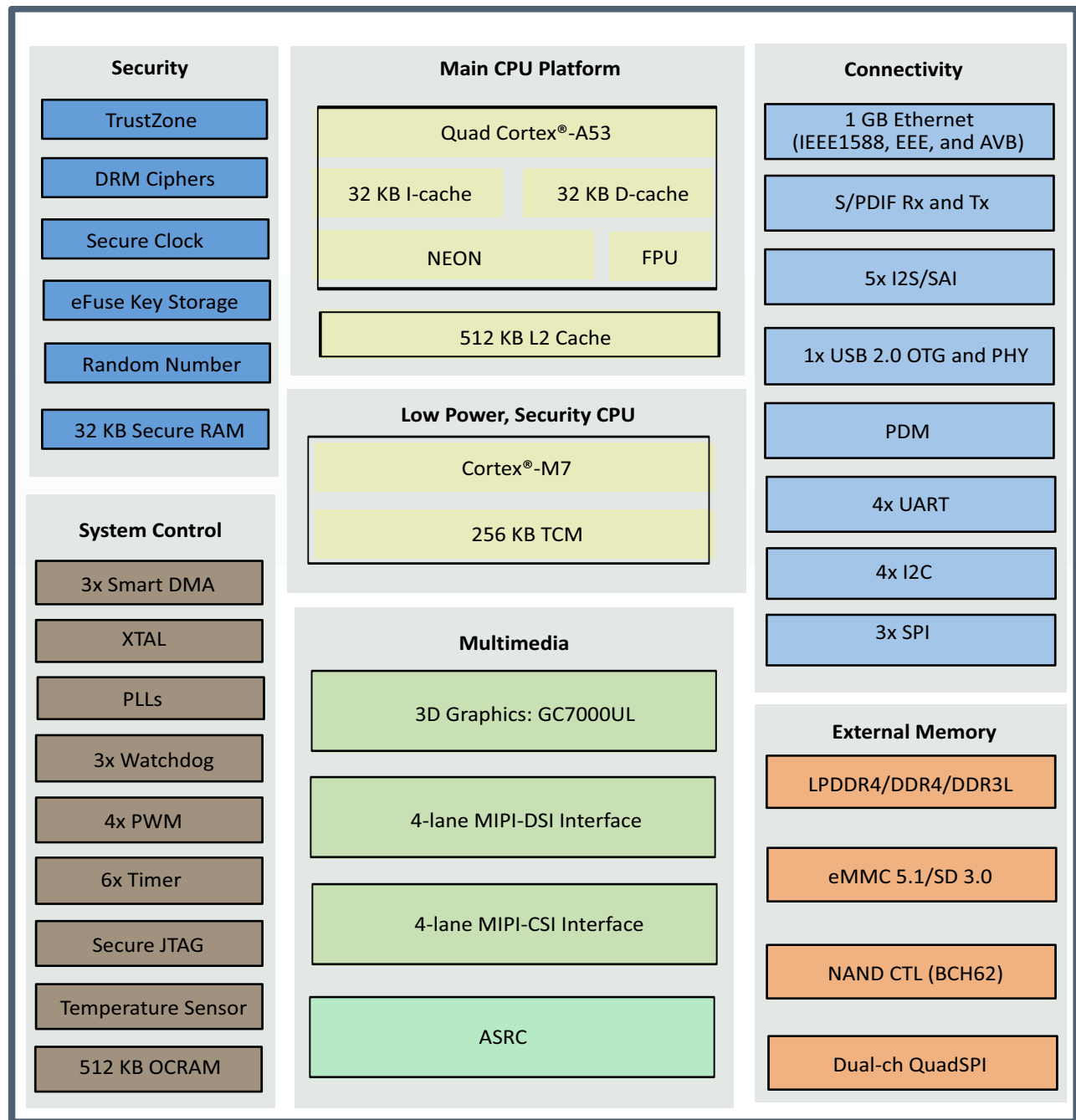


Figure 1. i.MX 8M Nano system block diagram

**NOTE**

Some modules shown in this block diagram are not offered on all derivatives. See [Table 2](#) for exceptions.

**Table 2. Modules supported**

| Key Modules | 6DVT | 5DVT | 4DVT | 3DVT | 2DVT | 1DVT | 5DVP | 3DVP | 1DVP |
|-------------|------|------|------|------|------|------|------|------|------|
| Cortex® A53 | 4x   | 4x   | 2x   | 2x   | 1x   | 1x   | 4x   | 2x   | 1x   |
| Cortex® M7  | 1x   | 1x   | 1x   | 1x   | 1x   | 1x   | 1x   | 1x   | 1x   |
| GPU         | 1x   | N/A  | 1x   | N/A  | 1x   | N/A  | N/A  | N/A  | N/A  |
| MIPI DSI    | 1x   | 1x   | 1x   | 1x   | 1x   | 1x   | N/A  | N/A  | N/A  |

**1.2 Ordering information**

[Table 3](#) shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

**Table 3. Orderable part numbers**

| Part number     | Sub-Family            | Options                                                                              | Cortex-A53 CPU speed grade | Qualification tier | Temperature T <sub>j</sub> (°C) | Package                  |
|-----------------|-----------------------|--------------------------------------------------------------------------------------|----------------------------|--------------------|---------------------------------|--------------------------|
| MIMX8MN6DVTJZAA | i.MX 8M Nano Quad     | 4x A53, M7, GPU, MIPI DSI                                                            | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN6DVTJZCA | i.MX 8M Nano Quad     | 4x A53, M7, GPU, Immersiv3D with Dolby ATMOS support <sup>1</sup> , MIPI DSI         | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN6DVTJZDA | i.MX 8M Nano Quad     | 4x A53, M7, GPU, Immersiv3D with Dolby ATMOS and DTS support <sup>1</sup> , MIPI DSI | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN5DVTJZAA | i.MX 8M Nano QuadLite | 4x A53, M7, No GPU, MIPI DSI                                                         | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN4DVTJZAA | i.MX 8M Nano Dual     | 2x A53, M7, GPU, MIPI DSI                                                            | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN3DVTJZAA | i.MX 8M Nano DualLite | 2x A53, M7, No GPU, MIPI DSI                                                         | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN2DVTJZAA | i.MX 8M Nano Solo     | 1x A53, M7, GPU, MIPI DSI                                                            | 1.5 GHz                    | Consumer           | 0 to 95                         | 14 x 14 mm, 0.5 mm pitch |

**Table 3. Orderable part numbers (continued)**

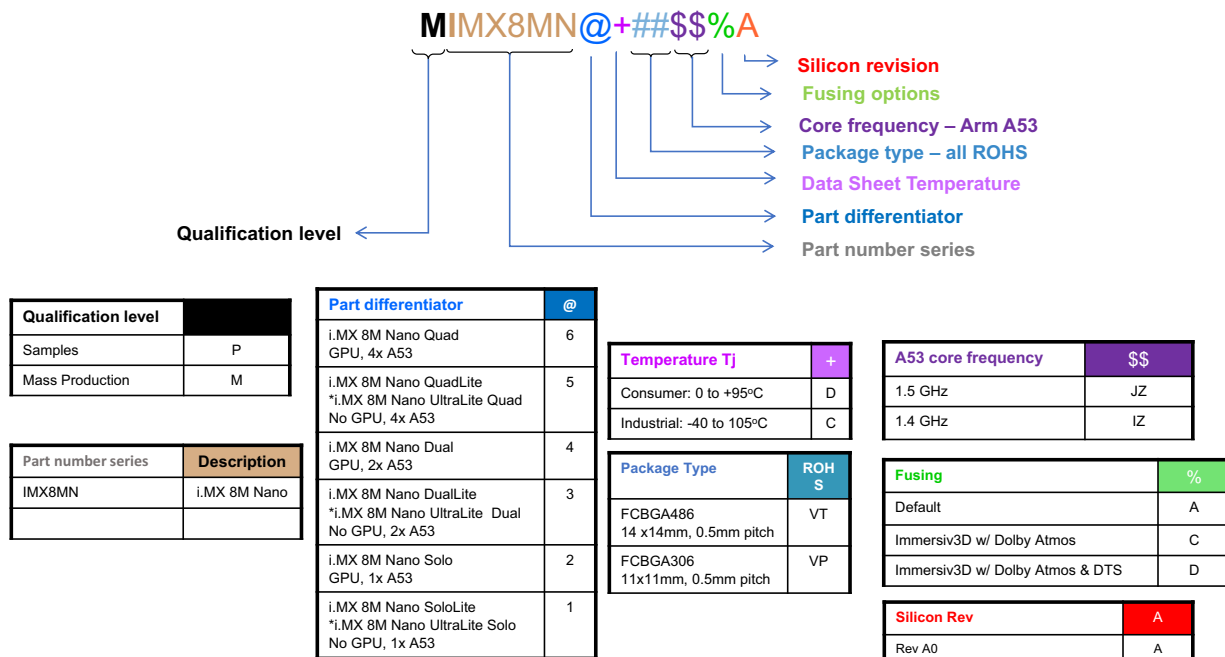
|                 |                             |                                                                                            |         |          |         |                          |
|-----------------|-----------------------------|--------------------------------------------------------------------------------------------|---------|----------|---------|--------------------------|
| MIMX8MN1DVTJZAA | i.MX 8M Nano SoloLite       | 1x A53, M7, No GPU, MIPI DSI                                                               | 1.5 GHz | Consumer | 0 to 95 | 14 x 14 mm, 0.5 mm pitch |
| MIMX8MN5DVPIZCA | i.MX 8M Nano UltraLite Quad | 4x A53, M7, Immersiv3D with Dolby ATMOS support <sup>1</sup> , No GPU, No MIPI DSI         | 1.4 GHz | Consumer | 0 to 95 | 11 x 11 mm, 0.5 mm pitch |
| MIMX8MN5DVPIZDA | i.MX 8M Nano UltraLite Quad | 4x A53, M7, Immersiv3D with Dolby ATMOS and DTS support <sup>1</sup> , No GPU, No MIPI DSI | 1.4 GHz | Consumer | 0 to 95 | 11 x 11 mm, 0.5 mm pitch |
| MIMX8MN5DVPIZAA | i.MX 8M Nano UltraLite Quad | 4x A53, M7, No GPU, No MIPI DSI                                                            | 1.4 GHz | Consumer | 0 to 95 | 11 x 11 mm, 0.5 mm pitch |
| MIMX8MN3DVPIZAA | i.MX 8M Nano UltraLite Dual | 2x A53, M7, No GPU, No MIPI DSI                                                            | 1.4 GHz | Consumer | 0 to 95 | 11 x 11 mm, 0.5 mm pitch |
| MIMX8MN1DVPIZAA | i.MX 8M Nano UltraLite Solo | 1x A53, M7, No GPU, No MIPI DSI                                                            | 1.4 GHz | Consumer | 0 to 95 | 11 x 11 mm, 0.5 mm pitch |

<sup>1</sup> Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.

## i.MX 8M Nano introduction



\*i.MX 8M Nano UltraLite Quad/Dual/Solo (11x11 package) has no MIPI DSI

**Figure 2. Part number nomenclature—i.MX 8M Nano family of processors**



## 2 Modules list

The i.MX 8M Nano family of processors contains a variety of digital and analog modules. [Table 4](#) describes these modules in alphabetical order.

**Table 4. i.MX 8M Nano modules list**

| Block mnemonic                            | Block name                                                              | Brief description                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| APBH-DMA                                  | NAND Flash and BCH ECC DMA Controller                                   | DMA controller used for GPMI2 operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Arm                                       | Arm Platform                                                            | The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M7 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M7 core is used as a customer microcontroller.                                                                                                                                     |
| BCH                                       | Binary-BCH ECC Processor                                                | The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)                                                                                                                                                                                                                                                                                                                                                                                          |
| CAAM                                      | Cryptographic accelerator and assurance module                          | CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Nano processors, the secure memory provided is 32 KB. |
| CCM<br>GPC<br>SRC                         | Clock Control Module, General Power Controller, System Reset Controller | These modules are responsible for clock and reset distribution in the system, and also for the system power management.                                                                                                                                                                                                                                                                                                                                                                  |
| CSU                                       | Central Security Unit                                                   | The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Nano platform.                                                                                                                                                                                                                                                                                                                                                               |
| CTI-0<br>CTI-1<br>CTI-2<br>CTI-3<br>CTI-4 | Cross Trigger Interface                                                 | Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.                                                                                                                                                                                                                                                                                                                         |
| DAP                                       | Debug Access Port                                                       | The DAP provides real-time access for the debugger without halting the core to access: <ul style="list-style-type: none"> <li>• System memory and peripheral registers</li> <li>• All debug configuration registers</li> </ul> The DAP also provides debugger access to JTAG scan chains.                                                                                                                                                                                                |
| DDRC                                      | Double Data Rate Controller                                             | The DDR Controller has the following features: <ul style="list-style-type: none"> <li>• Supports 16-bit LPDDR4-3200, DDR4-2400, and DDR3L-1600</li> <li>• Supports up to 8 Gbyte DDR memory space</li> </ul>                                                                                                                                                                                                                                                                             |
| eCSPI1<br>eCSPI2<br>eCSPI3                | Configurable SPI                                                        | Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.                                                                                                                                                                                                                                                                                                        |

Table 4. i.MX 8M Nano modules list (continued)

| Block mnemonic                               | Block name                       | Brief description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ENET1                                        | Ethernet Controller              | The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the <i>i.MX 8M Nano Applications Processor Reference Manual</i> (IMX8MNRM) for details.                                                                                                                                                                                                                                                 |
| FlexSPI                                      | FlexSPI                          | The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features: <ul style="list-style-type: none"> <li>• Flexible sequence engine to support various flash vendor devices</li> <li>• Single pad/Dual pad/Quad pad mode of operation</li> <li>• Single Data Rate/Double Data Rate mode of operation</li> <li>• Parallel Flash mode</li> <li>• DMA support</li> <li>• Memory mapped read access to connected flash devices</li> <li>• Multi master access with priority and flexible and configurable buffer for each master</li> </ul>                                                                          |
| GIC                                          | Generic Interrupt Controller     | The GIC handles all interrupts from the various subsystems and is ready for virtualization.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| GPC                                          | General Power Control Module     | The GPC independently control reset and gated clock to each switched power domain when powering on/off the domain.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GPIO1<br>GPIO2<br>GPIO3<br>GPIO4<br>GPIO5    | General Purpose I/O Modules      | Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| GPMI                                         | General Purpose Memory Interface | The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| GPT1<br>GPT2<br>GPT3<br>GPT4<br>GPT5<br>GPT6 | General Purpose Timer            | Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |
| GPU3D                                        | Graphics Processing Unit-3D      | The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| I2C1<br>I2C2<br>I2C3<br>I2C4                 | I <sup>2</sup> C Interface       | I <sup>2</sup> C provides serial interface for external devices. Data rates of up to 320 kbps are supported.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

Table 4. i.MX 8M Nano modules list (continued)

| Block mnemonic                       | Block name                    | Brief description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IOMUXC                               | IOMUX Control                 | This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| LCDIF                                | LCD interface                 | The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability, the key feature of the display controller includes: <ul style="list-style-type: none"> <li>• Support 8-bit/16-bit/24-bit/32-bit pixel depth</li> <li>• Support DOTCLK mode for MIPI-DPI interface</li> <li>• Support resolution up to 1920 x 1200p60</li> </ul>                                                                                                                                                                                                                                                                                                                                               |
| MIPI CSI (four-lane)                 | MIPI Camera Serial Interface  | This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| MIPI DSI (four-lane)                 | MIPI Display Serial Interface | This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| OCOTP_CTRL                           | OTP Controller                | The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility. |
| OCRAM                                | On-Chip Memory controller     | The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module.<br>In i.MX 8M Nano processors, the OCRAM is used for controlling the 512 KB multimedia RAM through a 64-bit AXI bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| PDM                                  | Pulse Density Modulation      | The PDM supports up to 8-channels (4 lanes).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| PWM1<br>PWM2<br>PWM3<br>PWM4         | Pulse Width Modulation        | The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SAI2<br>SAI3<br>SAI5<br>SAI6<br>SAI7 | Synchronous Audio Interface   | The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

Table 4. i.MX 8M Nano modules list (continued)

| Block mnemonic                   | Block name                               | Brief description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDMA                             | Smart Direct Memory Access               | <p>The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features:</p> <ul style="list-style-type: none"> <li>• Powered by a 16-bit Instruction-Set micro-RISC engine</li> <li>• Multi channel DMA supporting up to 32 time-division multiplexed DMA channels</li> <li>• 48 events with total flexibility to trigger any combination of channels</li> <li>• Memory accesses including linear, FIFO, and 2D addressing</li> <li>• Shared peripherals between Arm and SDMA</li> <li>• Very fast Context-Switching with 2-level priority based preemptive multi tasking</li> <li>• DMA units with auto-flush and prefetch capability</li> <li>• Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)</li> <li>• DMA ports can handle unidirectional and bidirectional flows (Copy mode)</li> <li>• Up to 8-word buffer for configurable burst transfers for EMIv2.5</li> <li>• Support of byte-swapping and CRC calculations</li> <li>• Library of Scripts and API is available</li> </ul> |
| SJC                              | Secure JTAG Controller                   | <p>The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Nano family of processors uses JTAG port for system debugging. The JTAG port must be accessible during platform initial laboratory bring-up, for troubleshooting, as well as for software debugging by authorized entities. The i.MX 8M Nano SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| SNVS                             | Secure Non-Volatile Storage              | Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| SPDIF1                           | Sony Philips Digital Interconnect Format | A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| TEMPSENSOR                       | Temperature Sensor                       | Temperature sensor                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| TZASC                            | Trust-Zone Address Space Controller      | The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| UART1<br>UART2<br>UART3<br>UART4 | UART Interface                           | <p>Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations:</p> <ul style="list-style-type: none"> <li>• 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none)</li> <li>• Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard.</li> <li>• 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

Table 4. i.MX 8M Nano modules list (continued)

| Block mnemonic             | Block name                                                                       | Brief description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| uSDHC1<br>uSDHC2<br>uSDHC3 | SD/MMC and SDXC<br>Enhanced Multi-Media Card /<br>Secure Digital Host Controller | i.MX 8M Nano SoC characteristics:<br>All the MMC/SD/SDIO controller IPs are based on the uSDHC IP.<br>They are designed to support: <ul style="list-style-type: none"> <li>• SD/SDIO standard, up to version 3.0.</li> <li>• MMC standard, up to version 5.1.</li> <li>• 1.8 V and 3.3 V operation, but do not support 1.2 V operation.</li> <li>• 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode.</li> </ul> One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface. |
| USB 2.0                    | 1x USB 2.0 controller and PHY                                                    | One USB controller and PHY that support USB 2.0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| WDOG1<br>WDOG2<br>WDOG3    | Watchdog                                                                         | The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.                                                                                                                                                                                                                                                                                                                       |

## 2.1 Recommended connections for unused input/output

If a function of the i.MX 8M Nano is not in use, the I/Os and power rails of that function can be terminated to reduce overall board power.

Table 5 shows the recommended connections for 14 x 14 mm package unused power supply rails.

Table 5. Recommended connections for 14 x 14 mm package unused power supply rails

| Function             | Ball Name                                                                                                                                                                                   | Recommendations if Unused                                                                                                                                                                                                                        |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIP-CSI and MIPI-DSI | VDD_MIPI_0P8, VDD_MIPI_1P2, VDD_MIPI_1P8                                                                                                                                                    | Leave unconnected                                                                                                                                                                                                                                |
| USB1                 | VDD_USB_0P8, VDD_USB_1P8, VDD_USB_3P3                                                                                                                                                       | Leave unconnected                                                                                                                                                                                                                                |
| GPU                  | VDD_GPU                                                                                                                                                                                     | Leave unconnected                                                                                                                                                                                                                                |
| Digital I/O supplies | NVCC_CLK, NVCC_ECSPi, NVDD_ENET, NVCC_GPIO1, NVCC_I2C, NVCC_JTAG, NVCC_NAND, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_SD1, NVCC_SD2, NVCC_UART, NVCC_SNVS_1P8, PVCC0_1P8, PVCC1_1P8, PVCC2_1P8 | All digital I/O supplies listed in this table must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to enable pull in pad control register to limit any floating gate current. |

Table 6 shows the recommended connections for 11 x 11 mm package unused power supply rails.

**Table 6. Recommended connections for 11 x 11 mm package unused power supply rails**

| Function             | Ball Name                                                                                                                      | Recommendations if Unused                                                                                                                                                                                                                        |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIP-CSI              | VDD_MIPI_1P2                                                                                                                   | Leave unconnected                                                                                                                                                                                                                                |
| USB1                 | VDD_USB_0P8, VDD_USB_1P8, VDD_USB_3P3                                                                                          | Leave unconnected                                                                                                                                                                                                                                |
| Digital I/O supplies | NVCC_ENET_GPIO_SAI2, NVCC_CLK_JTAG_PVCC_1P8, NVCC_I2C_UART, NVCC_SAI3_SAI5, NVCC_SD1_NAND, NVCC_ECSPI, NVCC_SD2, NVCC_SNV5_1P8 | All digital I/O supplies listed in this table must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to enable pull in pad control register to limit any floating gate current. |

Table 7 shows recommended connections for 14 x 14 mm package unused signal contacts/interfaces.

**Table 7. Recommended connections for 14 x 14 mm package unused signal contacts/interfaces**

| Function | Ball Name                                                                   | Recommendations if Unused |
|----------|-----------------------------------------------------------------------------|---------------------------|
| MIPI-CSI | MIPI_CSI_CLK_P, MIPI_CSI_CLK_N, MIPI_CSI_Dx_P, MIPI_CSI_Dx_N                | Tie all signals to ground |
| MIPI-DSI | MIPI_VREG_CAP, MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N | Leave unconnected         |
| USB1     | USB1_VBUS, USB1_DN, USB1_DP, USB1_ID, USB1_TXRTUNE                          | Leave unconnected         |

Table 8 shows recommended connections for 11 x 11 mm package unused signal contacts/interfaces.

**Table 8. Recommended connections for 11 x 11 mm package unused signal contacts/interfaces**

| Function | Ball Name                                                    | Recommendations if Unused |
|----------|--------------------------------------------------------------|---------------------------|
| USB1     | USB1_VBUS, USB1_DN, USB1_DP, USB1_ID, USB1_TXRTUNE           | Leave unconnected         |
| MIPI-CSI | MIPI_CSI_CLK_P, MIPI_CSI_CLK_N, MIPI_CSI_Dx_P, MIPI_CSI_Dx_N | Tie all signals to ground |

## 3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Nano family of processors.

### 3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See [Table 9](#) for a quick reference to the individual tables and sections.

**Table 9. i.MX 8M Nano chip-level conditions**

| For these characteristics, ...                               | Topic appears ...          |
|--------------------------------------------------------------|----------------------------|
| <a href="#">Absolute maximum ratings</a>                     | <a href="#">on page 15</a> |
| <a href="#">Thermal resistance</a>                           | <a href="#">on page 18</a> |
| <a href="#">Operating ranges</a>                             | <a href="#">on page 19</a> |
| <a href="#">External clock sources</a>                       | <a href="#">on page 22</a> |
| <a href="#">Estimated power supply maximum currents</a>      | <a href="#">on page 23</a> |
| <a href="#">Power modes</a>                                  | <a href="#">on page 24</a> |
| <a href="#">Power supplies requirements and restrictions</a> | <a href="#">on page 28</a> |

#### 3.1.1 Absolute maximum ratings

##### CAUTION

Stresses beyond those listed under [Table 10](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

**Table 10. Absolute maximum ratings for 14 x 14 mm package**

| Parameter description   | Symbol             | Min  | Max   | Unit | Notes |
|-------------------------|--------------------|------|-------|------|-------|
| Core supply voltages    | VDD_ARM<br>VDD_SOC | -0.3 | 1.15  | V    | —     |
| Power supply for GPU    | VDD_GPU            | -0.3 | 1.15  | V    | —     |
| DDR PHY supply voltage  | VDD_DRAM           | -0.3 | 1.15  | V    | —     |
| DDR I/O supply voltage  | NVCC_DRAM          | -0.3 | 1.575 | V    | —     |
| DRAM PLL supply voltage | VDD_DRAM_PLL_0P8   | -0.3 | 1.15  | V    | —     |
|                         | VDD_DRAM_PLL_1P8   | -0.3 | 2.15  | V    | —     |
| SNVS IO supply voltage  | NVCC_SNVS_1P8      | -0.3 | 2.15  | V    | —     |
| VDD_SNVS supply voltage | VDD_SNVS_0V8       | -0.3 | 0.95  | V    | —     |

Table 10. Absolute maximum ratings for 14 x 14 mm package (continued)

| Parameter description          | Symbol                                                                                                                                                                          | Min  | Max  | Unit | Notes |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| GPIO supply voltage            | NVCC_JTAG,<br>NVCC_GPIO1,<br>NVCC_ENET,<br>NVCC_SD1,<br>NVCC_SD2,<br>NVCC_NAND,<br>NVCC_SAI2,<br>NVCC_SAI3,<br>NVCC_SAI5,<br>NVCC_ECSP1,<br>NVCC_I2C,<br>NVCC_UART,<br>NVCC_CLK | -0.3 | 3.8  | V    | —     |
| GPIO pre-driver supply voltage | PVCC0_1P8,<br>PVCC1_1P8,<br>PVCC2_1P8                                                                                                                                           | -0.3 | 2.15 | V    | —     |
| Isolated core supply voltage   | VDD_ANA_0P8                                                                                                                                                                     | -0.3 | 1.15 | V    | —     |
| Analog core supply voltage     | VDD_ANA0_1P8                                                                                                                                                                    | -0.3 | 2.15 | V    | —     |
|                                | VDD_ANA1_1P8                                                                                                                                                                    | -0.3 | 2.15 | V    | —     |
| Arm PLL supply voltage         | VDD_ARM_PLL_0P8                                                                                                                                                                 | -0.3 | 1.15 | V    | —     |
|                                | VDD_ARM_PLL_1P8                                                                                                                                                                 | -0.3 | 2.15 | V    | —     |
| MIPI PHY supply voltage        | VDD_MIPI_0P8                                                                                                                                                                    | -0.3 | 1.15 | V    | —     |
|                                | VDD_MIPI_1P2                                                                                                                                                                    | -0.3 | 1.45 | V    | —     |
|                                | VDD_MIPI_1P8                                                                                                                                                                    | -0.3 | 2.15 | V    | —     |
| USB PHY supply voltage         | VDD_USB_0P8                                                                                                                                                                     | -0.3 | 1.15 | V    | —     |
|                                | VDD_USB_1P8                                                                                                                                                                     | -0.3 | 2.15 | V    | —     |
|                                | VDD_USB_3P3                                                                                                                                                                     | -0.3 | 3.95 | V    | —     |
| USB_VBUS input detected        | USB1_VBUS                                                                                                                                                                       | -0.3 | 3.95 | V    | —     |
| XTAL supply voltage            | VDD_24M_XTAL_1P8                                                                                                                                                                | -0.3 | 2.15 | V    | —     |
| Storage temperature range      | T <sub>STORAGE</sub>                                                                                                                                                            | -40  | 150  | °C   | —     |

Table 11. Absolute maximum ratings for 11 x 11 mm package

| Parameter description           | Symbol           | Min  | Max   | Unit | Notes |
|---------------------------------|------------------|------|-------|------|-------|
| Core and DDR PHY supply voltage | VDD_SOC          | -0.3 | 1.15  | V    | —     |
| DDR I/O supply voltage          | NVCC_DRAM        | -0.3 | 1.575 | V    | —     |
| DRAM PLL supply voltage         | VDD_DRAM_PLL_1P8 | -0.3 | 2.15  | V    | —     |
| SNVS IO supply voltage          | NVCC_SNVS_1P8    | -0.3 | 2.15  | V    | —     |



Table 11. Absolute maximum ratings for 11 x 11 mm package (continued)

| Parameter description                                              | Symbol                                                                                                     | Min  | Max  | Unit | Notes |
|--------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| VDD_SNVs supply voltage                                            | VDD_SNVs_0V8                                                                                               | -0.3 | 0.95 | V    | —     |
| GPIO supply voltage                                                | NVCC_ENET_GPIO_S<br>AI2,<br>NVCC_I2C_UART,<br>NVCC_SAI3_SAI5,<br>NVCC_SD1_NAND,<br>NVCC_ECSPI,<br>NVCC_SD2 | -0.3 | 3.8  | V    | —     |
| GPIO supply voltage                                                | NVCC_CLK_JTAG_PV<br>CC_1P8                                                                                 | -0.3 | 2.15 | V    | —     |
| XTAL, Analog core, MIPI PHY<br>and USB PHY 1.8 V supply<br>voltage | VDD_ANA1_XTAL_MIP<br>I_USB_1P8                                                                             | -0.3 | 2.15 | V    | —     |
| Analog core and ARM PLL 1.8 V<br>supply voltage                    | VDD_ANA0_ARM_PLL<br>_1P8                                                                                   | -0.3 | 2.15 | V    | —     |
| MIPI PHY 1.2 V supply voltage                                      | VDD_MIPI_1P2                                                                                               | -0.3 | 1.45 | V    | —     |
| USB PHY 3.3 V supply voltage                                       | VDD_USB_3P3                                                                                                | -0.3 | 3.95 | V    | —     |
| USB_VBUS input detected                                            | USB1_VBUS                                                                                                  | -0.3 | 3.95 | V    | —     |
| XTAL supply voltage                                                | VDD_24M_XTAL_1P8                                                                                           | -0.3 | 2.15 | V    | —     |
| Storage temperature range                                          | T <sub>STORAGE</sub>                                                                                       | -40  | 150  | °C   | —     |

Table 12. Electrostatic discharge and latch up ratings

| Parameter description         |                                                                                                     | Rating  | Reference   | Comment                                                                                                    |
|-------------------------------|-----------------------------------------------------------------------------------------------------|---------|-------------|------------------------------------------------------------------------------------------------------------|
| Electrostatic Discharge (ESD) | Human Body Model (HBM)                                                                              | ±1000 V | JS-001-2017 | —                                                                                                          |
|                               | Charged Device Model (CDM)                                                                          | ±250 V  | JS-002-2018 | —                                                                                                          |
| Latch UP (LU)                 | Immunity level:<br>• Class I @ 25 °C ambient temperature<br>• Class II @ 105 °C ambient temperature | A<br>A  | JESD78E     | Mandatory requirement:<br>JTAG_TMS pin must be connected with a 50 ohm series resistor near the component. |

## 3.1.2 Thermal resistance

### 3.1.2.1 14 x 14 mm FCBGA package thermal resistance

Table 13 displays the 14 x 14 mm FCBGA package thermal resistance data.

**Table 13. 14 x 14 mm package thermal resistance data**

| Rating                                    | Test conditions                                    | Symbol           | Value | Unit | Notes   |
|-------------------------------------------|----------------------------------------------------|------------------|-------|------|---------|
| Junction to Ambient<br>Natural Convection | Single layer board (1s)<br>Four layer board (2s2p) | $R_{\theta JA}$  | 30    | °C/W | 1, 2    |
| Junction to Ambient<br>Natural Convection | Four layer board (2s2p)<br>Four layer board (2s2p) | $R_{\theta JA}$  | 22.9  | °C/W | 1, 2, 3 |
| Junction to Ambient (@200 ft/min)         | Single layer board (1s)                            | $R_{\theta JMA}$ | 24    | °C/W | 1, 3    |
| Junction to Ambient (@200 ft/min)         | Four layer board (2s2p)                            | $R_{\theta JMA}$ | 18.5  | °C/W | 1, 3    |
| Junction to Board                         | —                                                  | $R_{\theta JB}$  | 7.8   | °C/W | 4       |
| Junction to Case                          | —                                                  | $R_{\theta JC}$  | 4     | °C/W | 5       |
| Junction to Package Top                   | Natural Convection                                 | $\Psi_{JT}$      | 0.2   | °C/W | 6       |

<sup>1</sup> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JESD51-2 with the single layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 3.1.2.2 11 x 11 mm FCBGA package thermal resistance

Table 14 displays the 11 x 11 mm FCBGA package thermal resistance data.

**Table 14. 11 x 11 mm thermal resistance data<sup>1</sup>**

| Rating                                                                     | Board type <sup>2</sup> | Symbol          | Value    | Unit |
|----------------------------------------------------------------------------|-------------------------|-----------------|----------|------|
|                                                                            |                         |                 | Coreless |      |
| Junction to Ambient Thermal Resistance <sup>3</sup>                        | JESD51-9, 2s2p          | $R_{\theta JA}$ | 27.7     | °C/W |
| Junction-to-Top of Package Thermal Characterization Parameter <sup>3</sup> | JESD51-9, 2s2p          | $\Psi_{JT}$     | 5.2      | °C/W |
| Junction to Case Resistance <sup>4</sup>                                   | JESD51-9, 1s            | $R_{\theta JC}$ | 11       | °C/W |

<sup>1</sup> Non-uniform power is applied on the die.

- <sup>2</sup> Thermal test board meets JEDEC specification for this package (JESD51-9). Test board has 40 vias under die shadow mapped according to BGA layout under die. Each via is 0.2 mm in diameter and connects top layer with the first buried plane layer.
- <sup>3</sup> Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
- <sup>4</sup> Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the surface temperature at the package top side.

### 3.1.3 Operating ranges

Table 15 provides the operating ranges of the i.MX 8M Nano applications processor. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM).

**Table 15. Operating ranges for 14 x 14 mm package**

| Symbol                                                                                                                                                              | Min   | Typ   | Max <sup>1</sup> | Unit | Comment                                                          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|------------------|------|------------------------------------------------------------------|
| VDD_ARM                                                                                                                                                             | 0.805 | 0.850 | 0.950            | V    | Power supply for Cortex® A53, 1.2 GHz                            |
|                                                                                                                                                                     | 0.900 | 0.950 | 1.000            | V    | Power supply for Cortex® A53, 1.4 GHz                            |
|                                                                                                                                                                     | 0.950 | 1.000 | 1.050            | V    | Power supply for Cortex® A53, 1.5 GHz <sup>2</sup>               |
| VDD_SOC <sup>3</sup>                                                                                                                                                | 0.805 | 0.850 | 0.900            | V    | Power supply for SoC logic <sup>4</sup> , Cortex® M7 600 MHz     |
|                                                                                                                                                                     | 0.900 | 0.950 | 1.000            | V    | Power supply for SoC logic, overdrive mode, Cortex® M7 750 MHz   |
| VDD_GPU <sup>3</sup>                                                                                                                                                | 0.805 | 0.850 | 0.900            | V    | Power supply for 3D GPU, nominal mode, 400 MHz                   |
|                                                                                                                                                                     | 0.900 | 0.950 | 1.000            | V    | Power supply for 3D GPU, overdrive mode, 600 MHz                 |
| VDD_DRAM <sup>3</sup>                                                                                                                                               | 0.805 | 0.850 | 0.900            | V    | Power supply for DDRC, 0.85 V supports up to 1.2 GHz (DDR clock) |
|                                                                                                                                                                     | 0.900 | 0.950 | 1.000            | V    | Power supply for DDRC, 0.95 V supports up to 1.6 GHz (DDR clock) |
| VDD_SNVS_0P8                                                                                                                                                        | 0.760 | 0.800 | 0.900            | V    | Power supply for SNVS core logic                                 |
| NVCC_SNVS_1P8                                                                                                                                                       | 1.620 | 1.800 | 1.980            | V    | Power supply for GPIO pre-driver in SNVS bank                    |
| NVCC_JTAG,<br>NVCC_GPIO1,<br>NVCC_ENET, NVCC_SD1,<br>NVCC_SD2, NVCC_NAND,<br>NVCC_SAI2, NVCC_SAI3,<br>NVCC_SAI5,<br>NVCC_ECSPi, NVCC_I2C,<br>NVCC_UART,<br>NVCC_CLK | 1.650 | 1.800 | 1.950            | V    | Power supply for GPIO when it is in 1.8 V mode                   |
|                                                                                                                                                                     | 3.000 | 3.300 | 3.600            | V    | Power supply for GPIO when it is in 3.3 V mode                   |
| NVCC_ENET                                                                                                                                                           | 2.250 | 2.500 | 2.750            | V    | Power supply for GPIO when it is in 2.5 V mode                   |

Table 15. Operating ranges for 14 x 14 mm package (continued)

| Symbol                                | Min                 | Typ                | Max <sup>1</sup>    | Unit | Comment                                                        |
|---------------------------------------|---------------------|--------------------|---------------------|------|----------------------------------------------------------------|
| PVCC0_1P8,<br>PVCC1_1P8,<br>PVCC2_1P8 | 1.650               | 1.800              | 1.950               | V    | Power supply for GPIO pre-driver                               |
| VSS                                   | —                   | —                  | —                   | V    | Ground for all core logic and I/O                              |
| NVCC_DRAM                             | 1.283               | 1.35               | 1.425               | V    | DDR3L                                                          |
|                                       | 1.14                | 1.2                | 1.26                | V    | DDR4                                                           |
|                                       | 1.06                | 1.1                | 1.14                | V    | LPDDR4                                                         |
| DRAM_VREF                             | 0.49 x<br>NVCC_DRAM | 0.5 x<br>NVCC_DRAM | 0.51 x<br>NVCC_DRAM | V    | Internal output, no connection is needed.                      |
| VDD_DRAM_PLL_0P8                      | 0.805               | 0.850              | 0.900               | V    | Power supply for DRAM PLL, nominal mode                        |
|                                       | 0.900               | 0.950              | 1.000               | V    | Power supply for DRAM PLL, overdrive mode                      |
| VDD_ANA0_1P8<br>VDD_ANA1_1P8          | 1.71                | 1.8                | 1.89                | V    | Analog 1.8 V core power                                        |
| VDD_ANA_0P8                           | 0.805               | 0.850              | 0.900               | V    | Supplies for Analog PLL, nominal mode                          |
|                                       | 0.900               | 0.950              | 1.000               | V    | Supplies for Analog PLL, overdrive mode                        |
| VDD_ARM_PLL_0P8                       | 0.805               | 0.850              | 0.900               | V    | Power supply for Arm PLL, nominal mode                         |
|                                       | 0.900               | 0.950              | 1.000               | V    | Power supply for Arm PLL, overdrive mode                       |
| VDD_ARM_PLL_1P8                       | 1.71                | 1.8                | 1.89                | V    | Arm PLL 1.8 V power                                            |
| VDD_24M_XTAL_1P8                      | 1.71                | 1.8                | 1.89                | V    | XTAL 1.8 V power                                               |
| VDD_DRAM_PLL_1P8                      | 1.71                | 1.8                | 1.89                | V    | Analog 1.8 V core power                                        |
| VDD_MIPI_0P8                          | 0.805               | 0.850              | 0.900               | V    | Digital supply for MIPI PHY, nominal mode                      |
|                                       | 0.900               | 0.950              | 1.000               | V    | Digital supply for MIPI PHY, overdrive mode                    |
| VDD_MIPI_1P2                          | 1.14                | 1.2                | 1.26                | V    | 1.2 V power for analog                                         |
| VDD_MIPI_1P8                          | 1.71                | 1.8                | 1.89                | V    | 1.8 V power for PLL and analog                                 |
| VDD_USB_0P8                           | 0.805               | 0.850              | 0.900               | V    | Digital power supply from PHY's I/O power pads, nominal mode   |
|                                       | 0.900               | 0.950              | 1.000               | V    | Digital power supply from PHY's I/O power pads, overdrive mode |
| VDD_USB_1P8                           | 1.71                | 1.80               | 1.89                | V    | 1.8 V analog power supply                                      |
| VDD_USB_3P3                           | 3.069               | 3.30               | 3.6                 | V    | 3.3 V analog power supply                                      |

Table 15. Operating ranges for 14 x 14 mm package (continued)

| Symbol                                   | Min  | Typ | Max <sup>1</sup> | Unit | Comment                                                             |
|------------------------------------------|------|-----|------------------|------|---------------------------------------------------------------------|
| USB1_VBUS                                | 1.34 | —   | 3.60             | V    | USB_VBUS input detect signal                                        |
| Temperature Sensor Accuracy <sup>5</sup> | —    | ±3  | ±5               | °C   | Sensing temperature range 10°C to 105°C                             |
| T <sub>J</sub>                           | 0    | —   | +95              | °C   | See Table 3 for complete list of junction temperature capabilities. |

<sup>1</sup> Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (V<sub>min</sub> + the supply tolerance) is recommended. This results in an optimized power/speed ratio.

<sup>2</sup> For VDD\_ARM at 1.0V typical, Power-on Hours will decreased if junction temperature is increased. Please refer to *i.MX 8M Nano Product Lifetime Usage (AN12983)* for details.

<sup>3</sup> VDD\_DRAM, VDD\_SOC, and VDD\_GPU are required to be tied together and keep same or ground.

<sup>4</sup> Booting VDD\_SOC at 0.800 V ±5% is acceptable (V<sub>min</sub> = 0.760 V). Software is expected to program the VDD\_SOC voltage to the typical value in this table prior to first DRAM memory access.

<sup>5</sup> “EN” of TMU Enable Register (TMU\_TER) is required to be always enabled for the part to operate correctly.

Table 16. Operating ranges for 11 x11 mm package

| Symbol                                                                                                 | Min                 | Typ                | Max <sup>1</sup>    | Unit | Comment                                                                                                               |
|--------------------------------------------------------------------------------------------------------|---------------------|--------------------|---------------------|------|-----------------------------------------------------------------------------------------------------------------------|
| VDD_SOC                                                                                                | 0.805               | 0.850              | 0.900               | V    | Power supply for SoC logic <sup>2</sup> , Cortex® M7 600 MHz; Cortex® A53, 1.2 GHz, nominal mode, 1.2 GHz DDR clock   |
|                                                                                                        | 0.900               | 0.950              | 1.000               | V    | Power supply for SoC logic <sup>2</sup> , Cortex® M7 750 MHz; Cortex® A53, 1.4 GHz, overdrive mode, 1.6 GHz DDR clock |
| VDD_SNVS_0P8                                                                                           | 0.760               | 0.800              | 0.900               | V    | Power supply for SNVS core logic                                                                                      |
| NVCC_SNVS_1P8                                                                                          | 1.620               | 1.800              | 1.980               | V    | Power supply for GPIO pre-driver in SNVS bank                                                                         |
| NVCC_I2C_UART,<br>NVCC_SAI3_SAI5,<br>NVCC_SD1_NAND,<br>NVCC_ECSPi,<br>NVCC_SD2,<br>NVCC_ENET_GPIO_SAI2 | 1.650               | 1.800              | 1.950               | V    | Power supply for GPIO when it is in 1.8 V mode                                                                        |
|                                                                                                        | 3.000               | 3.300              | 3.600               | V    | Power supply for GPIO when it is in 3.3 V mode                                                                        |
| NVCC_CLK_JTAG_PVCC_1P8                                                                                 | 1.650               | 1.800              | 1.950               | V    | Power supply for GPIO and GPIO pre-driver in 1.8 V mode                                                               |
| VSS                                                                                                    | —                   | —                  | —                   | V    | Ground for all core logic and I/O                                                                                     |
| NVCC_DRAM                                                                                              | 1.283               | 1.35               | 1.425               | V    | DDR3L                                                                                                                 |
|                                                                                                        | 1.14                | 1.2                | 1.26                | V    | DDR4                                                                                                                  |
|                                                                                                        | 1.06                | 1.1                | 1.14                | V    | LPDDR4                                                                                                                |
| DRAM_VREF                                                                                              | 0.49 x<br>NVCC_DRAM | 0.5 x<br>NVCC_DRAM | 0.51 x<br>NVCC_DRAM | V    | Internal output, no connection is needed.                                                                             |

Table 16. Operating ranges for 11 x11 mm package (continued)

| Symbol                                                      | Min   | Typ  | Max <sup>1</sup> | Unit | Comment                                                                              |
|-------------------------------------------------------------|-------|------|------------------|------|--------------------------------------------------------------------------------------|
| VDD_ANA1_XTAL_MIP1_U<br>SB_1P8,<br>VDD_ANA0_ARM_PLL_1P<br>8 | 1.71  | 1.8  | 1.89             | V    | 1.8 V power for Analog core, XTAL, MIP1<br>PLL and analog, USB analog and ARM<br>PLL |
| VDD_DRAM_PLL_1P8                                            | 1.71  | 1.8  | 1.89             | V    | Analog 1.8 V core power                                                              |
| VDD_MIP1_1P2                                                | 1.14  | 1.2  | 1.26             | V    | 1.2 V power for analog                                                               |
| VDD_USB_3P3                                                 | 3.069 | 3.30 | 3.6              | V    | 3.3 V analog power supply                                                            |
| USB1_VBUS                                                   | 1.34  | —    | 3.60             | V    | USB_VBUS input detect signal                                                         |
| Temperature Sensor<br>Accuracy <sup>2</sup>                 | —     | ±3   | ±5               | °C   | Sensing temperature range 10°C to<br>105°C                                           |
| T <sub>J</sub>                                              | 0     | —    | +95              | °C   | See Table 3 for complete list of junction<br>temperature capabilities.               |

<sup>1</sup> Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio.

<sup>2</sup> “EN” of TMU Enable Register (TMU\_TER) is required to be always enabled for the part to operate correctly.

### 3.1.4 External clock sources

Each i.MX 8M Nano processor has two external input system clocks: a low frequency (RTC\_XTALI) and a high frequency (XTALI).

The RTC\_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can only be connected to an external oscillator. RTC\_XTALO should be directly connected to VDD\_SNVS\_0P8.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 17 shows the interface frequency requirements.

Table 17. External input clock frequency

| Parameter Description             | Symbol            | Min | Typ                 | Max | Unit |
|-----------------------------------|-------------------|-----|---------------------|-----|------|
| RTC_XTALI Oscillator <sup>1</sup> | f <sub>ckil</sub> | —   | 32.768 <sup>2</sup> | —   | kHz  |
| XTALI Oscillator <sup>1,3</sup>   | f <sub>xtal</sub> |     | 24                  |     | MHz  |

<sup>1</sup> The required frequency stability of this clock source is application dependent.

<sup>2</sup> Recommended nominal frequency 32.768 kHz.

<sup>3</sup> External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

The typical values shown in Table 17 are required for use with NXP software to ensure precise time keeping and USB operation. For RTC\_XTALI operation, an external oscillator is necessary. RTC\_XTALO should be directly connected to VDD\_SNVS\_0P8 when using an external 32.768 kHz oscillator.

**NOTE**

There is no internal RC oscillator.

Table 18 shows the external input clock for OSC32K.

**Table 18. External input clock for OSC32K**

|           | Symbol | Min                 | Typ    | Max                 | Unit |
|-----------|--------|---------------------|--------|---------------------|------|
| Frequency | f      | —                   | 32.768 | —                   | kHz  |
| RTC_XTALI | VIH    | 0.7 x NVCC_SNVS_1P8 | —      | NVCC_SNVS_1P8       | V    |
|           | VIL    | 0                   | —      | 0.3 x NVCC_SNVS_1P8 | V    |

### 3.1.5 Estimated power supply maximum currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

The table below represents the estimated maximum current on the power supply rails and should be used as a guideline for power supply selection. The data below is based on a combination of design simulation and characterization data based on typical datasheet voltages. Actual power consumption for typical use cases are lower than values presented on the table below.

**Table 19. Estimated power supply maximum currents for 14 x 14 mm package**

| Power rail                   | Max current                                                                                                                                                                                                                                                                                                                    | Unit |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| VDD_ARM                      | 2200                                                                                                                                                                                                                                                                                                                           | mA   |
| VDD_SOC                      | 1000                                                                                                                                                                                                                                                                                                                           | mA   |
| VDD_GPU                      | 800                                                                                                                                                                                                                                                                                                                            | mA   |
| VDD_DRAM                     | 800                                                                                                                                                                                                                                                                                                                            | mA   |
| VDD_ANA_0P8                  | 50                                                                                                                                                                                                                                                                                                                             | mA   |
| VDD_ANA0_1P8<br>VDD_ANA1_1P8 | 250                                                                                                                                                                                                                                                                                                                            | mA   |
| NVCC_SNVS_1P8                | 3                                                                                                                                                                                                                                                                                                                              | mA   |
| NVCC_<XXX>                   | $I_{max} = N \times C \times V \times (0.5 \times F)$<br>Where:<br>N—Number of IO pins supplied by the power line<br>C—Equivalent external capacitive load<br>V—IO voltage<br>(0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F).<br>In this equation, $I_{max}$ is in Amps, C in Farads, V in Volts, and F in Hertz. |      |
| NVCC_DRAM                    |                                                                                                                                                                                                                                                                                                                                |      |
| DRAM_VFEF                    | 10                                                                                                                                                                                                                                                                                                                             | mA   |

Table 20. Estimated power supply maximum currents for 11 x 11 mm package

| Power rail                                                               | Max current                                                                                                                                                                                                                                                                                                                      | Unit |
|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| VDD_SOC                                                                  | 3000                                                                                                                                                                                                                                                                                                                             | mA   |
| NVCC_SNVS_1P8                                                            | 3                                                                                                                                                                                                                                                                                                                                | mA   |
| VDD_ANA1_XTAL_MIPI_USB_1P8,<br>VDD_ANA0_ARM_PLL_1P8,<br>VDD_DRAM_PLL_1P8 | 250                                                                                                                                                                                                                                                                                                                              | mA   |
| VDD_MIPI_1P2                                                             | 100                                                                                                                                                                                                                                                                                                                              | mA   |
| NVCC_<XXX>                                                               | $I_{\max} = N \times C \times V \times (0.5 \times F)$<br>Where:<br>N—Number of IO pins supplied by the power line<br>C—Equivalent external capacitive load<br>V—IO voltage<br>(0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F).<br>In this equation, $I_{\max}$ is in Amps, C in Farads, V in Volts, and F in Hertz. |      |
| NVCC_DRAM                                                                |                                                                                                                                                                                                                                                                                                                                  |      |
| DRAM_VFEF                                                                | 10                                                                                                                                                                                                                                                                                                                               | mA   |

### 3.1.6 Power modes

The i.MX 8M Nano supports the following power modes:

- **RUN Mode:** All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- **IDLE Mode:** When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M7 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.
- **SUSPEND Mode:** The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.
- **SNVS Mode:** This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- **OFF Mode:** All power rails are off.



Table 21 summaries the power supply states in all the power modes.

**Table 21. Chip power in different LP mode for 14 x 14 mm package**

| Mode                       | Supply             | Typ. <sup>1</sup> | Unit |
|----------------------------|--------------------|-------------------|------|
| SNVS                       | VDD_SNVS_0P8       | 0.10              | mW   |
|                            | NVCC_SNVS_1P8      | 1.20              |      |
|                            | Total <sup>2</sup> | 1.30              |      |
| SUSPEND                    | NVCC               | 0.80              | mW   |
|                            | NVCC_DRAM          | 2.40              |      |
|                            | NVCC_ENET          | 0.10              |      |
|                            | NVCC_SNVS_1P8      | 0.20              |      |
|                            | PVCC               | 0.60              |      |
|                            | VDD_DRAM           | 9.40              |      |
|                            | VDD_MIPI_0P8       | 0.10              |      |
|                            | VDD_SNVS_0P8       | 0.10              |      |
|                            | VDD_SOC            | 4.50              |      |
|                            | VDD_ARM_PLL_0P8    | 0.10              |      |
|                            | VDD_USB_0P8        | 2.50              |      |
|                            | Total <sup>2</sup> | 20.80             |      |
| Low-V SUSPEND <sup>3</sup> | NVCC               | 0.70              | mW   |
|                            | NVCC_DRAM          | 1.50              |      |
|                            | NVCC_ENET          | 0.10              |      |
|                            | NVCC_SNVS_1P8      | 0.20              |      |
|                            | PVCC               | 0.60              |      |
|                            | VDD_DRAM           | 6.80              |      |
|                            | VDD_MIPI_0P8       | 0.20              |      |
|                            | VDD_SNVS_0P8       | 0.10              |      |
|                            | VDD_SOC            | 3.50              |      |
|                            | VDD_ARM_PLL_0P8    | 0.10              |      |
|                            | VDD_USB_0P8        | 2.60              |      |
|                            | Total <sup>2</sup> | 16.40             |      |

<sup>1</sup> All the power numbers defined in the table are for information only. These numbers are based on typical silicon at 25°C, under non-OS environment and use case dependent. For power numbers with OS and real use cases, see *Power consumption measurement application note* for more details.

<sup>2</sup> Sum of the listed supply rails.

<sup>3</sup> Low-V suspend mode is low voltage suspend mode. Comparing with suspend mode (VDD\_SOC/GPU/DRAM at 0.8 V), Low-V suspend mode sets VDD\_SOC/GPU/DRAM at 0.75 V.

Table 22. Chip power in different LP mode for 11 x 11 mm package

| Mode                       | Supply                                                                     | Typ. <sup>1</sup> | Unit |
|----------------------------|----------------------------------------------------------------------------|-------------------|------|
| SUSPEND                    | VDD_SOC                                                                    | 12.1              | mW   |
|                            | NVCC_DRAM                                                                  | 2                 |      |
|                            | VDD_SNVS_0P8                                                               | 0.1               |      |
|                            | NVCC_SNVS_1P8                                                              | 0.2               |      |
|                            | NVCC_CLK_JTAG_PVCC_1P8                                                     | 1                 |      |
|                            | NVCC_I2C_UART<br>NVCC_SAI3_SAI5<br>NVCC_SD1_NAND<br>NVCC_ECSPi<br>NVCC_SD2 | 0.2               |      |
|                            | NVCC_ENET_GPIO_SAI2                                                        | 0.3               |      |
|                            | Total                                                                      | 15.9              |      |
| Low-V SUSPEND <sup>2</sup> | VDD_SOC                                                                    | 9.9               | mW   |
|                            | NVCC_DRAM                                                                  | 1.5               |      |
|                            | VDD_SNVS_0P8                                                               | 0.1               |      |
|                            | NVCC_SNVS_1P8                                                              | 0.2               |      |
|                            | NVCC_CLK_JTAG_PVCC_1P8                                                     | 0.9               |      |
|                            | NVCC_I2C_UART<br>NVCC_SAI3_SAI5<br>NVCC_SD1_NAND<br>NVCC_ECSPi<br>NVCC_SD2 | 0.2               |      |
|                            | NVCC_ENET_GPIO_SAI2                                                        | 0.3               |      |
|                            | Total                                                                      | 13.1              |      |
| SNVS                       | VDD_SNVS_0P8                                                               | 0.1               | mW   |
|                            | NVCC_SNVS_1P8                                                              | 0.3               |      |
|                            | Total                                                                      | 0.4               |      |

<sup>1</sup> All the power numbers defined in the table are for information only. These numbers are based on typical silicon at 25°C, under non-OS environment and use case dependent. For power numbers with OS and real use cases, see *Power consumption measurement application note* for more details.

<sup>2</sup> Low-V suspend mode is low voltage suspend mode. Comparing with suspend mode (VDD\_SOC at 0.8 V), Low-V suspend mode sets VDD\_SOC at 0.75 V.

Table 23 and Table 25 summary the power supply states in all the power modes.

**Table 23. The power supply states for 14 x 14 mm package**

| Power rail            | OFF | SNVS | SUSPEND <sup>1</sup> | IDLE | RUN    |
|-----------------------|-----|------|----------------------|------|--------|
| VDD_ARM               | OFF | OFF  | OFF                  | ON   | ON     |
| VDD_SOC               | OFF | OFF  | ON                   | ON   | ON     |
| VDD_GPU               | OFF | OFF  | OFF                  | OFF  | ON/OFF |
| VDD_DRAM              | OFF | OFF  | ON                   | ON   | ON     |
| Misc_1P8 <sup>2</sup> | OFF | OFF  | ON                   | ON   | ON     |
| Misc_0P8 <sup>1</sup> | OFF | OFF  | ON                   | ON   | ON     |
| VDD_MIPI_1P2          | OFF | OFF  | ON                   | ON   | ON     |
| VDD_MIPI_0P8          | OFF | OFF  | ON                   | ON   | ON     |
| VDD_DRAM_PLL_0P8      | OFF | OFF  | ON                   | ON   | ON     |
| VDD_SNVS_0P8          | OFF | ON   | ON                   | ON   | ON     |
| NVCC_SNVS_1P8         | OFF | ON   | ON                   | ON   | ON     |
| NVCC_<XXX>            | OFF | OFF  | ON                   | ON   | ON     |
| PVCCx_1P8             | OFF | OFF  | ON                   | ON   | ON     |
| NVCC_DRAM             | OFF | OFF  | ON                   | ON   | ON     |

<sup>1</sup> SUSPEND is covering normal suspend mode (VDD\_SOC/GPU/DRAM at 0.8 V) and Low-V suspend (VDD\_SOC/GPU/DRAM at 0.75 V).

<sup>2</sup> See Table 24

**Table 24. Group name**

|          |                                                                                                                        |
|----------|------------------------------------------------------------------------------------------------------------------------|
| Misc_1P8 | VDD_24M_XTAL_1P8<br>VDD_ANA0_1P8<br>VDD_ANA1_1P8<br>VDD_ARM_PLL_1P8<br>VDD_DRAM_PLL_1P8<br>VDD_MIPI_1P8<br>VDD_USB_1P8 |
| Misc_0P8 | VDD_ANA_0P8<br>VDD_ARM_PLL_0P8<br>VDD_USB_0P8                                                                          |

Table 25. The power supply states for 11 x 11 mm package

| Power rail                                                           | OFF | SNVS | SUSPEND | IDLE | RUN |
|----------------------------------------------------------------------|-----|------|---------|------|-----|
| VDD_SOC                                                              | OFF | OFF  | ON      | ON   | ON  |
| VDD_ANA1_XTAL_MIP1_1P8,<br>VDD_ANA0_ARM_PLL_1P8,<br>VDD_DRAM_PLL_1P8 | OFF | OFF  | ON      | ON   | ON  |
| VDD_MIP1_1P2                                                         | OFF | OFF  | ON      | ON   | ON  |
| VDD_SNVS_0P8                                                         | OFF | ON   | ON      | ON   | ON  |
| NVCC_SNVS_1P8                                                        | OFF | ON   | ON      | ON   | ON  |
| NVCC_<XXX>                                                           | OFF | OFF  | ON      | ON   | ON  |
| NVCC_DRAM                                                            | OFF | OFF  | ON      | ON   | ON  |

### 3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

### 3.2.1 Power-up sequence

Figure 3 illustrates the power-up sequence for 14 x 14 mm package of i.MX 8M Nano applications processor.

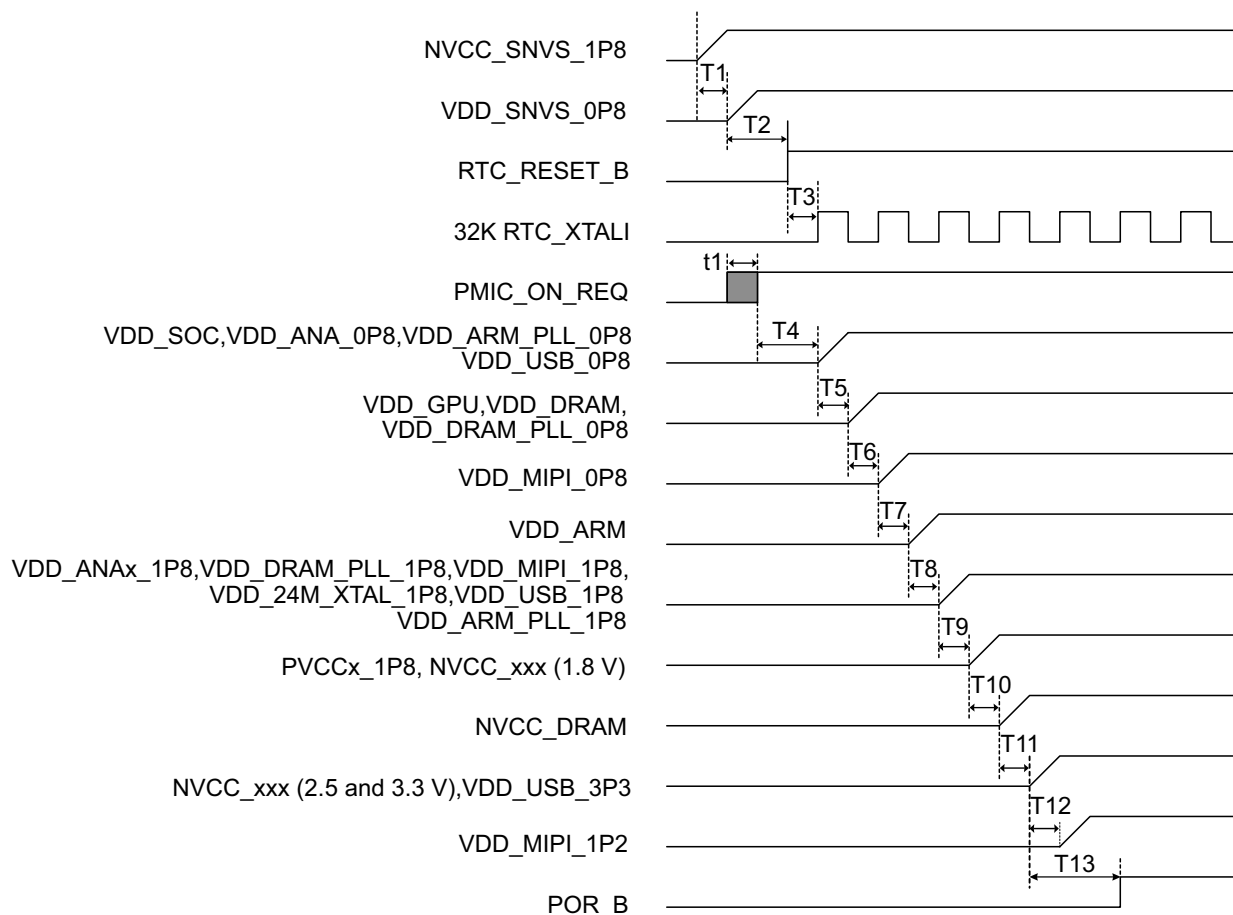


Figure 3. The power-up sequence for 14 x 14 mm package

#### NOTE

VDD\_MIPI\_1P2 should power up after VDD\_MIPI\_0P8 and VDD\_MIPI\_1P8, and it can power up before the POR\_B release or after the POR\_B release.

Table 26 represents the timing parameters of the power-up sequence for 14 x 14 mm package.

Table 26. Power-up sequence for 14 x 14 mm package

|    | Description                                         | Min | Typ | Max | Unit |
|----|-----------------------------------------------------|-----|-----|-----|------|
| T1 | Delay from NVCC_SNVS_1P8 to VDD_SNVS_0P8            | 0   | 2   | —   | ms   |
| T2 | Delay from VDD_SNVS_0P8 high or RTC_SET_B de-assert | 0   | 10  | —   | ms   |

Table 26. Power-up sequence for 14 x 14 mm package (continued)

|                  | Description                                                                                                                                                             | Min | Typ | Max | Unit |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| T3               | Delay from RTC_RESET_B de-assert to stable 32 k existed                                                                                                                 | —   | 40  | 100 | μs   |
| T4               | Delay from PMIC_ON_REQ assert to analog 0.8 V on                                                                                                                        | 0   | 0.2 | —   | ms   |
| T5               | Delay from analog 0.8 V on to analog 0.8/0.9 V on                                                                                                                       | 0   | 2   | —   | ms   |
| T6               | Delay from analog 0.8/0.9 V on to PHY 0.9 V on                                                                                                                          | 0   | 15  | —   | μs   |
| T7               | Delay from PHY 0.9 V on to VDD_ARM on                                                                                                                                   | 0   | 2   | —   | ms   |
| T8               | Delay from VDD_ARM on to analog 1.8 V on                                                                                                                                | 0   | 15  | —   | μs   |
| T9               | Delay from analog 1.8 V on to digital 1.8 V on                                                                                                                          | 0   | 2   | —   | ms   |
| T10              | Delay from digital 1.8 V on to NVCC_DRAM on                                                                                                                             | 0   | 2   | —   | ms   |
| T11              | Delay from NVCC_DRAM on to digital 2.5 V and 3.3 V on                                                                                                                   | 0   | 2   | —   | ms   |
| T12              | Delay from digital 2.5 V and 3.3 V on to PHY 1.2 V on                                                                                                                   | 0   | 2   | —   | ms   |
| T13 <sup>1</sup> | Delay from digital 2.5 V and 3.3 V on to POR_B de-assert                                                                                                                | 0   | 20  | —   | ms   |
| t1               | Uncertain period before PMIC_ON_REQ assert during VDD_SNVS_0P8 ramp up.                                                                                                 |     |     |     |      |
|                  | For ramp up requirement, only VDD_ANA0_1P8 has 5 μs minimum requirement, others do not have such requirement.<br>During power-up, make sure NVCC_xxx - PVCCx_1P8 < 2 V. |     |     |     |      |

<sup>1</sup> The values of T13 depend on T2. RTC\_RESET\_B must be de-assert before POR\_B de-asserts.

Figure 4 illustrates the power-up sequence for 11 x 11 mm package of i.MX 8M Nano applications processor.

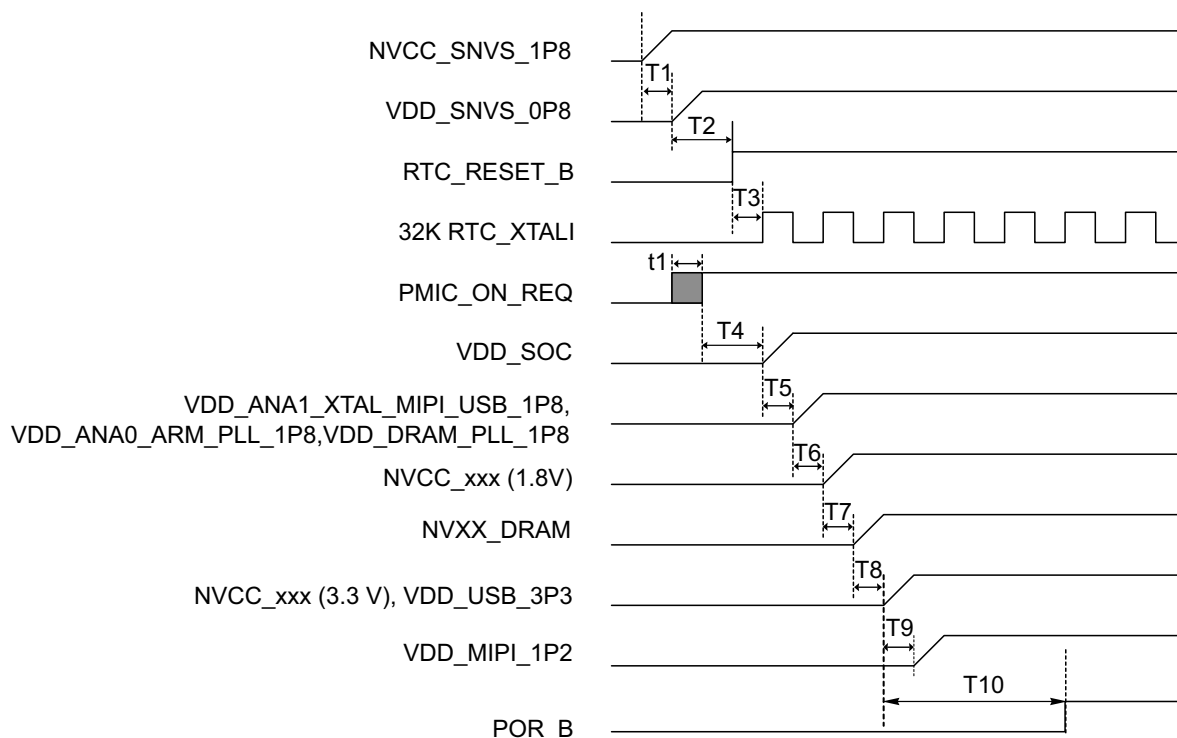


Figure 4. The power-up sequence for 11 x 11 mm package

#### NOTE

VDD\_MIPI\_1P2 should power up after Analog 1.8 V on, and it can power up before POR\_B release or after POR\_B release.

Table 27 represents the timing parameters of the power-up sequence for 11 x 11 mm package.

Table 27. Power-up sequence for 11 x 11 mm package

|    | Description                                                       | Min | Typ | Max | Unit |
|----|-------------------------------------------------------------------|-----|-----|-----|------|
| T1 | Delay from NVCC_SNVS_1P8 to VDD_SNVS_0P8                          | 0   | 2   | —   | ms   |
| T2 | Delay from VDD_SNVS_0P8 high or RTC_RESET_B de-assert             | 0   | 10  | —   | ms   |
| T3 | Delay from RTC_RESET_B de-assert to stable 32 k existed           | —   | 40  | 100 | μs   |
| T4 | Delay from PMIC_ON_REQ assert to ARM, analog and PHY 0.8/0.9 V on | 0   | 5   | —   | ms   |
| T5 | Delay from SOC, analog and PHY 0.8/0.9 V to analog 1.8 V on       | 0   | 15  | —   | μs   |
| T6 | Delay from analog 1.8 V on to digital 1.8 V on                    | 0   | 2   | —   | ms   |
| T7 | Delay from digital 1.8 V on to NVCC_DRAM on                       | 0   | 2   | —   | ms   |
| T8 | Delay from NVCC_DRAM on to digital 3.3 V on                       | 0   | 2   | —   | ms   |

**Table 27. Power-up sequence for 11 x 11 mm package (continued)**

|     | Description                                                                                                                | Min | Typ | Max | Unit |
|-----|----------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| T9  | Delay from analog 1.8 V on to PHY 1.2 V on                                                                                 | 0   | 2   | —   | ms   |
| T10 | Delay from digital 3.3 V on to POR_B de-assert <sup>1</sup>                                                                | 0   | 20  | —   | ms   |
| t1  | Uncertain period before PMIC_ON_REQ assert during VDD_SNVS_0P8 ramp up.                                                    |     |     |     |      |
|     | For ramp up requirement, only VDD_ANA0_ARM_PLL_1P8 has 5 $\mu$ s minimum requirement, others do not have such requirement. |     |     |     |      |

<sup>1</sup> The values of T10 depend on T2. RTC\_RESET\_B must be de-assert before POR\_B de-asserts.

### 3.2.2 Power-down sequence

Figure 5 illustrates the power-down sequence for 14 x 14 mm package of i.MX 8M Nano applications processor.

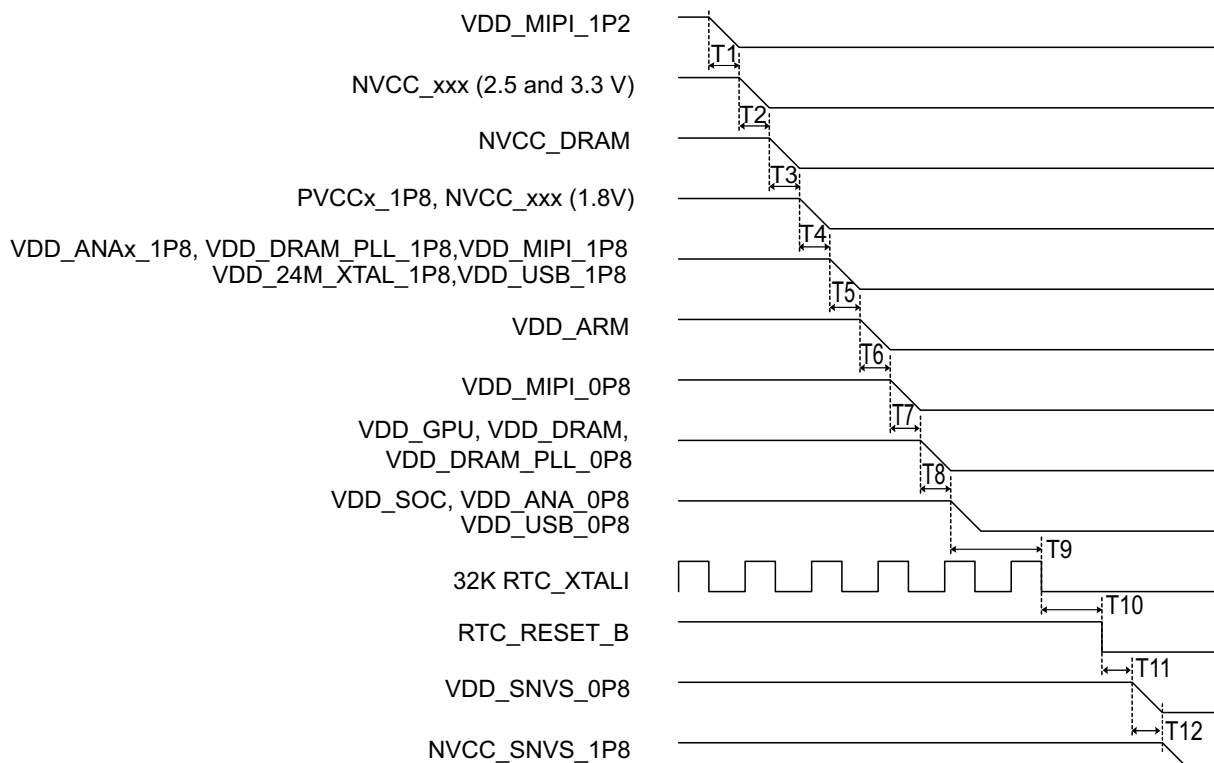
**Figure 5. The power-down sequence for 14 x 14 mm package**

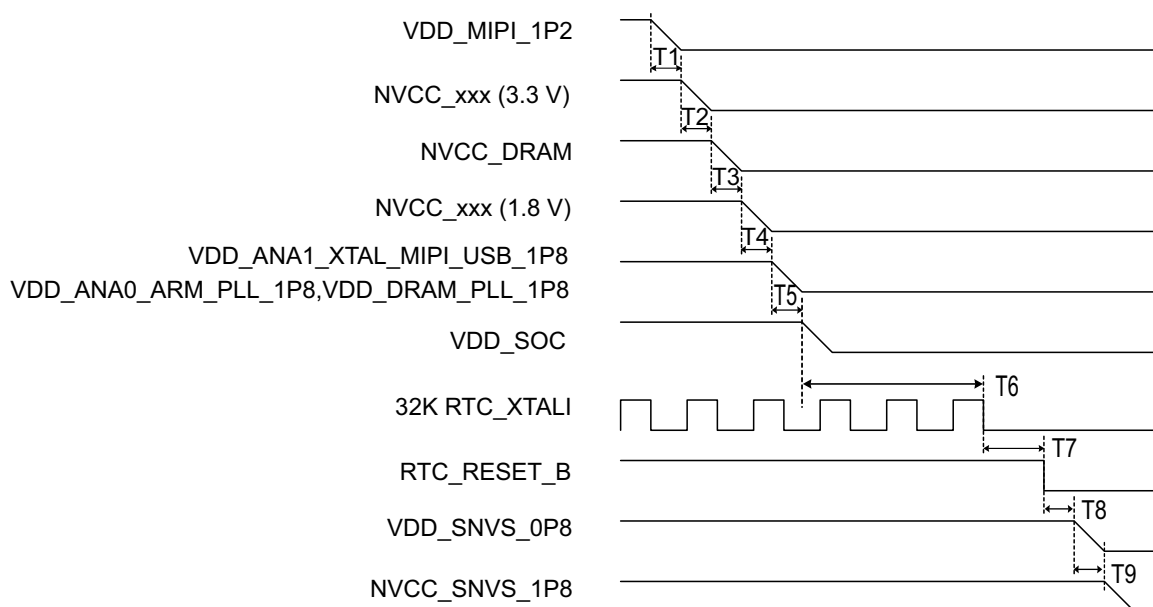


Table 28 represents the timing parameters of the power-down sequence for 14 x 14 mm package.

**Table 28. Power-down sequence for 14 x 14 mm package**

|     | Description                                              | Min | Typ | Max | Unit |
|-----|----------------------------------------------------------|-----|-----|-----|------|
| T1  | Delay from PHY 1.2 V off to digital 2.5 V and 3.3 V off  | 0   | 10  | —   | ms   |
| T2  | Delay from digital 2.5 V and 3.3 V off to NVCC_DRAM off  | 0   | 10  | —   | ms   |
| T3  | Delay from NVCC_DRAM off to digital 1.8 V off            | 0   | 10  | —   | ms   |
| T4  | Delay from digital 1.8 V off to analog 1.8 V off         | 0   | 10  | —   | ms   |
| T5  | Delay from analog 1.8 V off to VDD_ARM off               | 0   | 10  | —   | ms   |
| T6  | Delay from VDD_ARM off to PHY 0.9 V off                  | 0   | 10  | —   | ms   |
| T7  | Delay from PHY 0.9 V off to analog 0.8/0.9 V off         | 0   | 10  | —   | ms   |
| T8  | Delay from analog 0.8/0.9 V off to analog 0.8 V off      | 0   | 10  | —   | ms   |
| T9  | Delay from analog 0.8 V off to 32k off                   | 0   | 10  | —   | ms   |
| T10 | Delay from 32k off to RTC_RESET_B assert                 | 0   | 10  | —   | ms   |
| T11 | Delay from RTC_RESET_B assert to VDD_SNVS_0P8 off        | 0   | 10  | —   | ms   |
| T12 | Delay from VDD_SNVS_0P8 off to NVCC_SNVS_1P8 off         | 0   | 10  | —   | ms   |
|     | During power-down, make sure NVCC_xxx - PVCCx_1P8 < 2 V. |     |     |     |      |

Figure 6 illustrates the power-down sequence for 11 x 11 mm package of i.MX 8M Nano applications processor.



**Figure 6. The power-down sequence for 11 x 11 mm package**

Table 29 represents the timing parameters of the power-down sequence for 11 x 11 mm package.

**Table 29. Power-down sequence for 11 x 11 mm package**

|    | Description                                             | Min | Typ | Max | Unit |
|----|---------------------------------------------------------|-----|-----|-----|------|
| T1 | Delay from PHY 1.2 V off to digital 2.5 V and 3.3 V off | 0   | 10  | —   | ms   |
| T2 | Delay from digital 2.5 V and 3.3 V off to NVCC_DRAM off | 0   | 10  | —   | ms   |
| T3 | Delay from NVCC_DRAM off to digital 1.8 V off           | 0   | 10  | —   | ms   |
| T4 | Delay from digital 1.8 V off to analog 1.8 V off        | 0   | 10  | —   | ms   |
| T5 | Delay from analog 1.8 V off to VDD_SOC off              | 0   | 40  | —   | ms   |
| T6 | Delay from VDD_SOC off to 32k off                       | 0   | 10  | —   | ms   |
| T7 | Delay from 32k off to RTC_RESET_B assert                | 0   | 10  | —   | ms   |
| T8 | Delay from RTC_RESET_B assert to VDD_SNVS_0P8 off       | 0   | 10  | —   | ms   |
| T9 | Delay from VDD_SNVS_0P8 off to NVCC_SNVS_1P8 off        | 0   | 10  | —   | ms   |

### 3.3 PLL electrical characteristics

Table 30 shows PLL electrical characteristics.

**Table 30. PLL electrical parameters**

| PLL type   | Parameter              | Value           |
|------------|------------------------|-----------------|
| AUDIO_PLL1 | Clock output range     | Maximum 650 MHz |
|            | Reference clock        | 24 MHz          |
|            | Lock time <sup>1</sup> | 500 $\mu$ s     |
| AUDIO_PLL2 | Clock output range     | Maximum 650 MHz |
|            | Reference clock        | 24 MHz          |
|            | Lock time              | 500 $\mu$ s     |
| VIDEO_PLL1 | Clock output range     | Maximum 650 MHz |
|            | Reference clock        | 24 MHz          |
|            | Lock time              | 500 $\mu$ s     |
| SYS_PLL1   | Clock output range     | 800 MHz         |
|            | Reference clock        | 24 MHz          |
|            | Lock time              | 50 $\mu$ s      |
| SYS_PLL2   | Clock output range     | 1 GHz           |
|            | Reference clock        | 24 MHz          |
|            | Lock time              | 50 $\mu$ s      |

Table 30. PLL electrical parameters (continued)

| PLL type   | Parameter          | Value              |
|------------|--------------------|--------------------|
| SYS_PLL3   | Clock output range | 600 MHz — 1 GHz    |
|            | Reference clock    | 24 MHz             |
|            | Lock time          | 50 $\mu$ s         |
| ARM_PLL    | Clock output range | 800 MHz — 2 GHz    |
|            | Reference clock    | 24 MHz             |
|            | Lock time          | 50 $\mu$ s         |
| M7_ALT_PLL | Clock output range | 400 MHz — 800 MHz  |
|            | Reference clock    | 24 MHz             |
|            | Lock time          | 50 $\mu$ s         |
| DRAM_PLL   | Clock output range | 400 MHz — 800 MHz  |
|            | Reference clock    | 24 MHz             |
|            | Lock time          | 500 $\mu$ s        |
| GPU_PLL    | Clock output range | 800 MHz — 1600 MHz |
|            | Reference clock    | 24 MHz             |
|            | Lock time          | 50 $\mu$ s         |

<sup>1</sup> Lock time is referring from PLL enable to valid lock flag time.

## 3.4 On-chip oscillators

### 3.4.1 OSC24M

A 24 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for the CPU, BUS, and high-speed interfaces. For fractional PLLs, the 24 MHz clock from the oscillator can be used as the PLL reference clock directly.

Table 31. Crystal specifications<sup>1</sup>

| Parameter Description | Min | Typ | Max | Unit     |
|-----------------------|-----|-----|-----|----------|
| Frequency             | —   | 24  | —   | MHz      |
| Load                  | —   | 12  | —   | pF       |
| Drive level           | 100 | —   | —   | $\mu$ W  |
| ESR                   | —   | —   | 80  | $\Omega$ |

<sup>1</sup> Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

### 3.4.2 OSC32K

An external 32.768 kHz oscillator is necessary.

## 3.5 General purpose I/O (GPIO) DC parameters

Table 32 shows DC parameters for GPIO pads. The parameters in Table 32 are guaranteed per the operating ranges in Table 15, unless otherwise noted.

**Table 32. GPIO DC parameters**

| Parameter                 | Symbol         | Test Conditions                                                                       | Min                 | Typ | Max                 | Unit          |
|---------------------------|----------------|---------------------------------------------------------------------------------------|---------------------|-----|---------------------|---------------|
| High-level output voltage | $V_{OH(1.8V)}$ | $I_{OH} = 1.6/3.2/6.4/9.6\text{ mA (1.8 V)}$<br>$I_{OH} = 2/4/8/12\text{ mA (3.3 V)}$ | $0.8 \times V_{DD}$ | —   | $V_{DD}$            | V             |
|                           | $V_{OH(3.3V)}$ |                                                                                       | $0.8 \times V_{DD}$ | —   | $V_{DD}$            | V             |
| Low-level output voltage  | $V_{OL(1.8V)}$ | $I_{OL} = 1.6/3.2/6.4/9.6\text{ mA (1.8 V)}$<br>$I_{OL} = 2/4/8/12\text{ mA (3.3 V)}$ | 0                   | —   | $0.2 \times V_{DD}$ | V             |
|                           | $V_{OL(3.3V)}$ |                                                                                       | 0                   | —   | $0.2 \times V_{DD}$ | V             |
| High-level input voltage  | $V_{IH}$       | —                                                                                     | $0.7 \times V_{DD}$ | —   | $V_{DD} + 0.3$      | V             |
| Low-level input voltage   | $V_{IL}$       | —                                                                                     | -0.3                | —   | $0.3 \times V_{DD}$ | V             |
| Pull-up resistor          | —              | $V_{DD} = 1.65 - 1.95\text{V}$<br>Temp = 0 - 95 °C                                    | 12                  | 22  | 49                  | K $\Omega$    |
| Pull-down resistor        | —              |                                                                                       | 13                  | 23  | 48                  | K $\Omega$    |
| Pull-up resistor          | —              | $V_{DD} = 2.25 - 2.75\text{V}$<br>Temp = 0 - 95 °C                                    | 13                  | 24  | 69                  | K $\Omega$    |
| Pull-down resistor        | —              |                                                                                       | 9.1                 | 33  | 69                  | K $\Omega$    |
| Pull-up resistor          | —              | $V_{DD} = 3.0 - 3.6\text{V}$<br>Temp = 0 - 95 °C                                      | 18                  | 37  | 72                  | K $\Omega$    |
| Pull-down resistor        | —              |                                                                                       | 24                  | 43  | 87                  | K $\Omega$    |
| High level input current  | $I_{IH}$       | —                                                                                     | -4                  | —   | 4                   | $\mu\text{A}$ |
| Low level input current   | $I_{IL}$       | —                                                                                     | -0.7                | —   | 0.7                 | $\mu\text{A}$ |

**Table 33. Additional leakage parameters**

| Parameter                | Symbol   | Pins                   | Min  | Max | Unit          |
|--------------------------|----------|------------------------|------|-----|---------------|
| High level input current | $I_{IH}$ | USB1_Dx                | -30  | 30  | $\mu\text{A}$ |
|                          |          | MIPI_CSI               | -4   | 4   |               |
|                          |          | USB1_ID, ONOFF, POR_B  | -1   | 1   |               |
| Low level input current  | $I_{IL}$ | USB1_ID                | -200 | 200 | $\mu\text{A}$ |
|                          |          | USB1_Dx                | -6   | 6   |               |
|                          |          | MIPI_CSI, ONOFF, POR_B | -0.7 | 0.7 |               |

### 3.5.1 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR 4, DDR4, and DDR3L operational modes. The DDR Memory Controller (DDRMC) is designed to be compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8M Nano applications processor.

## 3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

The GPIO load circuit and output transition time waveforms are shown in [Figure 7](#) and [Figure 8](#).

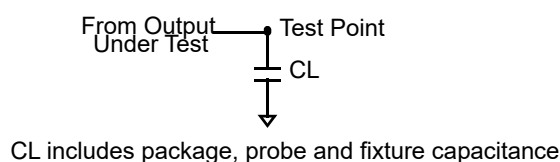


Figure 7. Load circuit for output

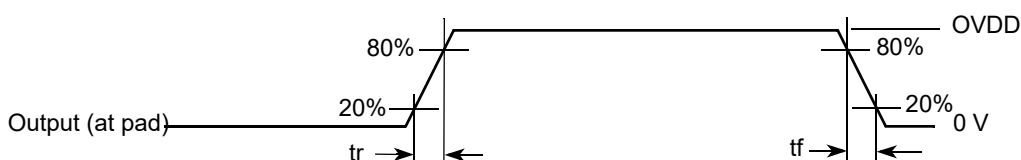


Figure 8. Output transition time waveform

### 3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 34. Maximum frequency of operation for input

| Maximum frequency (MHz) |                         |
|-------------------------|-------------------------|
| VDD = 1.8 V, CL = 50 pF | VDD = 3.3 V, CL = 50 pF |
| 450                     | 440                     |

Table 35. Maximum frequency of operation for output

| Parameter |          |              | Maximum Frequency (MHz) |            |             |            |
|-----------|----------|--------------|-------------------------|------------|-------------|------------|
|           |          |              | VDD = 1.8 V             |            | VDD = 3.3 V |            |
| dse[2:0]  | sre[1:0] | Driver type  | CL = 10 pF              | CL = 20 pF | CL = 10 pF  | CL = 20 pF |
| 00X       | 0X       | 1x Slow Slew | 150                     | 80         | 120         | 65         |
| 00X       | 1X       | 1x Fast Slew | 150                     | 80         | 120         | 65         |
| 10X       | 0X       | 2x Slow Slew | 160                     | 90         | 150         | 80         |
| 10X       | 1X       | 2x Fast Slew | 160                     | 90         | 150         | 80         |
| 01X       | 0X       | 4x Slow Slew | 200                     | 100        | 180         | 90         |
| 01X       | 1X       | 4x Fast Slew | 200                     | 100        | 180         | 90         |
| 11X       | 0X       | 6x Slow Slew | 250                     | 130        | 200         | 100        |
| 11X       | 1X       | 6x Fast Slew | 250                     | 130        | 200         | 100        |

### 3.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Nano family of processors for the following I/O types:

#### NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance  $Z_{tl}$  attached to I/O pad and incident wave launched into transmission line.  $R_{pu}/R_{pd}$  and  $Z_{tl}$  form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see [Figure 9](#)).

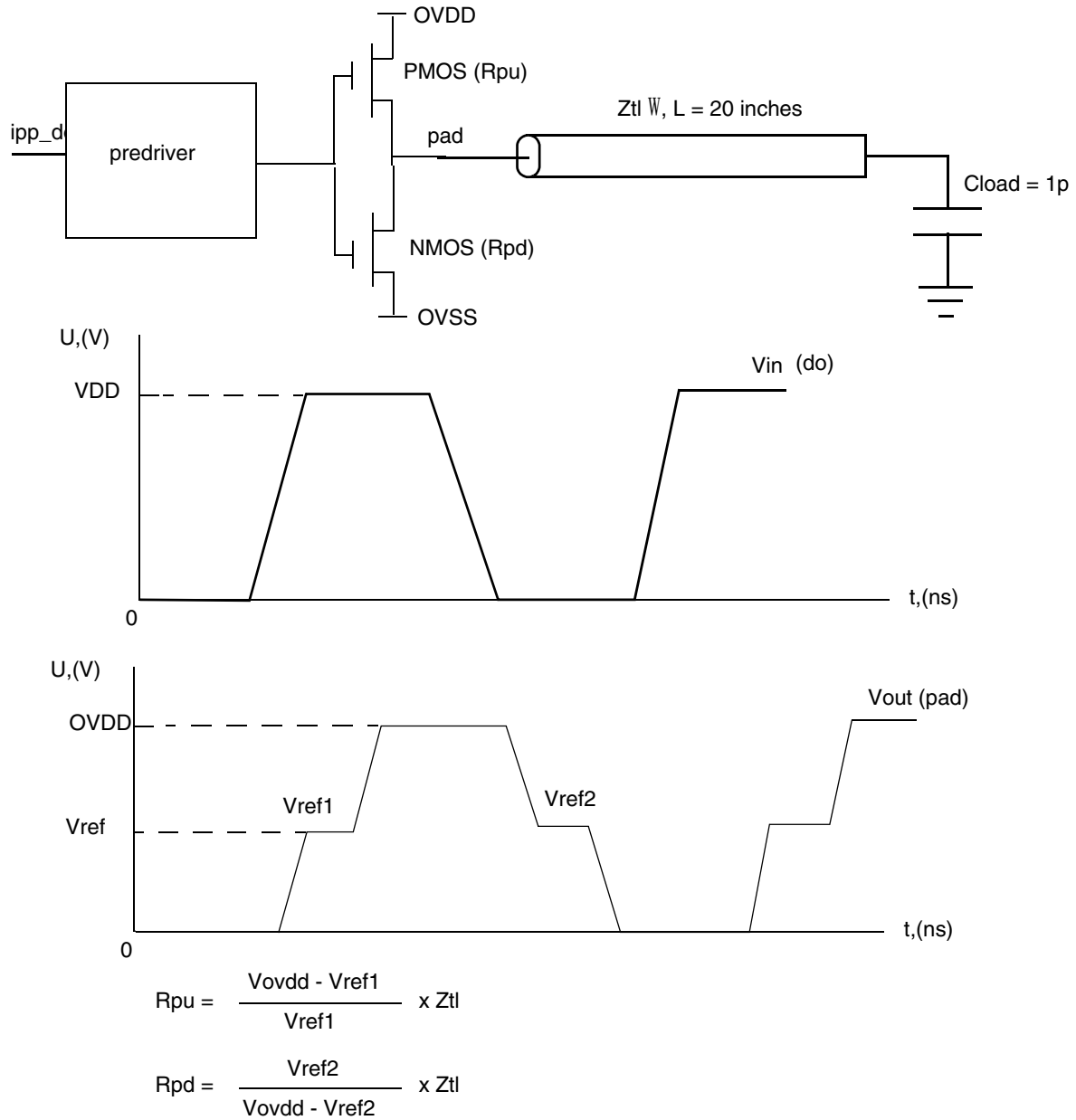


Figure 9. Impedance matching load for measurement

### 3.7.1 DDR I/O output buffer impedance

Table 36 shows DDR I/O output buffer impedance of i.MX 8M Nano family of processors.

**Table 36. DDR I/O output buffer impedance**

| Parameter               | Symbol | Test Conditions<br>DSE<br>(Drive Strength) | Typical                       |                             |                               | Unit     |
|-------------------------|--------|--------------------------------------------|-------------------------------|-----------------------------|-------------------------------|----------|
|                         |        |                                            | NVCC_DRAM = 1.35 V<br>(DDR3L) | NVCC_DRAM = 1.2 V<br>(DDR4) | NVCC_DRAM = 1.1 V<br>(LPDDR4) |          |
| Output Driver Impedance | Rdrv   | 000000                                     | Hi-Z                          | Hi-Z                        | Hi-Z                          | $\Omega$ |
|                         |        | 000010                                     | 240                           | 240                         | 240                           |          |
|                         |        | 001000                                     | 120                           | 120                         | 120                           |          |
|                         |        | 001010                                     | 80                            | 80                          | 80                            |          |
|                         |        | 011000                                     | 60                            | 60                          | 60                            |          |
|                         |        | 011010                                     | 48                            | 48                          | 48                            |          |
|                         |        | 111000                                     | 40                            | 40                          | 40                            |          |
|                         |        | 111010                                     | 34                            | 34                          | 34                            |          |

**Note:**

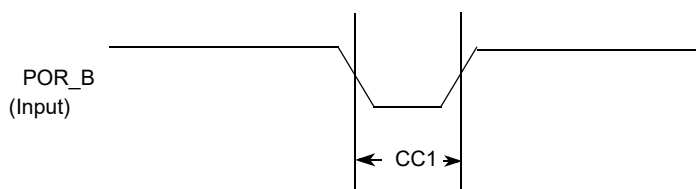
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240  $\Omega$  external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is  $\pm 5\%$  (max/min impedance) across PVTs.

## 3.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 8M Nano processor.

### 3.8.1 Reset timings parameters

Figure 10 shows the reset timing and Table 37 lists the timing parameters.



**Figure 10. Reset timing diagram**

**Table 37. Reset timing parameters**

| ID  | Parameter                                   | Min | Max | Unit            |
|-----|---------------------------------------------|-----|-----|-----------------|
| CC1 | Duration of POR_B to be qualified as valid. | 1   | —   | RTC_XTALI cycle |



### 3.8.2 WDOG Reset timing parameters

Figure 11 shows the WDOG reset timing and Table 38 lists the timing parameters.

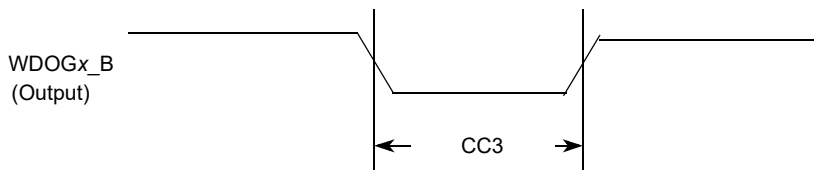


Figure 11. WDOGx\_B timing diagram

Table 38. WDOGx\_B timing parameters

| ID  | Parameter                     | Min | Max | Unit            |
|-----|-------------------------------|-----|-----|-----------------|
| CC3 | Duration of WDOG1_B Assertion | 1   | —   | RTC_XTALI cycle |

#### NOTE

RTC\_XTALI is approximately 32 kHz. RTC\_XTALI cycle is one period or approximately 30  $\mu$ s.

#### NOTE

WDOGx\_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for detailed information.

## 3.9 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

### 3.9.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

### 3.9.1.1 ECSPi Master mode timing

Figure 12 depicts the timing of ECSPi in master mode. Table 39 lists the ECSPi master mode timing characteristics.

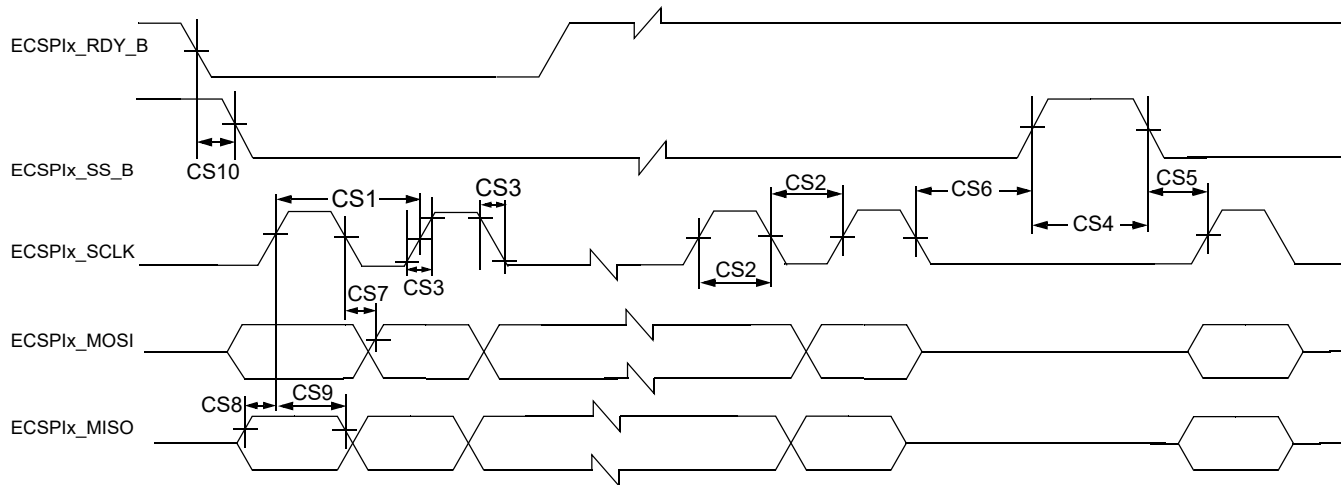


Figure 12. ECSPi Master mode timing diagram

Table 39. ECSPi Master mode timing parameters

| ID   | Parameter                                                             | Symbol          | Min                        | Max | Unit |
|------|-----------------------------------------------------------------------|-----------------|----------------------------|-----|------|
| CS1  | ECSPi_SCLK Cycle Time–Read<br>ECSPi_SCLK Cycle Time–Write             | $t_{clk}$       | 43<br>15                   | —   | ns   |
| CS2  | ECSPi_SCLK High or Low Time–Read<br>ECSPi_SCLK High or Low Time–Write | $t_{sw}$        | 21.5<br>7                  | —   | ns   |
| CS3  | ECSPi_SCLK Rise or Fall <sup>1</sup>                                  | $t_{RISE/FALL}$ | —                          | —   | ns   |
| CS4  | ECSPi_SS_B pulse width                                                | $t_{CSLH}$      | Half ECSPi_SCLK period     | —   | ns   |
| CS5  | ECSPi_SS_B Lead Time (CS setup time)                                  | $t_{SCS}$       | Half ECSPi_SCLK period - 4 | —   | ns   |
| CS6  | ECSPi_SS_B Lag Time (CS hold time)                                    | $t_{HCS}$       | Half ECSPi_SCLK period - 2 | —   | ns   |
| CS7  | ECSPi_MOSI Propagation Delay ( $C_{LOAD} = 20$ pF)                    | $t_{PDmosi}$    | -1                         | 1   | ns   |
| CS8  | ECSPi_MISO Setup Time                                                 | $t_{Smiso}$     | 18                         | —   | ns   |
| CS9  | ECSPi_MISO Hold Time                                                  | $t_{Hmiso}$     | 0                          | —   | ns   |
| CS10 | RDY to ECSPi_SS_B Time <sup>2</sup>                                   | $t_{SDRY}$      | 5                          | —   | ns   |

<sup>1</sup> See specific I/O AC parameters [Section 3.6, I/O AC parameters](#).

<sup>2</sup> SPI\_RDY is sampled internally by ipg\_clk and is asynchronous to all other CSPI signals.

### 3.9.1.2 ECSPi Slave mode timing

Figure 13 depicts the timing of ECSPi in Slave mode. Table 40 lists the ECSPi Slave mode timing characteristics.

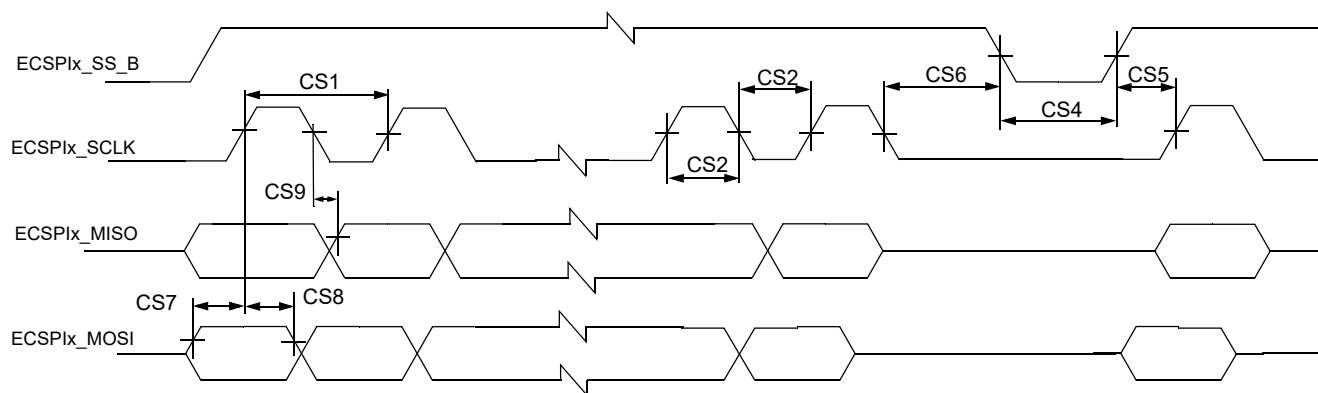


Figure 13. ECSPi Slave mode timing diagram

Table 40. ECSPi Slave mode timing parameters

| ID  | Parameter                                                             | Symbol       | Min                    | Max | Unit |
|-----|-----------------------------------------------------------------------|--------------|------------------------|-----|------|
| CS1 | ECSPi_SCLK Cycle Time–Read<br>ECSPi_SCLK Cycle Time–Write             | $t_{clk}$    | 15<br>43               | —   | ns   |
| CS2 | ECSPi_SCLK High or Low Time–Read<br>ECSPi_SCLK High or Low Time–Write | $t_{SW}$     | 7<br>21.5              | —   | ns   |
| CS4 | ECSPi_SS_B pulse width                                                | $t_{CSLH}$   | Half ECSPi_SCLK period | —   | ns   |
| CS5 | ECSPi_SS_B Lead Time (CS setup time)                                  | $t_{SCS}$    | 5                      | —   | ns   |
| CS6 | ECSPi_SS_B Lag Time (CS hold time)                                    | $t_{HCS}$    | 5                      | —   | ns   |
| CS7 | ECSPi_MOSI Setup Time                                                 | $t_{Smosi}$  | 4                      | —   | ns   |
| CS8 | ECSPi_MOSI Hold Time                                                  | $t_{Hmosi}$  | 4                      | —   | ns   |
| CS9 | ECSPi_MISO Propagation Delay ( $C_{LOAD} = 20$ pF)                    | $t_{PDmiso}$ | 4                      | 19  | ns   |

### 3.9.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC 5.1 (single data rate) timing, eMMC 5.1/SD3.0 (dual data rate) AC timing, and SDR50/SDR104 AC timing.

#### 3.9.2.1 SD/eMMC5.1 (single data rate) AC timing

Figure 14 depicts the timing of SD3.0/eMMC5.1 (SDR), and Table 41 lists the SD3.0/eMMC5.1 (SDR) timing characteristics.

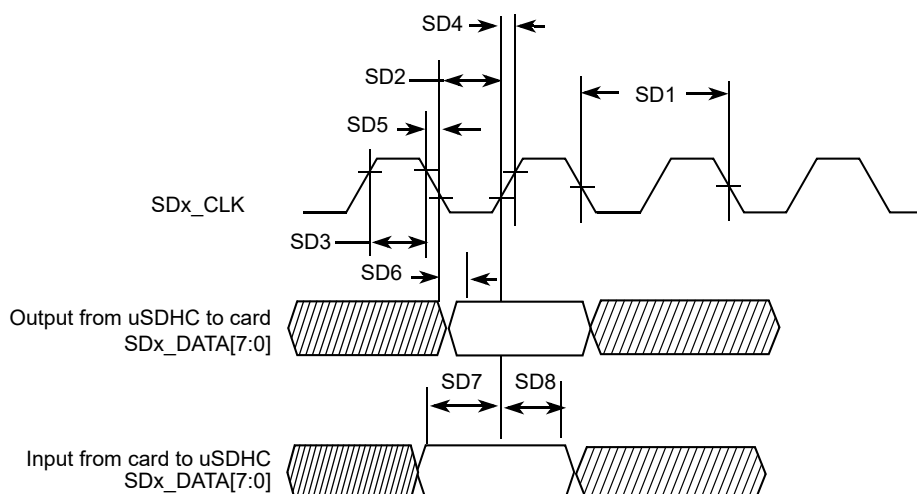


Figure 14. SD3.0/eMMC5.1 (SDR) timing

Table 41. SD3.0/eMMC5.1 (SDR) interface timing specification

| ID                                                                   | Parameter                                       | Symbols    | Min | Max   | Unit |
|----------------------------------------------------------------------|-------------------------------------------------|------------|-----|-------|------|
| <b>Card Input Clock</b>                                              |                                                 |            |     |       |      |
| SD1                                                                  | Clock Frequency (Low Speed)                     | $f_{PP}^1$ | 0   | 400   | kHz  |
|                                                                      | Clock Frequency (SD/SDIO Full Speed/High Speed) | $f_{PP}^2$ | 0   | 25/50 | MHz  |
|                                                                      | Clock Frequency (MMC Full Speed/High Speed)     | $f_{PP}^3$ | 0   | 20/52 | MHz  |
|                                                                      | Clock Frequency (Identification Mode)           | $f_{OD}$   | 100 | 400   | kHz  |
| SD2                                                                  | Clock Low Time                                  | $t_{WL}$   | 7   | —     | ns   |
| SD3                                                                  | Clock High Time                                 | $t_{WH}$   | 7   | —     | ns   |
| SD4                                                                  | Clock Rise Time                                 | $t_{TLH}$  | —   | 3     | ns   |
| SD5                                                                  | Clock Fall Time                                 | $t_{THL}$  | —   | 3     | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                                                 |            |     |       |      |
| SD6                                                                  | uSDHC Output Delay                              | $t_{OD}$   | 6.6 | 3.6   | ns   |

**Table 41. SD3.0/eMMC5.1 (SDR) interface timing specification (continued)**

| ID                                                                   | Parameter                          | Symbols   | Min | Max | Unit |
|----------------------------------------------------------------------|------------------------------------|-----------|-----|-----|------|
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                                    |           |     |     |      |
| SD7                                                                  | uSDHC Input Setup Time             | $t_{ISU}$ | 2.5 | —   | ns   |
| SD8                                                                  | uSDHC Input Hold Time <sup>4</sup> | $t_{IH}$  | 1.5 | —   | ns   |

<sup>1</sup> In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

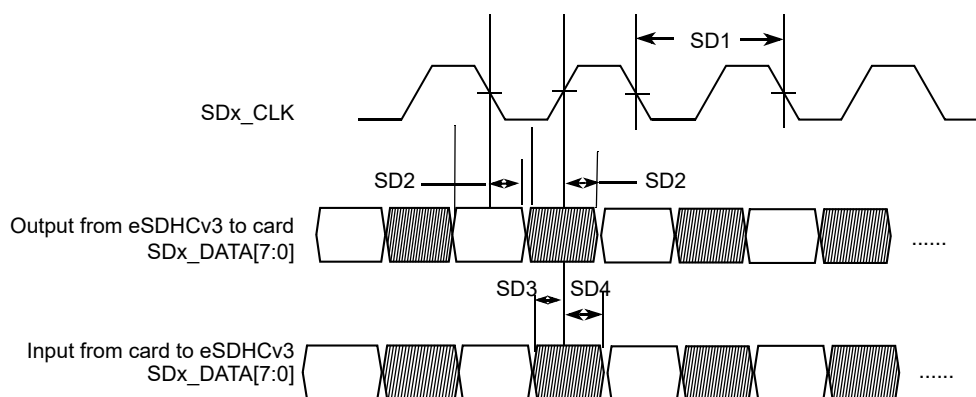
<sup>2</sup> In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0 — 25 MHz. In High-speed mode, clock frequency can be any value between 0 — 50 MHz.

<sup>3</sup> In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0 — 20 MHz. In High-speed mode, clock frequency can be any value between 0 — 52 MHz.

<sup>4</sup> To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

### 3.9.2.2 eMMC5.1/SD3.0 (dual data rate) AC timing

Figure 15 depicts the timing of eMMC5.1/SD3.0 (DDR). Table 42 lists the eMMC5.1/SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

**Figure 15. eMMC5.1/SD3.0 (DDR) timing****Table 42. eMMC5.1/SD3.0 (DDR) interface timing specification**

| ID                                                                     | Parameter                     | Symbols  | Min | Max | Unit |
|------------------------------------------------------------------------|-------------------------------|----------|-----|-----|------|
| <b>Card Input Clock</b>                                                |                               |          |     |     |      |
| SD1                                                                    | Clock Frequency (eMMC5.1 DDR) | $f_{PP}$ | 0   | 52  | MHz  |
| SD1                                                                    | Clock Frequency (SD3.0 DDR)   | $f_{PP}$ | 0   | 50  | MHz  |
| <b>uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                               |          |     |     |      |
| SD2                                                                    | uSDHC Output Delay            | $t_{OD}$ | 2.7 | 6.9 | ns   |
| <b>uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                               |          |     |     |      |

Table 42. eMMC5.1/SD3.0 (DDR) interface timing specification (continued)

| ID  | Parameter              | Symbols   | Min | Max | Unit |
|-----|------------------------|-----------|-----|-----|------|
| SD3 | uSDHC Input Setup Time | $t_{ISU}$ | 2.4 | —   | ns   |
| SD4 | uSDHC Input Hold Time  | $t_{IH}$  | 1.3 | —   | ns   |

### 3.9.2.3 HS400 DDR AC timing

Figure 16 depicts the timing of HS400 mode, and Table 43 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 45 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

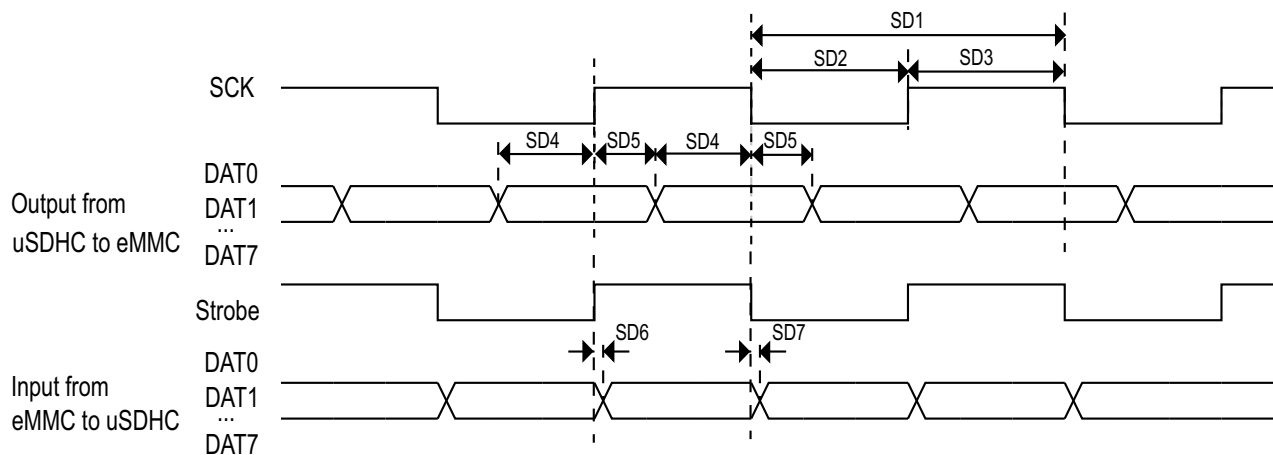


Figure 16. HS400 Mode timing

Table 43. HS400 interface timing specification

| ID                                                        | Parameter                            | Symbols      | Min                   | Max                   | Unit |
|-----------------------------------------------------------|--------------------------------------|--------------|-----------------------|-----------------------|------|
| <b>Card Input Clock</b>                                   |                                      |              |                       |                       |      |
| SD1                                                       | Clock frequency                      | $f_{PP}$     | 0                     | 200                   | MHz  |
| SD2                                                       | Clock low time                       | $t_{CL}$     | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| SD3                                                       | Clock high time                      | $t_{CH}$     | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| <b>uSDHC Output/Card Inputs DAT (Reference to SCK)</b>    |                                      |              |                       |                       |      |
| SD4                                                       | Output skew from data of edge of SCK | $t_{OSkew1}$ | 0.45                  | —                     | ns   |
| SD5                                                       | Output skew from edge of SCK to data | $t_{OSkew2}$ | 0.45                  | —                     | ns   |
| <b>uSDHC Input/Card Outputs DAT (Reference to Strobe)</b> |                                      |              |                       |                       |      |

Table 43. HS400 interface timing specification (continued)

| ID  | Parameter        | Symbols   | Min | Max  | Unit |
|-----|------------------|-----------|-----|------|------|
| SD6 | uSDHC input skew | $t_{RQ}$  | —   | 0.45 | ns   |
| SD7 | uSDHC hold skew  | $t_{RQH}$ | —   | 0.45 | ns   |

### 3.9.2.4 HS200 Mode AC timing

Figure 17 depicts the timing of HS200 mode, and Table 44 lists the HS200 timing characteristics.

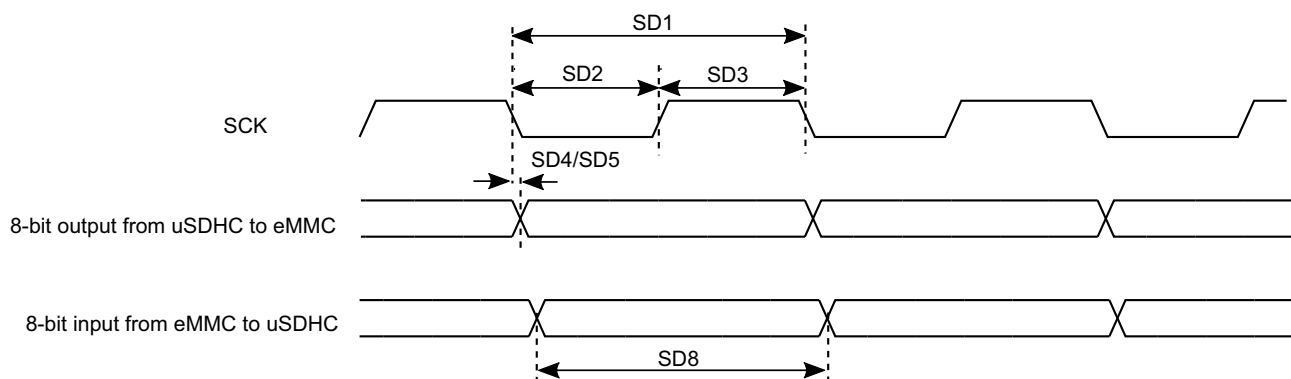


Figure 17. HS200 timing

Table 44. HS200 interface timing specification

| ID                                                                                        | Parameter                | Symbols   | Min                  | Max                  | Unit |
|-------------------------------------------------------------------------------------------|--------------------------|-----------|----------------------|----------------------|------|
| <b>Card Input Clock</b>                                                                   |                          |           |                      |                      |      |
| SD1                                                                                       | Clock Frequency Period   | $t_{CLK}$ | 5.0                  | —                    | ns   |
| SD2                                                                                       | Clock Low Time           | $t_{CL}$  | $0.3 \times t_{CLK}$ | $0.7 \times t_{CLK}$ | ns   |
| SD3                                                                                       | Clock High Time          | $t_{CH}$  | $0.3 \times t_{CLK}$ | $0.7 \times t_{CLK}$ | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)</b>             |                          |           |                      |                      |      |
| SD5                                                                                       | uSDHC Output Delay       | $t_{OD}$  | -1.6                 | 1                    | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)<sup>1</sup></b> |                          |           |                      |                      |      |
| SD8                                                                                       | uSDHC Output Data Window | $t_{ODW}$ | $0.5 \times t_{CLK}$ | —                    | ns   |

<sup>1</sup> HS200 is for 8 bits while SDR104 is for 4 bits.

### 3.9.2.5 SDR50/SDR104 AC timing

Figure 18 depicts the timing of SDR50/SDR104, and Table 45 lists the SDR50/SDR104 timing characteristics.

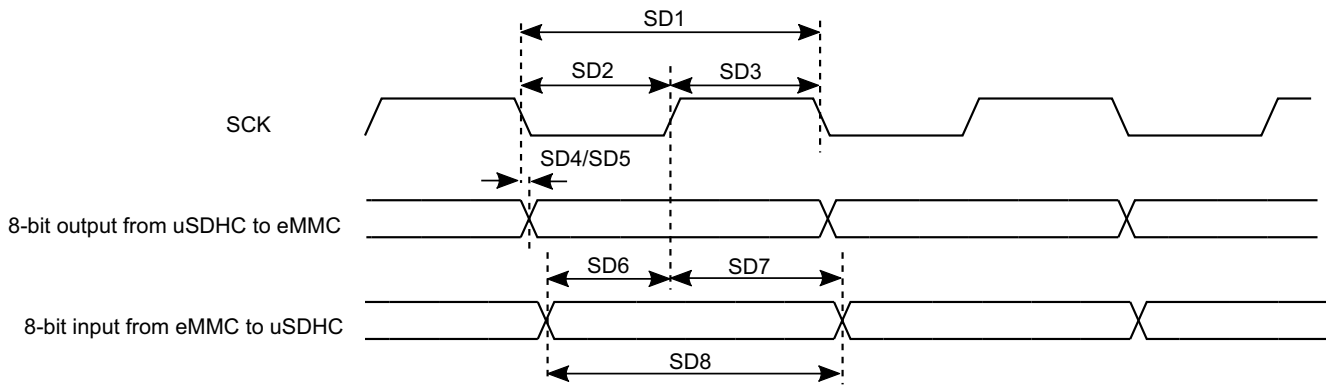


Figure 18. SDR50/SDR104 timing

Table 45. SDR50/SDR104 interface timing specification

| ID                                                                                         | Parameter                | Symbols   | Min                   | Max                   | Unit |
|--------------------------------------------------------------------------------------------|--------------------------|-----------|-----------------------|-----------------------|------|
| <b>Card Input Clock</b>                                                                    |                          |           |                       |                       |      |
| SD1                                                                                        | Clock Frequency Period   | $t_{CLK}$ | 5                     | —                     | ns   |
| SD2                                                                                        | Clock Low Time           | $t_{CL}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| SD3                                                                                        | Clock High Time          | $t_{CH}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)</b>              |                          |           |                       |                       |      |
| SD4                                                                                        | uSDHC Output Delay       | $t_{OD}$  | -3                    | 1                     | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)</b>             |                          |           |                       |                       |      |
| SD5                                                                                        | uSDHC Output Delay       | $t_{OD}$  | -1.6                  | 1                     | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)</b>              |                          |           |                       |                       |      |
| SD6                                                                                        | uSDHC Input Setup Time   | $t_{ISU}$ | 2.4                   | —                     | ns   |
| SD7                                                                                        | uSDHC Input Hold Time    | $t_{IH}$  | 1.4                   | —                     | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)<sup>1</sup></b> |                          |           |                       |                       |      |
| SD8                                                                                        | uSDHC Output Data Window | $t_{ODW}$ | $0.5 \times t_{CLK}$  | —                     | ns   |

<sup>1</sup> Data window in SDR100 mode is variable.

### 3.9.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for the NVCC\_SD1, NVCC\_SD2 and NVCC\_SD3 supplies are identical to those shown in Table 32, "GPIO DC parameters," on page 36.



### 3.9.3 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

**Table 46. ENET signal mapping**

| Pad name    | RGMII/RMII signal | Mode       | Alt mode | Direction | Comments                                                                                                                                                                                                                                                                                                                           |
|-------------|-------------------|------------|----------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ENET_MDC    | MDC               | RMII/RGMII | ALT0     | O         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_MDIO   | MDIO              | RMII/RGMII | ALT0     | I/O       | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_TD3    | TX_D3             | RGMII      | ALT0     | O         | Only used for RGMII                                                                                                                                                                                                                                                                                                                |
| ENET_TD2    | REF_CLK           | RMII       | ALT1     | I/O       | Used as RMII clock and RGMII data, there are two RMII clock schemes.<br><ul style="list-style-type: none"> <li>• MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock.</li> <li>• MAC use external 50M clock.</li> </ul> For RMII—ENET_TD2 functions as RMII REF_CLK when configured in the ALT1 mode. |
|             | TX_D2             | RGMII      | ALT0     |           |                                                                                                                                                                                                                                                                                                                                    |
| ENET_TD1    | TX_D1             | RMII/RGMII | ALT0     | O         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_TD0    | TX_D0             | RMII/RGMII | ALT0     | O         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_TX_CTL | TX_EN             | RMII       | ALT0     | O         | —                                                                                                                                                                                                                                                                                                                                  |
|             | TX_CTL            | RGMII      | ALT0     |           |                                                                                                                                                                                                                                                                                                                                    |
| ENET_TXC    | TX_ER             | RMII       | ALT1     | O         | For RMII—ENET_TXC functions as RMII TX_ER when configured in the ALT1 mode.<br>For RGMII—ENET_TXC functions as RGMII TXC when configured in the ALT0 mode.                                                                                                                                                                         |
|             | TXC               | RGMII      | ALT0     |           |                                                                                                                                                                                                                                                                                                                                    |
| ENET_RX_CTL | RX_EN (CRS_DV)    | RMII       | ALT0     | I         | —                                                                                                                                                                                                                                                                                                                                  |
|             | RX_CTL            | RGMII      | ALT0     |           |                                                                                                                                                                                                                                                                                                                                    |
| ENET_RXC    | RX_ER             | RMII       | ALT1     | I         | For RMII—ENET_RXC functions as RMII RX_ER when configured in the ALT1 mode.<br>For RGMII—ENET_RXC functions as RGMII RXC when configured in the ALT0 mode.                                                                                                                                                                         |
|             | RXC               | RGMII      | ALT0     |           |                                                                                                                                                                                                                                                                                                                                    |
| ENET_RD0    | RX_D0             | RMII/RGMII | ALT0     | I         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_RD1    | RX_D1             | RMII/RGMII | ALT0     | I         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_RD2    | RX_D2             | RGMII      | ALT0     | I         | —                                                                                                                                                                                                                                                                                                                                  |
| ENET_RD3    | RX_D3             | RGMII      | ALT0     | I         | —                                                                                                                                                                                                                                                                                                                                  |
| GPIO1_IO06  | MDC               | RMII/RGMII | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                  |
| GPIO1_IO07  | MDIO              | RMII/RGMII | ALT1     | I/O       | —                                                                                                                                                                                                                                                                                                                                  |
| I2C1_SCL    | MDC               | RMII/RGMII | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                  |
| I2C1_SDA    | MDIO              | RMII/RGMII | ALT1     | I/O       | —                                                                                                                                                                                                                                                                                                                                  |

Table 46. ENET signal mapping (continued)

| Pad name    | RGMII/RMII signal     | Mode       | Alt mode | Direction | Comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|-----------------------|------------|----------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1_IO08  | 1588_EVENT0_IN        | RMII/RGMII | ALT1     | I         | Capture/compare block input/output event bus signal. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_EVENT is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TCSRn[TDRE] is set. |
| GPIO1_IO09  | 1588_EVENT0_OUT       | RMII/RGMII | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| I2C2_SCL    | 1588_EVENT1_IN        | RMII/RGMII | ALT1     | I         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| I2C2_SDA    | 1588_EVENT1_OUT       | RMII/RGMII | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| GPIO1_IO00  | ENET_PHY_REF_CLK_ROOT | RGMII      | ALT1     | O         | Reference clock for PHY.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| SD1_CLK     | MDC                   | RMII       | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_CMD     | MDIO                  | RMII       | ALT1     | I/O       | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA0   | TX_D1                 | RMII       | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA1   | TX_D0                 | RMII       | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA2   | RX_D0                 | RMII       | ALT1     | I         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA3   | RX_D1                 | RMII       | ALT1     | I         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA4   | TX_EN                 | RMII       | ALT1     | O         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA5   | TX_ER                 | RMII       | ALT1     | O         | For RMII—SD1_DATA5 functions as RMII TX_ER when configured in the ALT1 mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| SD1_DATA6   | RX_EN (CRS_DV)        | RMII       | ALT1     | I         | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SD1_DATA7   | RX_ER                 | RMII       | ALT1     | I         | For RMII—SD1_DATA7 functions as RMII RX_ER when configured in the ALT1 mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| SD1_RESET_B | REF_CLK               | RMII       | ALT1     | O         | For RMII—SD1_RESET_B functions as RMII REF_CLK when configured in the ALT1 mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

### 3.9.3.1 RMII mode timing

Figure 19 shows RMII mode timings. Table 47 describes the timing parameters (M16–M21) shown in the figure.

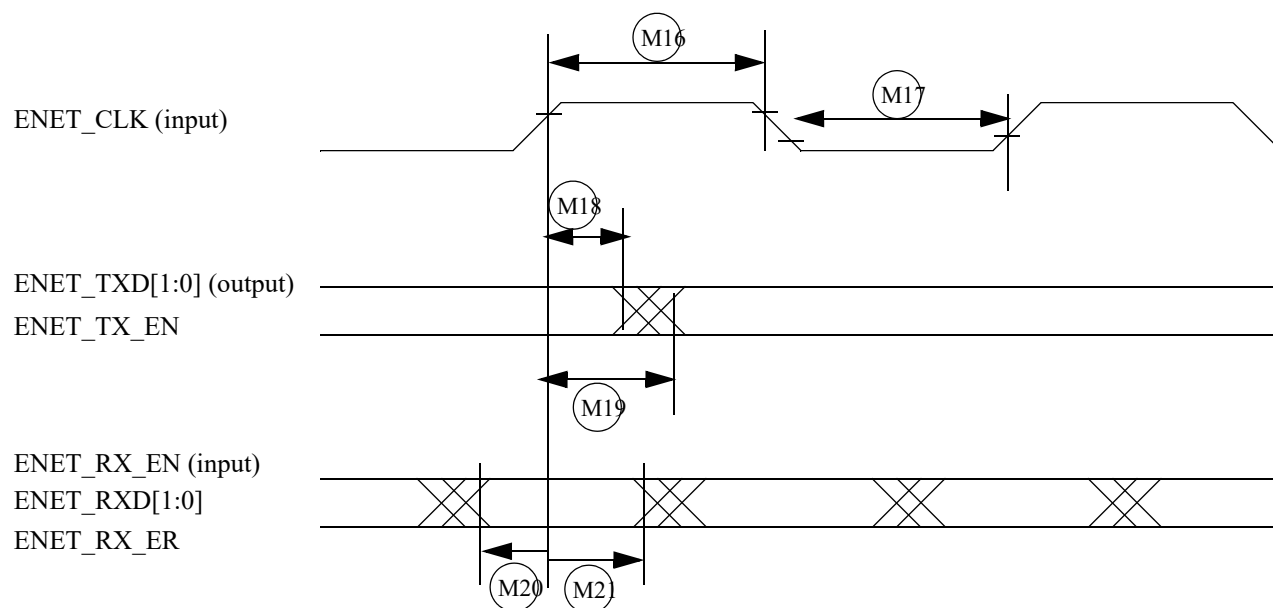


Figure 19. RMII mode signal timing diagram

Table 47. RMII signal timing

| ID  | Characteristic                                          | Min. | Max. | Unit            |
|-----|---------------------------------------------------------|------|------|-----------------|
| M16 | ENET_CLK pulse width high                               | 35%  | 65%  | ENET_CLK period |
| M17 | ENET_CLK pulse width low                                | 35%  | 65%  | ENET_CLK period |
| M18 | ENET_CLK to ENET_TXD[1:0], ENET_TXD invalid             | 4    | —    | ns              |
| M19 | ENET_CLK to ENET_TXD[1:0], ENET_TXD valid               | —    | 15   | ns              |
| M20 | ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER to ENET_CLK setup | 4    | —    | ns              |
| M21 | ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold  | 2    | —    | ns              |

### 3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

**Table 48. RGMII signal switching specifications<sup>1</sup>**

| Symbol              | Description                              | Min. | Max. | Unit |
|---------------------|------------------------------------------|------|------|------|
| $T_{cyc}^2$         | Clock cycle duration                     | 7.2  | 8.8  | ns   |
| $T_{skewT}^3$       | Data to clock output skew at transmitter | -500 | 500  | ps   |
| $T_{skewR}^3$       | Data to clock input skew at receiver     | 1    | 2.6  | ns   |
| Duty_G <sup>4</sup> | Duty cycle for Gigabit                   | 45   | 55   | %    |
| Duty_T <sup>4</sup> | Duty cycle for 10/100T                   | 40   | 60   | %    |
| Tr/Tf               | Rise/fall time (20–80%)                  | —    | 0.75 | ns   |

<sup>1</sup> The timings assume the following configuration:

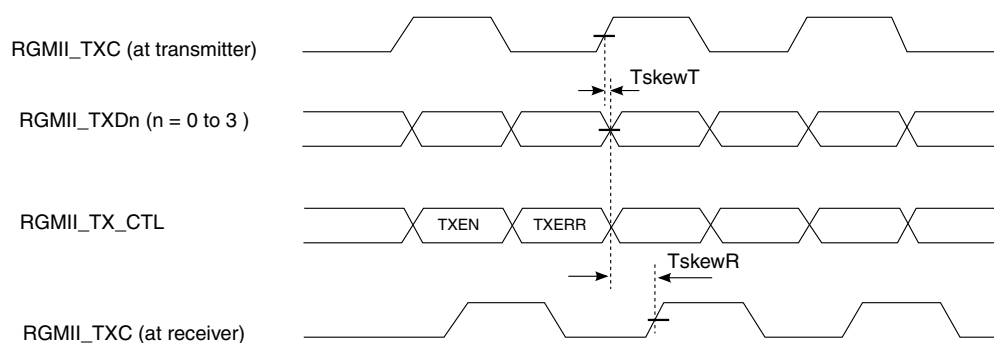
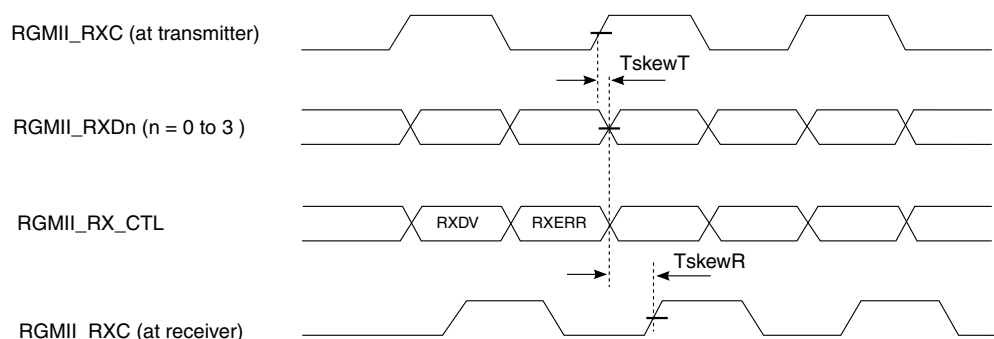
DDR\_SEL = (11)b

DSE (drive-strength) = (111)b

<sup>2</sup> For 10 Mbps and 100 Mbps,  $T_{cyc}$  will scale to 400 ns  $\pm$  40 ns and 40 ns  $\pm$  4 ns respectively.

<sup>3</sup> For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

<sup>4</sup> Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three  $T_{cyc}$  of the lowest speed transitioned between.

**Figure 20. RGMII transmit signal timing diagram original****Figure 21. RGMII receive signal timing diagram original**

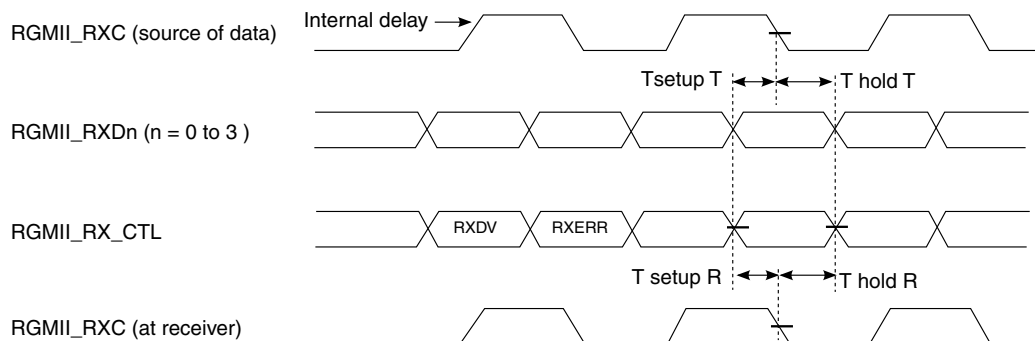


Figure 22. RGMII receive signal timing diagram with internal delay

### 3.9.4 General-purpose media interface (GPMI) timing

The i.MX 8M Nano GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

#### 3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. [Figure 23](#) through [Figure 26](#) depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. [Table 49](#) describes the timing parameters (NF1–NF17) that are shown in the figures.

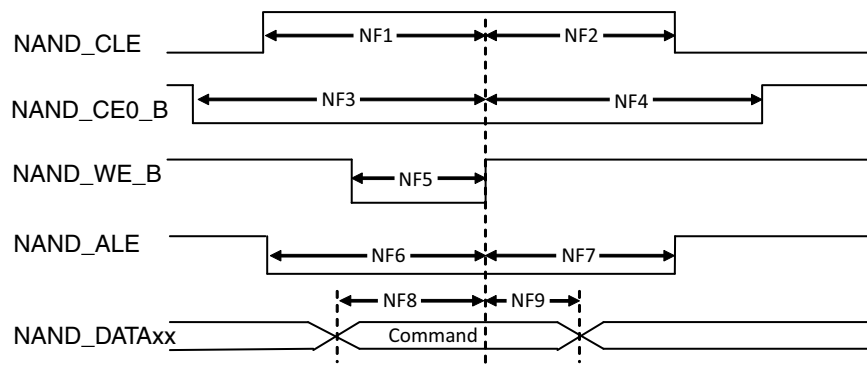


Figure 23. Command Latch cycle timing diagram

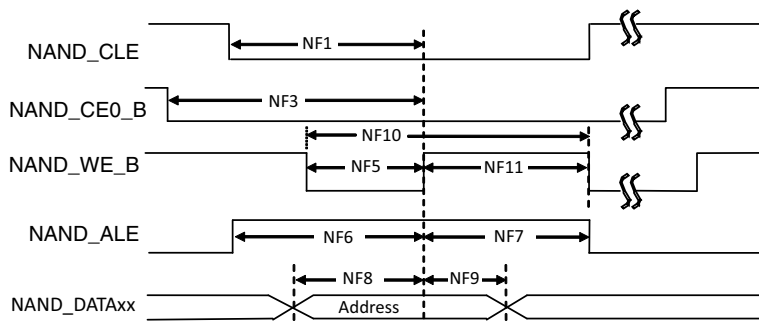


Figure 24. Address Latch cycle timing diagram

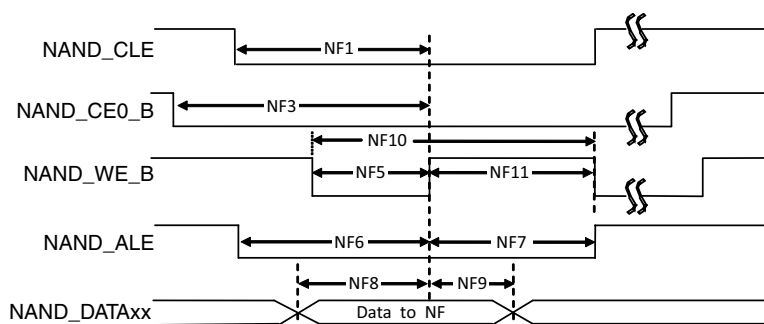


Figure 25. Write Data Latch cycle timing diagram

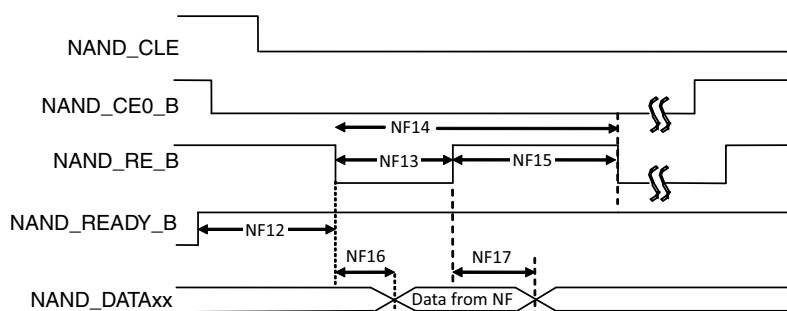


Figure 26. Read Data Latch cycle timing diagram (Non-EDO Mode)

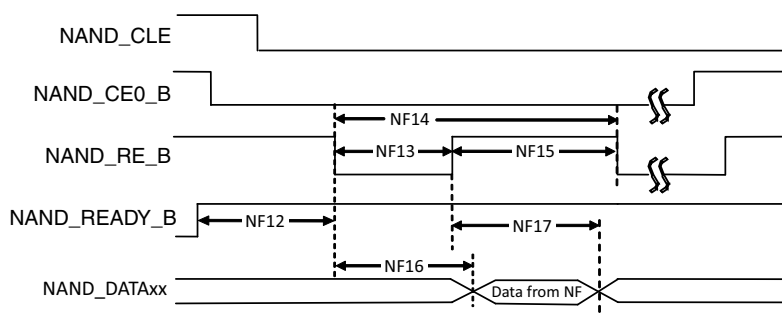


Figure 27. Read Data Latch cycle timing diagram (EDO mode)

Table 49. Asynchronous mode timing parameters<sup>1</sup>

| ID   | Parameter                | Symbol           | Timing<br>T = GPMI Clock Cycle                          |                                                          | Unit |
|------|--------------------------|------------------|---------------------------------------------------------|----------------------------------------------------------|------|
|      |                          |                  | Min.                                                    | Max.                                                     |      |
| NF1  | NAND_CLE setup time      | tCLS             | $(AS + DS) \times T - 0.12$ [see notes <sup>2,3</sup> ] |                                                          | ns   |
| NF2  | NAND_CLE hold time       | tCLH             | $DH \times T - 0.72$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF3  | NAND_CE0_B setup time    | tCS              | $(AS + DS + 1) \times T$ [see notes <sup>3,2</sup> ]    |                                                          | ns   |
| NF4  | NAND_CE0_B hold time     | tCH              | $(DH+1) \times T - 1$ [see note <sup>2</sup> ]          |                                                          | ns   |
| NF5  | NAND_WE_B pulse width    | tWP              | $DS \times T$ [see note <sup>2</sup> ]                  |                                                          | ns   |
| NF6  | NAND_ALE setup time      | tALS             | $(AS + DS) \times T - 0.49$ [see notes <sup>3,2</sup> ] |                                                          | ns   |
| NF7  | NAND_ALE hold time       | tALH             | $DH \times T - 0.42$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF8  | Data setup time          | tDS              | $DH \times T - 0.26$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF9  | Data hold time           | tDH              | $DH \times T - 1.37$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF10 | Write cycle time         | tWC              | $(DS + DH) \times T$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF11 | NAND_WE_B hold time      | tWH              | $DH \times T$ [see note <sup>2</sup> ]                  |                                                          | ns   |
| NF12 | Ready to NAND_RE_B low   | tRR <sup>4</sup> | $(AS + 2) \times T$ [see <sup>3,2</sup> ]               | —                                                        | ns   |
| NF13 | NAND_RE_B pulse width    | tRP              | $DS \times T$ [see note <sup>2</sup> ]                  |                                                          | ns   |
| NF14 | READ cycle time          | tRC              | $(DS + DH) \times T$ [see note <sup>2</sup> ]           |                                                          | ns   |
| NF15 | NAND_RE_B high hold time | tREH             | $DS \times T$ [see note <sup>2</sup> ]                  |                                                          | ns   |
| NF16 | Data setup on read       | tDSR             | —                                                       | $(DS \times T - 0.67)/18.38$ [see notes <sup>5,6</sup> ] | ns   |
| NF17 | Data hold on read        | tDHR             | 0.82/11.83 [see notes <sup>5,6</sup> ]                  | —                                                        | ns   |

<sup>1</sup> GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW\_GPMI\_TIMING0\_ADDRESS\_SETUP, HW\_GPMI\_TIMING0\_DATA\_SETUP, and HW\_GPMI\_TIMING0\_DATA\_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

<sup>2</sup> AS minimum value can be 0, while DS/DH minimum value is 1.

<sup>3</sup> T = GPMI clock period -0.075 ns (half of maximum p-p jitter).

<sup>4</sup> NF12 is guaranteed by the design.

<sup>5</sup> Non-EDO mode.

<sup>6</sup> EDO mode, GPMI clock  $\approx$  100 MHz  
(AS=DS=DH=1, GPMI\_CTL1 [RDN\_DELAY] = 8, GPMI\_CTL1 [HALF\_PERIOD] = 0).

In EDO mode (Figure 26), NF16/NF17 are different from the definition in non-EDO mode (Figure 25). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND\_DATAxx at the rising edge of delayed NAND\_RE\_B provided by an internal DPLL. The delay value can be controlled by GPMI\_CTRL1.RDN\_DELAY (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

### 3.9.4.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 28 to Figure 30 show the write and read timing of Source Synchronous mode.

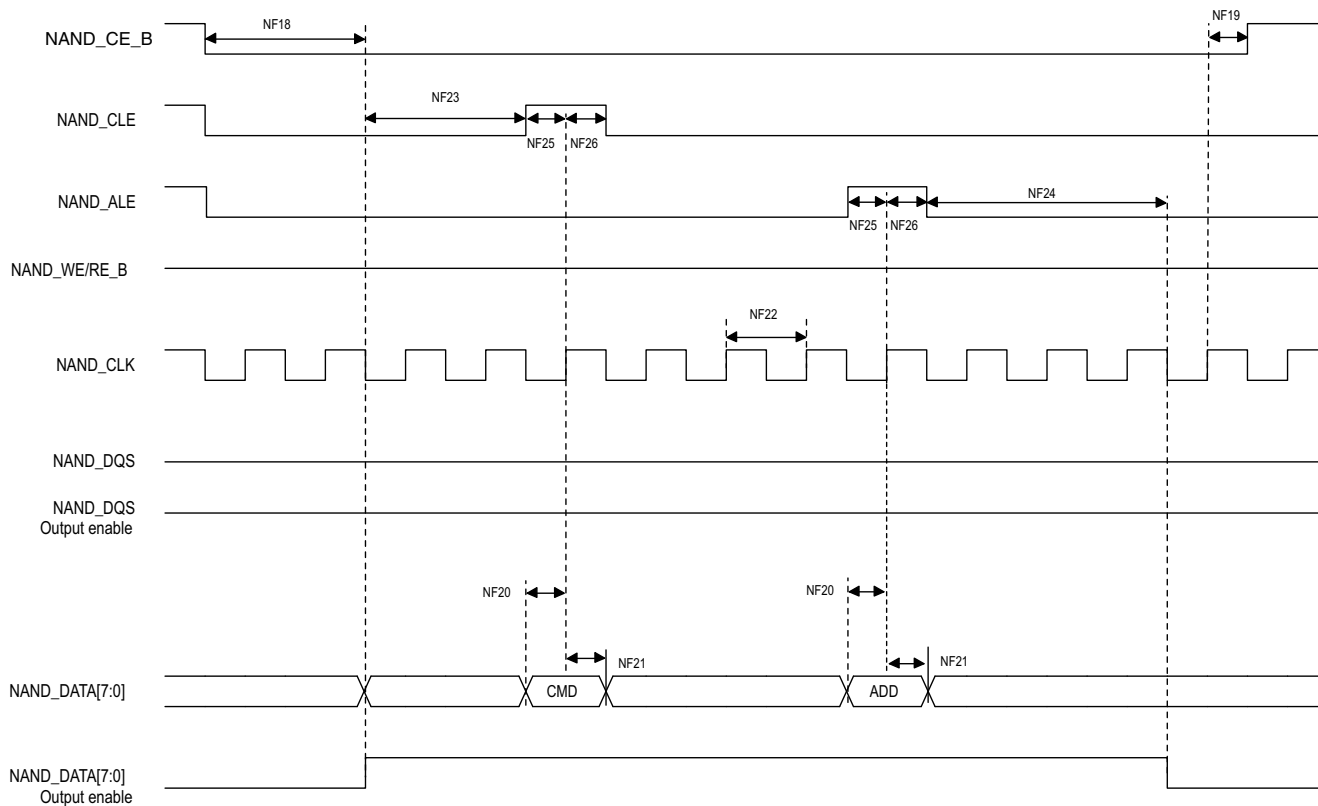


Figure 28. Source Synchronous mode command and address timing diagram



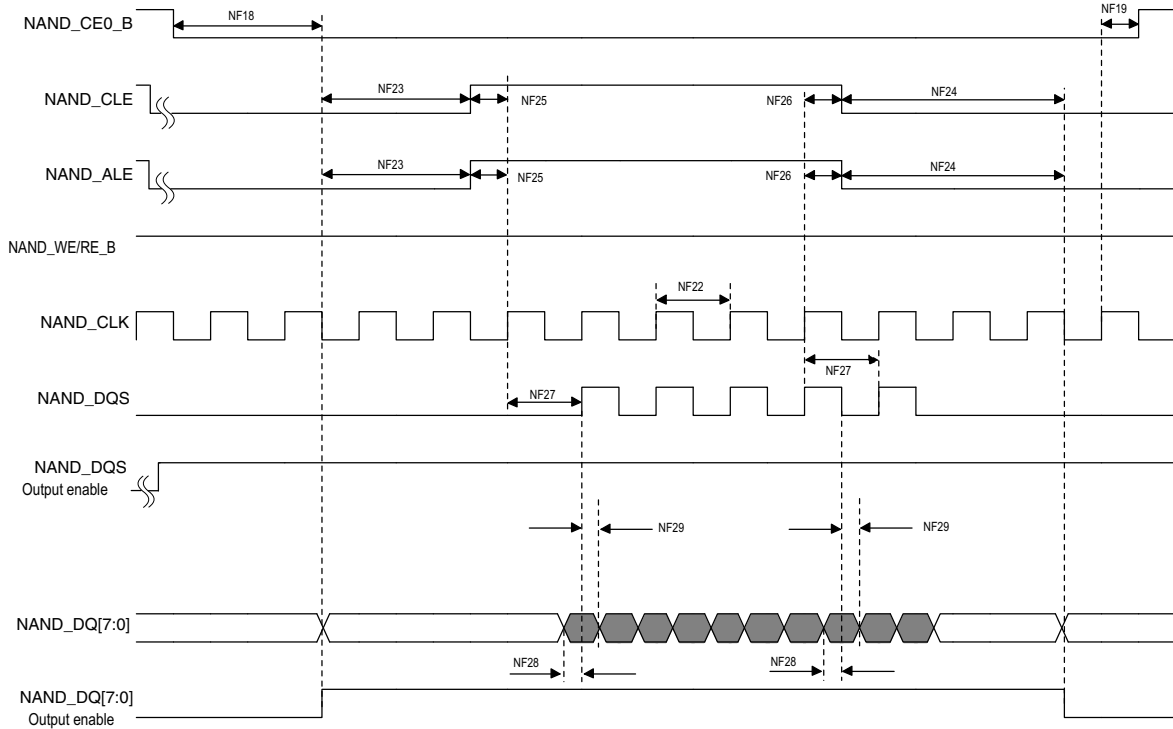


Figure 29. Source Synchronous mode data write timing diagram

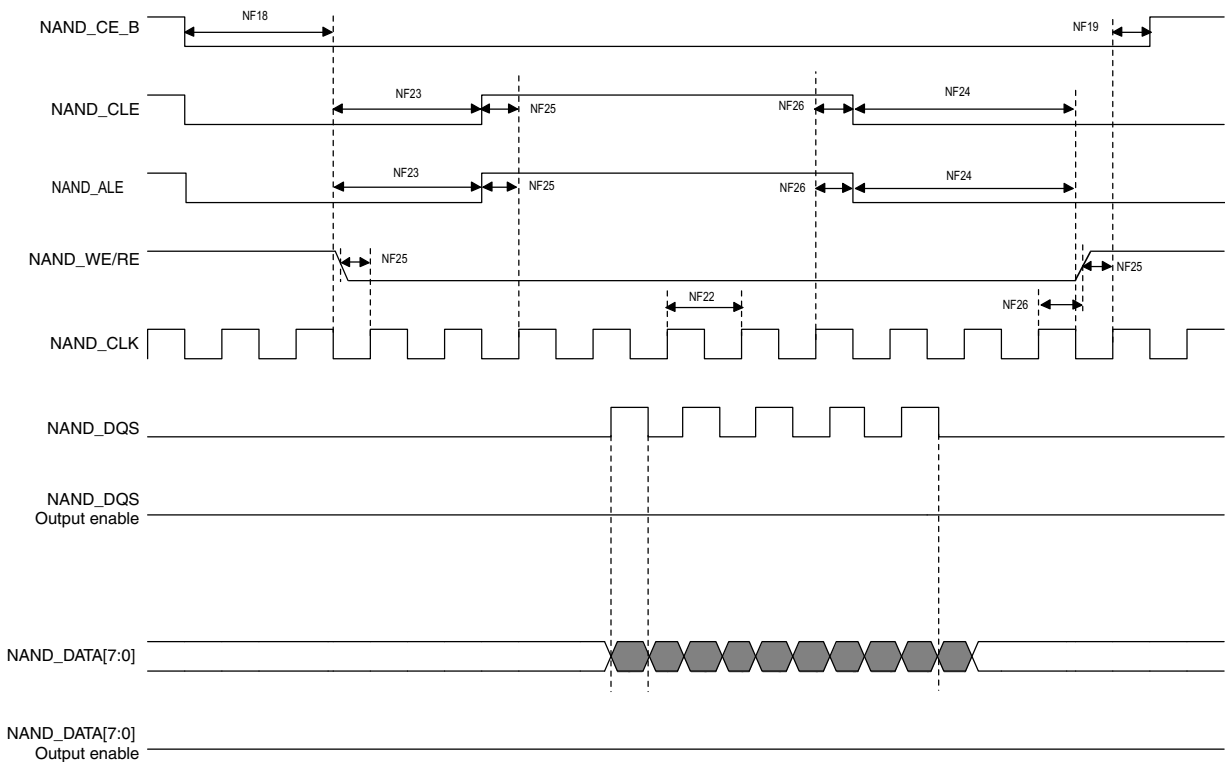


Figure 30. Source Synchronous mode data read timing diagram

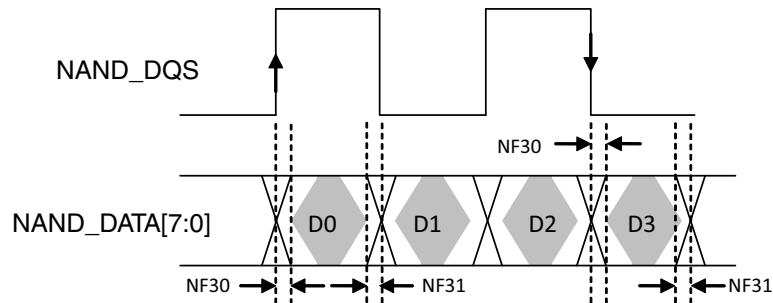


Figure 31. NAND\_DQS/NAND\_DQ read valid window

Table 50. Source Synchronous mode timing parameters<sup>1</sup>

| ID   | Parameter                                      | Symbol | Timing<br>T = GPMI Clock Cycle                         |      | Unit |
|------|------------------------------------------------|--------|--------------------------------------------------------|------|------|
|      |                                                |        | Min.                                                   | Max. |      |
| NF18 | NAND_CE0_B access time                         | tCE    | $CE\_DELAY \times T - 0.79$ [see note <sup>2</sup> ]   |      | ns   |
| NF19 | NAND_CE0_B hold time                           | tCH    | $0.5 \times tCK - 0.63$ [see note <sup>2</sup> ]       |      | ns   |
| NF20 | Command/address NAND_DATAxx setup time         | tCAS   | $0.5 \times tCK - 0.05$                                |      | ns   |
| NF21 | Command/address NAND_DATAxx hold time          | tCAH   | $0.5 \times tCK - 1.23$                                |      | ns   |
| NF22 | clock period                                   | tCK    | —                                                      |      | ns   |
| NF23 | preamble delay                                 | tPRE   | $PRE\_DELAY \times T - 0.29$ [see note <sup>2</sup> ]  |      | ns   |
| NF24 | postamble delay                                | tPOST  | $POST\_DELAY \times T - 0.78$ [see note <sup>2</sup> ] |      | ns   |
| NF25 | NAND_CLE and NAND_ALE setup time               | tCALS  | $0.5 \times tCK - 0.86$                                |      | ns   |
| NF26 | NAND_CLE and NAND_ALE hold time                | tCALH  | $0.5 \times tCK - 0.37$                                |      | ns   |
| NF27 | NAND_CLK to first NAND_DQS latching transition | tDQSS  | $T - 0.41$ [see note <sup>2</sup> ]                    |      | ns   |
| NF28 | Data write setup                               | —      | $0.25 \times tCK - 0.35$                               |      |      |
| NF29 | Data write hold                                | —      | $0.25 \times tCK - 0.85$                               |      |      |
| NF30 | NAND_DQS/NAND_DQ read setup skew               | —      | —                                                      | 2.06 |      |
| NF31 | NAND_DQS/NAND_DQ read hold skew                | —      | —                                                      | 1.95 |      |

<sup>1</sup> GPMI's Source Synchronous mode output timing can be controlled by the module's internal registers GPMI\_TIMING2\_CE\_DELAY, GPMI\_TIMING2\_PREAMBLE\_DELAY, GPMI\_TIMING2\_POST\_DELAY. This AC timing depends on these registers settings. In the table, CE\_DELAY/PRE\_DELAY/POST\_DELAY represents each of these settings.

<sup>2</sup> T = tCK(GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

For DDR Source Synchronous mode, Figure 31 shows the timing diagram of NAND\_DQS/NAND\_DATAxx read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND\_DATA[7:0] at both rising and falling edge of an delayed NAND\_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI\_READ\_DDR\_DLL\_CTRL.SLV\_DLY\_TARGET (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

### 3.9.4.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

#### 3.9.4.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See [Section 3.9.4.1, Asynchronous mode AC timing \(ONFI 1.0 compatible\)](#), for details.

#### 3.9.4.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See [Section 3.9.4.4, Toggle mode AC Timing](#), for details.

### 3.9.4.4 Toggle mode AC Timing

#### 3.9.4.4.1 Command and address timing

##### NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See [Section 3.9.4.1, Asynchronous mode AC timing \(ONFI 1.0 compatible\)](#), for details.

#### 3.9.4.4.2 Read and write timing

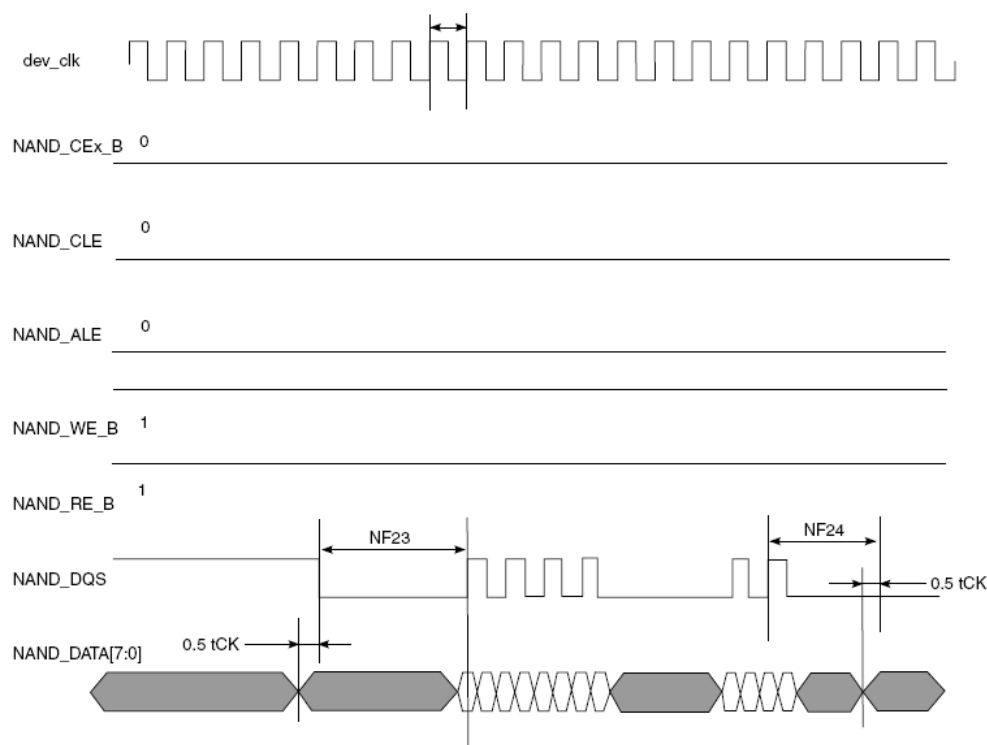


Figure 32. Toggle mode data write timing

## Electrical characteristics

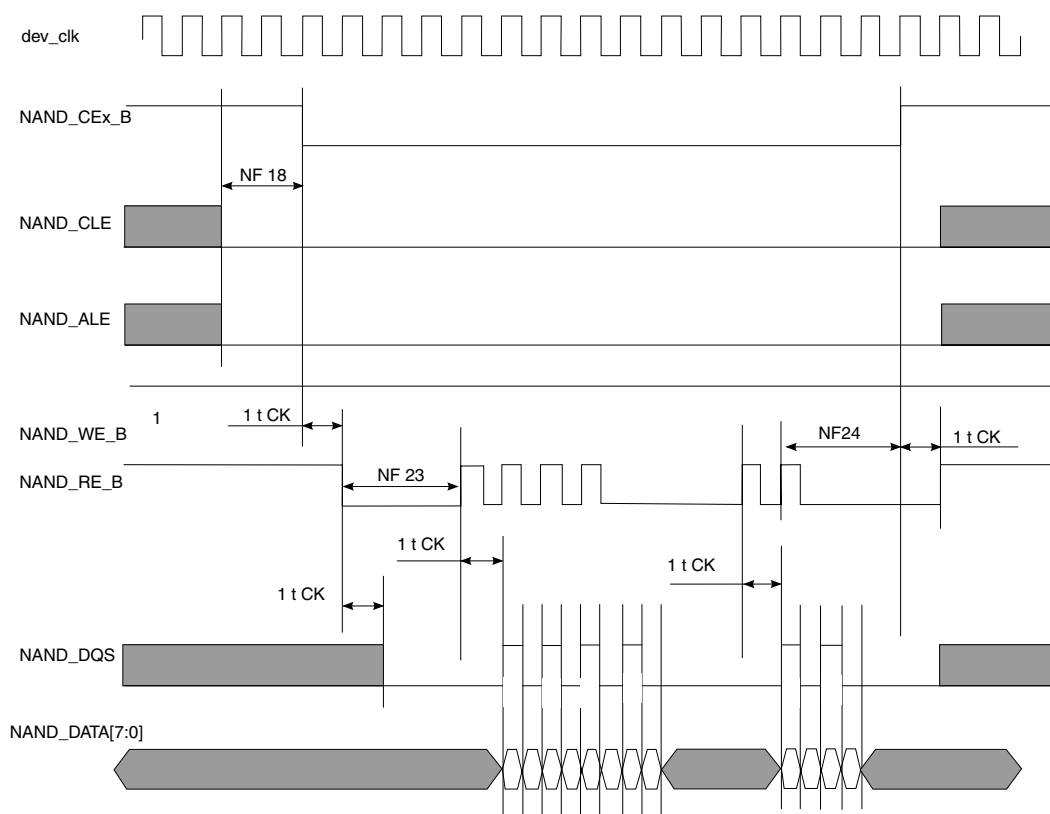


Figure 33. Toggle mode data read timing

Table 51. Toggle mode timing parameters

| ID   | Parameter                              | Symbol | Timing<br>T = GPML Clock Cycle                         |      | Unit |
|------|----------------------------------------|--------|--------------------------------------------------------|------|------|
|      |                                        |        | Min.                                                   | Max. |      |
| NF1  | NAND_CLE setup time                    | tCLS   | $(AS + DS) \times T - 0.12$ [see note <sup>1,2</sup> ] |      |      |
| NF2  | NAND_CLE hold time                     | tCLH   | $DH \times T - 0.72$ [see note <sup>2</sup> ]          |      |      |
| NF3  | NAND_CE0_B setup time                  | tCS    | $(AS + DS) \times T - 0.58$ [see notes <sup>2</sup> ]  |      |      |
| NF4  | NAND_CE0_B hold time                   | tCH    | $DH \times T - 1$ [see note <sup>2</sup> ]             |      |      |
| NF5  | NAND_WE_B pulse width                  | tWP    | $DS \times T$ [see note <sup>2</sup> ]                 |      |      |
| NF6  | NAND_ALE setup time                    | tALS   | $(AS + DS) \times T - 0.49$ [see notes <sup>2</sup> ]  |      |      |
| NF7  | NAND_ALE hold time                     | tALH   | $DH \times T - 0.42$ [see note <sup>2</sup> ]          |      |      |
| NF8  | Command/address NAND_DATAxx setup time | tCAS   | $DS \times T - 0.26$ [see note <sup>2</sup> ]          |      |      |
| NF9  | Command/address NAND_DATAxx hold time  | tCAH   | $DH \times T - 1.37$ [see note <sup>2</sup> ]          |      |      |
| NF18 | NAND_CEx_B access time                 | tCE    | $CE\_DELAY \times T$ [see notes <sup>3,2</sup> ]       | —    | ns   |
| NF22 | clock period                           | tCK    | —                                                      | —    | ns   |
| NF23 | preamble delay                         | tPRE   | $PRE\_DELAY \times T$ [see notes <sup>4,2</sup> ]      | —    | ns   |

Table 51. Toggle mode timing parameters (continued)

| ID   | Parameter                        | Symbol             | Timing<br>T = GPMI Clock Cycle                 |      | Unit |
|------|----------------------------------|--------------------|------------------------------------------------|------|------|
|      |                                  |                    | Min.                                           | Max. |      |
| NF24 | postamble delay                  | tPOST              | POST_DELAY × T + 0.43 [see note <sup>2</sup> ] | —    | ns   |
| NF28 | Data write setup                 | tDS <sup>5</sup>   | 0.25 × tCK - 0.32                              | —    | ns   |
| NF29 | Data write hold                  | tDH <sup>5</sup>   | 0.25 × tCK - 0.79                              | —    | ns   |
| NF30 | NAND_DQS/NAND_DQ read setup skew | tDQSQ <sup>6</sup> | —                                              | 3.18 | ns   |
| NF31 | NAND_DQS/NAND_DQ read hold skew  | tQHS <sup>6</sup>  | —                                              | 3.27 | ns   |

<sup>1</sup> AS minimum value can be 0, while DS/DH minimum value is 1.

<sup>2</sup> T = tCK (GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

<sup>3</sup> CE\_DELAY represents HW\_GPMI\_TIMING2[CE\_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

<sup>4</sup> PRE\_DELAY + 1 ≥ (AS + DS)

<sup>5</sup> Shown in Figure 32.

<sup>6</sup> Shown in Figure 33.

For DDR Toggle mode, Figure 31 shows the timing diagram of NAND\_DQS/NAND\_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI samples NAND\_DATA[7:0] at both the rising and falling edges of a delayed NAND\_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by the GPMI register GPMI\_READ\_DDR\_DLL\_CTRL.SLV\_DLY\_TARGET (see the GPMI chapter of the *i.MX 8M Nano Applications Processor Reference Manual* [IMX8MNRM]). Generally, the typical delay value is equal to 0x7, which means a 1/4 clock cycle delay is expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

### 3.9.5 I<sup>2</sup>C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

### 3.9.6 MIPI D-PHY timing parameters

MIPI D-PHY electrical specifications are compliance.

Table 52. MIPI PHY worst power dissipation<sup>1</sup>

| MODE     |                 | Power consume on VDD_MIPI_0P8 (mW) | Power consume on VDD_MIPI_1P2 (mW) | Power consume on VDD_MIPI_1P8 (mW) | Total power consume (mW) |
|----------|-----------------|------------------------------------|------------------------------------|------------------------------------|--------------------------|
| 2.1 Gbps | M4 on<br>S4 on  | 226.1                              | 4.1                                | 35.6                               | 265.8                    |
|          | M4 on<br>S4 off | 164.7                              | 4.03                               | 28.6                               | 197.33                   |
|          | M4 off<br>S4 on | 63.02                              | 0                                  | 15.8                               | 78.82                    |
| ULPS     |                 | 4.26                               | 0.0367                             | 0.0584                             | 4.36                     |

<sup>1</sup> M4 indicates MIPI DSI have 4 data lane enable (at least 1 clock lane enable). S4 indicates MIPI CSI have 4 data lane enable (at least 1 clock lane enable).

### 3.9.7 PDM timing parameters

Figure 34 illustrates the input timing of the PDM.

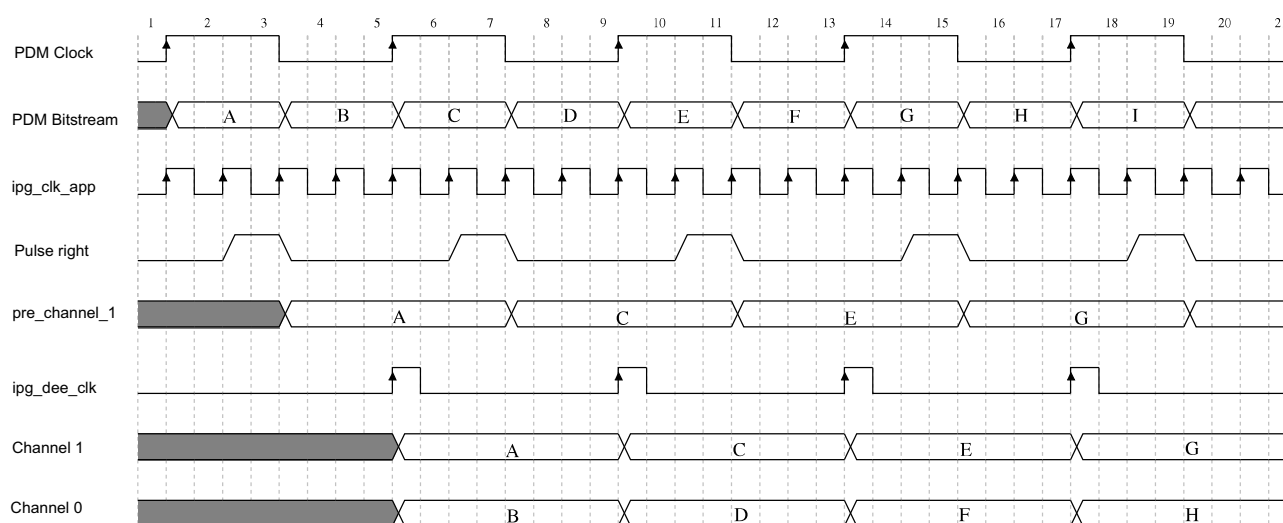


Figure 34. PDM input timing

PDM clock operative range is from 500 kHz to 6 MHz. Within range, only need to configure ipg\_clk\_app rate and CLKDIV without I/O timing concerns.

### 3.9.8 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before

being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 35 depicts the timing of the PWM, and Table 53 lists the PWM timing parameters.

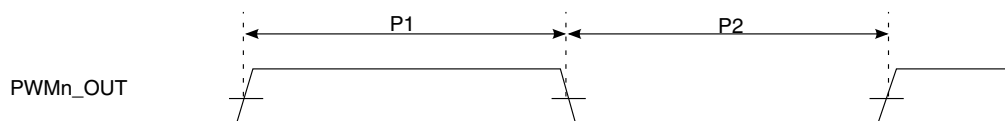


Figure 35. PWM timing

Table 53. PWM output timing parameters

| ID | Parameter                   | Min | Max          | Unit |
|----|-----------------------------|-----|--------------|------|
|    | PWM Module Clock Frequency  | 0   | 66 (ipg_clk) | MHz  |
| P1 | PWM output pulse width high | 12  | —            | ns   |
| P2 | PWM output pulse width low  | 12  | —            | ns   |

### 3.9.9 FlexSPI timing parameters

Measurements are with a load of 15 pF and an input slew rate of 1 V/ns.

#### 3.9.9.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI<sub>in</sub>\_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI<sub>in</sub>\_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI<sub>in</sub>\_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these four internal sample clock sources.

##### 3.9.9.1.1 SDR mode with FlexSPI<sub>in</sub>\_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Table 54. FlexSPI input timing in SDR mode where FlexSPI<sub>in</sub>\_MCR0[RXCLKSRC] = 0x0

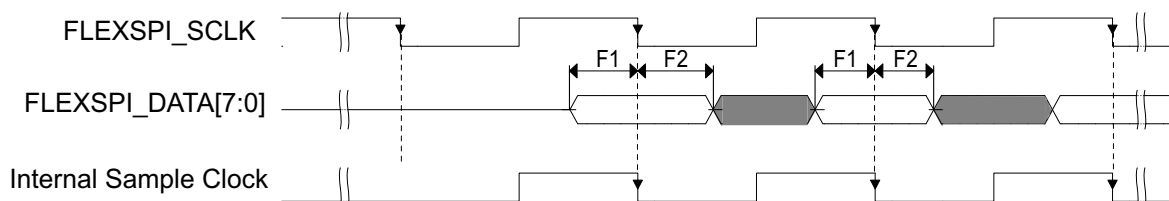
| Symbol | Parameter                         | Min. | Max. | Unit | Notes        |
|--------|-----------------------------------|------|------|------|--------------|
| —      | [D:] Frequency of operation       | —    | 66   | MHz  | —            |
| F1     | [D:] Setup time for incoming data | 8.67 | —    | ns   | <sup>1</sup> |
| F2     | [D:] Hold time for incoming data  | 0    | —    | ns   | —            |

<sup>1</sup> The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

**Table 55. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x1, 0x2**

| Symbol | Parameter                         | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| —      | [D:] Frequency of operation       | —    | 133  | MHz  | —     |
| F1     | [D:] Setup time for incoming data | 1.5  | —    | ns   | 1     |
| F2     | [D:] Hold time for incoming data  | 1    | —    | ns   | —     |

<sup>1</sup> The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

**Figure 36. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2****NOTE**

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

**3.9.9.1.2 SDR mode with FlexSPIn\_MCR0[RXCLKSRC] = 0x3**

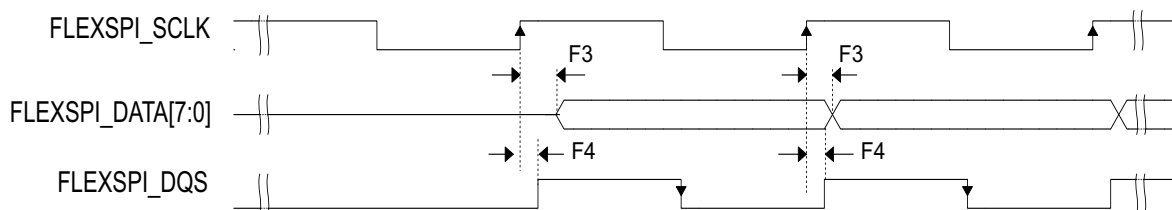
There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

**Table 56. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (Case A1)**

| Symbol | Parameter                                 | Min. | Max. | Unit |
|--------|-------------------------------------------|------|------|------|
| —      | [D:] Frequency of operation               | —    | 166  | MHz  |
| F3     | [D:] Time from SCK to data valid          | —    | —    | ns   |
| F4     | [D:] Time from SCK to DQS                 | —    | —    | ns   |
| —      | [D:] Time delta between TSCKD and TSCKDQS | -2   | 2    | ns   |





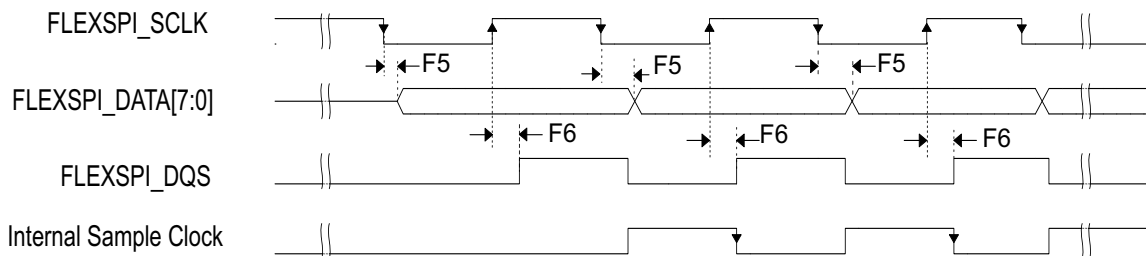
**Figure 37. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (Case A1)**

#### NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

**Table 57. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (Case A2)**

| Symbol | Parameter                                  | Min. | Max. | Unit |
|--------|--------------------------------------------|------|------|------|
| —      | [D:] Frequency of operation                | —    | 166  | MHz  |
| F5     | [D:] Time from SCK to data valid           | —    | —    | ns   |
| F6     | [D:] Time from SCK to DQS                  | —    | —    | ns   |
| —      | [D:] Time delta between TSCKD and TSCKDQDS | -2   | 2    | ns   |



**Figure 38. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (Case A2)**

#### NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half-cycle delayed DQS falling edge.

### 3.9.9.1.3 DDR mode with FlexSPIn\_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

**Table 58. FlexSPI input timing in DDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x0**

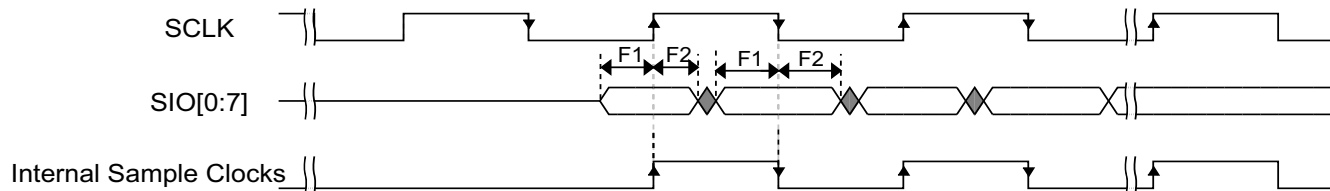
| Symbol | Parameter                         | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| —      | [D:] Frequency of operation       | —    | 33   | MHz  | —     |
| F1     | [D:] Setup time for incoming data | 8.67 | —    | ns   | 1     |
| F2     | [D:] Hold time for incoming data  | 0    | —    | ns   | —     |

<sup>1</sup> The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

**Table 59. FlexSPI input timing in DDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x1, 0x2**

| Symbol | Parameter                         | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| —      | [D:] Frequency of operation       | —    | 66   | MHz  | —     |
| F1     | [D:] Setup time for incoming data | 1.5  | —    | ns   | 1     |
| F2     | [D:] Hold time for incoming data  | 1    | —    | ns   | —     |

<sup>1</sup> The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.



**Figure 39. FlexSPI input timing in DDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2**

### 3.9.9.1.4 DDR mode with FlexSPIn\_MCR0[RXCLKSRC] = 0x3

**Table 60. FlexSPI input timing in DDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (Case 1)**

| Symbol                                  | Parameter                                 | Min. | Max. | Unit |
|-----------------------------------------|-------------------------------------------|------|------|------|
| —                                       | [D:] Frequency of operation               | —    | 166  | MHz  |
| T <sub>SCKD</sub>                       | [D:] Time from SCK to data valid          | —    | —    | ns   |
| T <sub>SCKDQS</sub>                     | [D:] Time from SCK to DQS                 | —    | —    | ns   |
| T <sub>SCKD</sub> - T <sub>SCKDQS</sub> | [D:] Time delta between TSCKD and TSCKDQS | -0.6 | 0.6  | ns   |

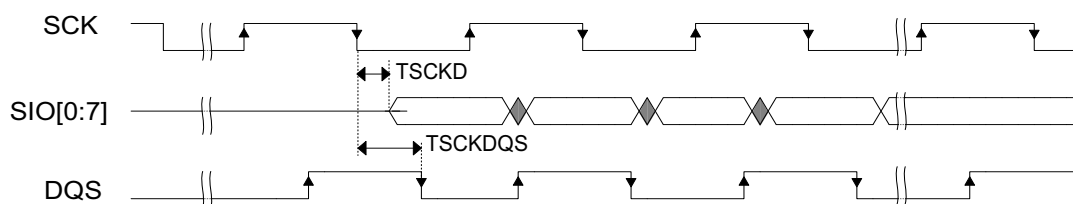


Figure 40. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3

### 3.9.9.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

#### 3.9.9.2.1 SDR mode

Table 61. FlexSPI output timing in SDR mode

| Symbol           | Parameter                                | Min.                    | Max. | Unit |
|------------------|------------------------------------------|-------------------------|------|------|
| —                | [D:] Frequency of operation <sup>1</sup> | —                       | 166  | MHz  |
| T <sub>CK</sub>  | [D:] SCK clock period                    | 6.02                    | —    | ns   |
| T <sub>DSO</sub> | [D:] Output data setup time              | 2                       | —    | ns   |
| T <sub>DHO</sub> | [D:] Output data hold time               | 2                       | —    | ns   |
| T <sub>CSS</sub> | [D:] Chip select output setup time       | 3 x T <sub>CK</sub> - 1 | —    | ns   |
| T <sub>CSH</sub> | [D:] Chip select output hold time        | 3 x T <sub>CK</sub> - 1 | —    | ns   |

<sup>1</sup> The actual maximum frequency supported is limited by the FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

#### NOTE

T<sub>CSS</sub> and T<sub>CSH</sub> are configured by the FlexSPI<sub>n</sub>\_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for more details.

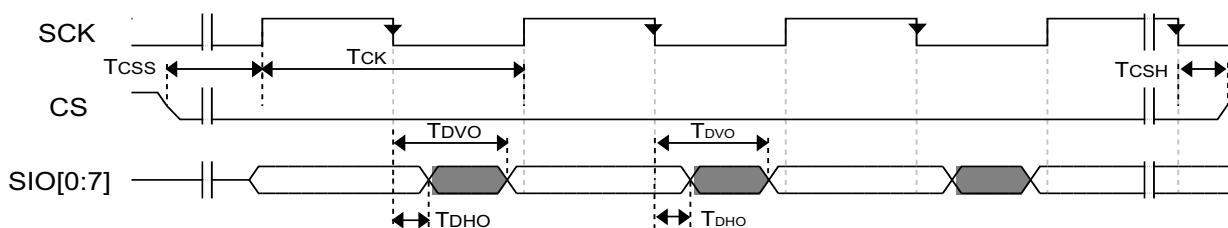


Figure 41. FlexSPI output timing in SDR mode

### 3.9.9.2.2 DDR mode

Table 62. FlexSPI output timing in DDR mode

| Symbol           | Parameter                                | Min.                        | Max. | Unit |
|------------------|------------------------------------------|-----------------------------|------|------|
| —                | [D:] Frequency of operation <sup>1</sup> | —                           | 166  | MHz  |
| T <sub>CK</sub>  | [D:] SCK clock period                    | 6.02                        | —    | ns   |
| T <sub>DSO</sub> | [D:] Output data setup time              | —                           | 0.6  | ns   |
| T <sub>DHO</sub> | [D:] Output data hold time               | 0.6                         | —    | ns   |
| T <sub>CSS</sub> | [D:] Chip select output setup time       | 3 x T <sub>CK</sub> - 1.075 | —    | ns   |
| T <sub>CSH</sub> | [D:] Chip select output hold time        | 3 x T <sub>CK</sub> - 1.075 | —    | ns   |

<sup>1</sup> The actual maximum frequency supported is limited by the FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

#### NOTE

T<sub>CSS</sub> and T<sub>CSH</sub> are configured by the FlexSPI<sub>n</sub>\_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM) for more details.

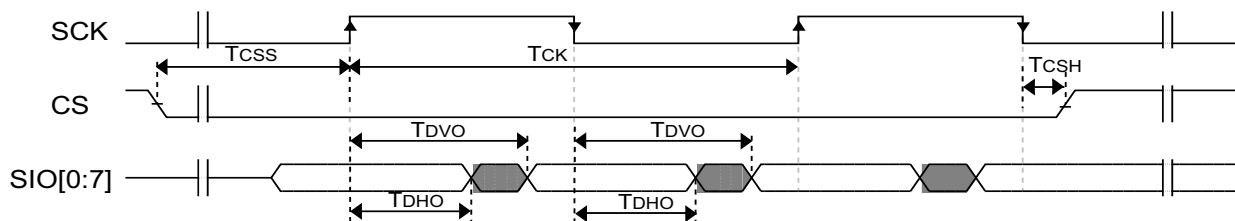


Figure 42. FlexSPI output timing in DDR mode

### 3.9.10 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI\_TCR[TSCKP] = 0, SAI\_RCR[RSCKP] = 0) and non inverted frame sync (SAI\_TCR[TFSI] = 0, SAI\_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI\_BCLK) and/or the frame sync (SAI\_FS) shown in the figures below.

Table 63. Master mode SAI timing (50 MHz)<sup>1</sup>

| Num | Characteristic                | Min | Max | Unit        |
|-----|-------------------------------|-----|-----|-------------|
| S1  | SAI_MCLK cycle time           | 20  | —   | ns          |
| S2  | SAI_MCLK pulse width high/low | 40% | 60% | MCLK period |
| S3  | SAI_BCLK cycle time           | 20  | —   | ns          |

**Table 63. Master mode SAI timing (50 MHz)<sup>1</sup> (continued)**

| Num | Characteristic                             | Min | Max | Unit        |
|-----|--------------------------------------------|-----|-----|-------------|
| S4  | SAI_BCLK pulse width high/low              | 40% | 60% | BCLK period |
| S5  | SAI_BCLK to SAI_FS output valid            | —   | 2   | ns          |
| S6  | SAI_BCLK to SAI_FS output invalid          | 0   | —   | ns          |
| S7  | SAI_BCLK to SAI_TXD valid                  | —   | 2   | ns          |
| S8  | SAI_BCLK to SAI_TXD invalid                | 0   | —   | ns          |
| S9  | SAI_RXD/SAI_FS input setup before SAI_BCLK | 2   | —   | ns          |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK   | 0   | —   | ns          |

<sup>1</sup> To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.

**Table 64. Master mode SAI timing (25 MHz)**

| Num | Characteristic                             | Min | Max | Unit        |
|-----|--------------------------------------------|-----|-----|-------------|
| S1  | SAI_MCLK cycle time                        | 40  | —   | ns          |
| S2  | SAI_MCLK pulse width high/low              | 40% | 60% | MCLK period |
| S3  | SAI_BCLK cycle time                        | 40  | —   | ns          |
| S4  | SAI_BCLK pulse width high/low              | 40% | 60% | BCLK period |
| S5  | SAI_BCLK to SAI_FS output valid            | —   | 2   | ns          |
| S6  | SAI_BCLK to SAI_FS output invalid          | 0   | —   | ns          |
| S7  | SAI_BCLK to SAI_TXD valid                  | —   | 2   | ns          |
| S8  | SAI_BCLK to SAI_TXD invalid                | 0   | —   | ns          |
| S9  | SAI_RXD/SAI_FS input setup before SAI_BCLK | 12  | —   | ns          |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK   | 0   | —   | ns          |

## Electrical characteristics

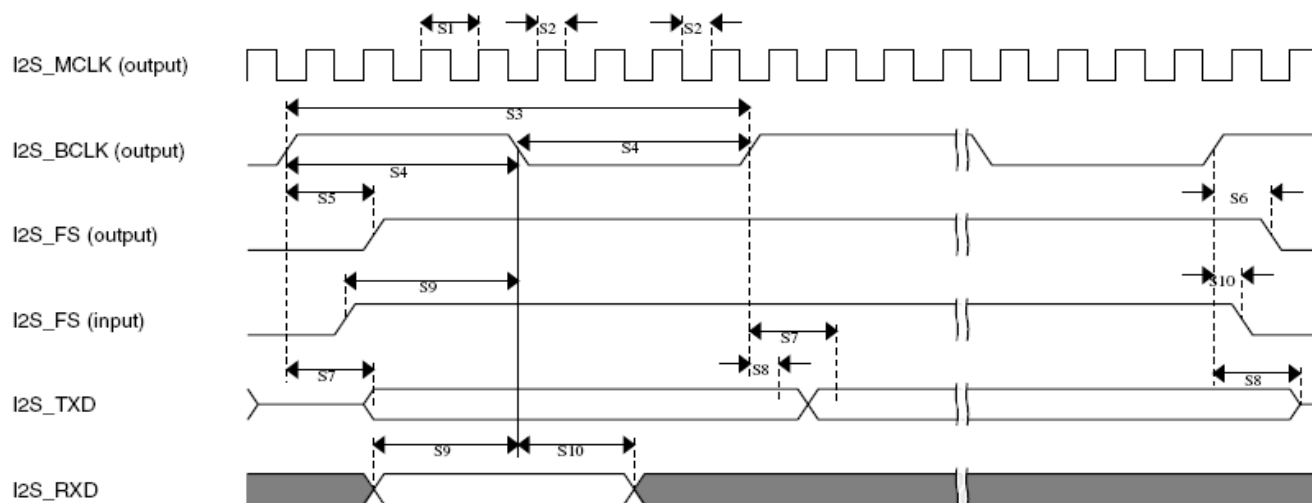


Figure 43. SAI timing—Master modes

Table 65. Slave mode SAI timing (50 MHz)<sup>1</sup>

| Num | Characteristic                        | Min | Max | Unit        |
|-----|---------------------------------------|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input)           | 20  | —   | ns          |
| S12 | SAI_BCLK pulse width high/low (input) | 40% | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK    | 2   | —   | ns          |
| S14 | SAI_FA input hold after SAI_BCLK      | 2   | —   | ns          |
| S17 | SAI_RXD setup before SAI_BCLK         | 2   | —   | ns          |
| S18 | SAI_RXD hold after SAI_BCLK           | 2   | —   | ns          |

<sup>1</sup> TX does not support 50 MHz operation in Slave mode.

Table 66. Slave mode SAI timing (25 MHz)

| Num | Characteristic                            | Min | Max | Unit        |
|-----|-------------------------------------------|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input)               | 40  | —   | ns          |
| S12 | SAI_BCLK pulse width high/low (input)     | 40% | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK        | 12  | —   | ns          |
| S14 | SAI_FA input hold after SAI_BCLK          | 2   | —   | ns          |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid   | —   | 7   | ns          |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0   | —   | ns          |
| S17 | SAI_RXD setup before SAI_BCLK             | 12  | —   | ns          |
| S18 | SAI_RXD hold after SAI_BCLK               | 2   | —   | ns          |

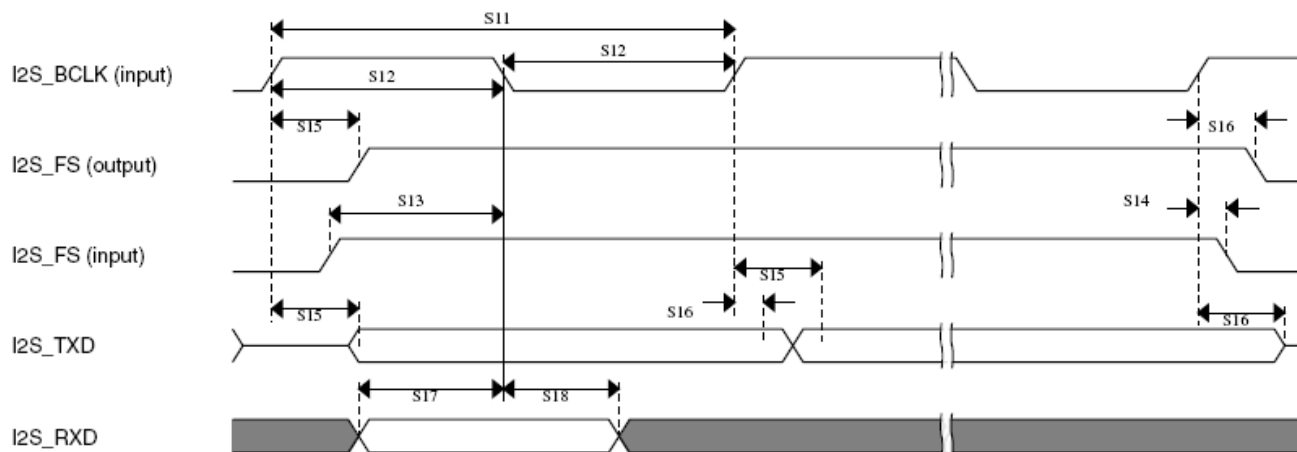


Figure 44. SAI Timing — Slave Modes

### 3.9.11 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 67 and Figure 45 and Figure 46 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF\_SR\_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF\_ST\_CLK) for SPDIF in Tx mode.

Table 67. SPDIF timing parameters

| Parameter                                          | Symbol  | Timing Parameter Range |      | Unit |
|----------------------------------------------------|---------|------------------------|------|------|
|                                                    |         | Min                    | Max  |      |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | —       | —                      | 0.7  | ns   |
| SPDIF_OUT output (Load = 50 pf)                    | —       | —                      | 1.5  | ns   |
| • Skew                                             | —       | —                      | 24.2 |      |
| • Transition rising                                | —       | —                      | 31.3 |      |
| • Transition falling                               | —       | —                      |      |      |
| SPDIF_OUT output (Load = 30 pf)                    | —       | —                      | 1.5  | ns   |
| • Skew                                             | —       | —                      | 13.6 |      |
| • Transition rising                                | —       | —                      | 18.0 |      |
| • Transition falling                               | —       | —                      |      |      |
| Modulating Rx clock (SPDIF_SR_CLK) period          | srckp   | 40.0                   | —    | ns   |
| SPDIF_SR_CLK high period                           | srckph  | 16.0                   | —    | ns   |
| SPDIF_SR_CLK low period                            | srckpl  | 16.0                   | —    | ns   |
| Modulating Tx clock (SPDIF_ST_CLK) period          | stclkp  | 40.0                   | —    | ns   |
| SPDIF_ST_CLK high period                           | stclkph | 16.0                   | —    | ns   |
| SPDIF_ST_CLK low period                            | stclkpl | 16.0                   | —    | ns   |

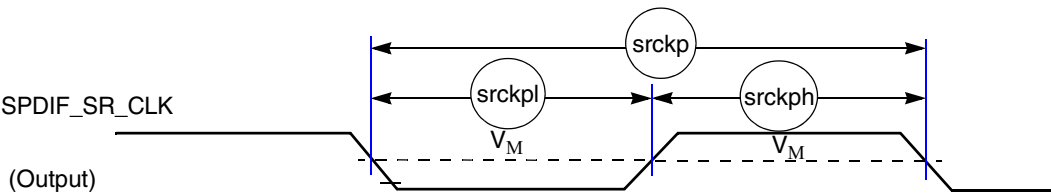


Figure 45. SPDIF\_SR\_CLK timing diagram

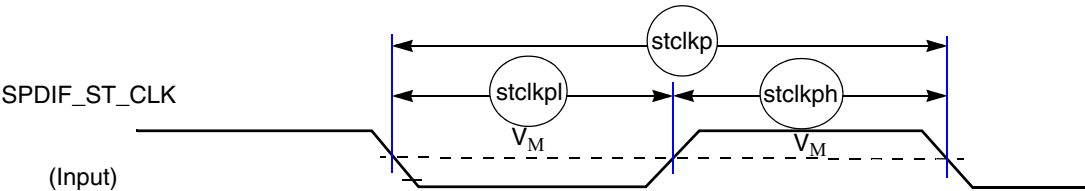


Figure 46. SPDIF\_ST\_CLK timing diagram

3.9.12 UART I/O configuration and timing parameters

3.9.12.1 UART RS-232 I/O configuration in different modes

The i.MX 8M Nano UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 68 shows the UART I/O configuration based on the enabled mode.

Table 68. UART I/O configuration vs. mode

| Port          | DTE Mode  |                             | DCE Mode  |                             |
|---------------|-----------|-----------------------------|-----------|-----------------------------|
|               | Direction | Description                 | Direction | Description                 |
| UARTx_RTS_B   | Output    | UARTx_RTS_B from DTE to DCE | Input     | UARTx_RTS_B from DTE to DCE |
| UARTx_CTS_B   | Input     | UARTx_CTS_B from DCE to DTE | Output    | UARTx_CTS_B from DCE to DTE |
| UARTx_TX_DATA | Input     | Serial data from DCE to DTE | Output    | Serial data from DCE to DTE |
| UARTx_RX_DATA | Output    | Serial data from DTE to DCE | Input     | Serial data from DTE to DCE |

3.9.12.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.



### 3.9.12.2.1 UART transmitter

Figure 47 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 69 lists the UART RS-232 Serial mode transmit timing characteristics.

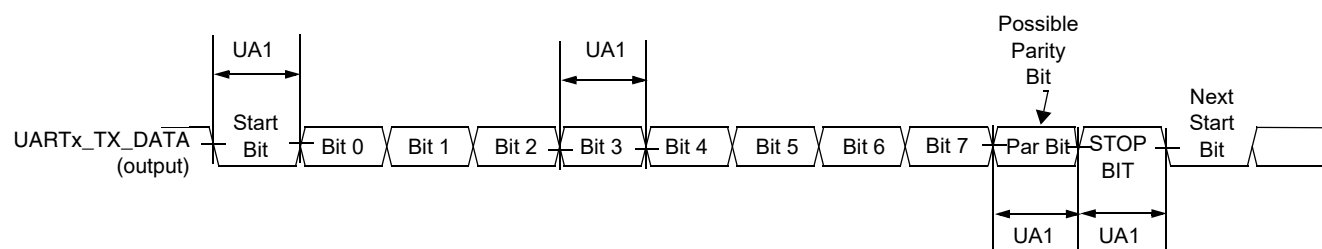


Figure 47. UART RS-232 Serial mode transmit timing diagram

Table 69. RS-232 Serial mode transmit timing parameters

| ID  | Parameter         | Symbol     | Min                                   | Max                               | Unit |
|-----|-------------------|------------|---------------------------------------|-----------------------------------|------|
| UA1 | Transmit Bit Time | $t_{Tbit}$ | $1/F_{baud\_rate}^1 - T_{ref\_clk}^2$ | $1/F_{baud\_rate} + T_{ref\_clk}$ | —    |

<sup>1</sup>  $F_{baud\_rate}$ : Baud rate frequency. The maximum baud rate the UART can support is  $(ipg\_perclk \text{ frequency})/16$ .

<sup>2</sup>  $T_{ref\_clk}$ : The period of UART reference clock  $ref\_clk$  ( $ipg\_perclk$  after RFDIV divider).

### 3.9.12.2.2 UART receiver

Figure 48 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 70 lists Serial mode receive timing characteristics.

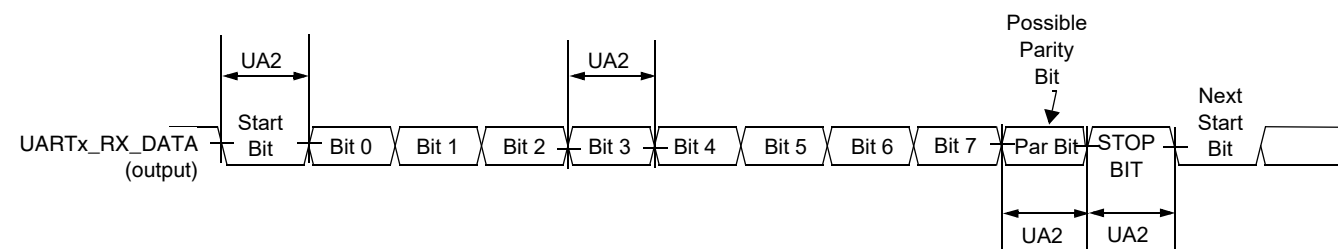


Figure 48. UART RS-232 Serial mode receive timing diagram

Table 70. RS-232 Serial mode receive timing parameters

| ID  | Parameter                     | Symbol     | Min                                                 | Max                                               | Unit |
|-----|-------------------------------|------------|-----------------------------------------------------|---------------------------------------------------|------|
| UA2 | Receive Bit Time <sup>1</sup> | $t_{Rbit}$ | $1/F_{baud\_rate}^2 - 1/(16 \times F_{baud\_rate})$ | $1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$ | —    |

<sup>1</sup> The UART receiver can tolerate  $1/(16 \times F_{baud\_rate})$  tolerance in each bit. But accumulation tolerance in one frame must not exceed  $3/(16 \times F_{baud\_rate})$ .

<sup>2</sup>  $F_{baud\_rate}$ : Baud rate frequency. The maximum baud rate the UART can support is  $(ipg\_perclk \text{ frequency})/16$ .

### 3.9.13 USB PHY parameters

This section describes the USB-OTG PHY parameters.

#### 3.9.13.1 Pad/Package/Board connections

The USB1\_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

The USB1\_VBUS pin must be isolated by an external 30 K $\Omega$  1% precision resistor.

The USB 2.0 PHY uses USB1\_TXRTUNE and an external resistor to calibrate the USB1\_DP/DN 45  $\Omega$  source impedance. The external resistor value is 200  $\Omega$  1% precision on USB1\_TXRTUNE pad to ground.

#### 3.9.13.2 USB PHY worst power consumption

Table 71 shows the USB 2.0 PHY worst power dissipation.

**Table 71. USB 2.0 PHY worst power dissipation**

| Mode    | VDD_USB_0P8 |    | VDD_USB_3P3 |    | VDD_USB_1P8 |    | Total Power |    |
|---------|-------------|----|-------------|----|-------------|----|-------------|----|
| HS TX   | 8.286       | mA | 4.63        | mA | 23.409      | mA | 70.448      | mW |
| FS TX   | 6.767       |    | 12.52       |    | 5.968       |    | 63.22       |    |
| LS TX   | 7.001       |    | 13.58       |    | 6.224       |    | 67.779      |    |
| Suspend | 0.752       |    | 0.164       |    | 0.106       |    | 1.465       |    |
| Sleep   | 0.761       |    | 0.163       |    | 0.106       |    | 1.472       |    |

## 4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

### 4.1 Boot mode configuration pins

Table 72 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT\_FUSE\_SEL fuse. The boot option pins are in effect when BT\_FUSE\_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the “System Boot, Fusemap, and eFuse” chapter in the *i.MX 8M Nano Applications Processor Reference Manual* (IMX8MNRM).

**Table 72. Fuses and associated pins used for boot**

| Interface  | IP instance | Allocated pads during boot | Comment             |
|------------|-------------|----------------------------|---------------------|
| BOOT_MODE0 | Input       | ccmsrcgpcmix.BOOT_MODE[0]  | Boot mode selection |
| BOOT_MODE1 | Input       | ccmsrcgpcmix.BOOT_MODE[1]  |                     |
| BOOT_MODE2 | Input       | ccmsrcgpcmix.BOOT_MODE[2]  |                     |
| BOOT_MODE3 | Input       | ccmsrcgpcmix.BOOT_MODE[3]  |                     |

### 4.2 Boot device interface allocation

Table 73 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

**Table 73. Interface allocation during boot**

| Interface  | IP Instance | Allocated Pads During Boot                                                                                                                                                                      | Comment                                                              |
|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|
| SPI        | ECSPI-1     | ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0                                                                                                                                               | The chip-select pin used depends on the fuse “CS select (SPI only)”. |
| SPI        | ECSPI-2     | ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0                                                                                                                                               | The chip-select pin used depends on the fuse “CS select (SPI only)”. |
| SPI        | ECSPI-3     | UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD                                                                                                                                                      | The chip-select pin used depends on the fuse “CS select (SPI only)”. |
| NAND Flash | GPMI        | NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B | 8-bit, only CS0 is supported.                                        |

**Table 73. Interface allocation during boot (continued)**

| Interface | IP Instance | Allocated Pads During Boot                                                                                                                                                                      | Comment           |
|-----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| SD/MMC    | USDHC-1     | GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7                           | 1, 4, or 8-bit    |
| SD/MMC    | USDHC-2     | GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3                                                                           | 1 or 4-bit        |
| SD/MMC    | USDHC-3     | NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B                       | 1, 4, or 8-bit    |
| FlexSPI   | FlexSPI     | NAND_ALE, NAND_CE0_B, NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B | For FlexSPI flash |
| USB       | USB_OTG PHY | Dedicated USB pins                                                                                                                                                                              | —                 |

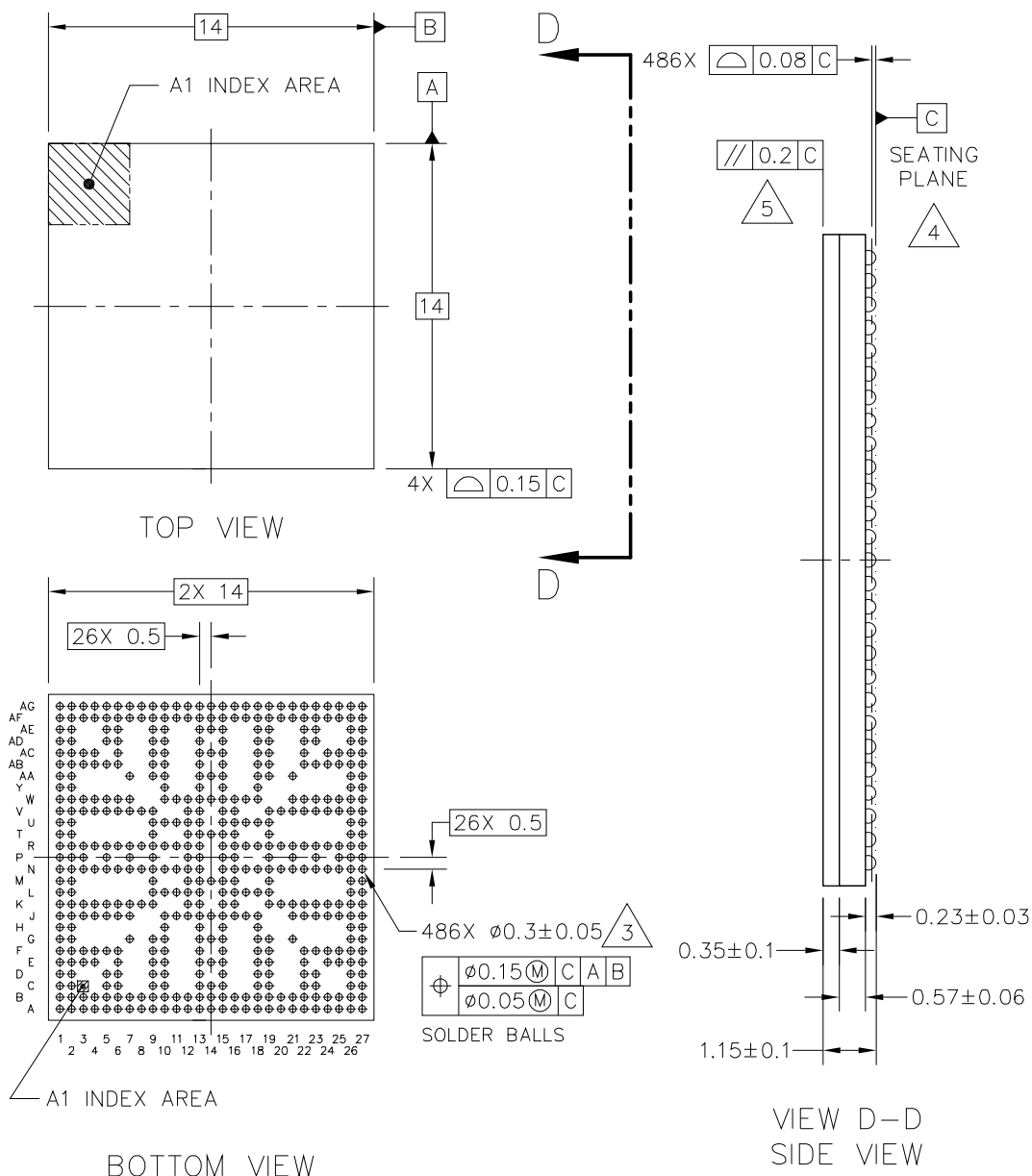
## 5 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

### 5.1 14 x 14 mm package information

#### 5.1.1 14 x 14 mm, 0.5 mm pitch, ball matrix

Figure 49 shows the top, bottom, and side views of the  $14 \times 14$  mm FCBGA package.



|                                                                              |                                 |                            |
|------------------------------------------------------------------------------|---------------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V.<br>ALL RIGHTS RESERVED                             | MECHANICAL OUTLINE              | PRINT VERSION NOT TO SCALE |
| TITLE: FCPBGA, MOLDED ARRAY,<br>14 X 14 X 1.15 PKG,<br>0.5 MM PITCH, 486 I/O | DOCUMENT NO: 98ASA01200D REV: B |                            |
|                                                                              | STANDARD: NON-JEDEC             |                            |
|                                                                              | SOT1967-1                       | 02 AUG 2018                |

Figure 49. 14 X 14 MM BGA, case x package top, bottom, and side views

## 5.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 74 shows supplies contact assignments for the 14 x 14 mm package.

**Table 74. i.MX 8M Nano 14 x 14 mm supplies contact assignments**

| Supply Rail Name | Ball(s) Position(s)                                                  | Remark                     |
|------------------|----------------------------------------------------------------------|----------------------------|
| NVCC_CLK         | M19                                                                  | Supply for CLK interface   |
| NVCC_DRAM        | P7, K8, N8, R8, V8, K9, L9, M9, N9, R9, T9, U9, V9                   | Supply for DRAM interface  |
| NVCC_ECSPi       | H10                                                                  | Supply for ECSPi interface |
| NVCC_ENET        | W22                                                                  | Supply for ENET interface  |
| NVCC_GPIO1       | W12                                                                  | Supply for GPIO1 interface |
| NVCC_I2C         | J11                                                                  | Supply for I2C interface   |
| NVCC_JTAG        | L19                                                                  | Supply for JTAG interface  |
| NVCC_NAND        | U19                                                                  | Supply for NAND interface  |
| NVCC_SAI2        | V19                                                                  | Supply for SAI interface   |
| NVCC_SAI3        | Y10                                                                  | Supply for SAI interface   |
| NVCC_SAI5        | W17                                                                  | Supply for SAI interface   |
| NVCC_SD1         | V20                                                                  | Supply for SD interface    |
| NVCC_SD2         | V22                                                                  | Supply for SD interface    |
| NVCC_SNVs_1P8    | J22                                                                  | Supply for SNVs interface  |
| NVCC_UART        | J12                                                                  | Supply for UART interface  |
| PVCC0_1P8        | AB13                                                                 | Digital IO pre-drive       |
| PVCC1_1P8        | T19                                                                  | Digital IO pre-drive       |
| PVCC2_1P8        | J13                                                                  | Digital IO pre-drive       |
| VDD_24M_XTAL_1P8 | N19                                                                  | Supply for XTAL            |
| VDD_ANA_0P8      | L17, N17                                                             | Supply for Analog logic    |
| VDD_ANA0_1P8     | AA14, Y15                                                            | Supply for Analog logic    |
| VDD_ANA1_1P8     | P19, N20                                                             | Supply for Analog logic    |
| VDD_ARM          | R13, T13, U13, V13, W13, T14, W14, R15, T15, U15, V15, W15, V16, W16 | Supply for ARM             |
| VDD_ARM_PLL_0P8  | P16                                                                  | Supply for ARM PLL         |
| VDD_ARM_PLL_1P8  | R19                                                                  | Supply for ARM PLL         |
| VDD_DRAM         | J10, L10, N10, R10, U10, W10                                         | Supply for DRAM module     |
| VDD_DRAM_PLL_0P8 | P9                                                                   | Supply for DRAM PLL        |
| VDD_DRAM_PLL_1P8 | P5                                                                   | Supply for DRAM PLL        |

Table 74. i.MX 8M Nano 14 x 14 mm supplies contact assignments (continued)

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                       |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| VDD_GPU      | R11, U11, W11, P12, V12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Supply for GPU        |
| VDD_MIPI_0P8 | J14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for MIPI PHY   |
| VDD_MIPI_1P2 | J15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for MIPI PHY   |
| VDD_MIPI_1P8 | H13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for MIPI PHY   |
| VDD_SNVS_0P8 | K22                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for SNVS logic |
| VDD_SOC      | N13, K15, L15, M15, N15, K16, R17, U17, L18, N18, R18, U18                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Supply for SOC logic  |
| VDD_USB_0P8  | J17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for USB PHY    |
| VDD_USB_1P8  | H15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for USB PHY    |
| VDD_USB_3P3  | K19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Supply for USB PHY    |
| VSS          | A1, AG1, C2, H2, Y2, AE2, B3, E3, F3, J3, K3, N3, P3, R3, V3, W3, AB3, AC3, AF3, C5, AE5, C6, AE6, G7, J7, K7, N7, R7, V7, W7, AA7, C9, G9, AA9, AE9, C10, G10, AA10, AE10, L12, M12, N12, R12, T12, U12, C13, G13, P13, Y13, AA13, AE13, C14, AE14, C15, G15, P15, AA15, AE15, L16, M16, N16, R16, T16, U16, C18, G18, H18, Y18, AA18, AE18, C19, G19, AA19, AE19, K20, R20, G21, J21, K21, N21, P21, R21, V21, W21, AA21, C22, AE22, C23, AE23, E25, F25, J25, K25, N25, P25, R25, V25, W25, AB25, AC25, B26, A27, AG27 | —                     |

Table 75 shows an alpha-sorted list of functional contact assignments for the 14 x 14 mm package.

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments

| Ball name  | Ball | Power group | Ball type | Reset condition |                           |                          |
|------------|------|-------------|-----------|-----------------|---------------------------|--------------------------|
|            |      |             |           | Default mode    | Default function          | Input/Output status      |
| 24M_XTALI  | B27  | NVCC_CLK    | ANALOG    | —               | —                         | Input                    |
| 24M_XTALO  | C26  | NVCC_CLK    | ANALOG    | —               | —                         | Output                   |
| BOOT_MODE0 | G26  | NVCC_JTAG   | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[0] | Input with PD            |
| BOOT_MODE1 | G27  | NVCC_JTAG   | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[1] | Input with PD            |
| BOOT_MODE2 | C27  | NVCC_JTAG   | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[2] | Input with PD            |
| BOOT_MODE3 | D26  | NVCC_JTAG   | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[3] | Input with PD            |
| CLKIN1     | H27  | NVCC_CLK    | GPIO      | —               | —                         | Input without PU/PD      |
| CLKIN2     | J27  | NVCC_CLK    | GPIO      | —               | —                         | Input without PU/PD      |
| CLKOUT1    | H26  | NVCC_CLK    | GPIO      | —               | —                         | Output low without PU/PD |



Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition |                  |                          |
|-----------|------|-------------|-----------|-----------------|------------------|--------------------------|
|           |      |             |           | Default mode    | Default function | Input/Output status      |
| CLKOUT2   | J26  | NVCC_CLK    | GPIO      | —               | —                | Output low without PU/PD |
| DRAM_AC00 | F4   | NVCC_DRAM   | DDR       | —               | —                | Output low               |
| DRAM_AC01 | F5   | NVCC_DRAM   | DDR       | —               | —                | Output low               |
| DRAM_AC02 | K4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC03 | J4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC04 | L2   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC05 | L1   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC06 | F6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC07 | J5   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC08 | J6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC09 | K6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC10 | E4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC11 | D5   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC12 | N4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC13 | N5   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC14 | K5   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC15 | N6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC16 | M1   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC17 | M2   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC19 | N2   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC20 | AB4  | NVCC_DRAM   | DDR       | —               | —                | Output low               |
| DRAM_AC21 | AB5  | NVCC_DRAM   | DDR       | —               | —                | Output low               |
| DRAM_AC22 | W4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC23 | V4   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC24 | U2   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC25 | U1   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC26 | N1   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC27 | R6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |
| DRAM_AC28 | W6   | NVCC_DRAM   | DDR       | —               | —                | Input                    |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name    | Ball | Power group | Ball type | Reset condition |                  |                     |
|--------------|------|-------------|-----------|-----------------|------------------|---------------------|
|              |      |             |           | Default mode    | Default function | Input/Output status |
| DRAM_AC29    | V6   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC30    | AC4  | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC31    | AD5  | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC32    | R4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC33    | R5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC34    | T1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC35    | T2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC36    | V5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC37    | W5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC38    | AB6  | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_ALERT_N | R2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DM0     | A4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DM1     | F1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ00    | A5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ01    | B5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ02    | D2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ03    | D1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ04    | C1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ05    | B1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ06    | A3   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ07    | B4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ08    | F2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ09    | G2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ10    | J1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ11    | J2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ12    | K2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ13    | K1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ14    | E1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ15    | E2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQS0_N  | B2   | NVCC_DRAM   | —         | —               | —                | Input               |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name    | Ball | Power group | Ball type | Reset condition |                  |                     |
|--------------|------|-------------|-----------|-----------------|------------------|---------------------|
|              |      |             |           | Default mode    | Default function | Input/Output status |
| DRAM_DQS0_P  | A2   | NVCC_DRAM   | DDRCLK    | —               | —                | Input               |
| DRAM_DQS1_N  | H1   | NVCC_DRAM   | —         | —               | —                | Input               |
| DRAM_DQS1_P  | G1   | NVCC_DRAM   | DDRCLK    | —               | —                | Input               |
| DRAM_RESET_N | R1   | NVCC_DRAM   | DDR       | —               | —                | Output low          |
| DRAM_VREF    | P1   | NVCC_DRAM   | DDR       | —               | —                | —                   |
| DRAM_ZN      | P2   | NVCC_DRAM   | DDR       | —               | —                | —                   |
| ECSPI1_MISO  | A7   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[8]      | Input with PD       |
| ECSPI1_MOSI  | B7   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[7]      | Input with PD       |
| ECSPI1_SCLK  | D6   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[6]      | Input with PD       |
| ECSPI1_SS0   | B6   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[9]      | Input with PD       |
| ECSPI2_MISO  | A8   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[12]     | Input with PD       |
| ECSPI2_MOSI  | B8   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[11]     | Input with PD       |
| ECSPI2_SCLK  | E6   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[10]     | Input with PD       |
| ECSPI2_SS0   | A6   | NVCC_ECSPI  | GPIO      | ALT5            | GPIO5.IO[13]     | Input with PD       |
| ENET_MDC     | AC27 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[16]     | Input with PD       |
| ENET_MDIO    | AB27 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[17]     | Input with PD       |
| ENET_RD0     | AE27 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[26]     | Input with PD       |
| ENET_RD1     | AD27 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[27]     | Input with PD       |
| ENET_RD2     | AD26 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[28]     | Input with PD       |
| ENET_RD3     | AC26 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[29]     | Input with PD       |
| ENET_RXC     | AE26 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[25]     | Input with PD       |
| ENET_RX_CTL  | AF27 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[24]     | Input with PD       |
| ENET_TD0     | AG26 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[21]     | Input with PD       |
| ENET_TD1     | AF26 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[20]     | Input with PD       |
| ENET_TD2     | AG25 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[19]     | Input with PD       |
| ENET_TD3     | AF25 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[18]     | Input with PD       |
| ENET_TXC     | AG24 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[23]     | Input with PD       |
| ENET_TX_CTL  | AF24 | NVCC_ENET   | GPIO      | ALT5            | GPIO1.IO[22]     | Input with PD       |
| GPIO1_IO00   | AG14 | NVCC_GPIO1  | GPIO      | ALT6            | GPIO1.IO[0]      | Input with PD       |
| GPIO1_IO01   | AF14 | NVCC_GPIO1  | GPIO      | ALT6            | GPIO1.IO[1]      | 1                   |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name             | Ball | Power group  | Ball type | Reset condition |                   |                     |
|-----------------------|------|--------------|-----------|-----------------|-------------------|---------------------|
|                       |      |              |           | Default mode    | Default function  | Input/Output status |
| GPIO1_IO02            | AG13 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[2]       | Input with PU       |
| GPIO1_IO03            | AF13 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[3]       | Input with PD       |
| GPIO1_IO04            | AG12 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[4]       | Input with PD       |
| GPIO1_IO05            | AF12 | NVCC_GPIO1   | GPIO      | ALT6            | GPIO1.IO[5]       | 1                   |
| GPIO1_IO06            | AG11 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[6]       | Input with PD       |
| GPIO1_IO07            | AF11 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[7]       | Input with PD       |
| GPIO1_IO08            | AG10 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[8]       | Input with PD       |
| GPIO1_IO09            | AF10 | NVCC_GPIO1   | GPIO      | ALT1            | GPIO1.IO[9]       | Input with PD       |
| GPIO1_IO10            | AD10 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[10]      | Input with PD       |
| GPIO1_IO11            | AC10 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[11]      | Input with PD       |
| GPIO1_IO12            | AB10 | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[12]      | Input with PD       |
| GPIO1_IO13            | AD9  | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[13]      | Input with PD       |
| GPIO1_IO14            | AC9  | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[14]      | Input with PD       |
| GPIO1_IO15            | AB9  | NVCC_GPIO1   | GPIO      | ALT0            | GPIO1.IO[15]      | Input with PD       |
| I2C1_SCL              | E9   | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[14]      | Input with PD       |
| I2C1_SDA              | F9   | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[15]      | Input with PD       |
| I2C2_SCL              | D10  | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[16]      | Input with PD       |
| I2C2_SDA              | D9   | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[17]      | Input with PD       |
| I2C3_SCL              | E10  | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[18]      | Input with PD       |
| I2C3_SDA              | F10  | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[19]      | Input with PD       |
| I2C4_SCL              | D13  | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[20]      | Input with PD       |
| I2C4_SDA              | E13  | NVCC_I2C     | GPIO      | ALT5            | GPIO5.IO[21]      | Input with PD       |
| JTAG_MOD              | D27  | NVCC_JTAG    | GPIO      | ALT0            | cjtag_wrapper.MOD | Input with PD       |
| JTAG_TCK              | F26  | NVCC_JTAG    | GPIO      | ALT0            | cjtag_wrapper.TCK | Input with PU       |
| JTAG_TDI              | E27  | NVCC_JTAG    | GPIO      | ALT0            | cjtag_wrapper.TDI | Input with PU       |
| JTAG_TDO              | E26  | NVCC_JTAG    | GPIO      | ALT0            | cjtag_wrapper.TDO | Input with PU       |
| JTAG_TMS <sup>2</sup> | F27  | NVCC_JTAG    | GPIO      | ALT0            | cjtag_wrapper.TMS | Input with PU       |
| MIPI_CSI_CLK_N        | A16  | VDD_MIPI_1P8 | PHY       | —               | —                 | Input               |
| MIPI_CSI_CLK_P        | B16  | VDD_MIPI_1P8 | PHY       | —               | —                 | Input               |
| MIPI_CSI_D0_N         | A14  | VDD_MIPI_1P8 | PHY       | —               | —                 | Input               |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name      | Ball | Power group   | Ball type | Reset condition |                  |                     |
|----------------|------|---------------|-----------|-----------------|------------------|---------------------|
|                |      |               |           | Default mode    | Default function | Input/Output status |
| MIPI_CSI_D0_P  | B14  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D1_N  | A15  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D1_P  | B15  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D2_N  | A17  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D2_P  | B17  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D3_N  | A18  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_CSI_D3_P  | B18  | VDD_MIPI_1P8  | PHY       | —               | —                | Input               |
| MIPI_DSI_CLK_N | A11  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_CLK_P | B11  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D0_N  | A9   | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D0_P  | B9   | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D1_N  | A10  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D1_P  | B10  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D2_N  | A12  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D2_P  | B12  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D3_N  | A13  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_DSI_D3_P  | B13  | VDD_MIPI_1P8  | PHY       | —               | —                | Output low          |
| MIPI_VREG_CAP  | D15  | 0.35 - 0.45 V | PHY       | —               | —                | Output              |
| NAND_ALE       | N22  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[0]      | Input with PD       |
| NAND_CE0_B     | N24  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[1]      | Input with PD       |
| NAND_CE1_B     | P27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[2]      | Input with PD       |
| NAND_CE2_B     | M27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[3]      | Input with PD       |
| NAND_CE3_B     | L27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[4]      | Input with PD       |
| NAND_CLE       | K27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[5]      | Input with PD       |
| NAND_DATA00    | P23  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[6]      | Input with PD       |
| NAND_DATA01    | K24  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[7]      | Input with PD       |
| NAND_DATA02    | K23  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[8]      | Input with PD       |
| NAND_DATA03    | N23  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[9]      | Input with PD       |
| NAND_DATA04    | M26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[10]     | Input with PD       |
| NAND_DATA05    | L26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[11]     | Input with PD       |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name     | Ball | Power group   | Ball type | Reset condition |                            |                                |
|---------------|------|---------------|-----------|-----------------|----------------------------|--------------------------------|
|               |      |               |           | Default mode    | Default function           | Input/Output status            |
| NAND_DATA06   | K26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[12]               | Input with PD                  |
| NAND_DATA07   | N26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[13]               | Input with PD                  |
| NAND_DQS      | R22  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[14]               | Input with PD                  |
| NAND_RE_B     | N27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[15]               | Input with PD                  |
| NAND_READY_B  | P26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[16]               | Input with PD                  |
| NAND_WE_B     | R26  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[17]               | Input with PD                  |
| NAND_WP_B     | R27  | NVCC_NAND     | GPIO      | ALT5            | GPIO3.IO[18]               | Input with PD                  |
| ONOFF         | A25  | NVCC_SNVS_1P8 | GPIO      | ALT0            | snvsmix.ONOFF              | Input without PU/PD            |
| PMIC_ON_REQ   | A24  | NVCC_SNVS_1P8 | GPIO      | ALT0            | snvsmix.PMIC_ON_REQ        | Open-drain output high with PU |
| PMIC_STBY_REQ | E24  | NVCC_SNVS_1P8 | GPIO      | ALT0            | ccmsrcgpcmix.PMIC_STBY_REQ | Output low with PD             |
| POR_B         | B24  | NVCC_SNVS_1P8 | GPIO      | ALT0            | snvsmix.POR_B              | Input without PU/PD            |
| RTC_XTALI     | A26  | NVCC_SNVS_1P8 | ANALOG    | ALT0            | snvsmix.RTC                | Input                          |
| RTC_XTALO     | B25  | NVCC_SNVS_1P8 | ANALOG    | —               | —                          | Output, inverted of RTC_XTALI  |
| RTC_RESET_B   | F24  | NVCC_SNVS_1P8 | GPIO      | ALT0            | snvsmix.RTC_POR_B          | Input without PU/PD            |
| SAI2_MCLK     | AD19 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[27]               | Input with PD                  |
| SAI2_RXC      | AB22 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[22]               | Input with PD                  |
| SAI2_RXD0     | AC24 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[23]               | Input with PD                  |
| SAI2_RXFS     | AC19 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[21]               | Input with PD                  |
| SAI2_TXC      | AD22 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[25]               | Input with PD                  |
| SAI2_TXD0     | AC22 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[26]               | Input with PD                  |
| SAI2_TXFS     | AD23 | NVCC_SAI2     | GPIO      | ALT5            | GPIO4.IO[24]               | Input with PD                  |
| SAI3_MCLK     | AD6  | NVCC_SAI3     | GPIO      | ALT5            | GPIO5.IO[2]                | Input with PD                  |
| SAI3_RXC      | AG7  | NVCC_SAI3     | GPIO      | ALT5            | GPIO4.IO[29]               | Input with PD                  |
| SAI3_RXD      | AF7  | NVCC_SAI3     | GPIO      | ALT5            | GPIO4.IO[30]               | Input with PD                  |
| SAI3_RXFS     | AG8  | NVCC_SAI3     | GPIO      | ALT5            | GPIO4.IO[28]               | Input with PD                  |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name   | Ball | Power group | Ball type | Reset condition |                  |                     |
|-------------|------|-------------|-----------|-----------------|------------------|---------------------|
|             |      |             |           | Default mode    | Default function | Input/Output status |
| SAI3_TXC    | AG6  | NVCC_SAI3   | GPIO      | ALT5            | GPIO5.IO[0]      | Input with PD       |
| SAI3_TXD    | AF6  | NVCC_SAI3   | GPIO      | ALT5            | GPIO5.IO[1]      | Input with PD       |
| SAI3_TXFS   | AC6  | NVCC_SAI3   | GPIO      | ALT5            | GPIO4.IO[31]     | Input with PD       |
| SAI5_MCLK   | AD15 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[25]     | 3                   |
| SAI5_RXC    | AC15 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[20]     | Input with PD       |
| SAI5_RXD0   | AD18 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[21]     | Input with PD       |
| SAI5_RXD1   | AC14 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[22]     | Input with PD       |
| SAI5_RXD2   | AD13 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[23]     | Input with PD       |
| SAI5_RXD3   | AC13 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[24]     | Input with PD       |
| SAI5_RXFS   | AB15 | NVCC_SAI5   | GPIO      | ALT5            | GPIO3.IO[19]     | Input with PD       |
| SD1_CLK     | V26  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[0]      | Input with PD       |
| SD1_CMD     | V27  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[1]      | Input with PD       |
| SD1_DATA0   | Y27  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[2]      | Input with PD       |
| SD1_DATA1   | Y26  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[3]      | Input with PD       |
| SD1_DATA2   | T27  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[4]      | Input with PD       |
| SD1_DATA3   | T26  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[5]      | Input with PD       |
| SD1_DATA4   | U27  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[6]      | Input with PD       |
| SD1_DATA5   | U26  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[7]      | Input with PD       |
| SD1_DATA6   | W27  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[8]      | Input with PD       |
| SD1_DATA7   | W26  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[9]      | Input with PD       |
| SD1_RESET_B | R23  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[10]     | Input with PD       |
| SD1_STROBE  | R24  | NVCC_SD1    | GPIO      | ALT5            | GPIO2.IO[11]     | Input with PD       |
| SD2_CD_B    | AA26 | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[12]     | Input with PD       |
| SD2_CLK     | W23  | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[13]     | Input with PD       |
| SD2_CMD     | W24  | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[14]     | Input with PD       |
| SD2_DATA0   | AB23 | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[15]     | Input with PD       |
| SD2_DATA1   | AB24 | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[16]     | Input with PD       |
| SD2_DATA2   | V24  | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[17]     | Input with PD       |
| SD2_DATA3   | V23  | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[18]     | Input with PD       |
| SD2_RESET_B | AB26 | NVCC_SD2    | GPIO      | ALT5            | GPIO2.IO[19]     | Input with PD       |

Table 75. i.MX 8M Nano 14 x 14 mm functional contact assignments (continued)

| Ball name        | Ball | Power group  | Ball type | Reset condition |                  |                     |
|------------------|------|--------------|-----------|-----------------|------------------|---------------------|
|                  |      |              |           | Default mode    | Default function | Input/Output status |
| SD2_WP           | AA27 | NVCC_SD2     | GPIO      | ALT5            | GPIO2.IO[20]     | Input with PD       |
| SPDIF_EXT_CLK    | AF8  | NVCC_SAI3    | GPIO      | ALT5            | GPIO5.IO[5]      | Input with PD       |
| SPDIF_RX         | AG9  | NVCC_SAI3    | GPIO      | ALT5            | GPIO5.IO[4]      | Input with PD       |
| SPDIF_TX         | AF9  | NVCC_SAI3    | GPIO      | ALT5            | GPIO5.IO[3]      | Input with PD       |
| TSensor_TEST_OUT | J23  | VDD_ANA1_1P8 | ANALOG    | —               | —                | Output low          |
| TSensor_RES_EXT  | J24  | VDD_ANA1_1P8 | ANALOG    | —               | —                | —                   |
| UART1_RXD        | E14  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[22]     | Input with PD       |
| UART1_TXD        | F13  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[23]     | Input with PD       |
| UART2_RXD        | F15  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[24]     | Input with PD       |
| UART2_TXD        | E15  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[25]     | Input with PD       |
| UART3_RXD        | E18  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[26]     | Input with PD       |
| UART3_TXD        | D18  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[27]     | Input with PD       |
| UART4_RXD        | F19  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[28]     | Input with PD       |
| UART4_TXD        | F18  | NVCC_UART    | GPIO      | ALT5            | GPIO5.IO[29]     | Input with PD       |
| USB1_DN          | A22  | VDD_USB_3P3  | PHY       | —               | —                | Input               |
| USB1_DP          | B22  | VDD_USB_3P3  | PHY       | —               | —                | Input               |
| USB1_ID          | D22  | VDD_USB_1P8  | PHY       | —               | —                | Input               |
| USB1_TXRTUNE     | E19  | VDD_USB_1P8  | PHY       | —               | —                | —                   |
| USB1_VBUS        | F22  | VDD_USB_3P3  | PHY       | —               | —                | —                   |

<sup>1</sup> During reset: output high without PU/PD; After reset: input with PU

<sup>2</sup> Mandatory requirement: JTAG\_TMS pin must be connected with a 50 ohm serial resistor near the component.

<sup>3</sup> During reset: input without PU/PD; After reset: input with PD

### 5.1.3 i.MX 8M Nano 14 x 14 mm 0.5 mm pitch ball map

Table 76 shows the i.MX 8M Nano 14 x 14 mm 0.5 mm pitch ball map.



Table 76. 14 x 14 mm, 0.5 mm pitch ball map

| G           | F           | E             | D             | C          | B              | A              |    |
|-------------|-------------|---------------|---------------|------------|----------------|----------------|----|
| DRAM_DQS1_P | DRAM_DM1    | DRAM_DQ14     | DRAM_DQ03     | DRAM_DQ04  | DRAM_DQ05      | VSS            | 1  |
| DRAM_DQ09   | DRAM_DQ08   | DRAM_DQ15     | DRAM_DQ02     | VSS        | DRAM_DQS0_N    | DRAM_DQS0_P    | 2  |
|             | VSS         | VSS           |               |            | VSS            | DRAM_DQ06      | 3  |
|             | DRAM_AC00   | DRAM_AC10     |               |            | DRAM_DQ07      | DRAM_DM0       | 4  |
|             | DRAM_AC01   |               | DRAM_AC11     | VSS        | DRAM_DQ01      | DRAM_DQ00      | 5  |
|             | DRAM_AC06   | ECSP12_SCLK   | ECSP11_SCLK   | VSS        | ECSP11_SS0     | ECSP12_SS0     | 6  |
| VSS         |             |               |               |            | ECSP11_MOSI    | ECSP11_MISO    | 7  |
|             |             |               |               |            | ECSP12_MOSI    | ECSP12_MISO    | 8  |
| VSS         | I2C1_SDA    | I2C1_SCL      | I2C2_SDA      | VSS        | MIPI_DSI_D0_P  | MIPI_DSI_D0_N  | 9  |
| VSS         | I2C3_SDA    | I2C3_SCL      | I2C2_SCL      | VSS        | MIPI_DSI_D1_P  | MIPI_DSI_D1_N  | 10 |
|             |             |               |               |            | MIPI_DSI_CLK_P | MIPI_DSI_CLK_N | 11 |
|             |             |               |               |            | MIPI_DSI_D2_P  | MIPI_DSI_D2_N  | 12 |
| VSS         | UART1_TXD   | I2C4_SDA      | I2C4_SCL      | VSS        | MIPI_DSI_D3_P  | MIPI_DSI_D3_N  | 13 |
|             |             | UART1_RXD     |               | VSS        | MIPI_CSI_D0_P  | MIPI_CSI_D0_N  | 14 |
| VSS         | UART2_RXD   | UART2_TXD     | MIPI_VREG_CAP | VSS        | MIPI_CSI_D1_P  | MIPI_CSI_D1_N  | 15 |
|             |             |               |               |            | MIPI_CSI_CLK_P | MIPI_CSI_CLK_N | 16 |
|             |             |               |               |            | MIPI_CSI_D2_P  | MIPI_CSI_D2_N  | 17 |
| VSS         | UART4_TXD   | UART3_RXD     | UART3_TXD     | VSS        | MIPI_CSI_D3_P  | MIPI_CSI_D3_N  | 18 |
| VSS         | UART4_RXD   | USB1_TXRTUNE  |               | VSS        |                |                | 19 |
|             |             |               |               |            |                |                | 20 |
| VSS         |             |               |               |            |                |                | 21 |
|             | USB1_VBUS   |               | USB1_ID       | VSS        | USB1_DP        | USB1_DN        | 22 |
|             |             |               |               | VSS        |                |                | 23 |
|             | RTC_RESET_B | PMIC_STBY_REQ |               |            | POR_B          | PMIC_ON_REQ    | 24 |
|             | VSS         | VSS           |               |            | RTC_XTALO      | ONOFF          | 25 |
| BOOT_MODE0  | JTAG_TCK    | JTAG_TDO      | BOOT_MODE3    | 24M_XTALO  | VSS            | RTC_XTALI      | 26 |
| BOOT_MODE1  | JTAG_TMS    | JTAG_TDI      | JTAG_MOD      | BOOT_MODE2 | 24M_XTALI      | VSS            | 27 |

Table 76. 14 x 14 mm, 0.5 mm pitch ball map (continued)

| P                | N                | M           | L           | K             | J                | H            |    |
|------------------|------------------|-------------|-------------|---------------|------------------|--------------|----|
| DRAM_VREF        | DRAM_AC26        | DRAM_AC16   | DRAM_AC05   | DRAM_DQ13     | DRAM_DQ10        | DRAM_DQS1_N  | 1  |
| DRAM_ZN          | DRAM_AC19        | DRAM_AC17   | DRAM_AC04   | DRAM_DQ12     | DRAM_DQ11        | VSS          | 2  |
| VSS              | VSS              |             |             | VSS           | VSS              |              | 3  |
|                  | DRAM_AC12        |             |             | DRAM_AC02     | DRAM_AC03        |              | 4  |
| VDD_DRAM_PLL_1P8 | DRAM_AC13        |             |             | DRAM_AC14     | DRAM_AC07        |              | 5  |
|                  | DRAM_AC15        |             |             | DRAM_AC09     | DRAM_AC08        |              | 6  |
| NVCC_DRAM        | VSS              |             |             | VSS           | VSS              |              | 7  |
|                  | NVCC_DRAM        |             |             | NVCC_DRAM     |                  |              | 8  |
| VDD_DRAM_PLL_0P8 | NVCC_DRAM        | NVCC_DRAM   | NVCC_DRAM   | NVCC_DRAM     |                  |              | 9  |
|                  | VDD_DRAM         |             | VDD_DRAM    |               | VDD_DRAM         | NVCC_ECSP1   | 10 |
|                  |                  |             |             |               | NVCC_I2C         |              | 11 |
| VDD_GPU          | VSS              | VSS         | VSS         |               | NVCC_UART        |              | 12 |
| VSS              | VDD_SOC          |             |             |               | PVCC2_1P8        | VDD_MIPI_1P8 | 13 |
|                  |                  |             |             |               | VDD_MIPI_0P8     |              | 14 |
| VSS              | VDD_SOC          | VDD_SOC     | VDD_SOC     | VDD_SOC       | VDD_MIPI_1P2     | VDD_USB_1P8  | 15 |
| VDD_ARM_PLL_0P8  | VSS              | VSS         | VSS         | VDD_SOC       |                  |              | 16 |
|                  | VDD_ANA_0P8      |             | VDD_ANA_0P8 |               | VDD_USB_0P8      |              | 17 |
|                  | VDD_SOC          |             | VDD_SOC     |               |                  | VSS          | 18 |
| VDD_ANA1_1P8     | VDD_24M_XTAL_1P8 | NVCC_CLK    | NVCC_JTAG   | VDD_USB_3P3   |                  |              | 19 |
|                  | VDD_ANA1_1P8     |             |             | VSS           |                  |              | 20 |
| VSS              | VSS              |             |             | VSS           | VSS              |              | 21 |
|                  | NAND_ALE         |             |             | VDD_SNVIS_0P8 | NVCC_SNVIS_1P8   |              | 22 |
| NAND_DATA00      | NAND_DATA03      |             |             | NAND_DATA02   | TSensor_TEST_OUT |              | 23 |
|                  | NAND_CE0_B       |             |             | NAND_DATA01   | TSensor_RES_EXT  |              | 24 |
| VSS              | VSS              |             |             | VSS           | VSS              |              | 25 |
| NAND_READY_B     | NAND_DATA07      | NAND_DATA04 | NAND_DATA05 | NAND_DATA06   | CLKOUT2          | CLKOUT1      | 26 |
| NAND_CE1_B       | NAND_RE_B        | NAND_CE2_B  | NAND_CE3_B  | NAND_CLE      | CLKIN2           | CLKIN1       | 27 |

Table 76. 14 x 14 mm, 0.5 mm pitch ball map (continued)

| AB          | AA           | Y            | W          | V         | U         | T         | R               |    |
|-------------|--------------|--------------|------------|-----------|-----------|-----------|-----------------|----|
|             |              |              |            |           | DRAM_AC25 | DRAM_AC34 | DRAM_RESET_N    | 1  |
|             |              | VSS          |            |           | DRAM_AC24 | DRAM_AC35 | DRAM_ALERT_N    | 2  |
| VSS         |              |              | VSS        | VSS       |           |           | VSS             | 3  |
| DRAM_AC20   |              |              | DRAM_AC22  | DRAM_AC23 |           |           | DRAM_AC32       | 4  |
| DRAM_AC21   |              |              | DRAM_AC37  | DRAM_AC36 |           |           | DRAM_AC33       | 5  |
| DRAM_AC38   |              |              | DRAM_AC28  | DRAM_AC29 |           |           | DRAM_AC27       | 6  |
|             | VSS          |              | VSS        | VSS       |           |           | VSS             | 7  |
|             |              |              |            | NVCC_DRAM |           |           | NVCC_DRAM       | 8  |
| GPIO1_IO15  | VSS          |              |            | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM       | 9  |
| GPIO1_IO12  | VSS          | NVCC_SAI3    | VDD_DRAM   |           | VDD_DRAM  |           | VDD_DRAM        | 10 |
|             |              |              | VDD_GPU    |           | VDD_GPU   |           | VDD_GPU         | 11 |
|             |              |              | NVCC_GPIO1 | VDD_GPU   | VSS       | VSS       | VSS             | 12 |
| PVCC0_1P8   | VSS          | VSS          | VDD_ARM    | VDD_ARM   | VDD_ARM   | VDD_ARM   | VDD_ARM         | 13 |
|             | VDD_ANA0_1P8 |              | VDD_ARM    |           |           | VDD_ARM   |                 | 14 |
| SAI5_RXFS   | VSS          | VDD_ANA0_1P8 | VDD_ARM    | VDD_ARM   | VDD_ARM   | VDD_ARM   | VDD_ARM         | 15 |
|             |              |              | VDD_ARM    | VDD_ARM   | VSS       | VSS       | VSS             | 16 |
|             |              |              | NVCC_SAI5  |           | VDD_SOC   |           | VDD_SOC         | 17 |
|             | VSS          | VSS          |            |           | VDD_SOC   |           | VDD_SOC         | 18 |
|             | VSS          |              |            | NVCC_SAI2 | NVCC_NAND | PVCC1_1P8 | VDD_ARM_PLL_1P8 | 19 |
|             |              |              |            | NVCC_SD1  |           |           | VSS             | 20 |
|             | VSS          |              | VSS        | VSS       |           |           | VSS             | 21 |
| SAI2_RXC    |              |              | NVCC_ENET  | NVCC_SD2  |           |           | NAND_DQS        | 22 |
| SD2_DATA0   |              |              | SD2_CLK    | SD2_DATA3 |           |           | SD1_RESET_B     | 23 |
| SD2_DATA1   |              |              | SD2_CMD    | SD2_DATA2 |           |           | SD1_STROBE      | 24 |
| VSS         |              |              | VSS        | VSS       |           |           | VSS             | 25 |
| SD2_RESET_B | SD2_CD_B     | SD1_DATA1    | SD1_DATA7  | SD1_CLK   | SD1_DATA5 | SD1_DATA3 | NAND_WE_B       | 26 |
| ENET_MDIO   | SD2_WP       | SD1_DATA0    | SD1_DATA6  | SD1_CMD   | SD1_DATA4 | SD1_DATA2 | NAND_WP_B       | 27 |

Table 76. 14 x 14 mm, 0.5 mm pitch ball map (continued)

|            | 1             | 2   | 3  | 4  | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
|------------|---------------|-----|----|----|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| AG         | AF            | AE  | AD | AC |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VSS        |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               | VSS |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            | VSS           |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| SAI3_TXC   | SAI3_TXD      | VSS |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| SAI3_RXC   | SAI3_RXD      |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| SAI3_RXFS  | SPDIF_EXT_CLK |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| SPDIF_RX   | SPDIF_TX      |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GPIO1_IO08 | GPIO1_IO09    |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GPIO1_IO06 | GPIO1_IO07    |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GPIO1_IO04 | GPIO1_IO05    |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GPIO1_IO02 | GPIO1_IO03    |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GPIO1_IO00 | GPIO1_IO01    |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|            |               |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ENET_TXC   | ENET_TX_CTL   |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ENET_TD2   | ENET_TD3      |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ENET_TD0   | ENET_TD1      |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VSS        | ENET_RX_CTL   |     |    |    |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

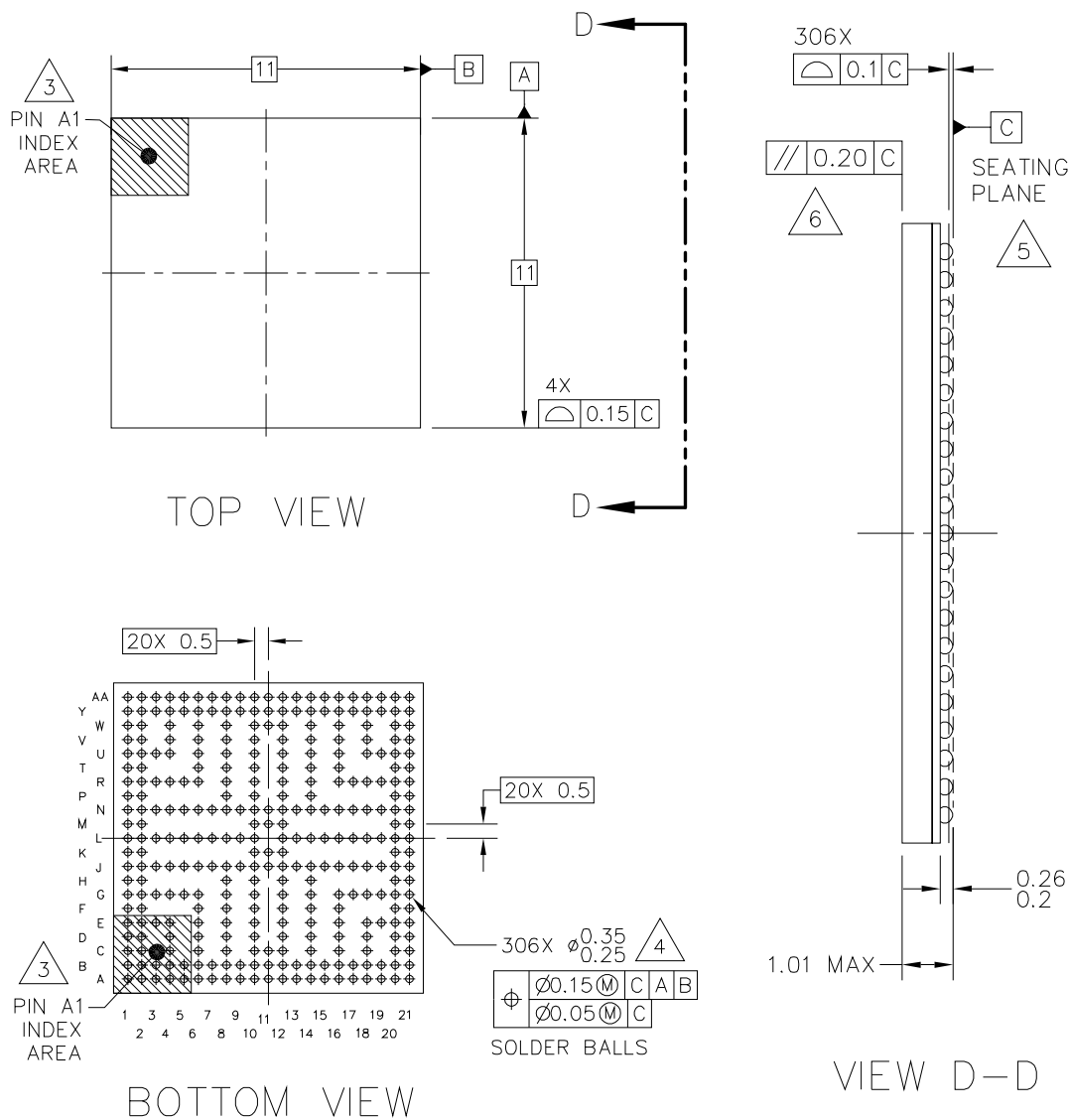
## 5.2 11 x 11 mm package information

### 5.2.1 11 x 11 mm, 0.5 mm pitch, ball matrix

Figure 50 shows the top, bottom, and side views of the  $11 \times 11$  mm FCBGA package.

FC-PBGA-306 I/O  
11 X 11 X 0.91 PKG, 0.5 PITCH, MOLDED ARRAY

SOT2064-1



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|--------------------------------------------------|------------------------|--------------------------------|----------------|-----------------|

**Figure 50. 11 X 11 MM BGA, case x package top, bottom, and side views**

## 5.2.2 11 x 11 mm supplies contact assignments and functional contact assignments

Table 77 shows supplies contact assignments for the 11 x 11 mm package.

**Table 77. i.MX 8M Nano 11 x 11 mm supplies contact assignments**

| Supply Rail Name           | Ball(s) Position(s)                                                                                                                                                                                                                         | Remark                                                   |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| NVCC_CLK_JTAG_PVCC_1P8     | L15                                                                                                                                                                                                                                         | Supply for CLK, JTAG interface and Digital I/O pre-drive |
| NVCC_DRAM                  | G6, J6, J7, L6, N6, N7, R6                                                                                                                                                                                                                  | Supply for DRAM interface                                |
| NVCC_ECSPi                 | G8                                                                                                                                                                                                                                          | Supply for ECSPi interface                               |
| NVCC_ENET_GPIO_SAI2        | R12                                                                                                                                                                                                                                         | Supply for ENET, GPIO1, and SAI2 interface               |
| NVCC_I2C_UART              | G10                                                                                                                                                                                                                                         | Supply for I2C and UART interface                        |
| NVCC_SAI3_SAI5             | R10                                                                                                                                                                                                                                         | Supply for SAI3 and SAI5 interface                       |
| NVCC_SD1_NAND              | N15                                                                                                                                                                                                                                         | Supply for SD1 and NAND interface                        |
| NVCC_SD2                   | R16                                                                                                                                                                                                                                         | Supply for SD interface                                  |
| NVCC_SNVS_1P8              | G14                                                                                                                                                                                                                                         | Supply for SNVS interface                                |
| VDD_ANA1_XTAL_MIPI_USB_1P8 | G12                                                                                                                                                                                                                                         | Supply for XTAL, Analog logic, MIPI, and USB 1.8 V       |
| VDD_ANA0_ARM_PLL_1P8       | R14                                                                                                                                                                                                                                         | Supply for Analog logic and ARM PLL 1.8 V                |
| VDD_DRAM_PLL_1P8           | L7                                                                                                                                                                                                                                          | Supply for DRAM PLL                                      |
| VDD_MIPI_1P2               | F12                                                                                                                                                                                                                                         | Supply for MIPI PHY                                      |
| VDD_SNVS_0P8               | J15                                                                                                                                                                                                                                         | Supply for SNVS logic                                    |
| VDD_SOC                    | J9, J10, J11, J12, J13, K10, K12, L9, L10, L12, L13, M10, M12, N9, N10, N11, N12, N13                                                                                                                                                       | Supply for SOC logic                                     |
| VDD_USB_3P3                | F14                                                                                                                                                                                                                                         | Supply for USB PHY                                       |
| VSS                        | A1, AA1, E3, G3, J3, L3, N3, R3, U3, C4, W4, C6, W6, C8, H8, J8, L8, N8, P8, W8, C10, H10, P10, W10, K11, M11, C12, H12, P12, W12, C14, H14, J14, L14, N14, P14, W14, C16, W16, C18, W18, E19, G19, J19, L19, N19, R19, U19, B20, A21, AA21 | —                                                        |

Table 78 shows an alpha-sorted list of functional contact assignments for the 11 x 11 mm package.

**Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments**

| Ball name  | Ball | Power group            | Ball type | Reset condition |                           |                          |
|------------|------|------------------------|-----------|-----------------|---------------------------|--------------------------|
|            |      |                        |           | Default mode    | Default function          | Input/Output status      |
| 24M_XTALI  | B21  | NVCC_CLK_JTAG_PVCC_1P8 | ANALOG    | —               | —                         | Input                    |
| 24M_XTALO  | C20  | NVCC_CLK_JTAG_PVCC_1P8 | ANALOG    | —               | —                         | Output                   |
| BOOT_MODE0 | G16  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[0] | Input with PD            |
| BOOT_MODE1 | G18  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[1] | Input with PD            |
| BOOT_MODE2 | F16  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[2] | Input with PD            |
| BOOT_MODE3 | G17  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | ccmsrcgpcmix.BOOT_MODE[3] | Input with PD            |
| CLKIN1     | E20  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | —               | —                         | Input without PU/PD      |
| CLKIN2     | F20  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | —               | —                         | Input without PU/PD      |
| CLKOUT1    | E21  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | —               | —                         | Output low without PU/PD |
| CLKOUT2    | F21  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | —               | —                         | Output low without PU/PD |
| DRAM_AC00  | P1   | NVCC_DRAM              | DDR       | —               | —                         | Output low               |
| DRAM_AC01  | N1   | NVCC_DRAM              | DDR       | —               | —                         | Output low               |
| DRAM_AC02  | N2   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC03  | P2   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC04  | G5   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC05  | G4   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC06  | D4   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC07  | E4   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC08  | R1   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC09  | R2   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |
| DRAM_AC10  | M2   | NVCC_DRAM              | DDR       | —               | —                         | Input                    |



Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name    | Ball | Power group | Ball type | Reset condition |                  |                     |
|--------------|------|-------------|-----------|-----------------|------------------|---------------------|
|              |      |             |           | Default mode    | Default function | Input/Output status |
| DRAM_AC11    | L2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC12    | L1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC13    | M1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC14    | Y1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC15    | L5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC16    | J4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC17    | J5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC20    | T1   | NVCC_DRAM   | DDR       | —               | —                | Output low          |
| DRAM_AC21    | T2   | NVCC_DRAM   | DDR       | —               | —                | Output low          |
| DRAM_AC23    | R4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC24    | Y2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC25    | AA2  | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC26    | W2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC28    | AA3  | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC29    | V4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC30    | W1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC31    | Y3   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC32    | R5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC33    | U2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC34    | V2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC35    | U4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_AC36    | V1   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_ALERT_N | N5   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DM0     | B2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DM1     | H2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ00    | B3   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ01    | A2   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ02    | A3   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ03    | B4   | NVCC_DRAM   | DDR       | —               | —                | Input               |
| DRAM_DQ04    | E2   | NVCC_DRAM   | DDR       | —               | —                | Input               |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name    | Ball | Power group         | Ball type | Reset condition |                  |                     |
|--------------|------|---------------------|-----------|-----------------|------------------|---------------------|
|              |      |                     |           | Default mode    | Default function | Input/Output status |
| DRAM_DQ05    | D1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ06    | C1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ07    | D2   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ08    | G1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ09    | H1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ10    | J1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ11    | J2   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ12    | K1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ13    | K2   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ14    | F2   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQ15    | E1   | NVCC_DRAM           | DDR       | —               | —                | Input               |
| DRAM_DQS0_N  | C2   | NVCC_DRAM           | —         | —               | —                | Input               |
| DRAM_DQS0_P  | B1   | NVCC_DRAM           | DDRCLK    | —               | —                | Input               |
| DRAM_DQS1_N  | F1   | NVCC_DRAM           | —         | —               | —                | Input               |
| DRAM_DQS1_P  | G2   | NVCC_DRAM           | DDRCLK    | —               | —                | Input               |
| DRAM_RESET_N | N4   | NVCC_DRAM           | DDR       | —               | —                | Output low          |
| DRAM_VREF    | L4   | NVCC_DRAM           | DDR       | —               | —                | —                   |
| DRAM_ZN      | U1   | NVCC_DRAM           | DDR       | —               | —                | —                   |
| ECSPI1_MISO  | D6   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[8]      | Input with PD       |
| ECSPI1_MOSI  | F6   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[7]      | Input with PD       |
| ECSPI1_SCLK  | E6   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[6]      | Input with PD       |
| ECSPI1_SS0   | B6   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[9]      | Input with PD       |
| ECSPI2_MISO  | B5   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[12]     | Input with PD       |
| ECSPI2_MOSI  | A6   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[11]     | Input with PD       |
| ECSPI2_SCLK  | A4   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[10]     | Input with PD       |
| ECSPI2_SS0   | A5   | NVCC_ECSPi          | GPIO      | ALT5            | GPIO5.IO[13]     | Input with PD       |
| ENET_MDC     | Y18  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[16]     | Input with PD       |
| ENET_MDIO    | T16  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[17]     | Input with PD       |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name   | Ball | Power group         | Ball type | Reset condition |                  |                     |
|-------------|------|---------------------|-----------|-----------------|------------------|---------------------|
|             |      |                     |           | Default mode    | Default function | Input/Output status |
| ENET_RD0    | AA19 | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[26]     | Input with PD       |
| ENET_RD1    | Y15  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[27]     | Input with PD       |
| ENET_RD2    | Y16  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[28]     | Input with PD       |
| ENET_RD3    | AA16 | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[29]     | Input with PD       |
| ENET_RXC    | U16  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[25]     | Input with PD       |
| ENET_RX_CTL | V16  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[24]     | Input with PD       |
| ENET_TD0    | U18  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[21]     | Input with PD       |
| ENET_TD1    | AA18 | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[20]     | Input with PD       |
| ENET_TD2    | V18  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[19]     | Input with PD       |
| ENET_TD3    | AA17 | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[18]     | Input with PD       |
| ENET_TXC    | Y19  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[23]     | Input with PD       |
| ENET_TX_CTL | Y17  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT5            | GPIO1.IO[22]     | Input with PD       |
| GPIO1_IO00  | V8   | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT6            | GPIO1.IO[0]      | Input with PD       |
| GPIO1_IO01  | R8   | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT6            | GPIO1.IO[1]      | 1                   |
| GPIO1_IO02  | AA8  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT0            | GPIO1.IO[2]      | Input with PU       |
| GPIO1_IO03  | Y9   | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT0            | GPIO1.IO[3]      | Input with PD       |
| GPIO1_IO04  | AA7  | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT0            | GPIO1.IO[4]      | Input with PD       |
| GPIO1_IO05  | T8   | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT6            | GPIO1.IO[5]      | 1                   |
| GPIO1_IO06  | Y8   | NVCC_ENET_GPIO_SAI2 | GPIO      | ALT0            | GPIO1.IO[6]      | Input with PD       |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name             | Ball | Power group            | Ball type | Reset condition |                   |                     |
|-----------------------|------|------------------------|-----------|-----------------|-------------------|---------------------|
|                       |      |                        |           | Default mode    | Default function  | Input/Output status |
| GPIO1_IO07            | U8   | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[7]       | Input with PD       |
| GPIO1_IO08            | V10  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[8]       | Input with PD       |
| GPIO1_IO09            | AA9  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT1            | GPIO1.IO[9]       | Input with PD       |
| GPIO1_IO10            | AA10 | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[10]      | Input with PD       |
| GPIO1_IO11            | Y11  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[11]      | Input with PD       |
| GPIO1_IO12            | U10  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[12]      | Input with PD       |
| GPIO1_IO13            | T10  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[13]      | Input with PD       |
| GPIO1_IO14            | Y10  | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[14]      | Input with PD       |
| GPIO1_IO15            | AA11 | NVCC_ENET_GPIO_SAI2    | GPIO      | ALT0            | GPIO1.IO[15]      | Input with PD       |
| I2C1_SCL              | B7   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[14]      | Input with PD       |
| I2C1_SDA              | A7   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[15]      | Input with PD       |
| I2C2_SCL              | F10  | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[16]      | Input with PD       |
| I2C2_SDA              | D8   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[17]      | Input with PD       |
| I2C3_SCL              | F8   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[18]      | Input with PD       |
| I2C3_SDA              | E8   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[19]      | Input with PD       |
| I2C4_SCL              | B8   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[20]      | Input with PD       |
| I2C4_SDA              | A8   | NVCC_I2C_UART          | GPIO      | ALT5            | GPIO5.IO[21]      | Input with PD       |
| JTAG_MOD              | D18  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | cjtag_wrapper.MOD | Input with PD       |
| JTAG_TCK              | D21  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | cjtag_wrapper.TCK | Input with PU       |
| JTAG_TDI              | C21  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | cjtag_wrapper.TDI | Input with PU       |
| JTAG_TDO              | D20  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | cjtag_wrapper.TDO | Input with PU       |
| JTAG_TMS <sup>2</sup> | E18  | NVCC_CLK_JTAG_PVCC_1P8 | GPIO      | ALT0            | cjtag_wrapper.TMS | Input with PU       |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name      | Ball | Power group                    | Ball type | Reset condition |                  |                     |
|----------------|------|--------------------------------|-----------|-----------------|------------------|---------------------|
|                |      |                                |           | Default mode    | Default function | Input/Output status |
| MIPI_CSI_CLK_N | A13  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_CLK_P | B13  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D0_N  | A11  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D0_P  | B11  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D1_N  | A12  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D1_P  | B12  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D2_N  | A14  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D2_P  | B14  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D3_N  | A15  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_CSI_D3_P  | B15  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| MIPI_VREG_CAP  | D12  | 0.35 - 0.45 V                  | PHY       | —               | —                | Output              |
| NAND_ALE       | J17  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[0]      | Input with PD       |
| NAND_CE0_B     | L21  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[1]      | Input with PD       |
| NAND_CE1_B     | H20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[2]      | Input with PD       |
| NAND_CE2_B     | L16  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[3]      | Input with PD       |
| NAND_CE3_B     | L20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[4]      | Input with PD       |
| NAND_CLE       | K20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[5]      | Input with PD       |
| NAND_DATA00    | M21  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[6]      | Input with PD       |
| NAND_DATA01    | J20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[7]      | Input with PD       |
| NAND_DATA02    | M20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[8]      | Input with PD       |
| NAND_DATA03    | K21  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[9]      | Input with PD       |
| NAND_DATA04    | L18  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[10]     | Input with PD       |
| NAND_DATA05    | J18  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[11]     | Input with PD       |
| NAND_DATA06    | N20  | NVCC_SD1_NAND                  | GPIO      | ALT5            | GPIO3.IO[12]     | Input with PD       |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name     | Ball | Power group          | Ball type | Reset condition |                            |                                |
|---------------|------|----------------------|-----------|-----------------|----------------------------|--------------------------------|
|               |      |                      |           | Default mode    | Default function           | Input/Output status            |
| NAND_DATA07   | G20  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[13]               | Input with PD                  |
| NAND_DQS      | H21  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[14]               | Input with PD                  |
| NAND_RE_B     | G21  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[15]               | Input with PD                  |
| NAND_READY_B  | L17  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[16]               | Input with PD                  |
| NAND_WE_B     | J16  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[17]               | Input with PD                  |
| NAND_WP_B     | J21  | NVCC_SD1_NAND        | GPIO      | ALT5            | GPIO3.IO[18]               | Input with PD                  |
| ONOFF         | E14  | NVCC_SNVS_1P8        | GPIO      | ALT0            | snvsmix.ONOFF              | Input without PU/PD            |
| PMIC_ON_REQ   | E16  | NVCC_SNVS_1P8        | GPIO      | ALT0            | snvsmix.PMIC_ON_REQ        | Open-drain output high with PU |
| PMIC_STBY_REQ | A19  | NVCC_SNVS_1P8        | GPIO      | ALT0            | ccmsrcgpcmix.PMIC_STBY_REQ | Output low with PD             |
| POR_B         | A18  | NVCC_SNVS_1P8        | GPIO      | ALT0            | snvsmix.POR_B              | Input without PU/PD            |
| RTC_XTALI     | A20  | NVCC_SNVS_1P8        | ANALOG    | ALT0            | snvsmix.RTC                | Input                          |
| RTC_XTALO     | B19  | NVCC_SNVS_1P8        | ANALOG    | —               | —                          | Output, inverted of RTC_XTALI  |
| RTC_RESET_B   | B18  | NVCC_SNVS_1P8        | GPIO      | ALT0            | snvsmix.RTC_POR_B          | Input without PU/PD            |
| SAI2_MCLK     | Y12  | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[27]               | Input with PD                  |
| SAI2_RXC      | AA15 | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[22]               | Input with PD                  |
| SAI2_RXD0     | AA14 | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[23]               | Input with PD                  |
| SAI2_RXFS     | Y13  | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[21]               | Input with PD                  |
| SAI2_TXC      | AA13 | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[25]               | Input with PD                  |
| SAI2_TXD0     | Y14  | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[26]               | Input with PD                  |
| SAI2_TXFS     | AA12 | NVCC_ENET_GPI O_SAI2 | GPIO      | ALT5            | GPIO4.IO[24]               | Input with PD                  |
| SAI3_MCLK     | AA5  | NVCC_SAI3_SAI5       | GPIO      | ALT5            | GPIO5.IO[2]                | Input with PD                  |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name   | Ball | Power group    | Ball type | Reset condition |                  |                     |
|-------------|------|----------------|-----------|-----------------|------------------|---------------------|
|             |      |                |           | Default mode    | Default function | Input/Output status |
| SAI3_RXC    | Y6   | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO4.IO[29]     | Input with PD       |
| SAI3_RXD    | AA6  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO4.IO[30]     | Input with PD       |
| SAI3_RXFS   | Y4   | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO4.IO[28]     | Input with PD       |
| SAI3_TXC    | Y5   | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO5.IO[0]      | Input with PD       |
| SAI3_TXD    | AA4  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO5.IO[1]      | Input with PD       |
| SAI3_TXFS   | Y7   | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO4.IO[31]     | Input with PD       |
| SAI5_MCLK   | W11  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[25]     | 3                   |
| SAI5_RXC    | V14  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[20]     | Input with PD       |
| SAI5_RXD0   | U12  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[21]     | Input with PD       |
| SAI5_RXD1   | T14  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[22]     | Input with PD       |
| SAI5_RXD2   | V12  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[23]     | Input with PD       |
| SAI5_RXD3   | U14  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[24]     | Input with PD       |
| SAI5_RXFS   | T12  | NVCC_SAI3_SAI5 | GPIO      | ALT5            | GPIO3.IO[19]     | Input with PD       |
| SD1_CLK     | R21  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[0]      | Input with PD       |
| SD1_CMD     | T21  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[1]      | Input with PD       |
| SD1_DATA0   | N18  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[2]      | Input with PD       |
| SD1_DATA1   | N17  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[3]      | Input with PD       |
| SD1_DATA2   | N21  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[4]      | Input with PD       |
| SD1_DATA3   | P20  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[5]      | Input with PD       |
| SD1_DATA4   | P21  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[6]      | Input with PD       |
| SD1_DATA5   | T20  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[7]      | Input with PD       |
| SD1_DATA6   | R20  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[8]      | Input with PD       |
| SD1_DATA7   | N16  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[9]      | Input with PD       |
| SD1_RESET_B | R18  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[10]     | Input with PD       |
| SD1_STROBE  | R17  | NVCC_SD1_NAND  | GPIO      | ALT5            | GPIO2.IO[11]     | Input with PD       |
| SD2_CD_B    | U20  | NVCC_SD2       | GPIO      | ALT5            | GPIO2.IO[12]     | Input with PD       |
| SD2_CLK     | Y21  | NVCC_SD2       | GPIO      | ALT5            | GPIO2.IO[13]     | Input with PD       |
| SD2_CMD     | V21  | NVCC_SD2       | GPIO      | ALT5            | GPIO2.IO[14]     | Input with PD       |
| SD2_DATA0   | AA20 | NVCC_SD2       | GPIO      | ALT5            | GPIO2.IO[15]     | Input with PD       |
| SD2_DATA1   | U21  | NVCC_SD2       | GPIO      | ALT5            | GPIO2.IO[16]     | Input with PD       |

Table 78. i.MX 8M Nano 11 x 11 mm functional contact assignments (continued)

| Ball name           | Ball | Power group                    | Ball type | Reset condition |                  |                     |
|---------------------|------|--------------------------------|-----------|-----------------|------------------|---------------------|
|                     |      |                                |           | Default mode    | Default function | Input/Output status |
| SD2_DATA2           | W20  | NVCC_SD2                       | GPIO      | ALT5            | GPIO2.IO[17]     | Input with PD       |
| SD2_DATA3           | V20  | NVCC_SD2                       | GPIO      | ALT5            | GPIO2.IO[18]     | Input with PD       |
| SD2_RESET_B         | Y20  | NVCC_SD2                       | GPIO      | ALT5            | GPIO2.IO[19]     | Input with PD       |
| SD2_WP              | W21  | NVCC_SD2                       | GPIO      | ALT5            | GPIO2.IO[20]     | Input with PD       |
| SPDIF_EXT_CLK       | T6   | NVCC_SAI3_SAI5                 | GPIO      | ALT5            | GPIO5.IO[5]      | Input with PD       |
| SPDIF_RX            | U6   | NVCC_SAI3_SAI5                 | GPIO      | ALT5            | GPIO5.IO[4]      | Input with PD       |
| SPDIF_TX            | V6   | NVCC_SAI3_SAI5                 | GPIO      | ALT5            | GPIO5.IO[3]      | Input with PD       |
| TSensor_RES_E<br>XT | D16  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | ANALOG    | —               | —                | —                   |
| UART1_RXD           | A9   | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[22]     | Input with PD       |
| UART1_TXD           | E10  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[23]     | Input with PD       |
| UART2_RXD           | B9   | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[24]     | Input with PD       |
| UART2_TXD           | C11  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[25]     | Input with PD       |
| UART3_RXD           | B10  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[26]     | Input with PD       |
| UART3_TXD           | E12  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[27]     | Input with PD       |
| UART4_RXD           | A10  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[28]     | Input with PD       |
| UART4_TXD           | D10  | NVCC_I2C_UART                  | GPIO      | ALT5            | GPIO5.IO[29]     | Input with PD       |
| USB1_DN             | A17  | VDD_USB_3P3                    | PHY       | —               | —                | Input               |
| USB1_DP             | B17  | VDD_USB_3P3                    | PHY       | —               | —                | Input               |
| USB1_ID             | D14  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | Input               |
| USB1_TXRTUNE        | B16  | VDD_ANA1_XTAL_<br>MIPI_USB_1P8 | PHY       | —               | —                | —                   |
| USB1_VBUS           | A16  | VDD_USB_3P3                    | PHY       | —               | —                | —                   |

<sup>1</sup> During reset: output high without PU/PD; After reset: input with PU

<sup>2</sup> Mandatory requirement: JTAG\_TMS pin must be connected with a 50 ohm serial resistor near the component.

<sup>3</sup> During reset: input without PU/PD; After reset: input with PD

### 5.2.3 i.MX 8M Nano 11 x 11 mm 0.5 mm pitch ball map

Table 79 shows the i.MX 8M Nano 11 x 11 mm 0.5 mm pitch ball map.



Table 79. 11 x 11 mm, 0.5 mm pitch ball map

| F            | E           | D               | C           | B              | A              |    |
|--------------|-------------|-----------------|-------------|----------------|----------------|----|
| DRAM_DQS1_N  | DRAM_DQ15   | DRAM_DQ05       | DRAM_DQ06   | DRAM_DQS0_P    | VSS            | 1  |
| DRAM_DQ14    | DRAM_DQ04   | DRAM_DQ07       | DRAM_DQS0_N | DRAM_DM0       | DRAM_DQ01      | 2  |
|              | VSS         |                 |             | DRAM_DQ00      | DRAM_DQ02      | 3  |
|              | DRAM_AC07   | DRAM_AC06       | VSS         | DRAM_DQ03      | ECSP12_SCLK    | 4  |
|              |             |                 |             | ECSP12_MISO    | ECSP12_SS0     | 5  |
| ECSP11_MOSI  | ECSP11_SCLK | ECSP11_MISO     | VSS         | ECSP11_SS0     | ECSP12_MOSI    | 6  |
|              |             |                 |             | I2C1_SCL       | I2C1_SDA       | 7  |
| I2C3_SCL     | I2C3_SDA    | I2C2_SDA        | VSS         | I2C4_SCL       | I2C4_SDA       | 8  |
|              |             |                 |             | UART2_RXD      | UART1_RXD      | 9  |
| I2C2_SCL     | UART1_TXD   | UART4_TXD       | VSS         | UART3_RXD      | UART4_RXD      | 10 |
|              |             |                 | UART2_TXD   | MIPI_CSI_D0_P  | MIPI_CSI_D0_N  | 11 |
| VDD_MIPI_1P2 | UART3_TXD   | MIPI_VREG_CAP   | VSS         | MIPI_CSI_D1_P  | MIPI_CSI_D1_N  | 12 |
|              |             |                 |             | MIPI_CSI_CLK_P | MIPI_CSI_CLK_N | 13 |
| VDD_USB_3P3  | ONOFF       | USB1_ID         | VSS         | MIPI_CSI_D2_P  | MIPI_CSI_D2_N  | 14 |
|              |             |                 |             | MIPI_CSI_D3_P  | MIPI_CSI_D3_N  | 15 |
| BOOT_MODE2   | PMIC_ON_REQ | TSensor_RES_EXT | VSS         | USB1_TXRTUNE   | USB1_VBUS      | 16 |
|              |             |                 |             | USB1_DP        | USB1_DN        | 17 |
|              | JTAG_TMS    | JTAG_MOD        | VSS         | RTC_RESET_B    | POR_B          | 18 |
|              | VSS         |                 |             | RTC_XTALO      | PMIC_STBY_REQ  | 19 |
| CLKIN2       | CLKIN1      | JTAG_TDO        | 24M_XTALO   | VSS            | RTC_XTALI      | 20 |
| CLKOUT2      | CLKOUT1     | JTAG_TCK        | JTAG_TDI    | 24M_XTALI      | VSS            | 21 |

Table 79. 11 x 11 mm, 0.5 mm pitch ball map (continued)

|             | 1                      | 2           | 3            | 4          | 5                          | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|-------------|------------------------|-------------|--------------|------------|----------------------------|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|
| M           | L                      | K           | J            | H          | G                          |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| DRAM_AC13   | DRAM_AC12              | DRAM_DQ12   | DRAM_DQ10    | DRAM_DQ09  | DRAM_DQ08                  |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| DRAM_AC10   | DRAM_AC11              | DRAM_DQ13   | DRAM_DQ11    | DRAM_DM1   | DRAM_DQS1_P                |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VSS                    |             | VSS          |            | VSS                        |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | DRAM_VREF              |             | DRAM_AC16    |            | DRAM_AC05                  |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | DRAM_AC15              |             | DRAM_AC17    |            | DRAM_AC04                  |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | NVCC_DRAM              |             | NVCC_DRAM    |            | NVCC_DRAM                  |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VDD_DRAM_PLL_1P8       |             | NVCC_DRAM    |            |                            |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VSS                    |             | VSS          | VSS        | NVCC_ECSP1                 |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VDD_SOC                |             | VDD_SOC      |            |                            |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| VDD_SOC     | VDD_SOC                | VDD_SOC     | VDD_SOC      | VSS        | NVCC_I2C_UART              |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| VSS         |                        | VSS         | VDD_SOC      |            |                            |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| VDD_SOC     | VDD_SOC                | VDD_SOC     | VDD_SOC      | VSS        | VDD_ANA1_XTAL_MIPI_USB_1P8 |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VDD_SOC                |             | VDD_SOC      |            |                            |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VSS                    |             | VSS          | VSS        | NVCC_SNV5_1P8              |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | NVCC_CLK_JTAG_PVCC_1P8 |             | VDD_SNV5_0P8 |            |                            |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | NAND_CE2_B             |             | NAND_WE_B    |            | BOOT_MODE0                 |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | NAND_READY_B           |             | NAND_ALE     |            | BOOT_MODE3                 |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | NAND_DATA04            |             | NAND_DATA05  |            | BOOT_MODE1                 |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|             | VSS                    |             | VSS          |            | VSS                        |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| NAND_DATA02 | NAND_CE3_B             | NAND_CLE    | NAND_DATA01  | NAND_CE1_B | NAND_DATA07                |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| NAND_DATA00 | NAND_CE0_B             | NAND_DATA03 | NAND_WP_B    | NAND_DQS   | NAND_RE_B                  |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |

Table 79. 11 x 11 mm, 0.5 mm pitch ball map (continued)

| W         | V           | U          | T             | R                    | P         | N             |    |
|-----------|-------------|------------|---------------|----------------------|-----------|---------------|----|
| DRAM_AC30 | DRAM_AC36   | DRAM_ZN    | DRAM_AC20     | DRAM_AC08            | DRAM_AC00 | DRAM_AC01     | 1  |
| DRAM_AC26 | DRAM_AC34   | DRAM_AC33  | DRAM_AC21     | DRAM_AC09            | DRAM_AC03 | DRAM_AC02     | 2  |
|           |             | VSS        |               | VSS                  |           | VSS           | 3  |
| VSS       | DRAM_AC29   | DRAM_AC35  |               | DRAM_AC23            |           | DRAM_RESET_N  | 4  |
|           |             |            |               | DRAM_AC32            |           | DRAM_ALERT_N  | 5  |
| VSS       | SPDIF_TX    | SPDIF_RX   | SPDIF_EXT_CLK | NVCC_DRAM            |           | NVCC_DRAM     | 6  |
|           |             |            |               |                      |           | NVCC_DRAM     | 7  |
| VSS       | GPIO1_IO00  | GPIO1_IO07 | GPIO1_IO05    | GPIO1_IO01           | VSS       | VSS           | 8  |
|           |             |            |               |                      |           | VDD_SOC       | 9  |
| VSS       | GPIO1_IO08  | GPIO1_IO12 | GPIO1_IO13    | NVCC_SAI3_SAI5       | VSS       | VDD_SOC       | 10 |
| SAI5_MCLK |             |            |               |                      |           | VDD_SOC       | 11 |
| VSS       | SAI5_RXD2   | SAI5_RXD0  | SAI5_RXFS     | NVCC_ENET_GPIO_SAI2  | VSS       | VDD_SOC       | 12 |
|           |             |            |               |                      |           | VDD_SOC       | 13 |
| VSS       | SAI5_RXC    | SAI5_RXD3  | SAI5_RXD1     | VDD_ANA0_ARM_PLL_1P8 | VSS       | VSS           | 14 |
|           |             |            |               |                      |           | NVCC_SD1_NAND | 15 |
| VSS       | ENET_RX_CTL | ENET_RXC   | ENET_MDIO     | NVCC_SD2             |           | SD1_DATA7     | 16 |
|           |             |            |               | SD1_STROBE           |           | SD1_DATA1     | 17 |
| VSS       | ENET_TD2    | ENET_TD0   |               | SD1_RESET_B          |           | SD1_DATA0     | 18 |
|           |             | VSS        |               | VSS                  |           | VSS           | 19 |
| SD2_DATA2 | SD2_DATA3   | SD2_CD_B   | SD1_DATA5     | SD1_DATA6            | SD1_DATA3 | NAND_DATA06   | 20 |
| SD2_WP    | SD2_CMD     | SD2_DATA1  | SD1_CMD       | SD1_CLK              | SD1_DATA4 | SD1_DATA2     | 21 |

Table 79. 11 x 11 mm, 0.5 mm pitch ball map (continued)

|    | 1         | 2         | 3         | 4         | 5         | 6        | 7          | 8          | 9          | 10         | 11         | 12        | 13        | 14        | 15       | 16       | 17          | 18       | 19       | 20          | 21      |
|----|-----------|-----------|-----------|-----------|-----------|----------|------------|------------|------------|------------|------------|-----------|-----------|-----------|----------|----------|-------------|----------|----------|-------------|---------|
| Y  | DRAM_AC14 | DRAM_AC24 | DRAM_AC31 | SAI3_RXFS | SAI3_TXC  | SAI3_RXC | SAI3_TXFS  | GPIO1_IO06 | GPIO1_IO03 | GPIO1_IO14 | GPIO1_IO11 | SAI2_MCLK | SAI2_RXFS | SAI2_TXD0 | ENET_RD1 | ENET_RD2 | ENET_TX_CTL | ENET_MDC | ENET_TXC | SD2_RESET_B | SD2_CLK |
| AA | VSS       | DRAM_AC25 | DRAM_AC28 | SAI3_TXD  | SAI3_MCLK | SAI3_RXD | GPIO1_IO04 | GPIO1_IO02 | GPIO1_IO09 | GPIO1_IO10 | GPIO1_IO15 | SAI2_TXFS | SAI2_TXC  | SAI2_RXD0 | SAI2_RXC | ENET_RD3 | ENET_TD3    | ENET_TD1 | ENET_RD0 | SD2_DATA0   | VSS     |

### 5.3 DDR pin function list

Table 80 shows the DDR pin function list.

Table 80. DDR pin function list

| Ball name   | LPDDR4   | DDR4               | DDR3/3L |
|-------------|----------|--------------------|---------|
| DRAM_DQS0_P | DQS0_t_A | DQSL_t_A           | DQSL_A  |
| DRAM_DQS0_N | DQS0_c_A | DQSL_c_A           | DQSL#_A |
| DRAM_DM0    | DMI0_A   | DML_n_A / DBIL_n_A | DML_A   |
| DRAM_DQ00   | DQ0_A    | DQL0_A             | DQL0_A  |
| DRAM_DQ01   | DQ1_A    | DQL1_A             | DQL1_A  |
| DRAM_DQ02   | DQ2_A    | DQL2_A             | DQL2_A  |
| DRAM_DQ03   | DQ3_A    | DQL3_A             | DQL3_A  |
| DRAM_DQ04   | DQ4_A    | DQL4_A             | DQL4_A  |
| DRAM_DQ05   | DQ5_A    | DQL5_A             | DQL5_A  |
| DRAM_DQ06   | DQ6_A    | DQL6_A             | DQL6_A  |
| DRAM_DQ07   | DQ7_A    | DQL7_A             | DQL7_A  |
| DRAM_DQS1_P | DQS1_t_A | DQSU_t_A           | DQSU_A  |
| DRAM_DQS1_N | DQS1_c_A | DQSU_c_A           | DQSU#_A |
| DRAM_DM1    | DMI1_A   | DMU_n_A / DBIU_n_A | DMU_A   |
| DRAM_DQ08   | DQ08_A   | DQU0_A             | DQU0_A  |
| DRAM_DQ09   | DQ09_A   | DQU1_A             | DQU1_A  |
| DRAM_DQ10   | DQ10_A   | DQU2_A             | DQU2_A  |
| DRAM_DQ11   | DQ11_A   | DQU3_A             | DQU3_A  |
| DRAM_DQ12   | DQ12_A   | DQU4_A             | DQU4_A  |
| DRAM_DQ13   | DQ13_A   | DQU5_A             | DQU5_A  |

Table 80. DDR pin function list (continued)

|              |         |                  |           |
|--------------|---------|------------------|-----------|
| DRAM_DQ14    | DQ14_A  | DQU6_A           | DQU6_A    |
| DRAM_DQ15    | DQ15_A  | DQU7_A           | DQU7_A    |
| DRAM_RESET_N | RESET_N | RESET_n          | RESET#    |
| DRAM_ALERT_N | MTEST1  | ALERT_n / MTEST1 | MTEST1    |
| DRAM_AC00    | CKE0_A  | CKE0             | CKE0      |
| DRAM_AC01    | CKE1_A  | CKE1             | CKE1      |
| DRAM_AC02    | CS0_A   | CS0_n            | CS0#      |
| DRAM_AC03    | CS1_A   | C0               | —         |
| DRAM_AC04    | CK_t_A  | BG0              | BA2       |
| DRAM_AC05    | CK_c_A  | BG1              | A14       |
| DRAM_AC06    | —       | ACT_n            | A15       |
| DRAM_AC07    | —       | A9               | A9        |
| DRAM_AC08    | CA0_A   | A12              | A12 / BC# |
| DRAM_AC09    | CA1_A   | A11              | A11       |
| DRAM_AC10    | CA2_A   | A7               | A7        |
| DRAM_AC11    | CA3_A   | A8               | A8        |
| DRAM_AC12    | CA4_A   | A6               | A6        |
| DRAM_AC13    | CA5_A   | A5               | A5        |
| DRAM_AC14    | —       | A4               | A4        |
| DRAM_AC15    | —       | A3               | A3        |
| DRAM_AC16    | —       | CK_t_A           | CK_A      |
| DRAM_AC17    | —       | CK_c_A           | CK#_A     |
| DRAM_AC19    | MTEST   | MTEST            | MTEST     |
| DRAM_AC20    | CKE0_B  | CK_t_B           | CK_B      |
| DRAM_AC21    | CKE1_B  | CK_c_B           | CK#_B     |
| DRAM_AC22    | CS1_B   | —                | —         |
| DRAM_AC23    | CS0_B   | —                | —         |
| DRAM_AC24    | CK_t_B  | A2               | A2        |
| DRAM_AC25    | CK_c_B  | A1               | A1        |
| DRAM_AC26    | —       | BA1              | BA1       |
| DRAM_AC27    | —       | PARITY           | —         |
| DRAM_AC28    | CA0_B   | A13              | A13       |
| DRAM_AC29    | CA1_B   | BA0              | BA0       |
| DRAM_AC30    | CA2_B   | A10 / AP         | A10 / AP  |

Table 80. DDR pin function list (continued)

|           |       |             |      |
|-----------|-------|-------------|------|
| DRAM_AC31 | CA3_B | A0          | A0   |
| DRAM_AC32 | CA4_B | C2          | —    |
| DRAM_AC33 | CA5_B | CAS_n / A15 | CAS# |
| DRAM_AC34 | —     | WE_n / A14  | WE#  |
| DRAM_AC35 | —     | RAS_n / A16 | RAS# |
| DRAM_AC36 | —     | ODT0        | ODT0 |
| DRAM_AC37 | —     | ODT1        | ODT1 |
| DRAM_AC38 | —     | CS1_n       | CS1# |
| DRAM_ZN   | ZQ    | ZQ          | ZQ   |
| DRAM_VREF | VREF  | VREF        | VREF |

## 6 Revision history

Table 81 provides a revision history for this data sheet.

**Table 81. Revision history**

| Rev.number | Date    | Substantive change(s)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
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| Rev. 1     | 03/2021 | <ul style="list-style-type: none"> <li>Added a note for the <a href="#">Figure 1, "i.MX 8M Nano system block diagram"</a> and <a href="#">Table 2, "Modules supported"</a></li> <li>Added part numbers for 11 x 11 mm package and descriptions in the <a href="#">Table 3, "Orderable part numbers"</a></li> <li>Updated the package type and part differentiator in the <a href="#">Figure 2, "Part number nomenclature—i.MX 8M Nano family of processors"</a></li> <li>Updated the LCDIF descriptions in the <a href="#">Table 4, "i.MX 8M Nano modules list"</a></li> <li>Updated the <a href="#">Section 2.1, Recommended connections for unused input/output</a></li> <li>Updated the title and the maximum values of VDD_ARM_PLL_0P8 and VDD_USB_0P8 in the <a href="#">Table 10, "Absolute maximum ratings for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Table 11, "Absolute maximum ratings for 11 x 11 mm package"</a></li> <li>Updated the title of <a href="#">Table 13, "14 x 14 mm package thermal resistance data"</a></li> <li>Added the new <a href="#">Section 3.1.2.2, 11 x 11 mm FCBGA package thermal resistance</a></li> <li>Updated the VDD_ANA_0P8, VDD_ARM_PLL_0P8, VDD_MIPI_0P8, VDD_USB_0P8, VDD_DRAM_PLL_0P8, and USB1_VBUS in the <a href="#">Table 15, "Operating ranges for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Table 16, "Operating ranges for 11 x 11 mm package"</a></li> <li>Updated the title of <a href="#">Table 19, "Estimated power supply maximum currents for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Table 20, "Estimated power supply maximum currents for 11 x 11 mm package"</a></li> <li>Updated and added Low-V suspend mode data in the <a href="#">Table 21, "Chip power in different LP mode for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Table 22, "Chip power in different LP mode for 11 x 11 mm package"</a></li> <li>Updated and added a foot note in the <a href="#">Table 23, "The power supply states for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Table 25, "The power supply states for 11 x 11 mm package"</a></li> <li>Updated POR_B and added a note for <a href="#">Figure 3, "The power-up sequence for 14 x 14 mm package"</a></li> <li>Updated the T13 descriptions in the <a href="#">Table 26, "Power-up sequence for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Figure 4, "The power-up sequence for 11 x 11 mm package"</a> and <a href="#">Table 27, "Power-up sequence for 11 x 11 mm package"</a></li> <li>Updated the titles of <a href="#">Figure 5, "The power-down sequence for 14 x 14 mm package"</a> and <a href="#">Table 28, "Power-down sequence for 14 x 14 mm package"</a></li> <li>Added the <a href="#">Figure 6, "The power-down sequence for 11 x 11 mm package"</a> and <a href="#">Table 29, "Power-down sequence for 11 x 11 mm package"</a></li> <li>Removed the Section, Power supplies constraints</li> <li>Updated the lock time and GPU values in the <a href="#">Table 30, "PLL electrical parameters"</a>; added the M7_ALT_PLL in the <a href="#">Table 30, "PLL electrical parameters"</a></li> <li>Fixed a typo in the <a href="#">Table 74, "i.MX 8M Nano 14 x 14 mm supplies contact assignments"</a></li> <li>Changed the name of TSENSOR_RES_EXT in the <a href="#">Table 75, "i.MX 8M Nano 14 x 14 mm functional contact assignments"</a>; updated the input/out status of GPIO1_IO07, NAND_CE0_B, and NAND_RE_B in the <a href="#">Table 75, "i.MX 8M Nano 14 x 14 mm functional contact assignments"</a></li> <li>Updated the names of H10, M1, and W22 in the <a href="#">Table 76, "14 x 14 mm, 0.5 mm pitch ball map"</a></li> <li>Added the <a href="#">Section 5.2, 11 x 11 mm package information</a></li> <li>Updated LPDDR4 information of DRAM_AC14 and DRAMAC34 in the <a href="#">Table 80, "DDR pin function list"</a></li> </ul> |

## Revision history

**Table 81. Revision history (continued)**

| Rev.number | Date    | Substantive change(s)                             |
|------------|---------|---------------------------------------------------|
| Rev. 0.1   | 03/2020 | • Updated the Table, "Power supplies constraints" |
| Rev. 0     | 10/2019 | • Initial version                                 |



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*Table continues on the next page...*

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Date of release: April, 2021

Document identifier: IMX8MNCCEC

