

PHU97NQ03LT

N-channel TrenchMOS logic level FET

Rev. 02 — 21 December 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

1.3 Applications

- Computer motherboards

1.4 Quick reference data

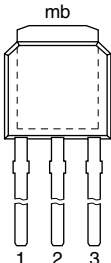
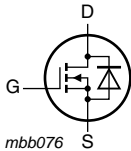
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	107	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	5.6	6.6	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 11 ; see Figure 12	-	1.9	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT533 (IPAK)

3. Ordering information

Table 3. Ordering information

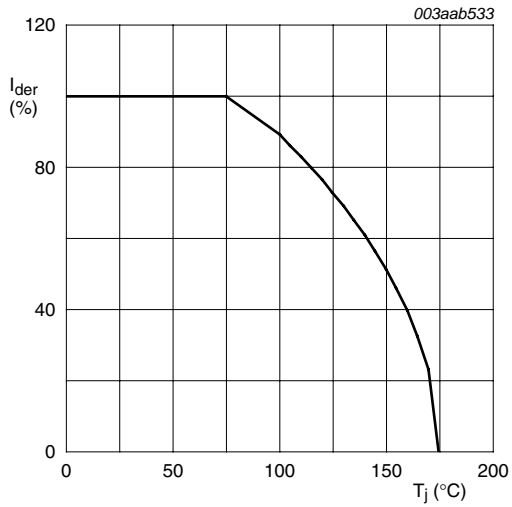
Type number	Package		Version
	Name	Description	
PHU97NQ03LT	IPAK	plastic single-ended package (IPAK); 3 leads (in-line)	SOT533

4. Limiting values

Table 4. Limiting values

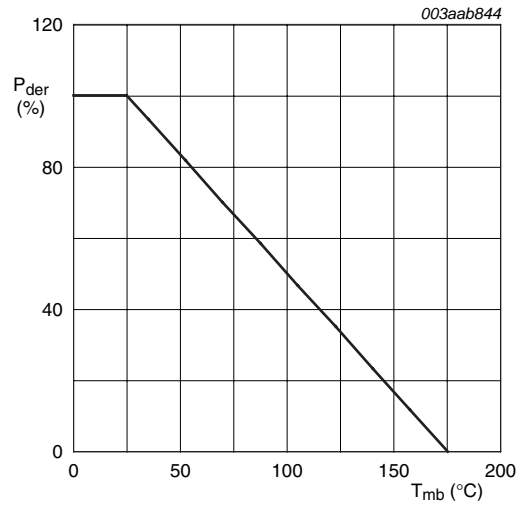
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	69	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	75	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	107	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	240	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 35\text{ A}$; $V_{sup} \leq 25\text{ V}$; unclamped; $t_p = 0.1\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	60	mJ



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

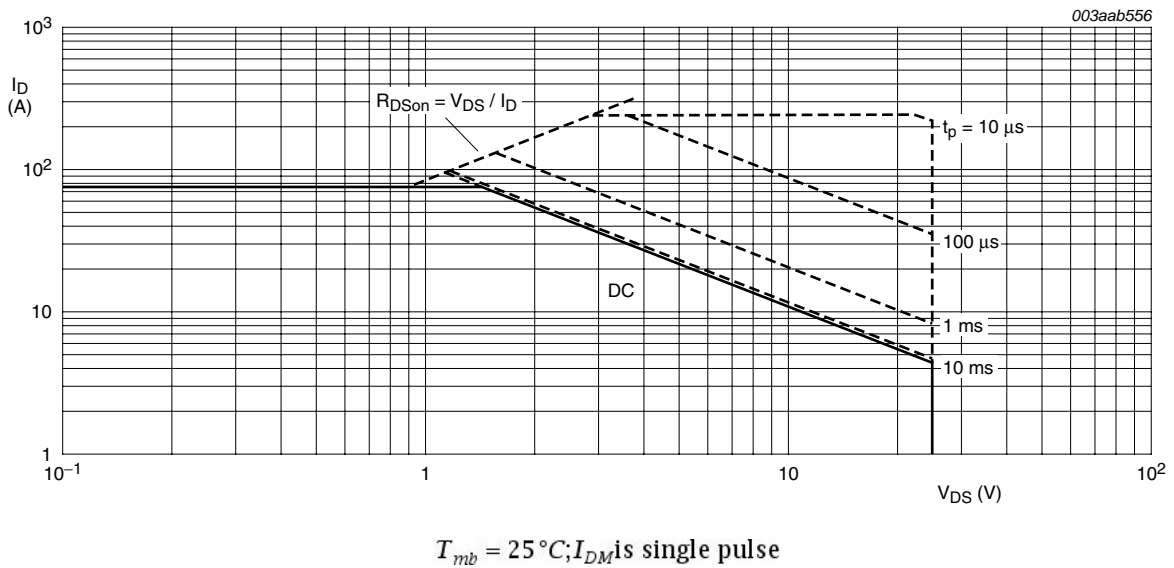


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT533 package	-	70	-	K/W

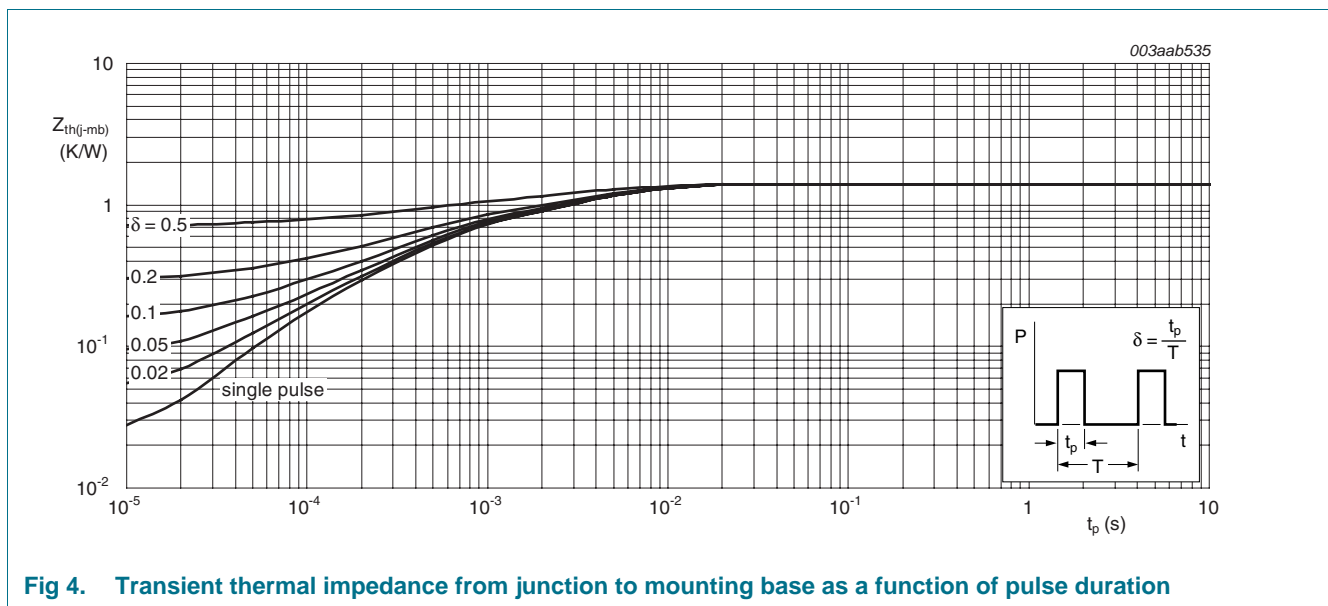


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ\text{C}$	22	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	0.7	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	-	-	2.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	1.3	1.7	2.15	V
I_{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	10.4	12.3	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	8.3	10.9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	5.6	6.6	m Ω
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1.5	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 11 ; see Figure 12	-	11.7	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 4.5 \text{ V}$	-	10.2	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 11 ; see Figure 12	-	6.2	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	3.4	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.8	-	nC
Q_{GD}	gate-drain charge		-	1.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V};$ see Figure 11 ; see Figure 12	-	3.1	-	V
C_{iss}	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	1570	-	pF
		$V_{DS} = 0 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	-	1800	-	pF
C_{oss}	output capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	380	-	pF
C_{rss}	reverse transfer capacitance		-	160	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega$	-	18	-	ns
t_r	rise time		-	33	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	12	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 14	-	0.87	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$	-	38	-	ns
Q_r	recovered charge	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	14	-	nC

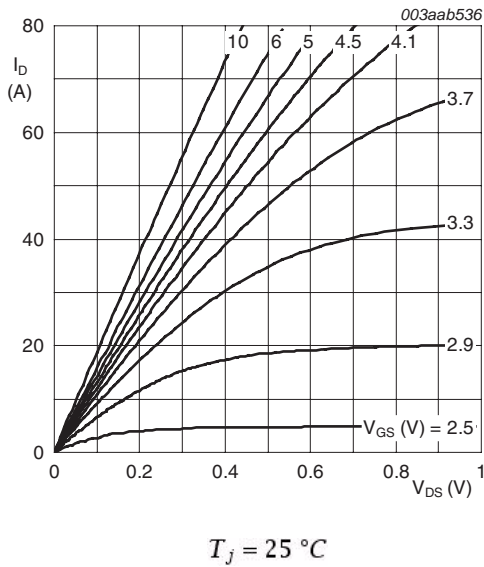


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

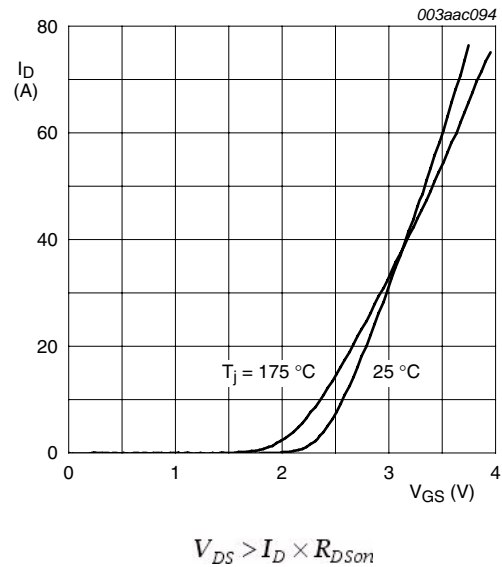


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

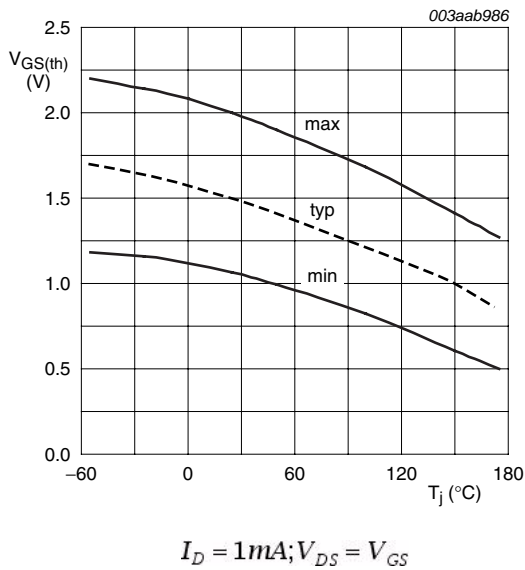


Fig 7. Gate-source threshold voltage as a function of junction temperature

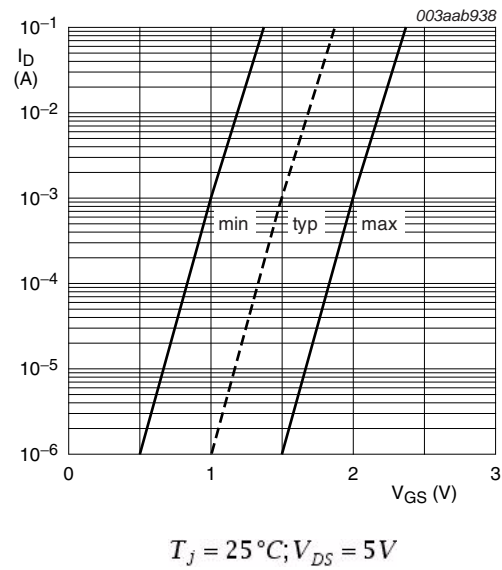
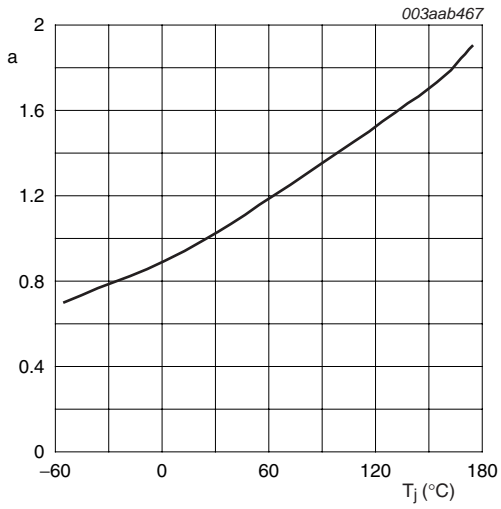
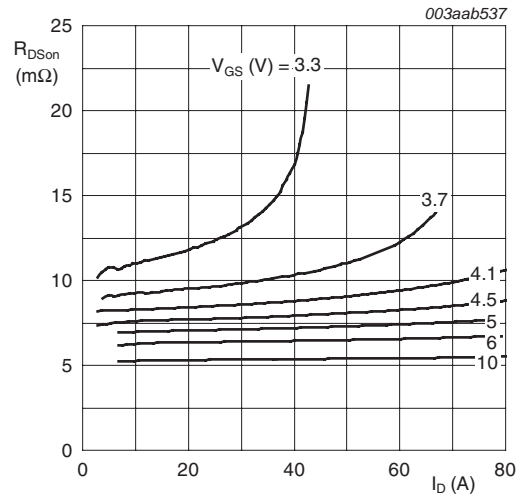


Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}C$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

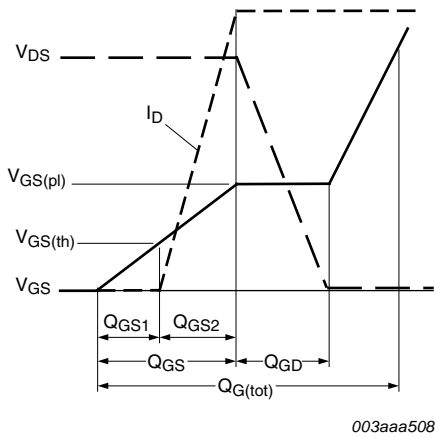
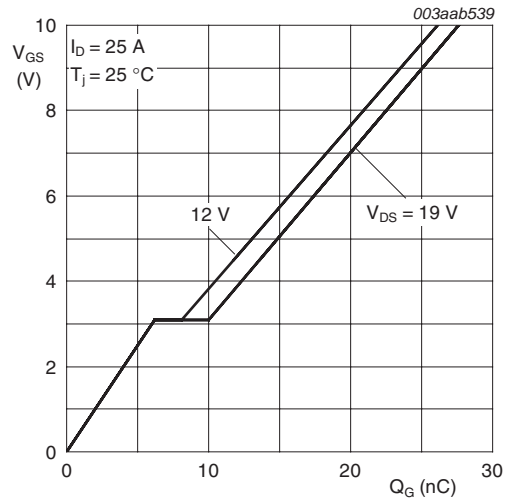
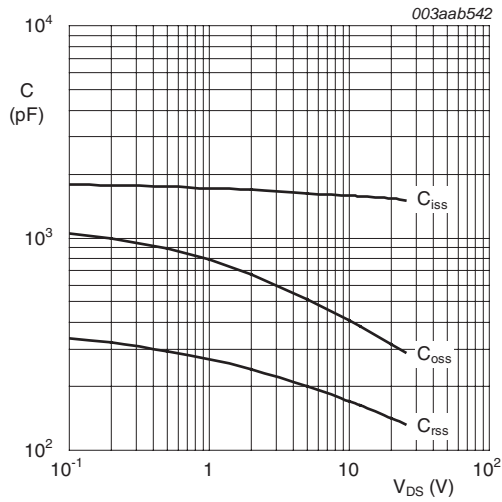


Fig 11. Gate charge waveform definitions



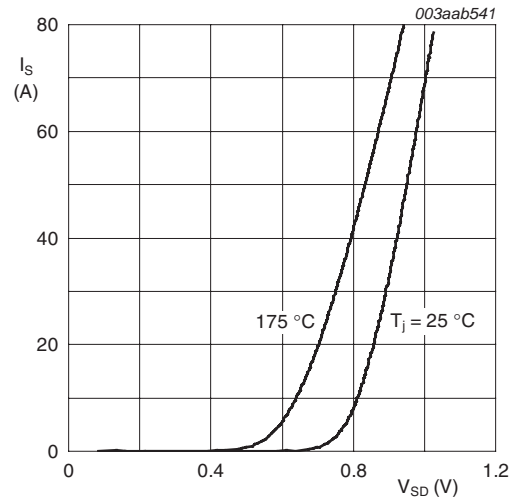
$I_D = 25A; V_{DS} = 12V \text{ and } 19V$

Fig 12. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^{\circ}C \text{ and } 175^{\circ}C; V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533

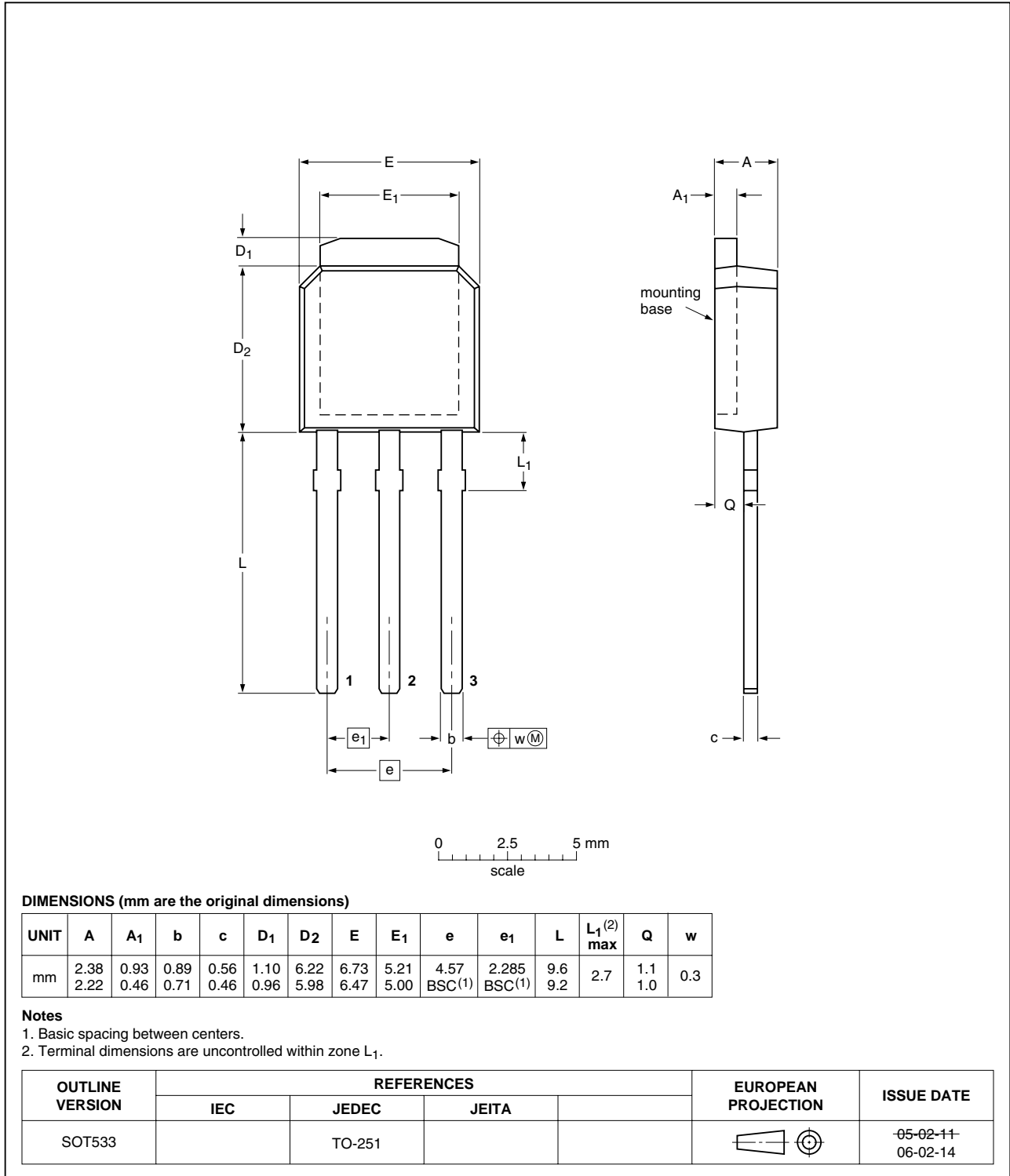


Fig 15. Package outline SOT533 (IPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHU97NQ03LT v.2	20101221	Product data sheet	-	PHU97NQ03LT v.1
Modifications:	• Various changes to content.			
PHU97NQ03LT v.1	20080225	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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