

74ACT258

Quad 2-Input Multiplexer with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multiplexer expansion by tying outputs together
- Inverting 3-STATE outputs
- Outputs source/sink 24mA
- TTL-compatible inputs

General Description

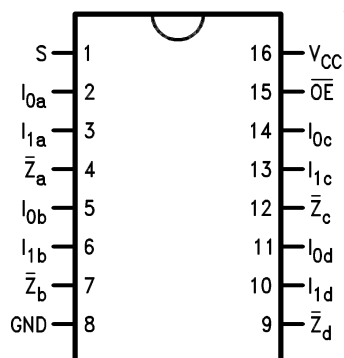
The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

Ordering Information

Order Number	Package Number	Package Description
74ACT258SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT258SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE 11, 5.3mm Wide
74ACT258MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

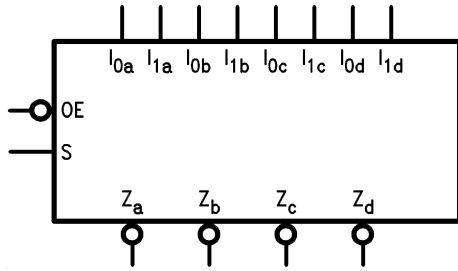
Connection Diagram



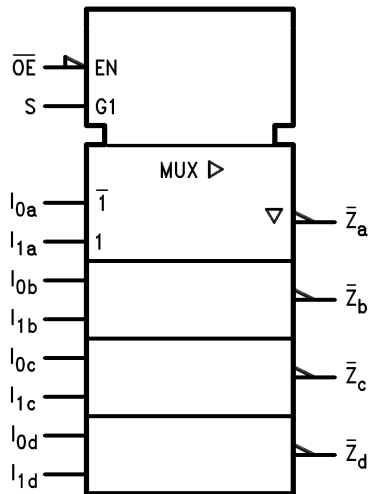
Pin Description

Pin Names	Description
S	Common Data Select Input
\overline{OE}	3-STATE Output Enable Input
$I_{0a}-I_{0d}$	Data Inputs from Source 0
$I_{1a}-I_{1d}$	Data Inputs from Source 1
$\overline{Z}_a-\overline{Z}_d$	3-STATE Inverting Data Outputs

Logic Symbol



IEEE/IEC



Functional Description

The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\bar{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$\bar{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$\bar{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$\bar{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
\overline{OE}	S	I_0	I_1	\bar{Z}
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L

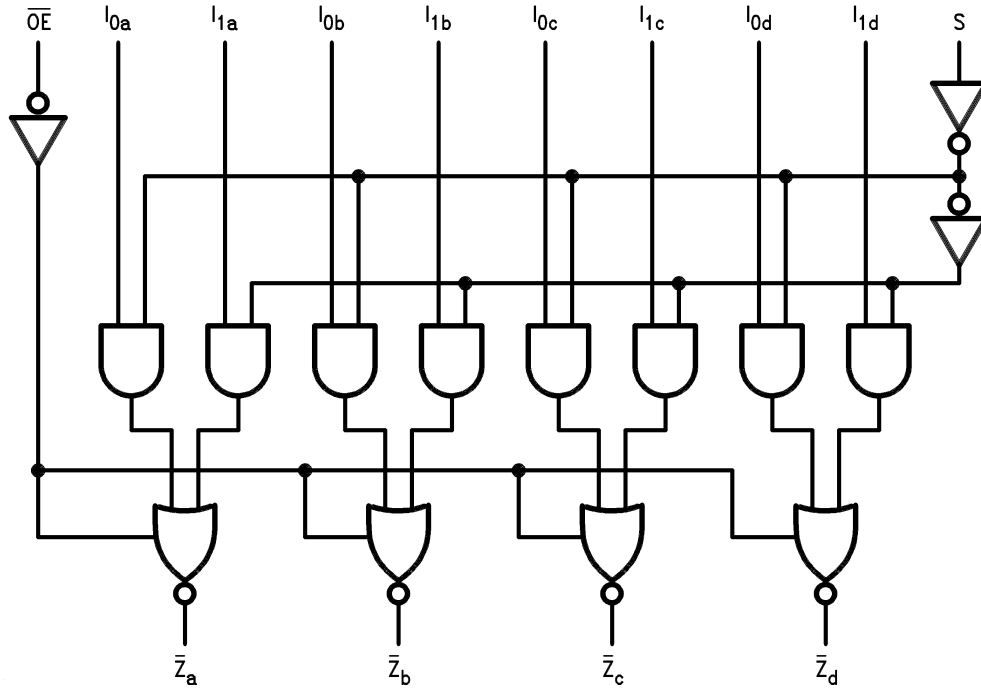
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0		V	
		5.5		1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8		V	
		5.5		1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50μA	4.49	4.4	4.4		V	
		5.5		5.49	5.4	5.4			
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OH} = -24mA			3.86	3.76		
		5.5	I _{OH} = -24mA ⁽¹⁾			4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V	
		5.5		0.001	0.1	0.1			
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA			0.36	0.44		
		5.5	I _{OL} = 24mA ⁽¹⁾			0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA	
I _{OZ}	Maximum 3-STATE Current	5.5	V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND		±0.25	±2.5		μA	
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V	0.6		1.5		mA	
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA	
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA	
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA	

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) ⁽³⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay, I _n to \bar{Z}_n	5.0	2.0	6.5	8.5	1.5	9.5	ns
t _{PHL}	Propagation Delay, I _n to \bar{Z}_n	5.0	2.0	5.5	7.5	1.5	8.0	ns
t _{PLH}	Propagation Delay, S to \bar{Z}_n	5.0	3.0	7.5	10.5	2.0	11.5	ns
t _{PHL}	Propagation Delay, S to \bar{Z}_n	5.0	1.5	7.0	9.5	1.5	11.0	ns
t _{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns
t _{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns
t _{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.0	ns
t _{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.5	9.0	ns

Notes:

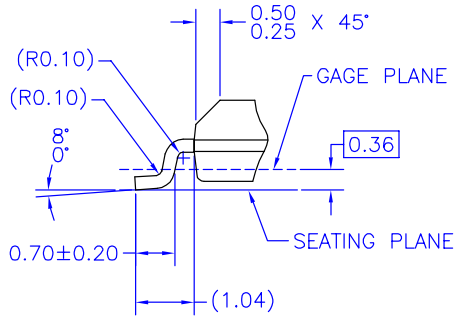
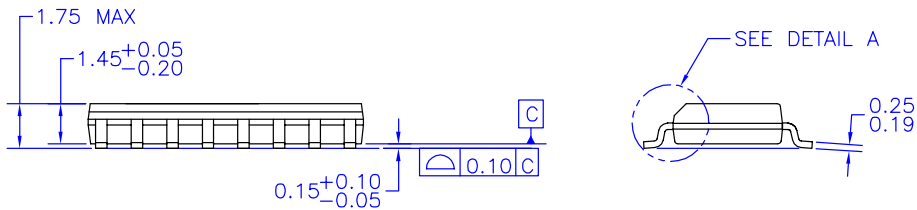
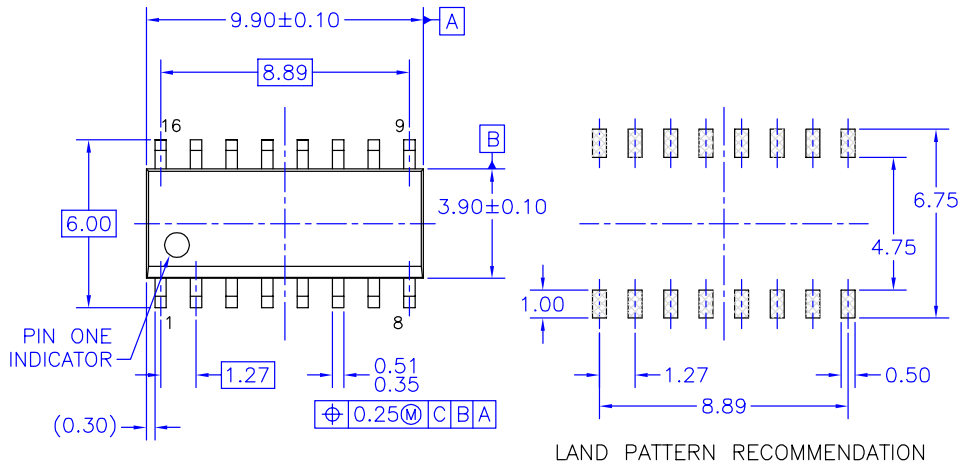
3. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	55.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

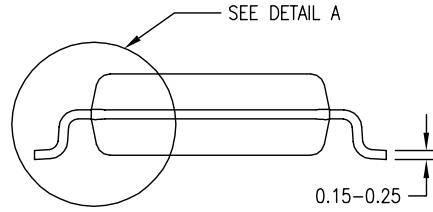
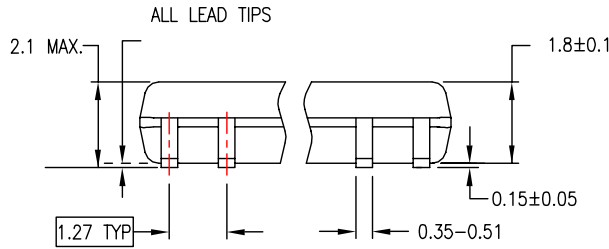
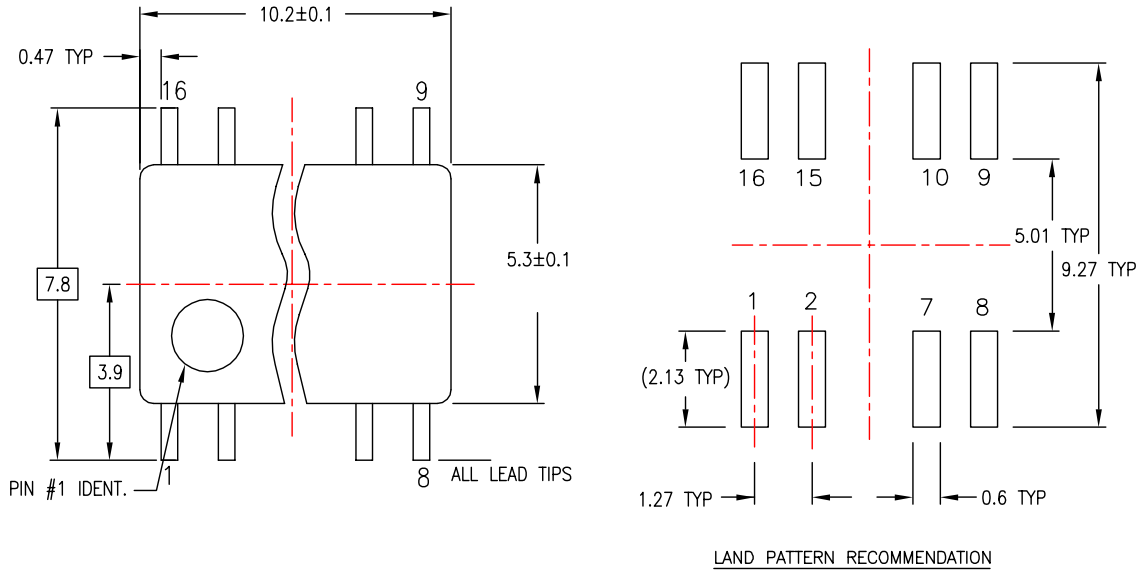
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:
200 MICRONS / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

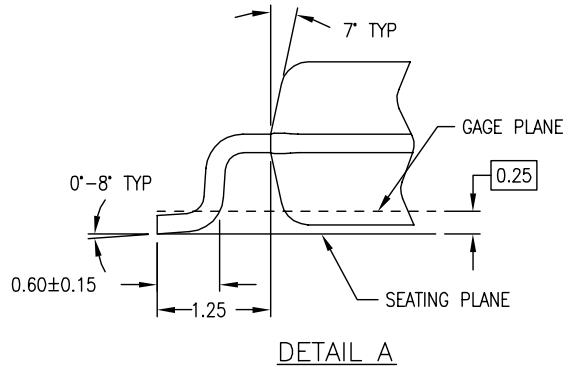
Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
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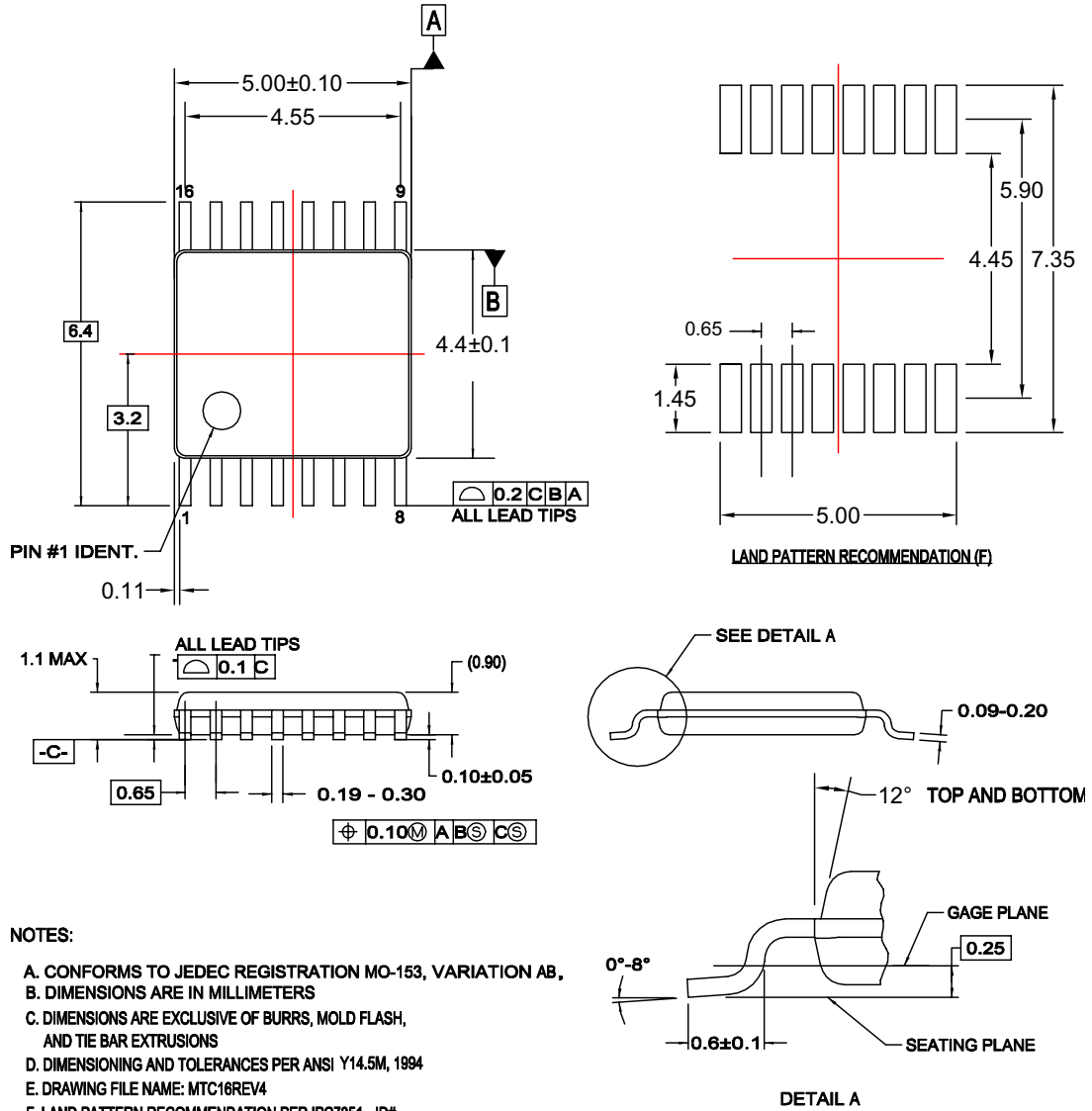


M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
- E. DRAWING FILE NAME: MTC16REV4
- F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



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