# CAT1026, CAT1027

# Dual Voltage Supervisory Circuits with I²C Serial 2k-bit CMOS EEPROM

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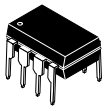

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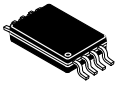
CASE 646AA



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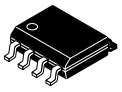

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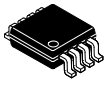

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TDFN−8
CASE 511AL

**ORDERING INFORMATION**

For Ordering Information details, see page 13.

### Description

The CAT1026 and CAT1027 are complete memory and supervisory solutions for microcontroller−based systems. A 2k−bit serial EEPROM memory and a system power supervisor with brown−out protection are integrated together in low power CMOS technology. Memory interface is via a 400 kHz I²C bus.

The CAT1026 and CAT1027 provide a precision $V_{CC}$ sense circuit with five reset threshold voltage options that support 5 V, 3.3 V and 3 V systems. The power supply monitor and reset circuit protects memory and systems controllers during power up/down and against brownout conditions. If power supply voltages are out of tolerance reset signals become active preventing the system microcontroller, ASIC, or peripherals from operating.

The CAT1026 features two open drain reset outputs: one (RESET) drives high and the other ($\overline{\text{RESET}}$) drives low whenever $V_{CC}$ falls below the threshold. Reset outputs become inactive typically 200 ms after the supply voltage exceeds the reset threshold value. With both active high and low reset signals, interface to microcontrollers and other ICs is simple. CAT1027 has only a $\overline{\text{RESET}}$ output. In addition, the $\overline{\text{RESET}}$ pin can be used as an input for push−button manual reset capability.

The CAT1026 and CAT1027 provide an auxiliary voltage sensor input, $V_{SENSE}$, which is used to monitor a second system supply. The auxiliary high impedance comparator drives the open drain output, $V_{LOW}$, whenever the sense voltage is below 1.25 V threshold.

The CAT1027 is designed with a 1.6 second watchdog timer circuit that resets a system to a known state if software or a hardware glitch halts or “hangs” the system. The CAT1027 features a watchdog timer interrupt input, WDI.

The on−chip 2k−bit EEPROM memory features a 16−byte page. In addition, hardware data protection is provided by a $V_{CC}$ sense circuit that prevents writes to memory whenever $V_{CC}$ falls below the reset threshold or until $V_{CC}$ reaches the reset threshold during power up.

Available packages include an 8−pin DIP and surface mount, 8−pin SO, 8−pin TSSOP, 8−pin TDFN and 8−pin MSOP packages. The TDFN package thickness is 0.8 mm maximum. TDFN footprint is 3 x 3 mm.

### Features

- Precision $V_{CC}$ Power Supply Voltage Monitor
  - 5 V, 3.3 V and 3 V Systems
  - Five Threshold Voltage Options
- Additional Voltage Monitoring
  - Externally Adjustable Down to 1.25 V
- Watchdog Timer (CAT1027 Only)
- Active High or Low Reset
  - Valid Reset Guaranteed at $V_{CC}$ = 1 V
- 400 kHz I²C Bus
- 2.7 V to 5.5 V Operation
- Low Power CMOS Technology
- 16−Byte Page Write Buffer
- Built−in Inadvertent Write Protection
- 1,000,000 Program/Erase Cycles
- Manual Reset Capability
- 100 Year Data Retention
- Industrial and Extended Temperature Ranges
- 8−Pin DIP, SOIC, TSSOP, MSOP or TDFN (3 x 3 mm foot−print) Packages
  - TDFN max Height is 0.8 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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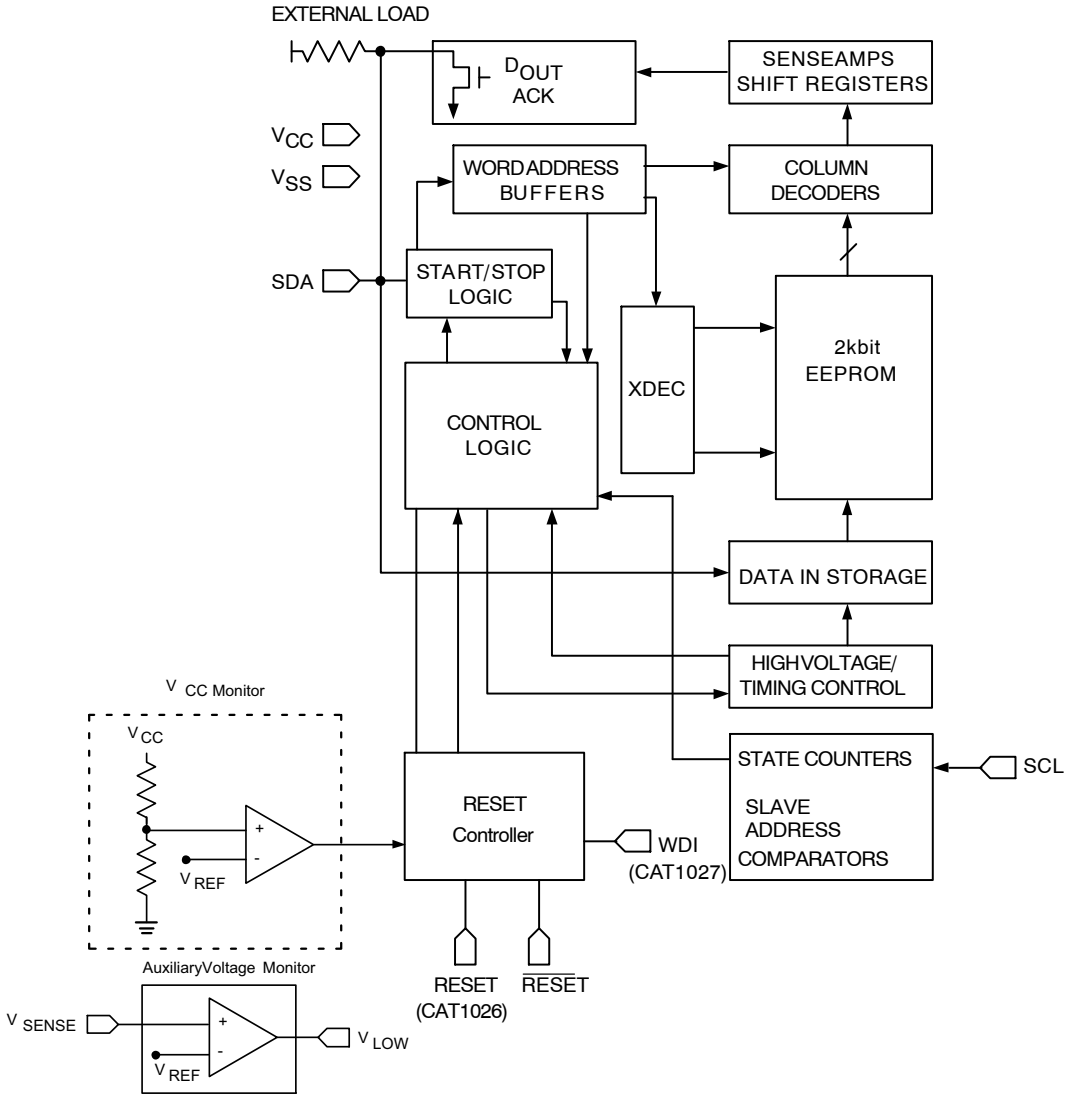
Publication Order Number:
CAT1026/D

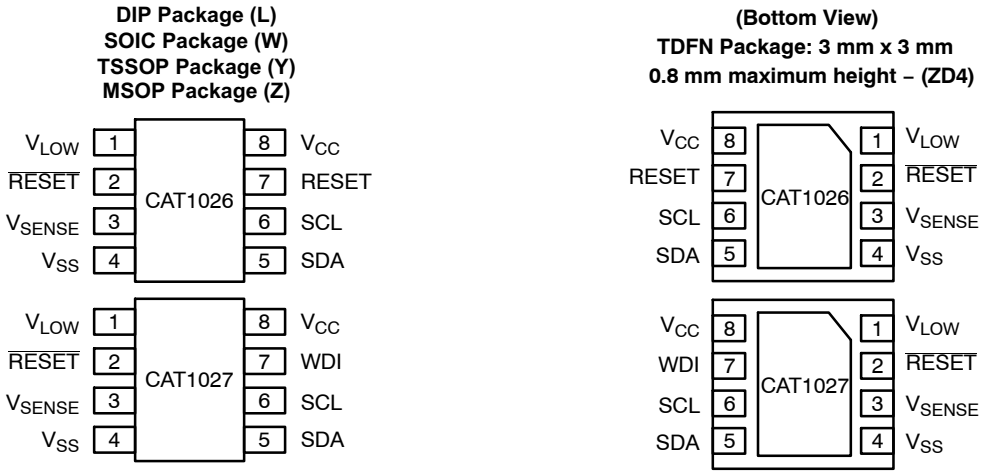
**Table 1. RESET THRESHOLD OPTION**

| Part Dash Number | Minimum Threshold | Maximum Threshold |
|---|---|---|
| −45 | 4.50 | 4.75 |
| −42 | 4.25 | 4.50 |
| −30 | 3.00 | 3.15 |
| −28 | 2.85 | 3.00 |
| −25 | 2.55 | 2.70 |

## BLOCK DIAGRAM



## PIN CONFIGURATION




## PIN DESCRIPTION

**RESET/$\overline{\text{RESET}}$**: RESET OUTPUTs (RESET CAT1026 Only)

These are open drain pins and $\overline{\text{RESET}}$ can be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull−down resistor, and the $\overline{\text{RESET}}$ pin must be connected through a pull−up resistor.

**SDA**: SERIAL DATA ADDRESS

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs.

**SCL**: SERIAL CLOCK

Serial clock input.

**$V_{SENSE}$** : AUXILIARY VOLTAGE MONITOR INPUT

The $V_{SENSE}$ input is a second voltage monitor which is compared against CAT1026 and CAT1027 internal reference voltage of 1.25 V typically. Whenever the input voltage is lower than 1.25 V, the open drain $V_{LOW}$ output will be driven low. An external resistor divider is used to set the voltage level to be sensed. Connect $V_{SENSE}$ to $V_{CC}$ if unused.

**$V_{LOW}$** : AUXILIARY VOLTAGE MONITOR OUTPUT

This open drain output goes low when $V_{SENSE}$ is less than 1.25 V and goes high when $V_{SENSE}$ exceeds the reference voltage.

**WDI** (CAT1027 Only): WATCHDOG TIMER INTERRUPT

Watchdog Timer Interrupt Input is used to reset the watchdog timer. If a transition from high to low or low to high does not occur every 1.6 seconds, the RESET outputs will be driven active.

**Table 2. PIN FUNCTION**

| Pin Name | Function |
|---|---|
| $\overline{\text{RESET}}$ | Active Low Reset Input/Output |
| $V_{SS}$ | Ground |
| SDA | Serial Data/Address |
| SCL | Clock Input |
| RESET | Active High Reset Output (CAT1026 Only) |
| $V_{CC}$ | Power Supply |
| $V_{SENSE}$ | Auxiliary Voltage Monitor Input |
| $V_{LOW}$ | Auxiliary Voltage Monitor Output |
| WDI | Watchdog Timer Interrupt (CAT1027 Only) |

**Table 3. OPERATING TEMPERATURE RANGE**

| | |
|---|---|
| Industrial | −40°C to 85°C |
| Extended | −40°C to 125°C |

**Table 4. CAT102X FAMILY OVERVIEW**

| Device | Manual Reset Input Pin | Watchdog | Watchdog Monitor Pin | Write Protection Pin | Independent Auxiliary Voltage Sense | RESET: Active High and LOW | EEPROM |
|---|---|---|---|---|---|---|---|
| CAT1021 | ✓ | ✓ | SDA | ✓ | | ✓ | 2k |
| CAT1022 | ✓ | ✓ | SDA | | | | 2k |
| CAT1023 | ✓ | ✓ | WDI | | | ✓ | 2k |
| CAT1024 | ✓ | | | | | | 2k |
| CAT1025 | ✓ | | | ✓ | | ✓ | 2k |
| CAT1026 | | | | | ✓ | ✓ | 2k |
| CAT1027 | | ✓ | WDI | | ✓ | | 2k |

NOTE: For supervisory circuits with embedded 16k EEPROM, please refer to the CAT1161, CAT1162 and CAT1163 data sheets.

## SPECIFICATIONS

**Table 5. ABSOLUTE MAXIMUM RATINGS**

| Parameters | Ratings | Units |
|---|---|---|
| Temperature Under Bias | –55 to +125 | °C |
| Storage Temperature | –65 to +150 | °C |
| Voltage on any Pin with Respect to Ground (Note 1) | –2.0 to $V_{CC}$ + 2.0 | V |
| $V_{CC}$ with Respect to Ground | –2.0 to 7.0 | V |
| Package Power Dissipation Capability ($T_A$ = 25°C) | 1.0 | W |
| Lead Soldering Temperature (10 s) | 300 | °C |
| Output Short Circuit Current (Note 2) | 100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ +0.5 V, which may overshoot to $V_{CC}$ +2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

**Table 6. D.C. OPERATING CHARACTERISTICS**

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions unless otherwise specified.

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | –2 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | –10 | | 10 | μA |
| $I_{CC1}$ | Power Supply Current (Write) | $f_{SCL}$ = 400 kHz<br>$V_{CC}$ = 5.5 V | | | | 3 | mA |
| $I_{CC2}$ | Power Supply Current (Read) | $f_{SCL}$ = 400 kHz<br>$V_{CC}$ = 5.5 V | | | | 1 | mA |
| $I_{SB}$ | Standby Current | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = GND or $V_{CC}$ | CAT1026 | | | 50 | μA |
| | | | CAT1027 | | | 60 | μA |
| $V_{IL}$ (Note 3) | Input Low Voltage | | | –0.5 | | 0.3 x $V_{CC}$ | V |
| $V_{IH}$ (Note 3) | Input High Voltage | | | 0.7 x $V_{CC}$ | | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage<br>(SDA, $\overline{\text{RESET}}$) | $I_{OL}$ = 3 mA<br>$V_{CC}$ = 2.7 V | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage<br>(RESET) | $I_{OH}$ = –0.4 mA<br>$V_{CC}$ = 2.7 V | | $V_{CC}$ – 0.75 | | | V |

**Table 6. D.C. OPERATING CHARACTERISTICS**

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{TH}$ | Reset Threshold | CAT102x−45 ($V_{CC}$ = 5.0 V) | 4.50 | | 4.75 | V |
| | | CAT102x−42 ($V_{CC}$ = 5.0 V) | 4.25 | | 4.50 | |
| | | CAT102x−30 ($V_{CC}$ = 3.3 V) | 3.00 | | 3.15 | |
| | | CAT102x−28 ($V_{CC}$ = 3.3 V) | 2.85 | | 3.00 | |
| | | CAT102x−25 ($V_{CC}$ = 3.0 V) | 2.55 | | 2.70 | |
| $V_{RVALID}$ | Reset Output Valid $V_{CC}$ Voltage | | 1.00 | | | V |
| $V_{RT}$ (Note 4) | Reset Threshold Hysteresis | | 15 | | | mV |
| $V_{REF}$ | Auxiliary Voltage Monitor Threshold | | 1.2 | 1.25 | 1.3 | VS |

3. $V_{IL}$ min and $V_{IH}$ max are reference values only and are not tested.
4. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.

**Table 7. CAPACITANCE**

$T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5 V

| Symbol | Test | Test Conditions | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ (Note 5) | Output Capacitance | $V_{OUT}$ = 0 V | 8 | pF |
| $C_{IN}$ (Note 5) | Input Capacitance | $V_{IN}$ = 0 V | 6 | pF |

**Table 8. AC CHARACTERISTICS**

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

**Memory Read & Write Cycle** (Note 6)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | 400 | kHz |
| $t_{SP}$ | Input Filter Spike Suppression (SDA, SCL) | | 100 | ns |
| $t_{LOW}$ | Clock Low Period | 1.3 | | μs |
| $t_{HIGH}$ | Clock High Period | 0.6 | | μs |
| $t_R$ (Note 5) | SDA and SCL Rise Time | | 300 | ns |
| $t_F$ (Note 5) | SDA and SCL Fall Time | | 300 | ns |
| $t_{HD; STA}$ | Start Condition Hold Time | 0.6 | | μs |
| $t_{SU; STA}$ | Start Condition Setup Time (for a Repeated Start) | 0.6 | | μs |
| $t_{HD; DAT}$ | Data Input Hold Time | 0 | | ns |
| $t_{SU; DAT}$ | Data Input Setup Time | 100 | | ns |
| $t_{SU; STO}$ | Stop Condition Setup Time | 0.6 | | μs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 900 | ns |
| $t_{DH}$ | Data Out Hold Time | 50 | | ns |
| $t_{BUF}$ (Note 5) | Time the Bus must be Free Before a New Transmission Can Start | 1.3 | | μs |
| $t_{WC}$ (Note 7) | Write Cycle Time (Byte or Page) | | 5 | ms |

5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. Test Conditions according to “AC Test Conditions” table.
7. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

**Table 9. RESET CIRCUIT AC CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PURST}$ | Power−Up Reset Timeout | Note 2 | 130 | 200 | 270 | ms |
| $t_{RDP}$ | $V_{TH}$ to RESET output Delay | Note 3 | | | 5 | μs |
| $t_{GLITCH}$ | $V_{CC}$ Glitch Reject Pulse Width | Notes 4 and 5 | | | 30 | ns |
| $t_{WD}$ | Watchdog Timeout | Note 1 | 1.0 | 1.6 | 2.1 | s |
| $t_{RPD2}$ | $V_{SENSE}$ to $V_{LOW}$ Delay | Note 5 | | | 5 | μs |

**Table 10. POWER−UP TIMING** (Notes 6 and 7)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PUR}$ | Power−Up to Read Operation | | | | 270 | ms |
| $t_{PUW}$ | Power−Up to Write Operation | | | | 270 | ms |

**Table 11. AC TEST CONDITIONS**

| Parameter | Test Conditions |
|---|---|
| Input Pulse Voltages | 0.2 x $V_{CC}$ to 0.8 x $V_{CC}$ |
| Input Rise and Fall Times | 10 ns |
| Input Reference Voltages | 0.3 x $V_{CC}$ , 0.7 x $V_{CC}$ |
| Output Reference Voltages | 0.5 x $V_{CC}$ |
| Output Load | Current Source: $I_{OL}$ = 3 mA; $C_L$ = 100 pF |

**Table 12. RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Reference Test Method | Min | Max | Units |
|---|---|---|---|---|---|
| $N_{END}$ (Note 6) | Endurance | MIL−STD−883, Test Method 1033 | 1,000,000 | | Cycles/Byte |
| $T_{DR}$ (Note 6) | Data Retention | MIL−STD−883, Test Method 1008 | 100 | | Years |
| $V_{ZAP}$ (Note 6) | ESD Susceptibility | MIL−STD−883, Test Method 3015 | 2000 | | Volts |
| $I_{LTH}$ (Notes 6 & 8) | Latch−Up | JEDEC Standard 17 | 100 | | mA |

1. Test Conditions according to “AC Test Conditions” table.
2. Power−up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
3. Power−Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
4. $V_{CC}$ Glitch Reference Voltage = $V_{THmin}$; Based on characterization data
5. $0 < V_{SENSE} - V_{CC}$, $V_{LOW}$ Output Reference Voltage and Load according to “AC Test Conditions” Table.
6. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
7. $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified memory operation can be initiated.
8. Latch−up protection is provided for stresses up to 100 mA on input and output pins from −1 V to $V_{CC}$ + 1 V.

## DEVICE OPERATON

### Reset Controller Description

The CAT1026 and CAT1027 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power−up, the RESET outputs remain active until $V_{CC}$ reaches the $V_{TH}$ threshold and will continue driving the outputs for approximately 200 ms ($t_{PURST}$) after reaching $V_{TH}$. After the $t_{PURST}$ timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors.

During power−down, the RESET outputs will be active when $V_{CC}$ falls below $V_{TH}$. The $\overline{\text{RESET}}$ output will be valid so long as $V_{CC}$ is > 1.0 V ($V_{RVALID}$). The device is designed to ignore the fast negative going $V_{CC}$ transient pulses (glitches).

Reset output timing is shown in Figure 1.

### Manual Reset Capability

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 ms timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

### Monitoring Two Voltages

The CAT1026 and CAT1027 feature a second voltage sensor, $V_{SENSE}$, which drives the open drain $V_{LOW}$ output low whenever the input voltage is below 1.25 V. The auxiliary voltage monitor timing is shown in Figure 2.

By using an external resistor divider the sense circuitry can be set to monitor a second supply in the system. The circuit shown in Figure 3 provides an externally adjustable threshold voltage, $V_{TH_ADJ}$ to monitor the auxiliary voltage. The low leakage current at $V_{SENSE}$ allows the use of large value resistors, to reduce the system power consumption. The $V_{LOW}$ output can be externally connected to the RESET output to generate a reset condition when either of the supplies is invalid. In other applications, $V_{LOW}$ signal can be used to interrupt the system controller for an impending power failure notification.

### Data Protection

The CAT1026 and CAT1027 devices have been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when incorrect data is stored in a memory location which is assumed to hold correct data.

Whenever the device is in a Reset condition, the embedded EEPROM is disabled for all operations, including write operations. If the Reset output(s) are active, in progress communications to the EEPROM are aborted and no new communications are allowed. In this condition an internal write cycle to the memory can not be started, but an in progress internal nonvolatile memory write cycle can not be aborted. An internal write cycle initiated before the Reset condition can be successfully finished if there is enough time (5 ms) before $V_{CC}$ reaches the minimum value of 2 V.

In addition, to avoid data corruption due to the loss of power supply voltage during the memory internal write operation, the system controller should monitor the unregulated DC power. Using the second voltage sensor, $V_{SENSE}$, to monitor an unregulated power supply, the CAT1026 and CAT1027 signals an impending power failure by setting $V_{LOW}$ low.

### Watchdog Timer

The Watchdog Timer provides an independent protection for microcontrollers. During a system failure, the CAT1027 device will provide a reset signal after a time−out interval of 1.6 seconds for a lack of activity. CAT1027 is designed with the Watchdog timer feature on the WDI pin. If WDI does not toggle within 1.6 second intervals, the reset condition will be generated on reset output. The watchdog timer is cleared by any transition on monitored line.

As long as reset signal is asserted, the watchdog timer will not count and will stay cleared.

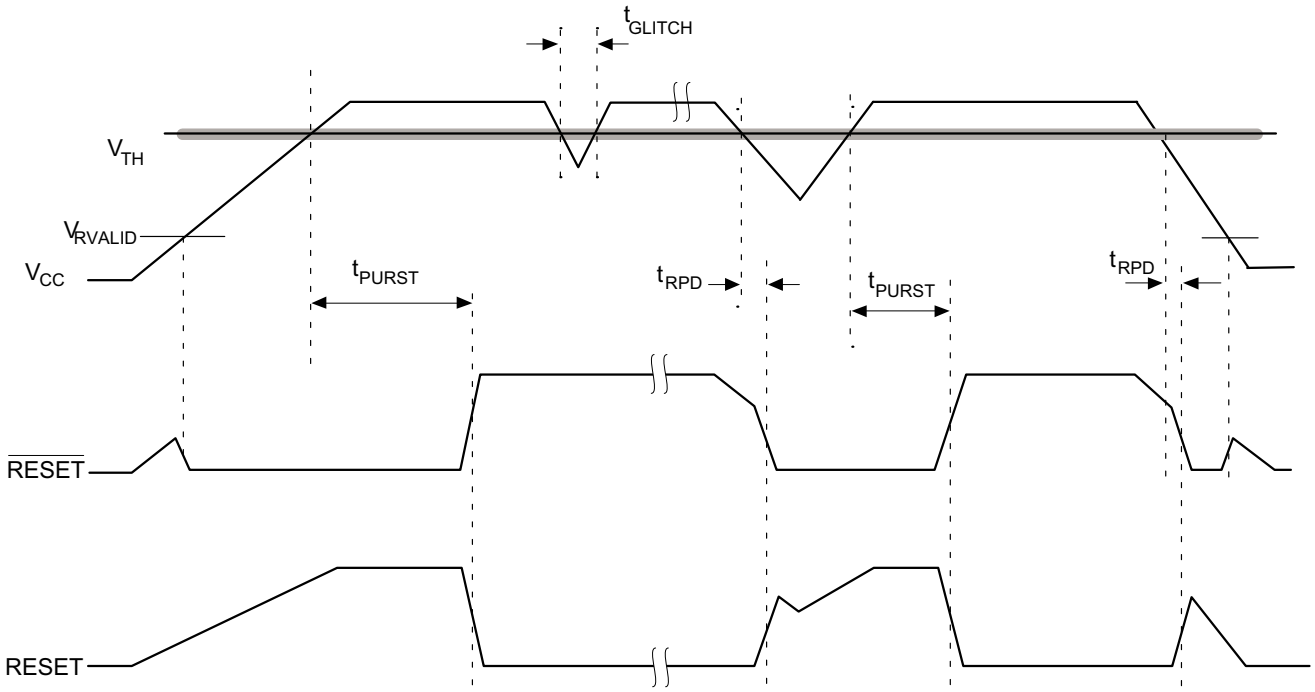



**Figure 1. RESET Output Timing**

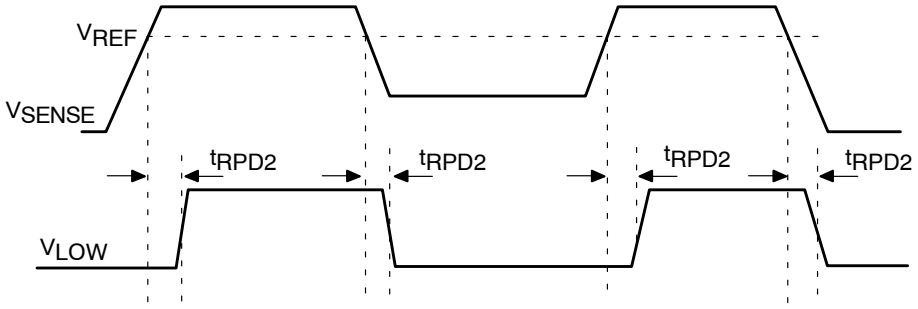
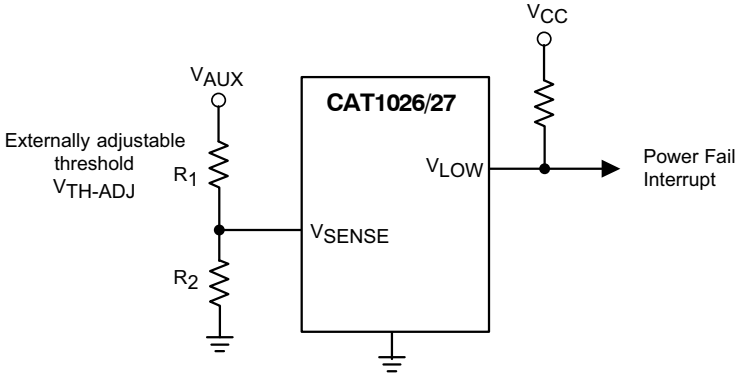



**Figure 2. Auxiliary Voltage Monitor Timing**




$$V_{TH\text{-}ADJ} = V_{REF} \times \frac{R_1 + R_2}{R_2} = 1.25V \times \frac{R_1 + R_2}{R_2}$$

**Figure 3. Auxiliary Voltage Monitor**

## EMBEDDED EEPROM OPERATON

The CAT1026 and CAT1027 feature a 2−kbit embedded serial EEPROM that supports the I$^2$C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

### I$^2$C Bus Protocol

The features of the I$^2$C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

### Start Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1026 and CAT1027 monitor the SDA and SCL lines and will not respond until this condition is met.

### Stop Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

## DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1026 and CAT1027 monitor the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1026 and CAT 1027 then perform a Read or Write operation depending on the R/$\overline{W}$ bit.

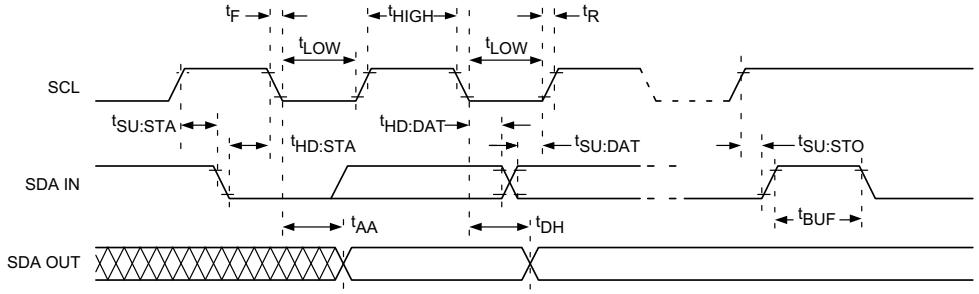



**Figure 4. Bus Timing**

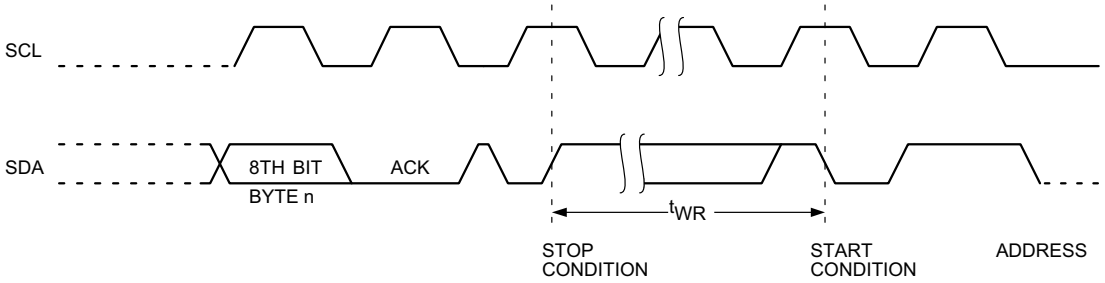



**Figure 5. Write Cycle Timing**

## ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1026 and CAT1027 respond with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT1026 and CAT1027 begin a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1026 and CAT1027 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

## WRITE OPERATIONS

### Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8−bit address that is to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1026 and CAT1027 acknowledge once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non−volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

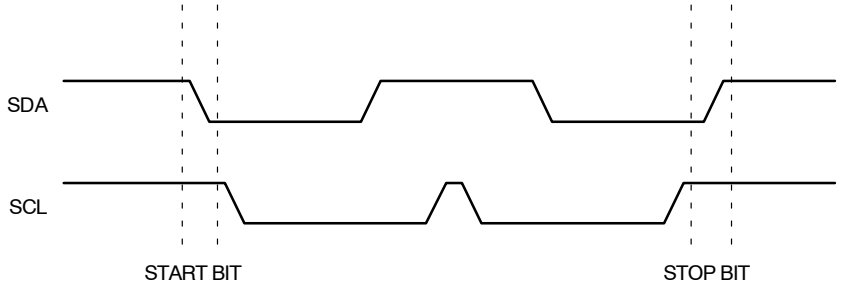



**Figure 6. Start/Stop Timing**

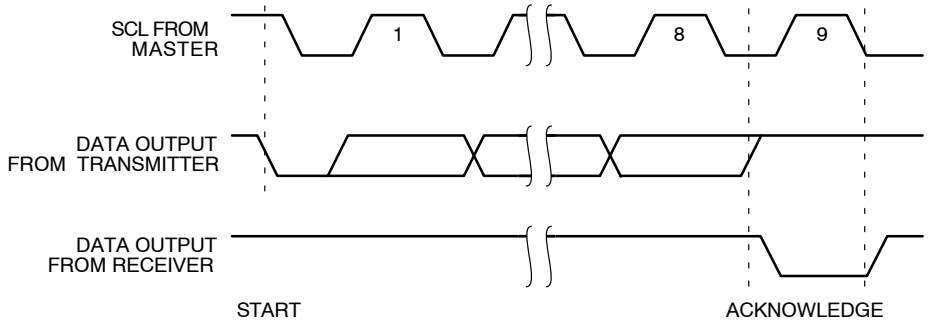



**Figure 7. Acknowledge Timing**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Default Configuration | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |

**Figure 8. Slave Address Bits**

### Page Write

The CAT1026 and CAT1027 write up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted, the CAT1026 and CAT1027 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 16 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1026 and CAT1027 in a single write cycle.

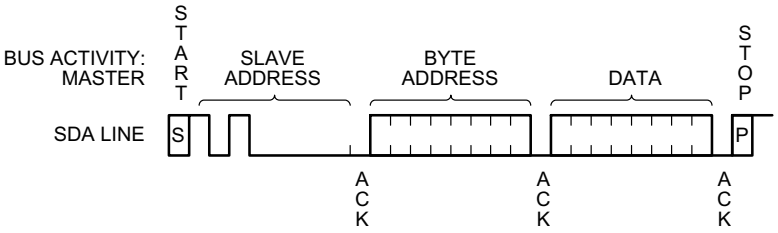



**Figure 9. Byte Write Timing**

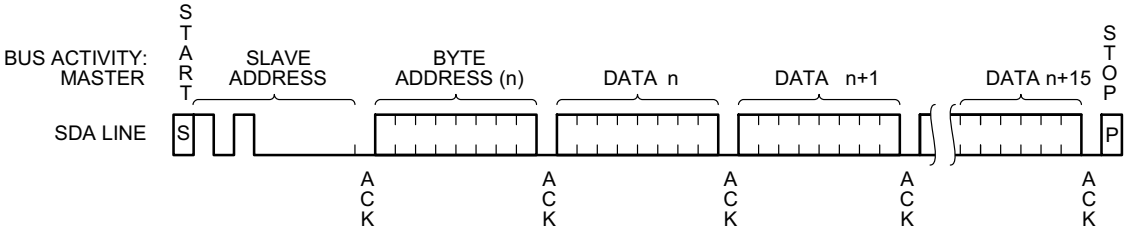



**Figure 10. Page Write Timing**

### Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT1026 and CAT1027 initiate the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

## READ OPERATIONS

The READ operation for the CAT1026 and CAT1027 is initiated in the same manner as the write operation with one exception, the R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

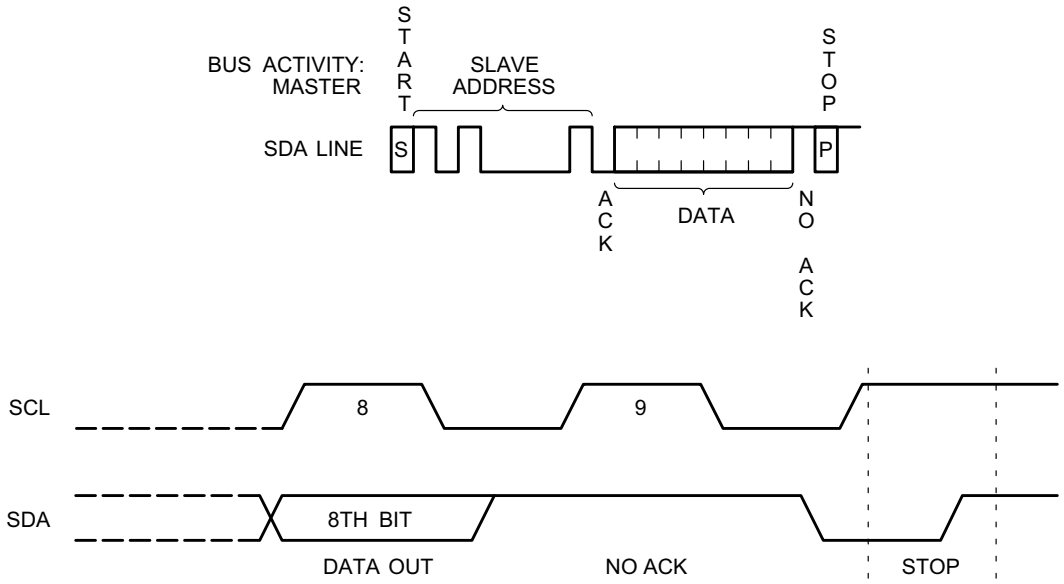



**Figure 11. Immediate Address Read Timing**

### Immediate/Current Address Read

The CAT1026 and CAT1027 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. For N = E = 255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1026 and CAT1027 receive its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8−bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

### Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1026 and CAT1027 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1026 and CAT1027 then respond with its acknowledge and send the 8−bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

### Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1026 and CAT1027 sends the initial 8− bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT1026 and CAT1027 will continue to output an 8−bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1026 and CAT1027 is sent sequentially with the data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT1026and CAT1027 address bits so that the entire memory array can be read during one operation.

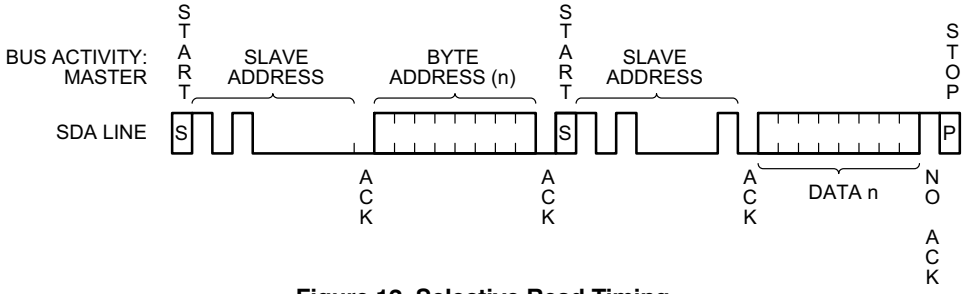



**Figure 12. Selective Read Timing**

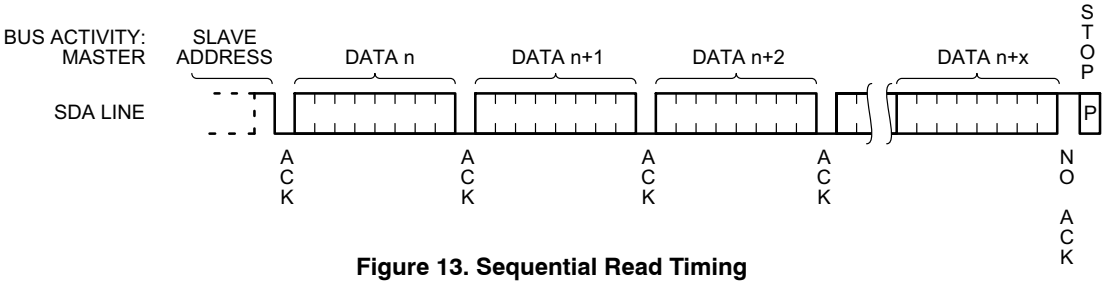



**Figure 13. Sequential Read Timing**

## ORDERING INFORMATION

| **Orderable Part Numbers – CAT1026 Series** (See Notes 1 – 5) | | | |
|---|---|---|---|
| Device | Reset Threshold | Package | Shipping |
| CAT1026LI−45−G | 4.50 V – 4.75 V | PDIP | 3000 Tape & Reel |
| CAT1026LI−42−G | 4.25 V – 4.50 V | | |
| CAT1026LI−30−G | 3.00 V – 3.15 V | | |
| CAT1026LI−28−G | 2.85 V – 3.00 V | | |
| CAT1026LI−25−G | 2.55 V – 2.70 V | | |
| CAT1026WI−45−GT3 | 4.50 V – 4.75 V | SOIC | |
| CAT1026WI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1026WI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1026WI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1026WI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1026YI−45−GT3 | 4.50 V – 4.75 V | TSSOP | |
| CAT1026YI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1026YI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1026YI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1026YI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1026ZI−45−GT3 | 4.50 V – 4.75 V | MSOP | |
| CAT1026ZI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1026ZI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1026ZI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1026ZI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1026ZD4I−45T3* | 4.50 V – 4.75 V | TDFN | |
| CAT1026ZD4I−42T3* | 4.25 V – 4.50 V | | |
| CAT1026ZD4I−30T3* | 3.00 V – 3.15 V | | |
| CAT1026ZD4I−28T3* | 2.85 V – 3.00 V | | |
| CAT1026ZD4I−25T3* | 2.55 V – 2.70 V | | |

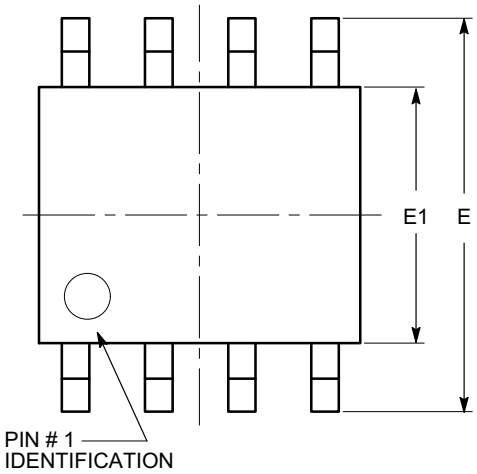
1. All packages are RoHS−compliant (Lead−free, Halogen−free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (−G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

| Orderable Part Numbers – CAT1027 Series (See Notes 1 – 5) | | | |
|---|---|---|---|
| Device | Reset Threshold | Package | Shipping |
| CAT1027LI–45–G | 4.50 V – 4.75 V | PDIP | 3000 Tape & Reel |
| CAT1027LI–42–G | 4.25 V – 4.50 V | | |
| CAT1027LI–30–G | 3.00 V – 3.15 V | | |
| CAT1027LI–28–G | 2.85 V – 3.00 V | | |
| CAT1027LI–25–G | 2.55 V – 2.70 V | | |
| CAT1027WI–45–GT3 | 4.50 V – 4.75 V | SOIC | |
| CAT1027WI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1027WI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1027WI–28–GT3 | 2.85 V – 3.00 V | | |
| CAT1027WI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1027YI–45–GT3 | 4.50 V – 4.75 V | TSSOP | |
| CAT1027YI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1027YI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1027YI–28–GT3 | 2.85 V – 3.00 V | | |
| CAT1027YI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1027ZI–45–GT3 | 4.50 V – 4.75 V | MSOP | |
| CAT1027ZI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1027ZI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1027ZI–28–GT3 | 2.85 V – 3.00 V | | |
| CAT1027ZI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1027ZD4I–45T3* | 4.50 V – 4.75 V | TDFN | |
| CAT1027ZD4I–42T3* | 4.25 V – 4.50 V | | |
| CAT1027ZD4I–30T3* | 3.00 V – 3.15 V | | |
| CAT1027ZD4I–28T3* | 2.85 V – 3.00 V | | |
| CAT1027ZD4I–25T3* | 2.55 V – 2.70 V | | |

1. All packages are RoHS–compliant (Lead–free, Halogen–free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (–G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

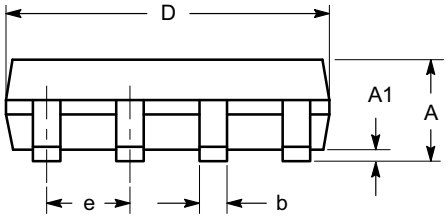
## PACKAGE DIMENSIONS

**SOIC 8, 150 mils**
CASE 751BD−01
ISSUE O

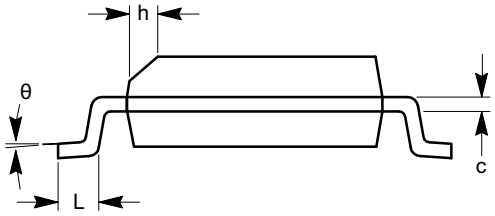



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |



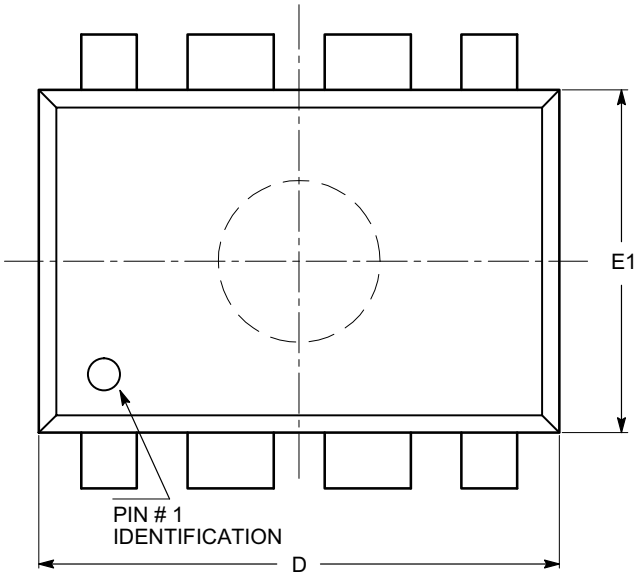

**SIDE VIEW**




**END VIEW**

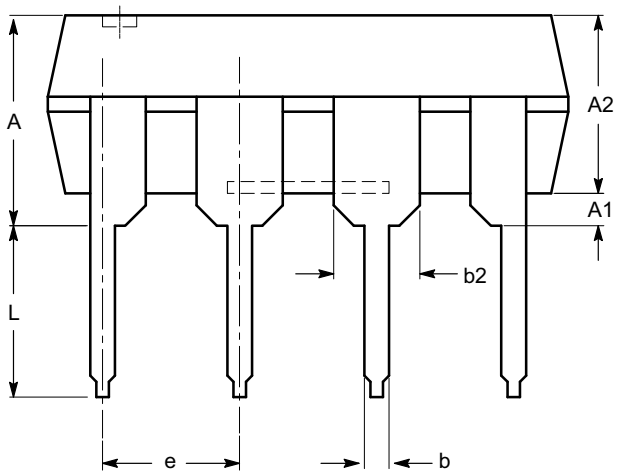
**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

**PDIP−8, 300 mils**
CASE 646AA−01
ISSUE A

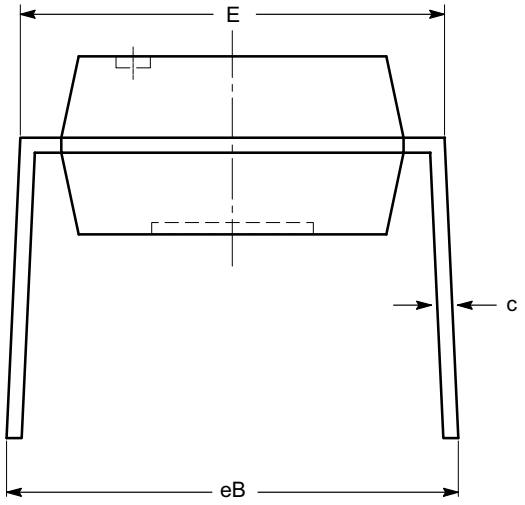



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| E1 | 6.10 | 6.35 | 7.11 |
| e | | 2.54 BSC | |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |

**TOP VIEW**



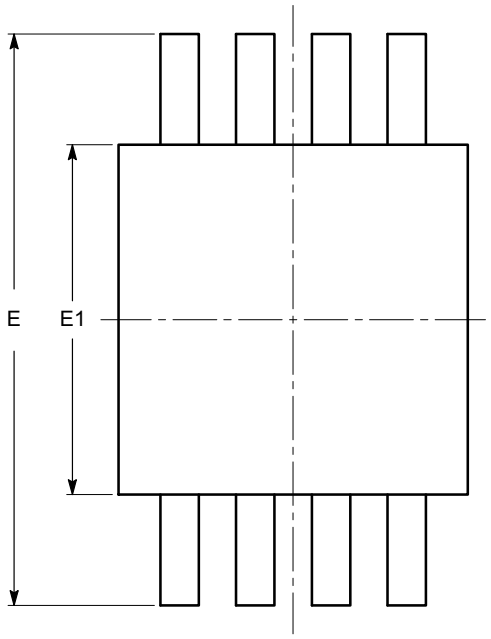

**SIDE VIEW**




**END VIEW**

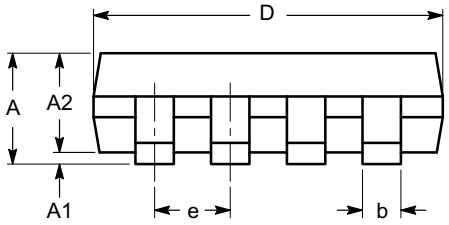
**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

**MSOP 8, 3x3**
CASE 846AD−01
ISSUE O

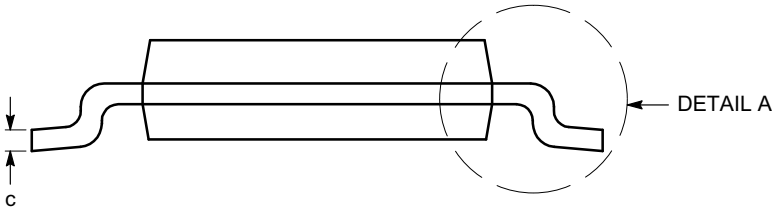



**TOP VIEW**

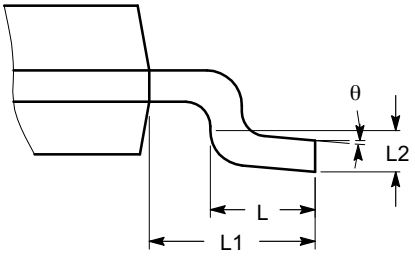
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.22 | | 0.38 |
| c | 0.13 | | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.65 BSC | | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | 0.95 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0º | | 6º |




**SIDE VIEW**



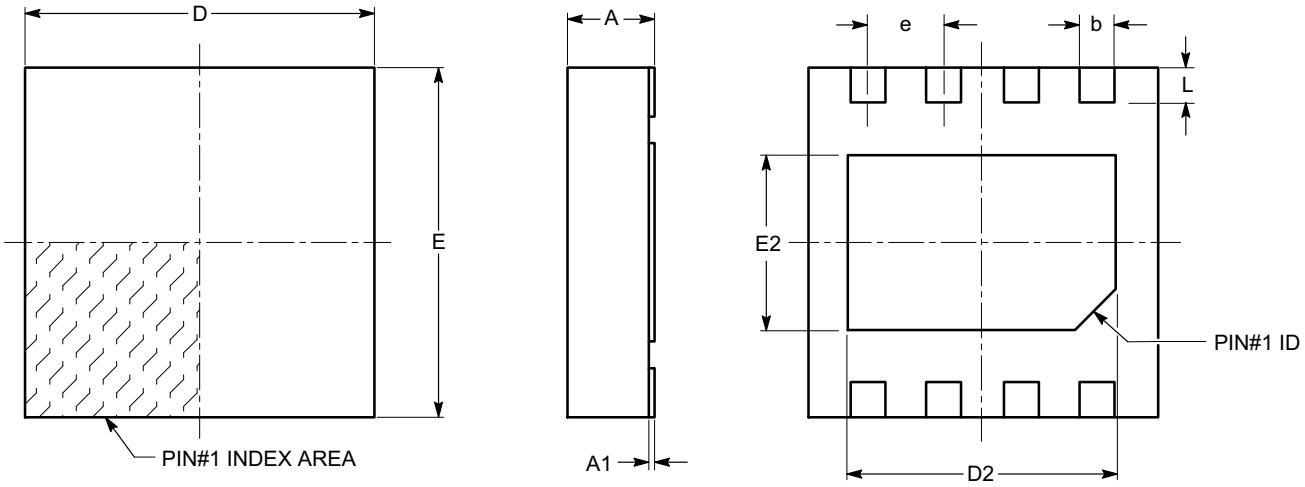

**END VIEW**




**DETAIL A**

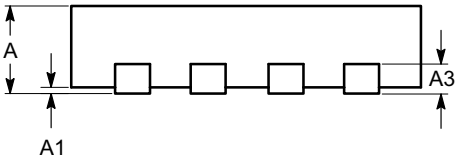
**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

**TDFN8, 3x3**
CASE 511AL−01
ISSUE A




**TOP VIEW** **SIDE VIEW** **BOTTOM VIEW**

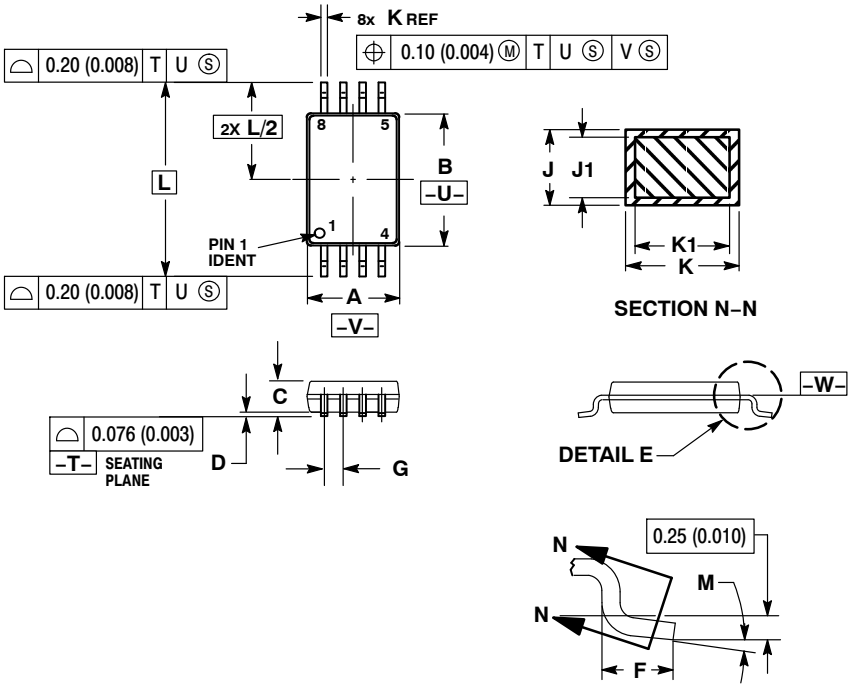
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.23 | 0.30 | 0.37 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.20 | −−− | 2.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.40 | −−− | 1.80 |
| e | | 0.65 TYP | |
| L | 0.20 | 0.30 | 0.40 |




**FRONT VIEW**

**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

**TSSOP−8**
CASE 948S−01
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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CAT1027PI-42 CAT1027PI-45 CAT1027UE-28-TE13 CAT1026UE-30-TE13 CAT1026UI-30-TE13 CAT1027UI-28-TE13 CAT1027SE-42 CAT1027SE-45 CAT1026RI-25-TE13 CAT1027PE-42-TE13 CAT1026RE-25-TE13 CAT1027PI-42-TE13 CAT1026RE-28 CAT1026RE-25 CAT1027SE-25 CAT1027SE-42-TE13 CAT1027SE-30 CAT1027SE-28 CAT1027SI-42-TE13 CAT1026UI-42-TE13 CAT1026UE-42-TE13 CAT1026RE-42-TE13 CAT1026RI-42-TE13 CAT1026PI-42-TE13 CAT1026PE-42-TE13 CAT1026RI-45-TE13 CAT1026RE-45-TE13 CAT1026SI-28 CAT1027UE-45-TE13 CAT1027UI-45-TE13 CAT1026SI-25 CAT1026SE-30-TE13 CAT1026SI-30-TE13 CAT1027PI-25-TE13 CAT1027PE-25-TE13 CAT1026UI-30 CAT1026UI-25 CAT1026UI-45 CAT1026UI-42 CAT1026UI-28 CAT1027SI-25-TE13 CAT1027SE-25-TE13 CAT1027RI-25-TE13 CAT1027RE-25-TE13 CAT1026SE-28-TE13 CAT1026SI-28-TE13 CAT1027UE-42-TE13 CAT1027UI-42-TE13 CAT1027UE-30 CAT1027PE-42 CAT1027PE-45 CAT1027PI-45-TE13 CAT1027PE-45-TE13 CAT1027SE-28-TE13 CAT1027SI-28-TE13 CAT1027RE-30 CAT1026SE-42-TE13 CAT1026SI-42-TE13 CAT1027RE-42 CAT1027RE-28 CAT1027RE-45 CAT1027RE-25 CAT1027PI-30 CAT1027PI-28 CAT1027PI-25 CAT1027UI-45 CAT1027UI-25 CAT1027UI-42 CAT1027UI-30 CAT1027UI-28 CAT1026RI-45 CAT1026RI-28 CAT1026RI-42 CAT1026RI-25 CAT1026PE-30 CAT1027RE-42-TE13 CAT1027RI-42-TE13 CAT1026PI-28 CAT1026PI-30 CAT1026PI-25 CAT1027UE-30-TE13 CAT1026PI-45 CAT1026PI-42 CAT1027UI-30-TE13 CAT1027UE-25-TE13 CAT1027UI-25-TE13 CAT1027SI-30 CAT1027SI-28 CAT1027SI-42 CAT1027SI-45 CAT1027SI-25 CAT1027SI-30-TE13 CAT1027SE-30-TE13 CAT1027RI-45 CAT1027RI-42 CAT1027RI-28 CAT1027RI-25 CAT1026RI-30 CAT1027PE-28-TE13 CAT1027PI-28-TE13