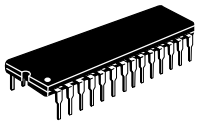
CAT28LV65

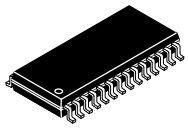
64 kb CMOS Parallel EEPROM

ON Semiconductor®

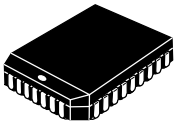
http://onsemi.com



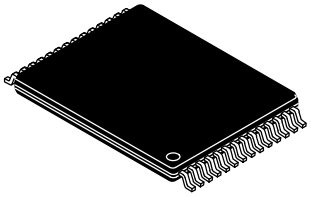
PDIP−28
P, L SUFFIX
CASE 646AE



SOIC−28
J, K, W, X SUFFIX
CASE 751BM



PLCC−32
N, G SUFFIX
CASE 776AK



TSOP−28
H13 SUFFIX
CASE 318AE

Description

The CAT28LV65 is a low voltage, low power, CMOS Parallel EEPROM organized as 8K x 8−bits. It requires a simple interface for in−system programming. On−chip address and data latches, self−timed write cycle with auto−clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling, RDY/$\overline{\text{BUSY}}$ and Toggle status bit signal the start and end of the self−timed write cycle. Additionally, the CAT28LV65 features hardware and software write protection.

The CAT28LV65 is manufactured using ON Semiconductor's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28−pin DIP, 28−pin TSOP, 28−pin SOIC or 32−pin PLCC packages.

Features

- 3.0 V to 3.6 V Supply
- Read Access Times:
  - 150/200/250 ns
- Low Power CMOS Dissipation:
  - Active: 8 mA Max.
  - Standby: 100 μA Max.
- Simple Write Operation:
  - On−chip Address and Data Latches
  - Self−timed Write Cycle with Auto−clear
- Fast Write Cycle Time:
  - 5 ms Max.
- Commercial, Industrial and Automotive Temperature Ranges
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - 1 to 32 bytes in 5 ms
  - Page Load Timer
- End of Write Detection:
  - Toggle Bit
  - $\overline{\text{DATA}}$ Polling
  - RDY/$\overline{\text{BUSY}}$
- Hardware and Software Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN FUNCTION

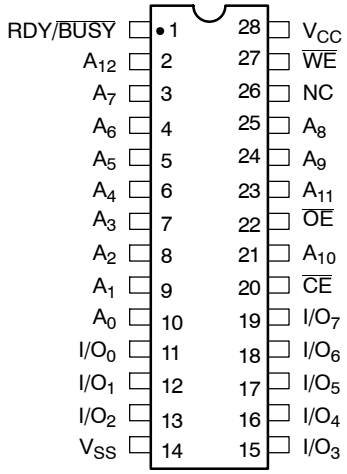
Pin Name	Function
A_0−A_{12}	Address Inputs
I/O_0−I/O_7	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
RDY/$\overline{\text{BSY}}$	Ready/$\overline{\text{BUSY}}$ Status
$\overline{\text{WE}}$	Write Enable
V_{CC}	3.0 V to 3.6 V Supply
V_{SS}	Ground
NC	No Connect

ORDERING INFORMATION

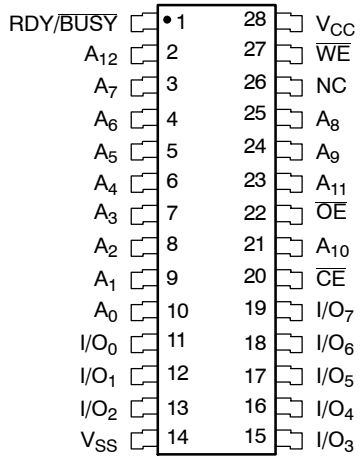
See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

PIN CONFIGURATIONS

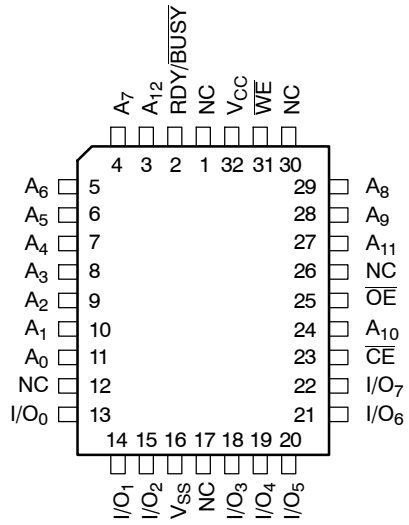
DIP Package (P, L)



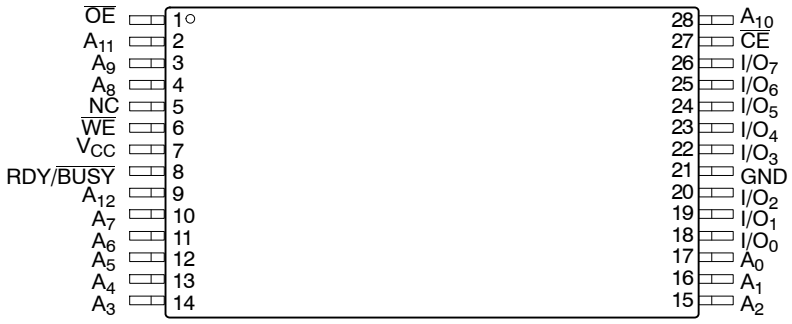
SOIC Package (J, K, W, X)



PLCC Package (N, G)



TSOP Package (8 mm x 13.4 mm) (H13)



(Top Views)

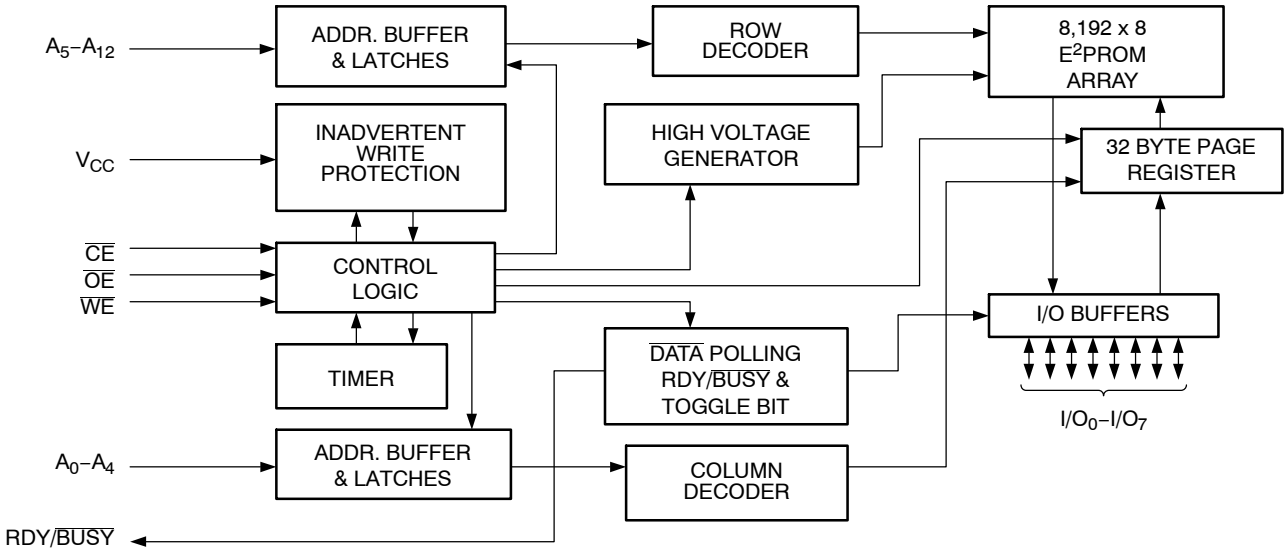


Figure 1. Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−2.0 V to +V_{CC} + 2.0 V	V
V_{CC} with Respect to Ground	−2.0 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 secs)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

Table 2. RELIABILITY CHARACTERISTICS (Note 3)

Symbol	Parameter	Test Method	Min	Max	Units
N_{END}	Endurance	MIL−STD−883, Test Method 1033	10^5		Cycles/Byte
T_{DR}	Data Retention	MIL−STD−883, Test Method 1008	100		Years
V_{ZAP}	ESD Susceptibility	MIL−STD−883, Test Method 3015	2,000		V
I_{LTH} (Note 4)	Latch−Up	JEDEC Standard 17	100		mA

3. These parameters are tested initially and after a design or process change that affects the parameters.
4. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V.

Table 3. MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby and Write Inhibit	H	X	X	High−Z	STANDBY
Read and Write Inhibit	X	H	H	High−Z	ACTIVE

Table 4. CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Test	Max	Conditions	Units
$C_{I/O}$ (Note 5)	Input/Output Capacitance	10	$V_{I/O}$ = 0 V	pF
C_{IN} (Note 5)	Input Capacitance	6	V_{IN} = 0 V	pF

5. This parameter is tested initially and after a design or process change that affects the parameter.

Table 5. D.C. OPERATING CHARACTERISTICS (V_{CC} = 3.0 V to 3.6 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{CC}	V_{CC} Current (Operating, TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open			8	mA
I_{SBC} (Note 6)	V_{CC} Current (Standby, CMOS)	$\overline{CE}$ = V_{IHC}, All I/O's Open			100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	−1		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}	−5		5	μA
V_{IH} (Note 6)	High Level Input Voltage		2		V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage		−0.3		0.6	V
V_{OH}	High Level Output Voltage	I_{OH} = −100 μA	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.0 mA			0.3	V
V_{WI}	Write Inhibit Voltage		2			V

6. V_{IHC} = V_{CC} − 0.3 V to V_{CC} + 0.3 V.

Table 6. A.C. CHARACTERISTICS, READ CYCLE (V_{CC} = 3.0 V to 3.6 V, unless otherwise specified.)

Symbol	Parameter	28LV65−15		28LV65−20		28LV65−25		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	$\overline{CE}$ Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	$\overline{OE}$ Access Time		70		80		100	ns
t_{LZ} (Note 7)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ} (Note 7)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ} (Notes 7, 8)	$\overline{CE}$ High to High−Z Output		50		50		55	ns
t_{OHZ} (Notes 7, 8)	$\overline{OE}$ High to High−Z Output		50		50		55	ns
t_{OH} (Note 7)	Output Hold from Address Change	0		0		0		ns

7. This parameter is tested initially and after a design or process change that affects the parameter.
8. Output floating (High−Z) is defined as the state when the external data line is no longer driven by the output buffer.

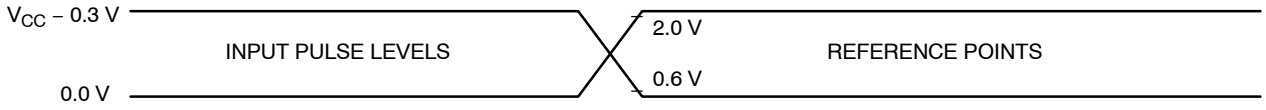
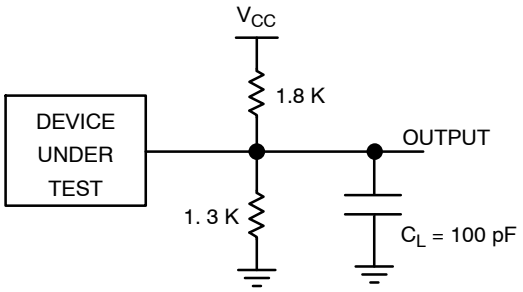


Figure 2. A.C. Testing Input/Output Waveform (Note 9)

9. Input rise and fall times (10% and 90%) < 10 ns.



C_L INCLUDES JIG CAPACITANCE

Figure 3. A.C. Testing Load Circuit (example)

Table 7. A.C. CHARACTERISTICS, WRITE CYCLE (V_{CC} = 3.0 V to 3.6 V, unless otherwise specified.)

Symbol	Parameter	28LV65−15		28LV65−20		28LV65−25		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{CW} (Note 10)	$\overline{CE}$ Pulse Time	110		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	0		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		10		10		ns
t_{WP} (Note 10)	$\overline{WE}$ Pulse Width	110		150		150		ns
t_{DS}	Data Setup Time	60		100		100		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT} (Note 11)	Write Inhibit Period After Power−up	5	10	5	10	5	10	ms
t_{BLC} (Notes 11, 12)	Byte Load Cycle Time	0.05	100	0.1	100	0.1	100	μs
t_{RB}	$\overline{WE}$ Low to RDY/$\overline{BUSY}$ Low		220		220		220	ns

10. A write pulse of less than 20 ns duration will not initiate a write cycle.
11. This parameter is tested initially and after a design or process change that affects the parameter.
12. A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

Read

Data stored in the CAT28LV65 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2−line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

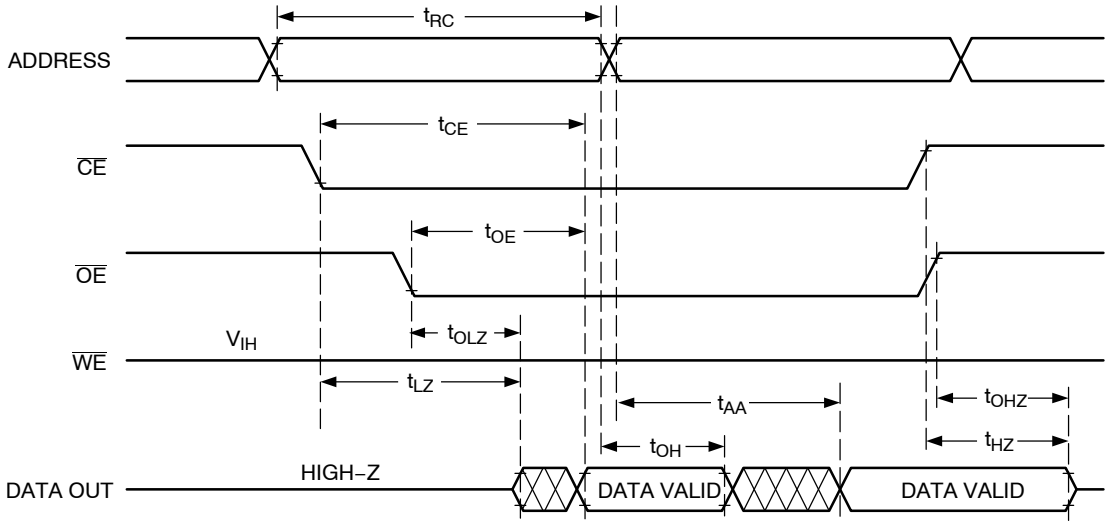


Figure 4. Read Cycle

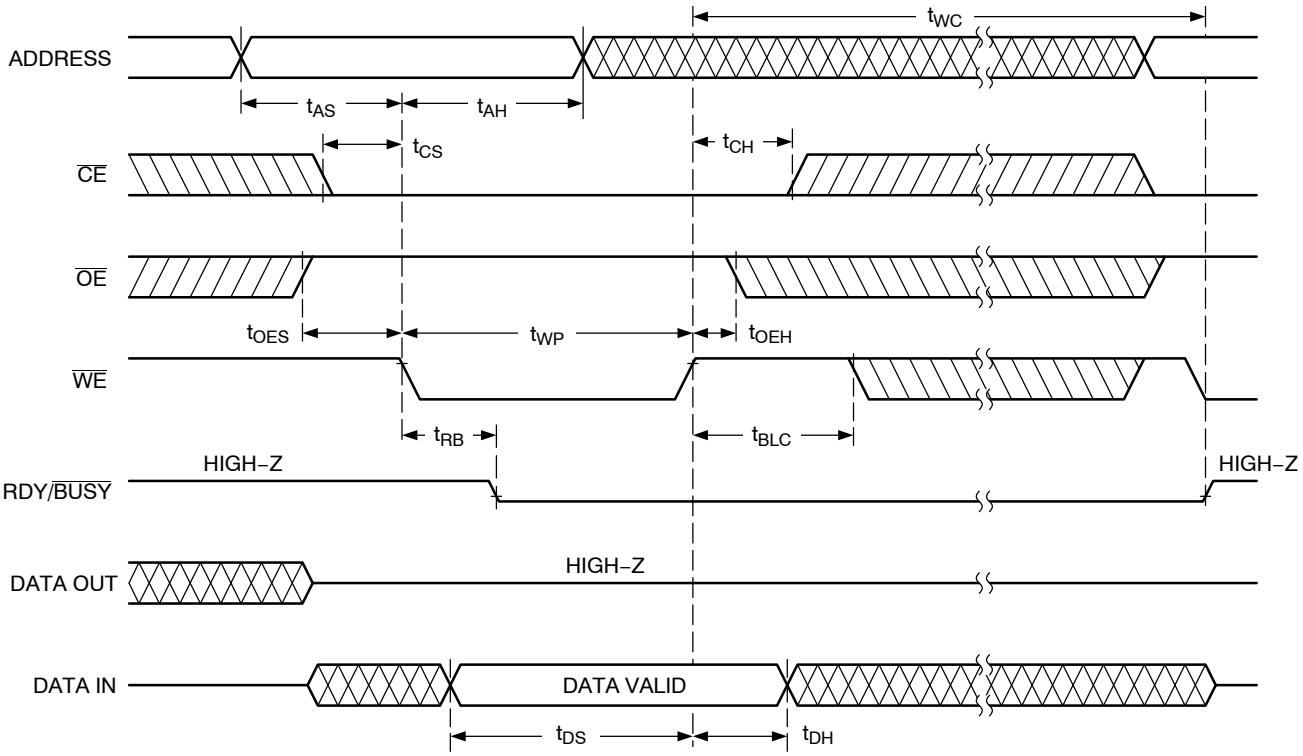


Figure 5. Byte Write Cycle [$\overline{WE}$ Controlled]

Page Write

The page write mode of the CAT28LV65 (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single EEPROM write cycle. This effectively reduces the byte−write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\,MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\,MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\,MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

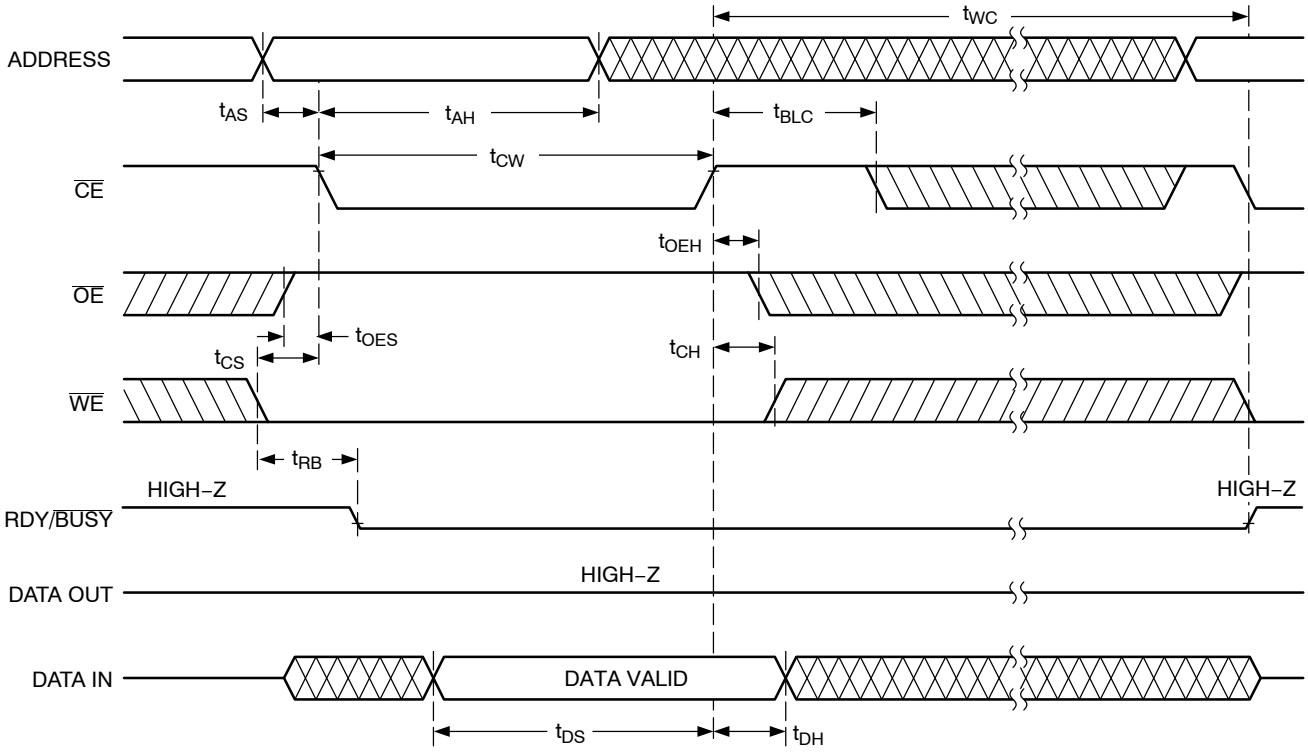


Figure 6. Byte Write Cycle [$\overline{CE}$ Controlled]

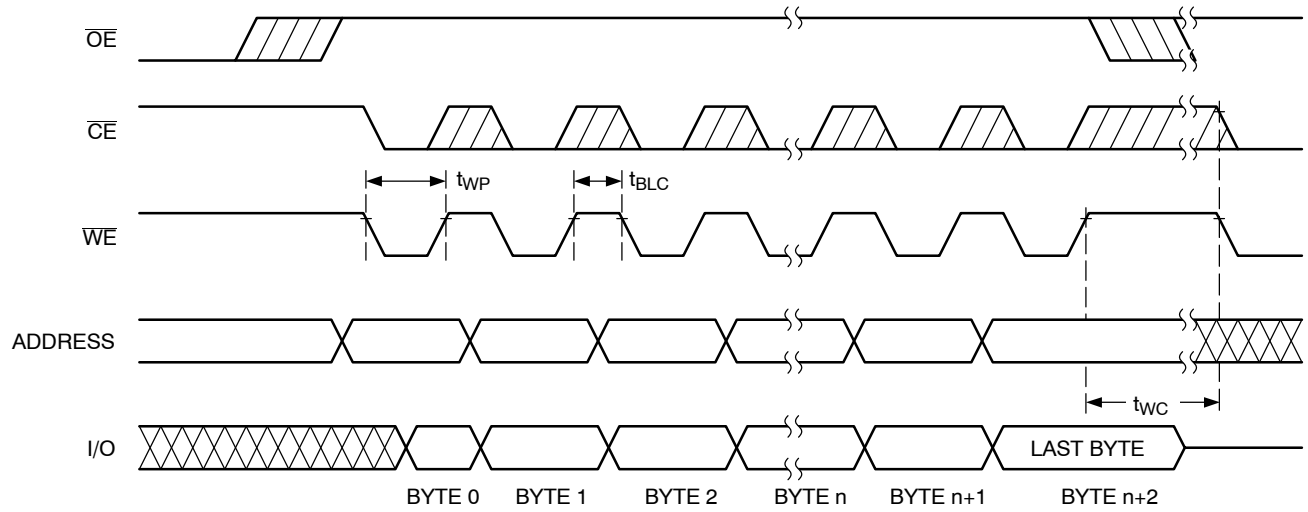


Figure 7. Page Mode Write Cycle

$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self−timed write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Ready/$\overline{\text{BUSY}}$ (RDY/$\overline{\text{BUSY}}$)

The RDY/$\overline{\text{BUSY}}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR−tied to the same RDY/$\overline{\text{BUSY}}$ line.

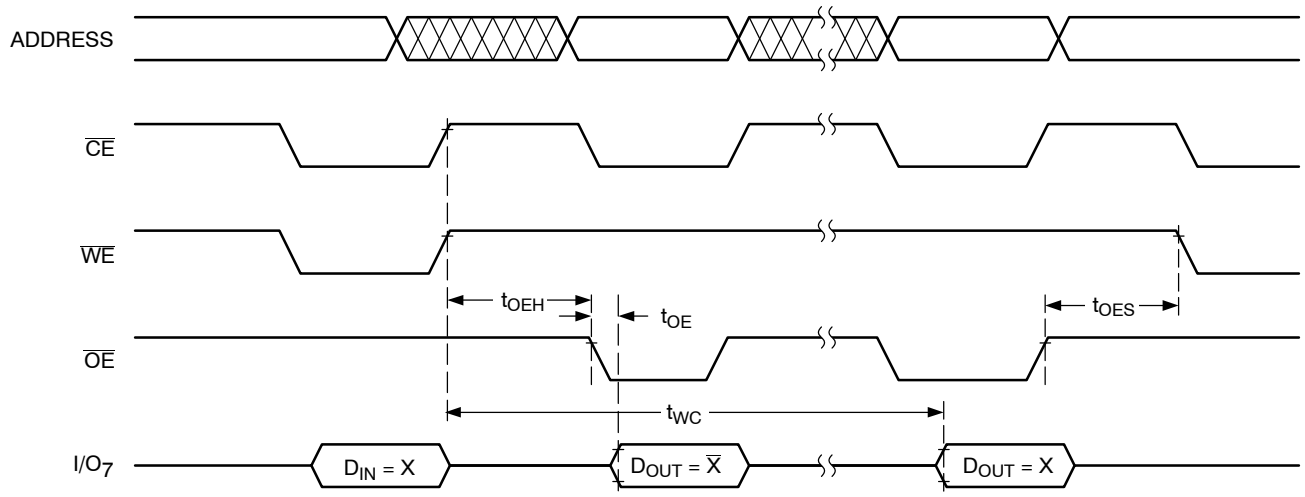


Figure 8. $\overline{\text{DATA}}$ Polling

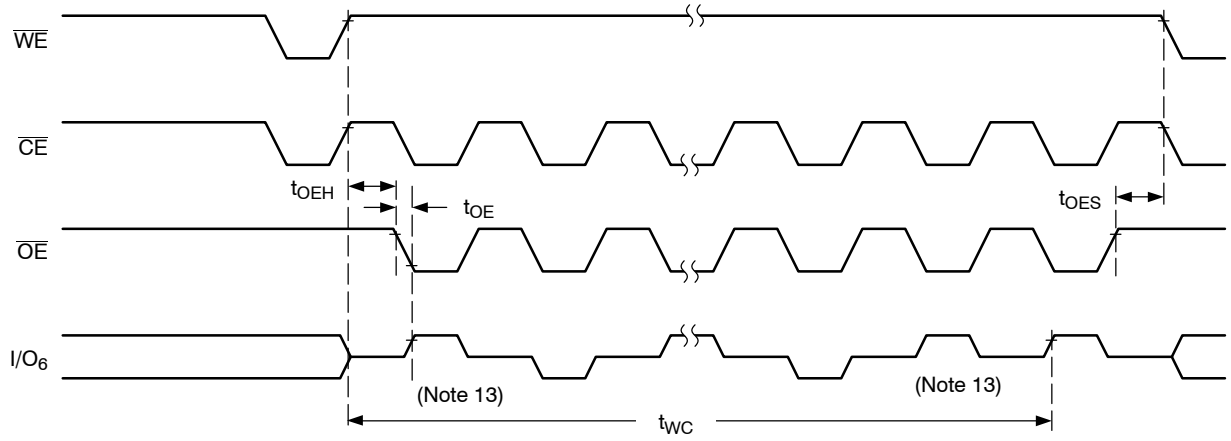


Figure 9. Toggle Bit

13. Beginning and ending state of I/O_6 is indeterminate.

Hardware Data Protection

The following is a list of hardware data protection features that are incorporated into the CAT28LV65.

1. V_{CC} sense provides for write protection when V_{CC} falls below 2.0 V min.
2. A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 2.40 V min.
3. Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.
4. Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

Software Data Protection

The CAT28LV65 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from ON Semiconductor with the software protection NOT ENABLED (the CAT28LV65 is in the standard operating mode).

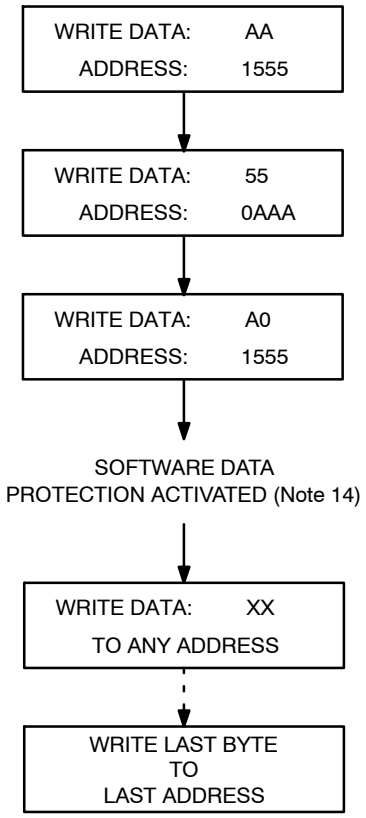


Figure 10. Write Sequence for Activating Software Data Protection

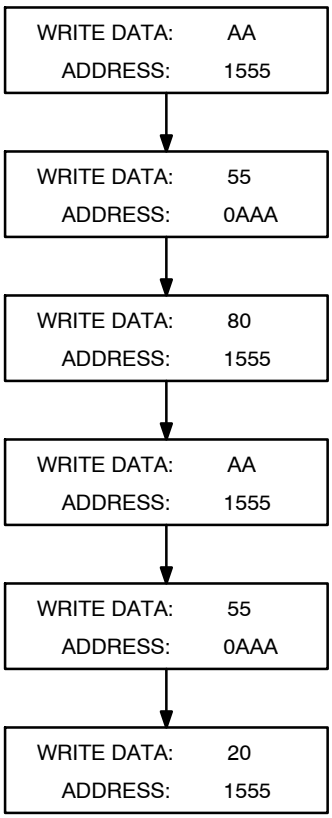


Figure 11. Write Sequence for Deactivating Software Data Protection

14. Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

Software Data Protection

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 10). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 12). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power−up in addition to the hardware protection provided.

To allow the user the ability to program the device with an EEPROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 11) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 13 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

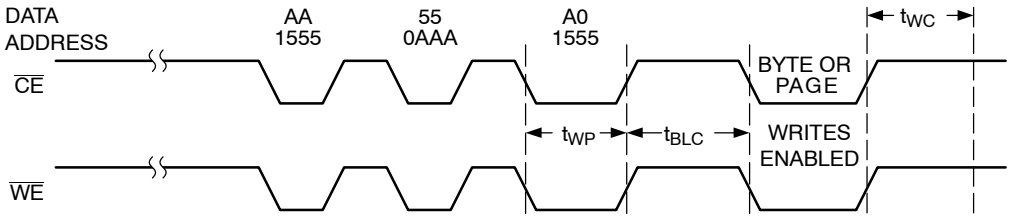


Figure 12. Software Data Protection Timing

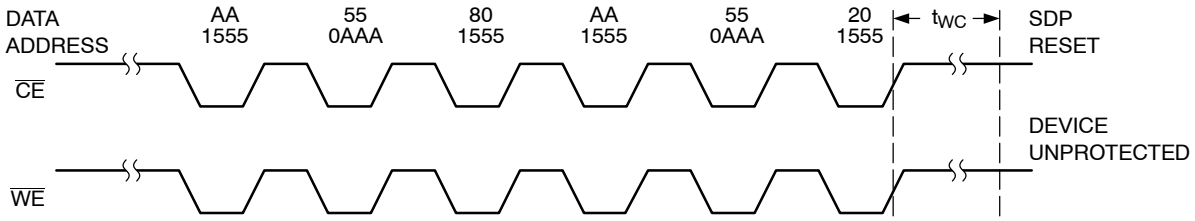
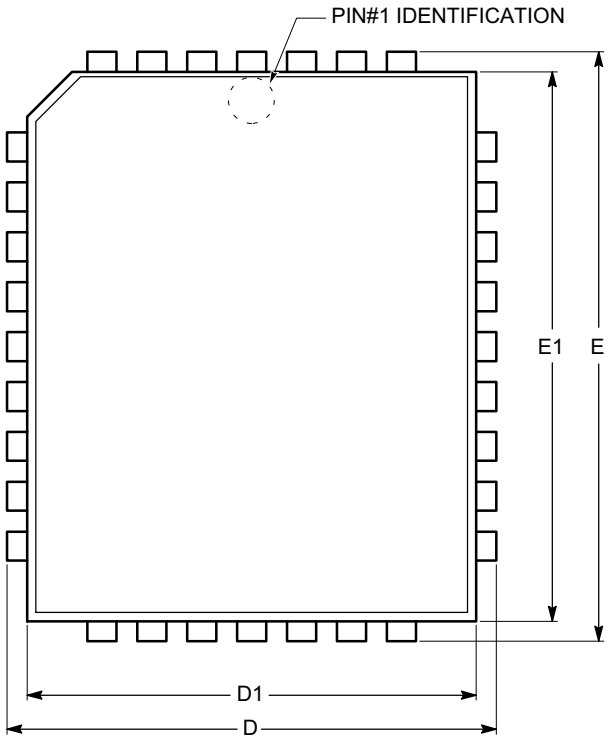


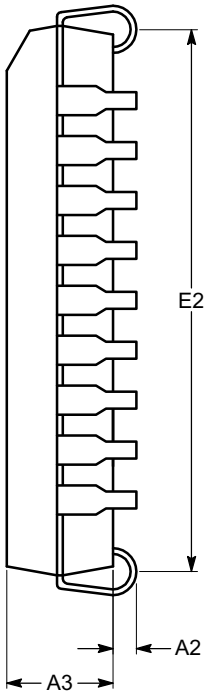
Figure 13. Resetting Software Data Protection Timing

PACKAGE DIMENSIONS

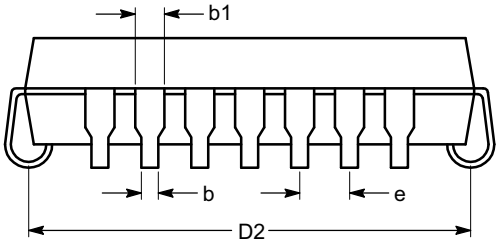
PLCC 32
CASE 776AK−01
ISSUE O



TOP VIEW



END VIEW



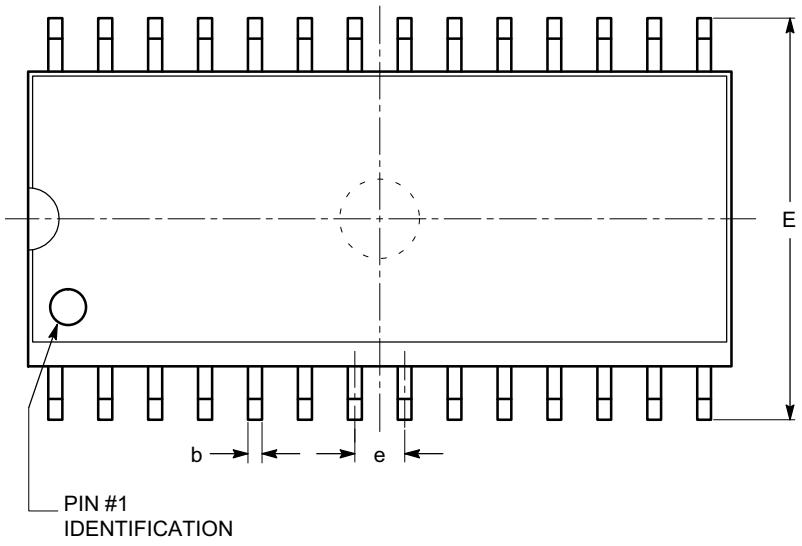
SIDE VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-016.

SYMBOL	MIN	NOM	MAX
A2	0.38		
A3	2.54		2.80
b	0.33		0.54
b1	0.66		0.82
D	12.32		12.57
D1	11.36		11.50
D2	9.56		11.32
E	14.86		15.11
E1	13.90		14.04
E2	12.10		13.86
e	1.27 BSC		

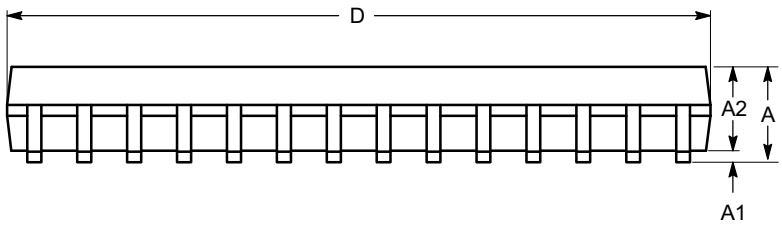
PACKAGE DIMENSIONS

SOIC−28, 300 mils
CASE 751BM−01
ISSUE O

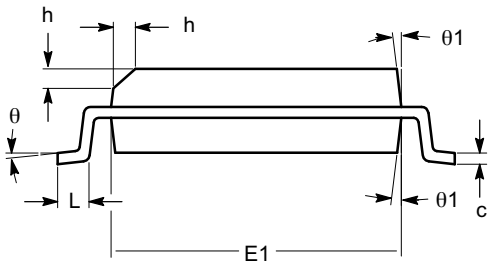


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	17.78		18.03
E	10.11		10.51
E1	7.34		7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40		1.27
θ	0º		8º
θ1	5º		15º



SIDE VIEW

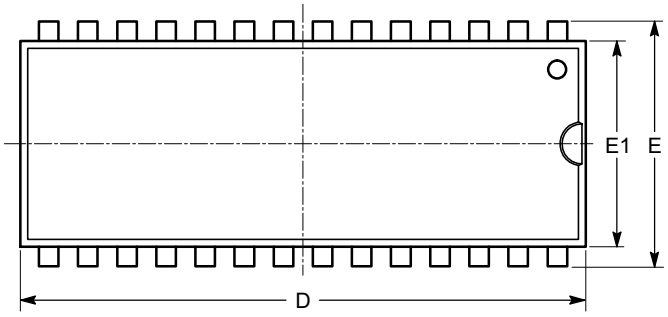


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

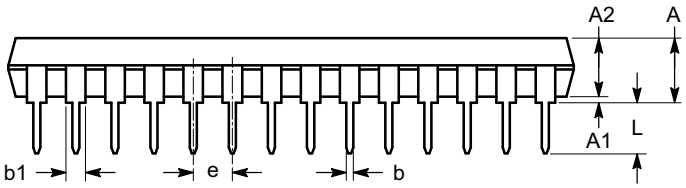
PACKAGE DIMENSIONS

PDIP−28, 600 mils
CASE 646AE−01
ISSUE A

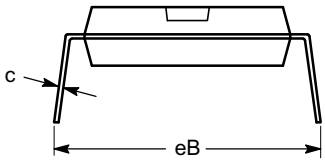


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			6.35
A1	0.39		
A2	3.18		4.95
b	0.36		0.55
b1	0.77		1.77
c	0.21		0.38
D	35.10		39.70
E	15.24		15.87
E1	12.32		14.73
e		2.54 BSC	
eB	15.24		17.78
L	2.93		5.08



SIDE VIEW

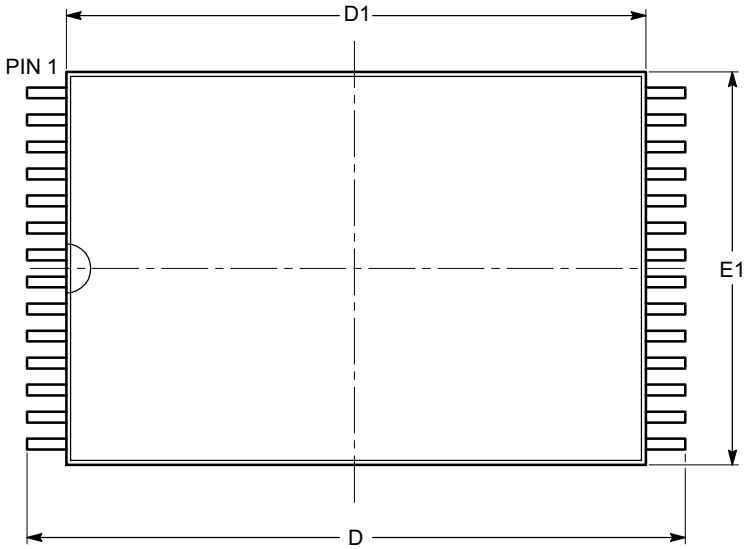


END VIEW

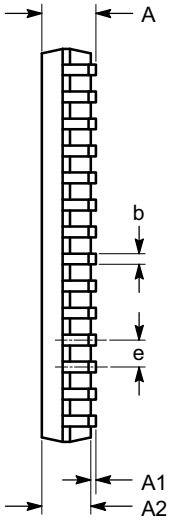
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-011.

PACKAGE DIMENSIONS

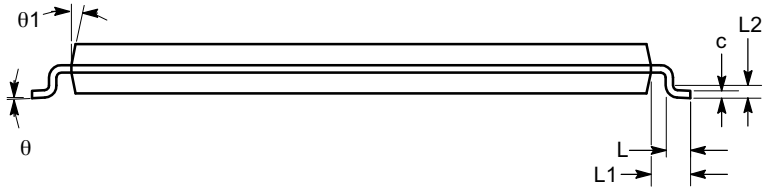
TSOP 28, 8x13.4
CASE 318AE−01
ISSUE O



TOP VIEW



END VIEW

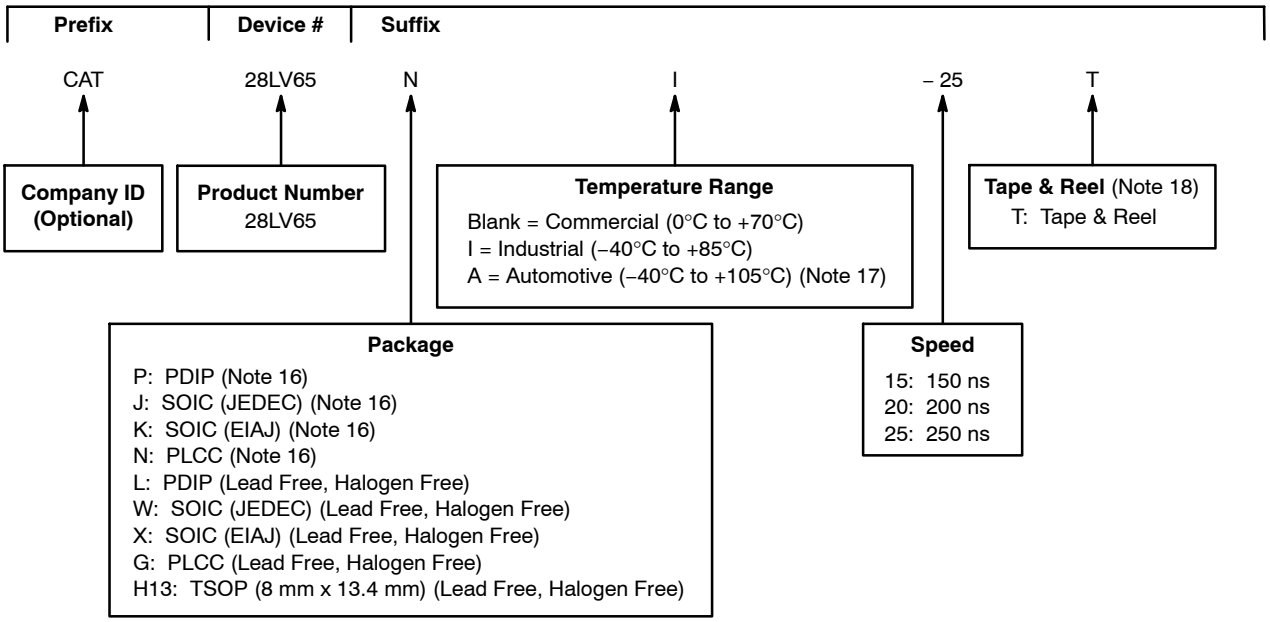


SIDE VIEW

SYMBOL	MIN	NOM	MAX
A	1.00	1.10	1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.20	13.40	13.60
D1	11.70	11.80	11.90
E	7.90	8.00	8.10
e		0.55 BSC	
L	0.30	0.50	0.70
L1	0.675		
L2		0.25 BSC	
θ	0°	3°	5°
θ1	10°	12°	16°

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-183.

Example of Ordering Information (Note 15)



15. The device used in the above example is a CAT28LV65NI–25T (PLCC, Industrial temperature, 250 ns Access Time, Tape & Reel).
16. Solder–plate (tin–lead) packages, contact Factory for availability.
17. –40°C to +125°C is available upon request.
18. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERING INFORMATION

Orderable Part Numbers (for Pb–Free Devices)			
CAT28LV65GI–15T	CAT28LV65H13A15T	CAT28LV65WI–15T	CAT28LV65XA–15T
CAT28LV65GI–20T	CAT28LV65H13A20T	CAT28LV65WI–20T	CAT28LV65XA–20T
CAT28LV65GI–25T	CAT28LV65H13A25T	CAT28LV65WI–25T	CAT28LV65XA–25T
CAT28LV65GA–15T	CAT28LV65LI15	CAT28LV65WA–15T	
CAT28LV65GA–20T	CAT28LV65LI20	CAT28LV65WA–20T	
CAT28LV65GA–25T	CAT28LV65LI25	CAT28LV65WA–25T	
CAT28LV65H13I15T	CAT28LV65LA15	CAT28LV65XI–15T	
CAT28LV65H13I20T	CAT28LV65LA20	CAT28LV65XI–20T	
CAT28LV65H13I25T	CAT28LV65LA25	CAT28LV65XI–25T	

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