

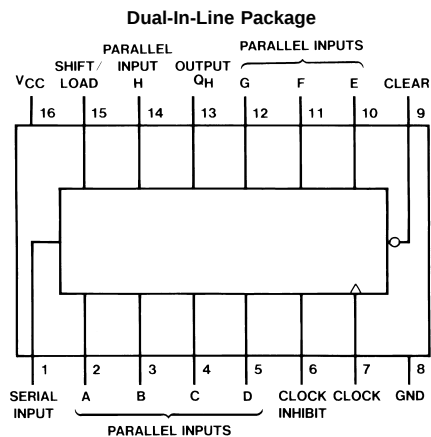
DM74LS166 8-Bit Parallel-In/Serial-Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading,

serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram



DS006400-1

Order Number DM74LS166WM or DM74LS166N
See Package Number M16B or N16A

Function Table

Inputs						Internal Outputs		Output Q _H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q _A	Q _B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a...h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note 1)Supply Voltage
Input Voltage7V
7V

Operating Free Air Temperature Range

DM74LS

0°C to +70°C

Storage Temperature Range

–65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM74LS166			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			–0.4	mA
I_{OL}	Low Level Output Current			8	mA
f_{CLK}	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)	0		20	MHz
t_W	Pulse Width (Note 7)	Clock	20		ns
		Clear	20		
t_{SU}	Setup Time (Note 7)	Mode	30		ns
		Data	20		
t_H	Hold Time (Note 7)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$			–1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$		0.35	0.5	V
		$I_{OL} = 4 \text{ mA}$, $V_{CC} = \text{Min}$		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$, $V_I = 0.4 \text{ V}$			–0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5)	–20		–100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 6)		22	38	mA

Note 2: $C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$.

Note 3: $C_L = 50 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$.

Note 4: All typicals are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V is applied to the CLOCK.

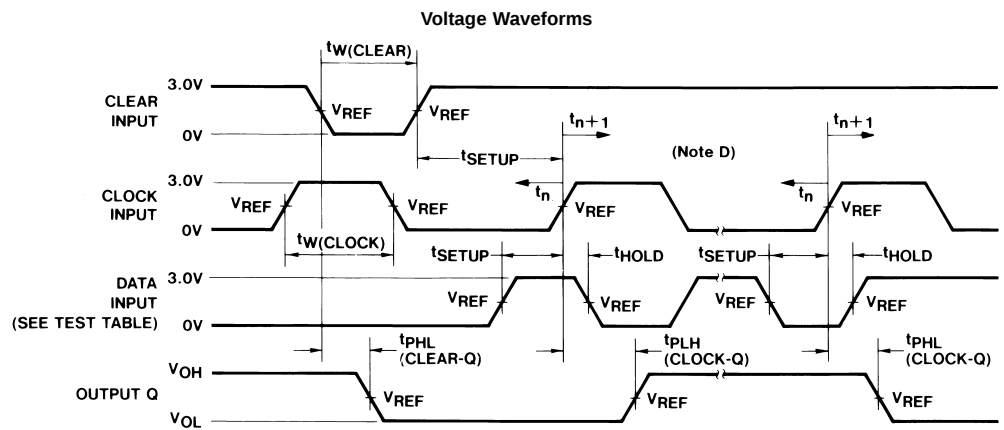
Note 7: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	R _L = 2 kΩ				Units
			C _L = 15 pF		C _L = 50 pF		
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency		25		20		MHz
t _{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	35		38	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	35		41	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output	6	30		36	ns

Parameter Measurement Information



Test Table for Synchronous Inputs

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(\text{clock})} \geq 20\text{ ns}$ and $\text{PRR} = 1\text{ MHz}$. The clear pulse has the following characteristics: $t_{W(\text{clear})} \geq 20\text{ ns}$ and $t_{\text{HOLD}} = 0\text{ ns}$. When testing f_{MAX} , vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.

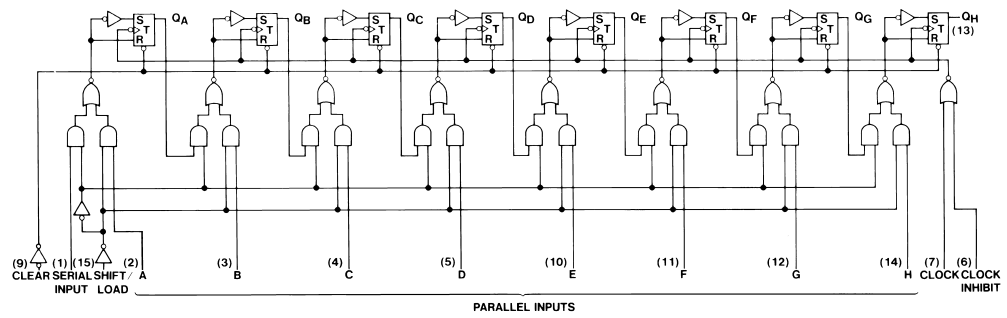
Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

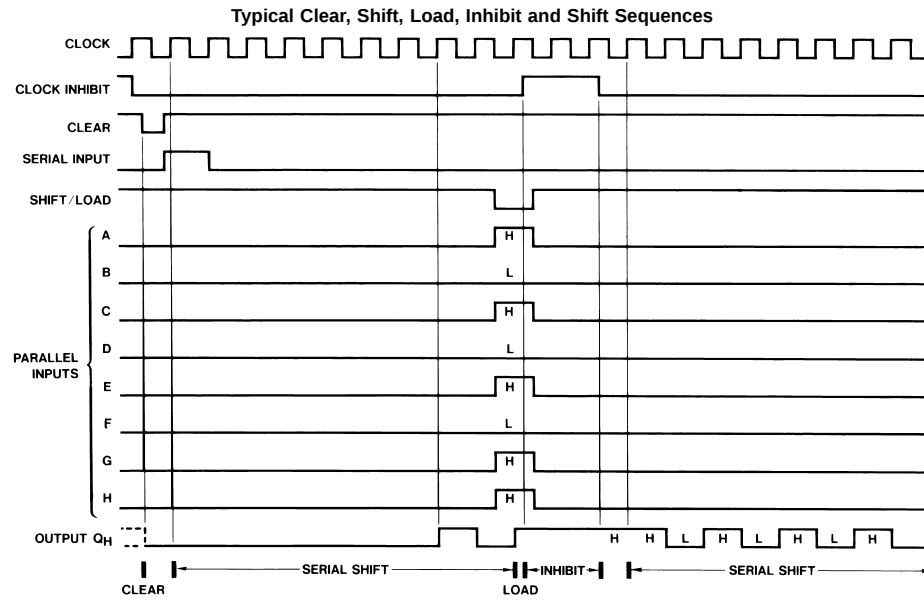
Note E: $V_{REF} = 1.3V$.

Logic Diagram



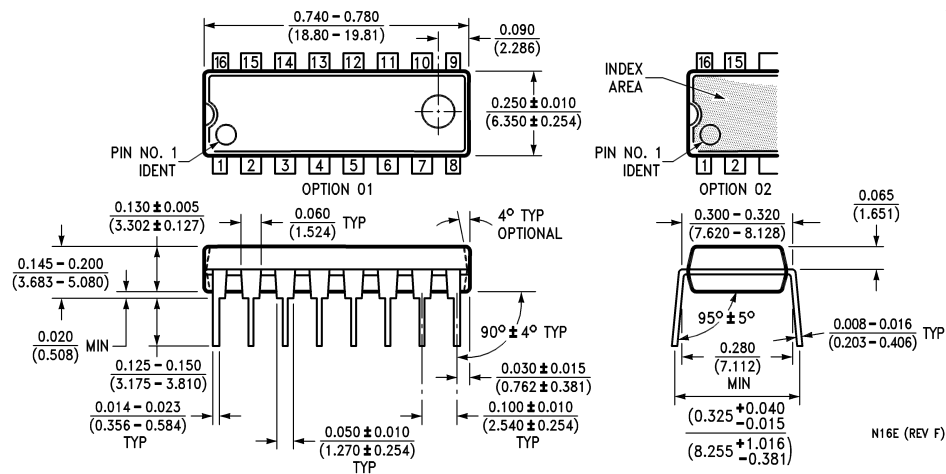
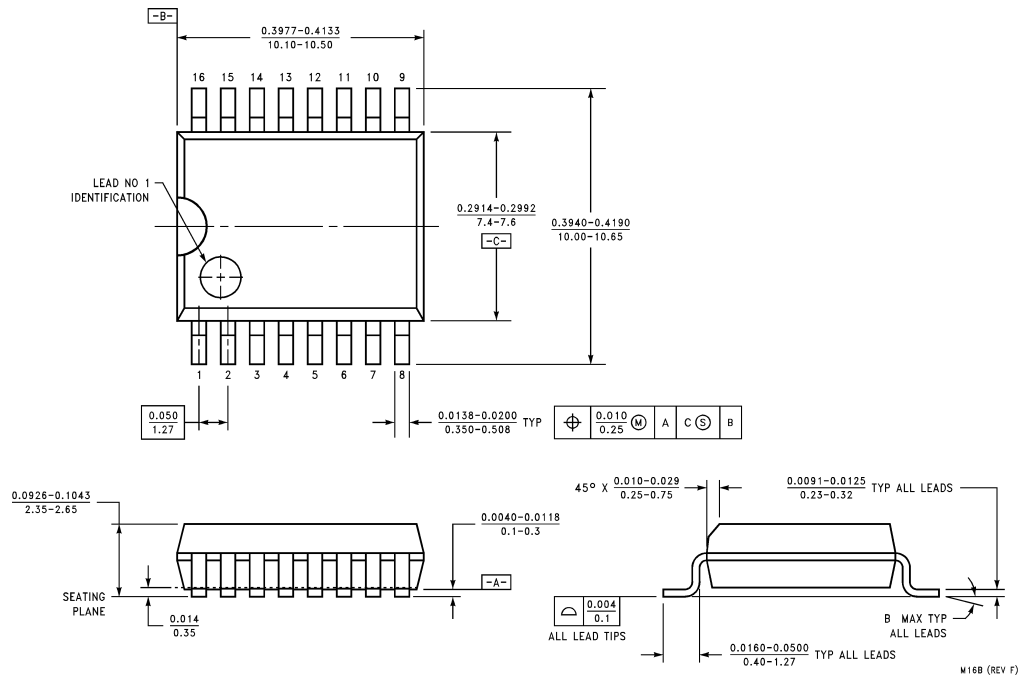
DS006400-3

Timing Diagram



DS006400-4

Physical Dimensions inches (millimeters) unless otherwise noted



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Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europa.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179