



# SANYO Semiconductors

## DATA SHEET

# LC07424LP — CMOS IC

## Audio CODEC with Video Driver

### Overview

The LC07424LP is an audio CODEC that has a built-in speaker amplifier and Line amplifier and incorporates a video driver.

A input line selector and ALC circuit are provided in the audio recording system.

A speaker amplifier and line output are provided in the playback system. A video driver that obviates the need for an output coupling capacitor is also included to enable AV playback processing with the single chip.

### Features

- Audio systems can be configured using this single chip since almost all the audio system circuits are provided.
- A high-performance ALC/limiter circuit that meets a variety of different conditions is incorporated.
- A wide range of different functions can be set using parameter settings.

### Functions

#### Recording system

- ADC : stereo single circuit,  $\Delta\Sigma$ Method 16bit, THD+N=-80dB(TYP, -1dBFS for input time)
- input to line : stereo single circuit, MIC Amplifier output
- analog PGA : stereo single circuit, for recording ALC, +34dB to -14dB (0.5dB step)
- ALC : The ADC output is detecting phase, analog PGA is controlled automatically.

#### Playback system

- DAC : stereo single circuit,  $\Delta\Sigma$ Method 16bit, THD+N=-80dB(TYP, 0dBFS for input time)
- Digital filter : De-emphasis filter, ( $f_s \Rightarrow 48\text{kHz}/44.1\text{kHz}/32\text{kHz}$ )
- Speaker amplifier : monaural single circuit, EVR block (+0dB to -65.2dB MUTE), BTL drive, 250mW (TYP  $8\Omega$   $V_{DDsp}=2.8\text{V}$  THD+N=1%)

#### Video system

- Video driver : 1 circuit. Y / C input and Video output. Compatible with changeover between the sag compensation type and DC direct-coupling type
- LPF :  $f_c=8\text{MHz}$
- Amplifier gain : 6.5dB $\pm$ 1.7dB, 0.1dB/step

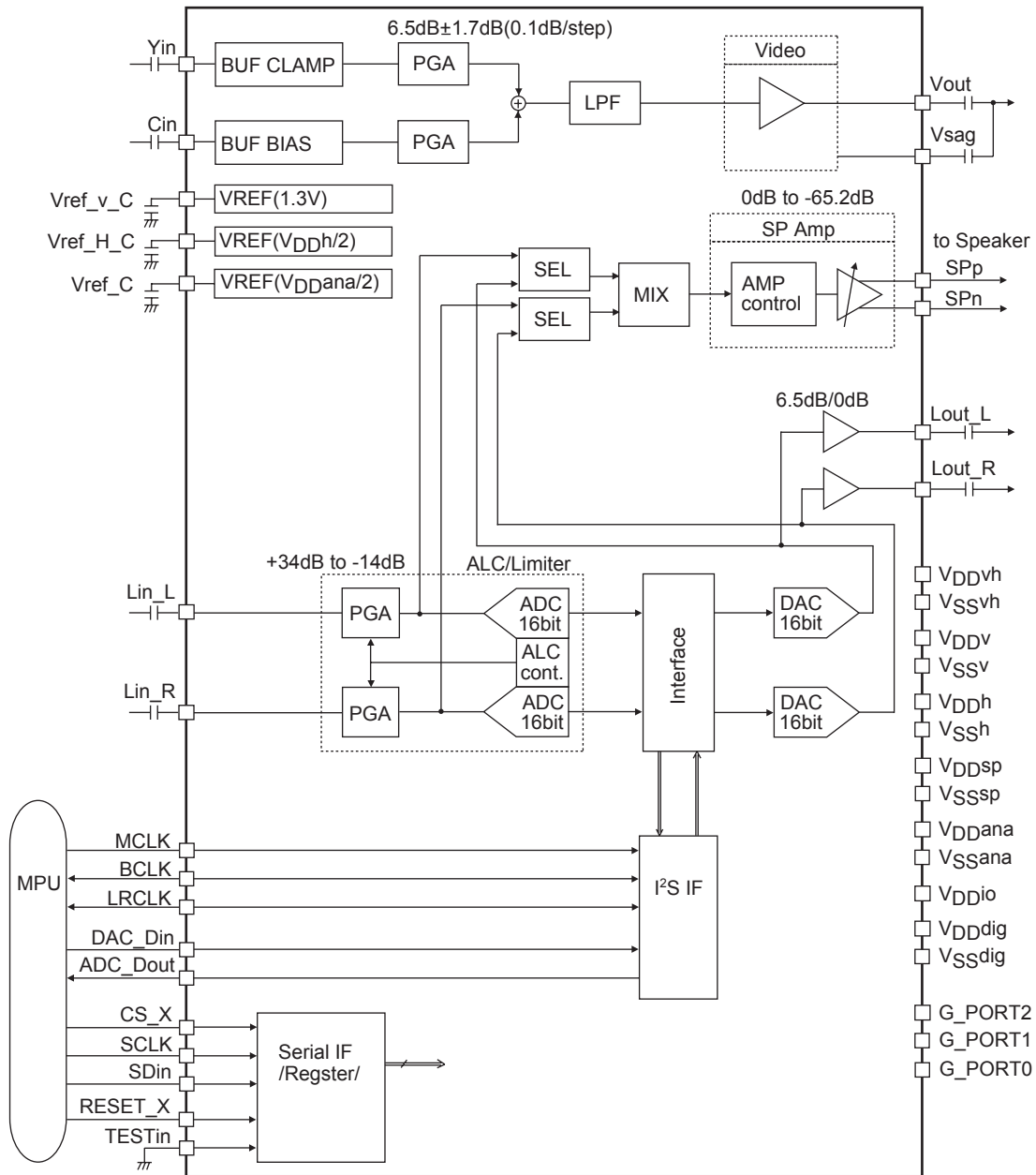
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# LC07424LP

## Block Diagram



# LC07424LP

## Pin Description

(Note) I/O: I=> input, Is=> Schmitt input, O=> output, IOs=> Schmitt input/output

PIN No.	I/O	Pin Name	Description
<b>Digital System</b>			
36	Is	RESET_X	Reset (negative polarity)
37	I	MCLK	Master Clock
38	IOs	LRCLK	LR Clock (sample rate clock) Audio IF
39	IOs	BCLK	B Clock (serial data bit clock) Audio IF
40	I	TESTin	For IC testing (V <sub>SS</sub> fixed in normal operation)
1	Is	DAC_Din	DAC serial data input Audio IF
2	O	ADC_Dout	ADC serial data output Audio IF
3	Is	CS_X	Chip select (negative polarity) Microcontroller IF
4	Is	SCLK	Serial clock Microcontroller IF
5	Is	SDin	Serial data input Microcontroller IF
9	IOs	G_PORT0	For IC testing (open in normal operation)
10	IOs	G_PORT1	For IC testing (open in normal operation)
11	O	G_PORT2	For IC testing (open in normal operation)
<b>Analog system</b>			
14	I	Yin	Y signal input
15	I	Cin	C signal input
16	O	Vref_v_C	Reference voltage (Video system) Connect an external capacitor
17	-	Vsag	Video signal output, for sag compensation. Connect an external capacitor
18	O	V <sub>OUT</sub>	Video signal output.
22	O	SPn	Speaker output
25	O	SPp	Speaker output
27	O	Vref_H_C	Reference voltage (4.8V system) Connect an external capacitor
29	O	Lout_L	Line output, Left channel
30	O	Lout_R	Line output, Right channel
31	I	Lin_L	Line input, Left channel
32	I	Lin_R	Line input, Right channel
34	O	Vref_C	Reference voltage (2.8V system) Connect an external capacitor
<b>Power pin, other</b>			
6	-	V <sub>DDdig</sub>	Digital power supply
7	-	V <sub>SSdig</sub>	Digital ground
8	-	V <sub>DDio</sub>	Digital IO power supply
12	-	V <sub>DDv</sub>	Analog power supply for video driver
13	-	V <sub>SSv</sub>	Analog ground for video driver
19	-	V <sub>DDvh</sub>	4.8V system analog power supply for video driver
20	-	V <sub>SSvh</sub>	4.8V system analog ground for video driver
21	-	N.C.	No connect
23	-	V <sub>DDsp</sub>	Speaker analog power supply
24	-	V <sub>SSsp</sub>	Speaker analog ground
26	-	V <sub>DDh</sub>	4.8V system analog power supply
28	-	V <sub>SSh</sub>	4.8V system analog ground
33	-	V <sub>SSana</sub>	Analog ground
35	-	V <sub>DDana</sub>	Analog power supply

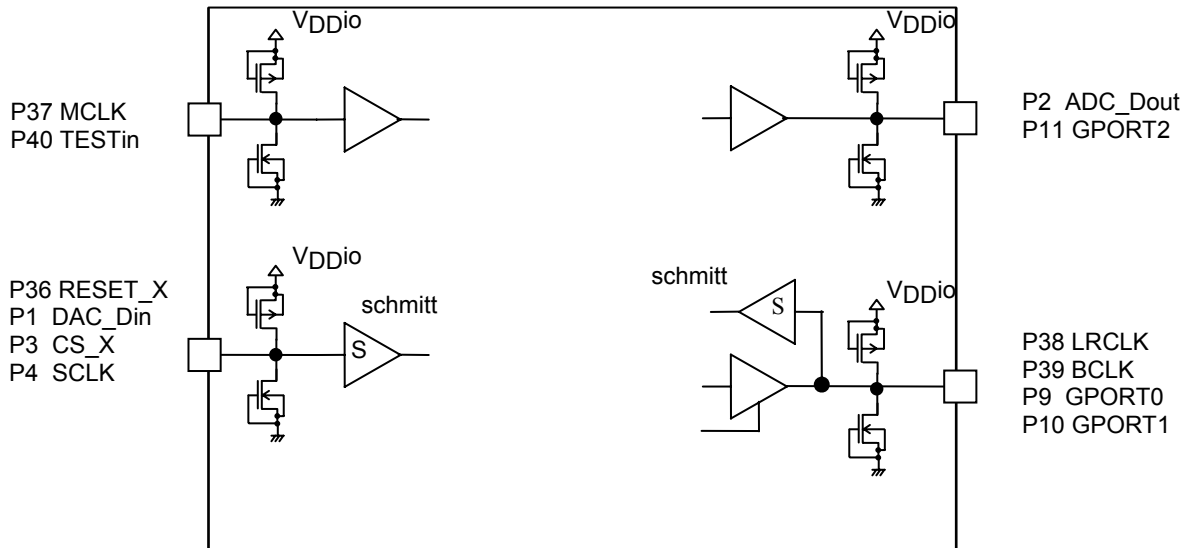
### Pin treatment when not using

- Keep the analog input/output pin in the OPEN state.  
L<sub>IN\_L</sub>, L<sub>IN\_R</sub>, L<sub>OUT\_L</sub>, L<sub>OUT\_R</sub>, Y<sub>IN</sub>, C<sub>IN</sub>, V<sub>OUT</sub>, Vsag
- Keep the digital output pin in the OPEN state.
- Do not keep the digital input pin in the OPEN state.

Pin internal equivalent circuit

Digital pin

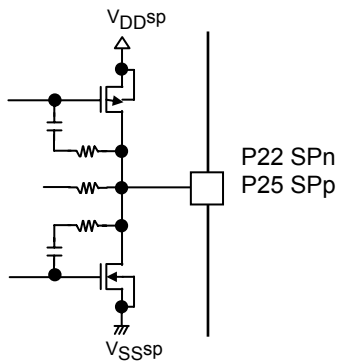
The input/output level can be set with the VDDio pin supply voltage.



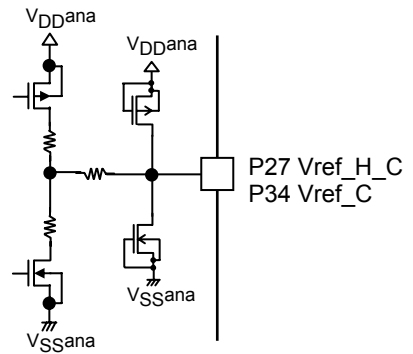
Analog pin

Speaker AMP

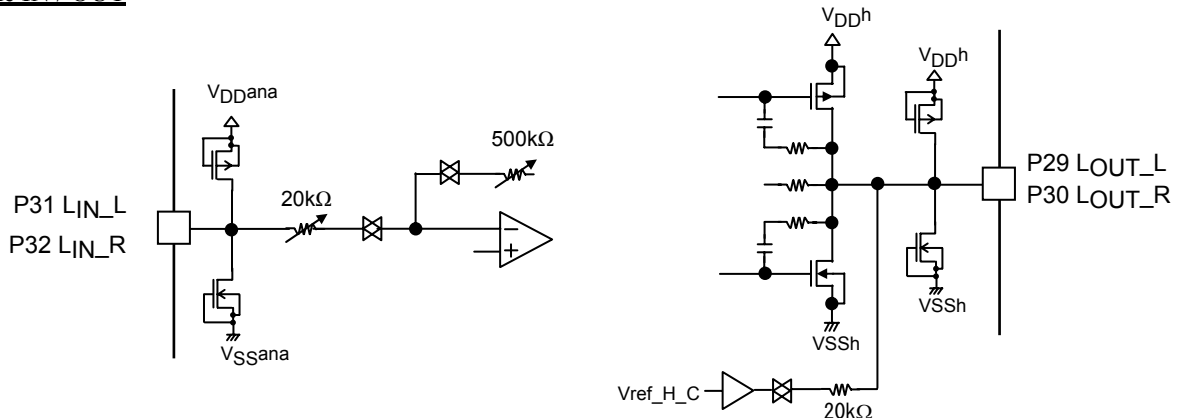
(Note) The resistance value is the TYPvalue.



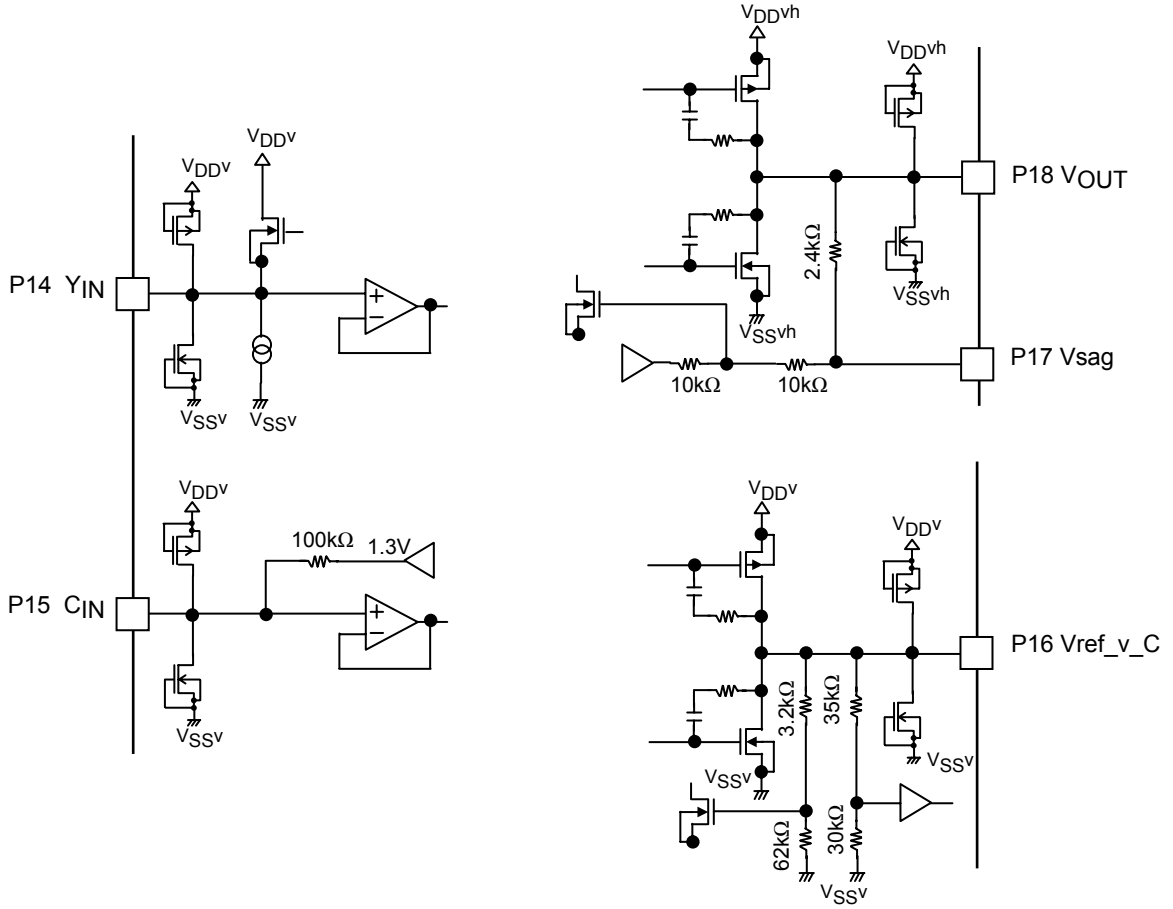
VREF



Line IN / OUT



Video



# LC07424LP

## Operating condition

**Absolute Maximum Ratings** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$

Parameter	Symbol	min	max	unit
Supply voltage (4.8V system) (*1) (*2)	$V_{DD48}$	-0.3	+7.0	V
Supply voltage (2.8V system) (*1) (*3)	$V_{DD28}$	-0.3	+4.0	V
Supply voltage (1.8V system) (*1) (*4)	$V_{DD18}$	-0.3	+4.0	V
Analog input voltage (*5)	$V_{INana}$	-0.3	$V_{DD28} + 0.3$	V
Digital input voltage (*6)	$V_{INdig}$	-0.3	$V_{DD18} + 0.3$	V
Allowable power dissipation (*7)	$P_d$		400	mW
Operating ambient temperature	$T_{opr}$	-10	+80	$^\circ\text{C}$
Storage ambient temperature	$T_{stg}$	-55	+125	$^\circ\text{C}$

(\*1) The supply voltage including rise/fall must maintain the following relationship:

$$V_{DD48} \geq V_{DD28} \geq V_{DD18}$$

(\*2) 4.8V system power pin:  $V_{DDh}$ ,  $V_{DDvh}$

(\*3) 2.8V system power pin:  $V_{DDana}$ ,  $V_{DDsp}$ ,  $V_{DDv}$

(\*4) 1.8V system power pin:  $V_{DDio}$ ,  $V_{DDdig}$ ,  $V_{DDio} \geq V_{DDdig}$

(\*5) Applicable pins:  $Y_{IN}$ ,  $C_{IN}$ ,  $L_{IN\_L}$ ,  $L_{IN\_R}$

(\*6) Applicable pins: MCLK, TESTin, RESET\_X, CS\_X, SCLK, SDin, BCLK, LRCLK (for the input mode), G\_PORT2 / 1 / 0 (for the input mode; the output mode only in case of normal operation)

(\*7)  $T_a \leq 80^\circ\text{C}$ , our standard substrate (size: 40 mm x 50 mm x 0.8 mm. In case of mounting of four-layer glass epoxy (2S2P) )

**Recommended Operating Range** at  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage	$V_{DDio}$	$V_{DDio}$ pin (*1)	1.71	1.80	3.6	V
	$V_{DDdig}$	$V_{DDdig}$ pin (*1)	1.71	1.80	$V_{DDio}$	V
	$V_{DDana}$	$V_{DDana}$ , $V_{DDv}$ , $V_{DDsp}$ pin (*1)	2.6	2.8	3.6	V
	$V_{DDh}$	$V_{DDh}$ , $V_{DDvh}$ pin (*1)	4.5	4.8	5.5	V
Input high level voltage	$V_{IH}$	(*2)	$(0.8)V_{DDio}$		$V_{DDio}$	V
Input low level voltage	$V_{IL}$	(*2)	$V_{SS}$		$(0.2)V_{DDio}$	V
Input clock frequency	fMCLK	(*3)	8.192		12.288	MHz
Input clock duty	DutyMCLK	fs=32kHz (*3)	30	50	70	%
		fs=48kHz, 44.1kHz (*3)	45	50	55	%
Analog line input dynamic range	$L_{IN}$	$L_{IN\_L}$ , $L_{IN\_R}$ pin (*4)			$(0.9)V_{DDana}$	Vp-p

(\*1)  $V_{DDh}=V_{DDvh}$ ,  $V_{DDana}=V_{DDsp}=V_{DDv} \geq V_{DDio} \geq V_{DDdig}$

(\*2) Applicable pins: MCLK, TESTin, RESET\_X, CS\_X, SCLK, SDin, BCLK (for the input mode) LRCLK (for the input mode), G\_PORT2 / 1 / 0 (for the input mode; the output mode only in case of normal operation)

(\*3) MCLK pin 8.192MHz => 32kHz x 256 12.288MHz => 48kHz x 256

(\*4) Specifications of the input selector circuit. The PGA output is not to exceed the full scale of ADC input.

**Electrical Characteristics** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{DDh}=V_{DDvh}=4.5$  to  $5.5\text{V}$ ,  $V_{DDana}=V_{DDsp}=V_{DDv}=2.6$  to  $3.6\text{V}$

$V_{DDio}=V_{DDdig}=1.71$  to  $3.6\text{V}$ ,  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	$I_{IH}$	$V_I=V_{DDio}$ (*1)			+1	$\mu\text{A}$
Input low level current	$I_{IL}$	$V_I=V_{SS}$ (*1)	-1			$\mu\text{A}$
Output high level voltage	$V_{OH1}$	$I_{OH}=-1\text{mA}$ (*2)	$(0.8)V_{DDio}$			V
Output low level voltage	$V_{OL1}$	$I_{OL}=1\text{mA}$ (*2)			$(0.2)V_{DDio}$	V
Input leak current	ILK	$V_I=V_{DDio}$ or $V_{SS}$ (*3)	-10		+10	$\mu\text{A}$

(\*1) Applicable pins: MCLK, TESTin, RESET\_X, CS\_X, SCLK, SDin,

(\*2) Applicable pins: ADC\_DOUT

BCLK, LRCLK (Output mode)

G\_PORT2 / 1 / 0 (For the output mode. Output mode only in case of normal operation.)

(\*3) Applicable pins: BCLK, LRCLK (Output mode)

G\_PORT2 / 1 / 0 (For the input mode. Output mode only in case of normal operation.)

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**Analog Characteristics** at Ta=25±2°C, V<sub>DDh</sub>=V<sub>DDvh</sub>=4.8V, V<sub>DDana</sub>=V<sub>DDsp</sub>=V<sub>DDv</sub>=2.8V, V<sub>DDio</sub>=V<sub>DDdig</sub>=1.8V,  
V<sub>SSvh</sub>=V<sub>SSh</sub>=V<sub>SSana</sub>=V<sub>SSsp</sub>=V<sub>SSv</sub>=V<sub>SSdig</sub>=0V, 0dBFS=-3.9dBV=1.8V

Unless otherwise specified, fs=48kHz, signal frequency =1kHz (sin wave), measurement range=20Hz to 20kHz DAC\_D<sub>IN</sub> pin input=0dBFS  
PGA gain setting=0dB, EVR gain setting=0dB

Analog Input / output						
Parameter	Symbol	Conditions	min	typ	max	unit
Input voltage	LI_V <sub>IN</sub>	(*1)			1.68	V
Input impedance	LI_R <sub>IN</sub>	(*1) (*2)	17	20	23	kΩ
Total harmonic distortion ratio and noise	AA_THD+N	L <sub>IN_L</sub> pin input: -1dBFS Measured at L <sub>OUT_L</sub> pin		-80	-72	dB
ADC analog Input						
Resolution	ADC_RES				16	Bits
SNR	ADC_SNR	A-Weighted	80	86		dB
Total harmonic distortion ratio and noise	ADC_THD+N	L <sub>IN_L</sub> pin input: -1dBFS Measured at ADC_D <sub>OUT</sub> pin		-80	-72	dB
Dynamic range	ADC_DR	L <sub>IN_L</sub> pin input: -60dBFS Measured at ADC_D <sub>OUT</sub> pin, A-Weighted	80	86		dB
Inter-channel isolation	ADC_ISO		80	100		dB
Inter-channel gain mismatch	ADC_LRG		-0.5		0.5	dB
PGA step width	PGA_GSTEP	L <sub>IN_L</sub> pin input, Measured at ADC_D <sub>OUT</sub> pin	0.1	0.5	0.9	dB
PGA variable range	PGA_GVB	L <sub>IN_L</sub> pin input, Measured at ADC_D <sub>OUT</sub> pin	-14		34	dB
DAC analog output						
Resolution	DAC_RES				16	Bits
SNR	DAC_SNR	A-Weighted	80	88		dB
Total harmonic distortion ratio and noise	DAC_THD+N	DAC_D <sub>IN</sub> pin input: 0dBFS Measured at L <sub>OUT_L</sub> pin		-80	-72	dB
Dynamic range	DAC_DR	DAC_D <sub>IN</sub> pin input: -60dBFS Measured at L <sub>OUT_L</sub> pin, A-Weighted	75	88		dB
Inter-channel isolation	DAC_ISO		80	100		dB
Inter-channel gain mismatch	DAC_LRG		-0.5		0.5	dB
Output voltage	LO_V	DAC_D <sub>IN</sub> pin input: 0dBFS LINE_AMP gain setting =6.5dB Measured at L <sub>OUT_L</sub> , L <sub>OUT_R</sub> pin	1.4	2.0	2.6	dBV
Output load resistance	LO_RL	L <sub>OUT_L</sub> , L <sub>OUT_R</sub> pin	10			kΩ
Output load capacity	LO_CL	L <sub>OUT_L</sub> , L <sub>OUT_R</sub> pin			30	pF
Speaker Amp EVR						
Gain value	EVR_G	DAC_D <sub>IN</sub> pin input: -6.5dBFS Measured at SP <sub>p</sub> and SP <sub>n</sub> pins	[EVR_GAIN]=3Fh [EVR_GAIN]=2Fh [EVR_GAIN]=20h [EVR_GAIN]=10h [EVR_GAIN]=00h		0.0 -2.2 -7.6 -22.8 -65.2	dB
Speaker Amp						
Total harmonic distortion ratio and noise	SP_THD+N	DAC_D <sub>IN</sub> pin input: 0dBFS, EVR=-2.5dB (*3)(*4)		1.0	2.0	%
Output level	SP_V	DAC_D <sub>IN</sub> pin input: 0dBFS, EVR=-2.5dB (*4)	2.1	3.0	3.9	dBV
SNR	SP_SNR	DAC_D <sub>IN</sub> pin input: 0dBFS, EVR=-2.5dB (*4)	78	86		dB
Output load resistance	SP_RL	SP <sub>p</sub> , SP <sub>n</sub> pin	8			Ω
Output load capacity	SP_CL	SP <sub>p</sub> , SP <sub>n</sub> pin			30	pF

(\*1) Applicable pins: Line input pin L<sub>IN\_L</sub>, L<sub>IN\_R</sub>

Analog input full-scale value of ADC (LI\_V<sub>IN</sub> = 2.8V x 0.6)

(\*2) The TYP resistance value varies from 10kΩ to 20kΩ depending on the gain setting of PGA.

(\*3) Output 250mW (8Ω)

(\*4) BTL converted value when the same signal has been set for Lch/Rch in the DAC input

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**Video characteristics** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{DDh}=V_{DDvh}=4.8\text{V}$ ,  $V_{DDana}=V_{DDsp}=V_{DDv}=2.8\text{V}$ ,  
 $V_{DDio}=V_{DDdig}=1.8\text{V}$ ,  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$   
 Unless otherwise specified, the AC input is the sine wave.

Parameter	Symbol	Conditions	min	typ	max	unit
Input range	$V_{D\_YDR}$	$Y_{IN}$ pin		1.0	1.2	Vp-p
	$V_{D\_CDR}$	$C_{IN}$ pin		0.7	0.9	Vp-p
Input impedance	$V_{D\_YRin}$	$Y_{IN}$ pin		1		M $\Omega$
	$V_{D\_CRin}$	$C_{IN}$ pin		100		k $\Omega$
Frequency characteristics (*1)	$V_{D\_LPF}$	Input signal: 8MHz (0.7Vp-p)	-6.0	-3.0	0.0	dB
		Input signal: 20MHz (0.7Vp-p)		-40	-30	dB
2nd harmonic distortion ratio 1 (*1)	$V_{D\_D1}$	Input signal: 1MHz (0.7Vp-p)		-50	-40	dB
2nd harmonic distortion ratio 2 (*1)	$V_{D\_D2}$	Input signal: 4MHz (0.7Vp-p)		-35	-30	dB
Differential gain	$V_{D\_DG}$		-1		1	%
Differential phase	$V_{D\_DP}$		-1		1	deg.
$V\_S / N$ (*2)	$V_{D\_VSNR}$	$V_{OUT}$ pin		-64		dBrms
$C\_S / N$ (*3)	$V_{D\_CSNR}$	AM		-70		dBrms
		PM		-62		dBrms
Output load resistance	$V_{D\_RL}$	Refer to Fig. 2.5.1.	140	150		$\Omega$
Output load capacity	$V_{D\_C1L}$	C1 Refer to Fig. 2.5.1.			15	pF
	$V_{D\_C2L}$	C2 Refer to Fig. 2.5.1.			400	pF
Group delay 1 (*4)	$V_{D\_GD1}$			20	60	ns
Group delay 2 (*5)	$V_{D\_GD2}$			15	45	ns
Gain value (*6)	$V_{D\_G}$	$[V_{D\_Y\_GAIN}] = [V_{D\_C\_GAIN}] = 22\text{h}$	7.2	8.2	9.2	dB
		$[V_{D\_Y\_GAIN}] = [V_{D\_C\_GAIN}] = 11\text{h}$	5.5	6.5	7.5	dB
		$[V_{D\_Y\_GAIN}] = [V_{D\_C\_GAIN}] = 00\text{h}$	3.8	4.8	5.8	dB
Gain step width	$V_{D\_GS}$	$[V_{D\_Y\_GAIN}] = 22\text{h}$ to $00\text{h}$ $[V_{D\_C\_GAIN}] = 22\text{h}$ to $00\text{h}$		0.1		dB

(\*1)  $Y_{IN}$  input current, as measured at  $V_{OUT}$  pin (0dB assumed at 100kHz)

(\*2) Noise Spectrum measurement

Measured at  $V_{OUT}$  pin, 50% White input, frequency range (100k-5MHz)

(\*3) Measured at  $V_{OUT}$  pin, 100% Red input, frequency range (10k-1MHz)

(\*4) Input:  $Y_{IN}$  pin, frequency range (100k-5MHz) Measurement:  $V_{OUT}$  pin

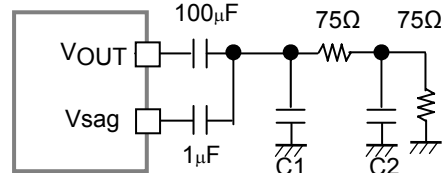
(\*5) Input:  $C_{IN}$  pin, frequency range (2MHz-5MHz) Measurement:  $V_{OUT}$  pin

(\*6) Enter 100kHz (0.5Vp-p) to  $Y_{IN}$  pin and measure at  $V_{OUT}$  pin.

Enter 3.58MHz (0.5Vp-p) to  $C_{IN}$  pin and measure at  $V_{OUT}$  pin.

Refer to Fig. 2.5.1. (Note here that  $C1=C2=0\mu\text{F}$ )

**Fig. 2.5.1 Video driver circuit**



**Current drain** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{DDh}=V_{DDvh}=4.8\text{V}$ ,  $V_{DDana}=V_{DDsp}=V_{DDv}=2.8\text{V}$   
 $V_{DDio}=V_{DDdig}=1.8\text{V}$ ,  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Source current at standby	IddS	Total of the following pins; $V_{DDio}$ , $V_{DDdig}$ , $V_{DDana}$ , $V_{DDsp}$ , $V_{DDv}$ , $V_{DDh}$ , and $V_{DDvh}$ (*1)		10	100	$\mu\text{A}$
1.8V system supply current	Idd18	Total of the following pins; $V_{DDdig}$ and $V_{DDio}$ (*2)		5		mA
2.8V system supply current	Idd28	Total of the following pins; $V_{DDana}$ , $V_{DDsp}$ , and $V_{DDv}$ (*2)		13		mA
4.8V system supply current	Idd48	Total of the following pins; $V_{DDh}$ , and $V_{DDvh}$ (*2)		6		mA

(\*1) RESET\_X pin = 0V, After input of clock in the MCLK pin, measure after stopping the clock.

(\*2) All circuits operating (Record & Playback & VIDEO)

MCLK: 12.288MHz (48kHz), Audio analog input signal: no signal, video input signal: Color bar

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**Digital filter characteristics** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{DDh}=V_{DDvh}=4.5$  to  $5.5\text{V}$ ,  $V_{DDana}=V_{DDsp}=V_{DDv}=2.6$  to  $3.6\text{V}$   
 $V_{DDio}=V_{DDdig}=1.71$  to  $3.6\text{V}$ ,  $V_{SSvh}=V_{SSh}=V_{SSana}=V_{SSsp}=V_{SSv}=V_{SSdig}=0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
<b>ADC block LPF fs=44.1kHz</b>						
Passband	ADC_PB	Gain=□0.05dB			20	kHz
Passband ripple	ADC_PR			□0.05		dB
Stopband	ADC_SB		24.1			kHz
Stopband attenuation	ADC_SA	Input signal =24.1kHz	-61			dB
<b>ADC block HPF fs=44.1kHz</b>						
Cutoff frequency	ADC_FC			0.882		Hz
<b>DAC block LPF fs=44.1kHz</b>						
Passband	DAC_PB				20	kHz
Passband ripple	DAC_PR			±0.015		dB
Stopband	ADC_SB		24.1			kHz
Stopband attenuation	ADC_SA	Input signal =24.1kHz	-58			dB
<b>DAC block HPF fs=44.1kHz</b>						
Cutoff frequency	ADC_FC			0.86		Hz

## Switching Characteristics

Parameter	Symbol	Conditions	min	typ	max	unit
<b>Microcontroller serial interface timing</b>						
SCLK Cycle time	tCYC		4T	8T		ns
SCLK high period	tSH		2T	4T		ns
SCLK low period	tSL		2T	4T		ns
Data setup time	tSU		2T	4T		ns
Data hold time	tHD		2T	4T		ns
CSX rise to SCLK wait time	tWSCLK		0T	2T		ns
SCLK to CSX rise wait time	tWCSX		4T	6T		ns
Rise time	tSR				50	ns
Fall time	tSF				50	ns
<b>Audio data timing</b>						
Clock phase (Note 2)	tPH		75			ns
Clock phase (Note 3)	tPH			1 / (128fs)		ns
Data delay time	tDD		0		75	ns
Data setup time	tSUA		1T			ns
Data hold time	tHDA		1T			ns

Note 1:  $T = 1 / f_{MCLK}$ ,  $f_{MCLK}$ : Frequency of MCLKIN pin; example: when  $f_{MCLK} = 10\text{MHz}$ ,  $T = 100\text{ns}$ ,  $2T = 200\text{ns}$

Note 2: LRCK and BCLK are inputs in Slave mode.

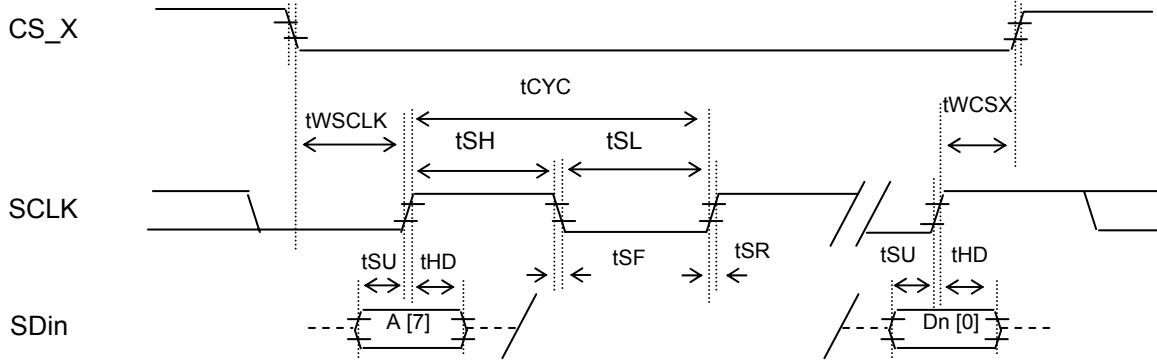
The MCLK timing needs only to be synchronized only with LRCK and BCLK and its phase is irrelevant.

Note 3: In master mode, LRCK and BCLK are output in master mode and fs is the sampling frequency.

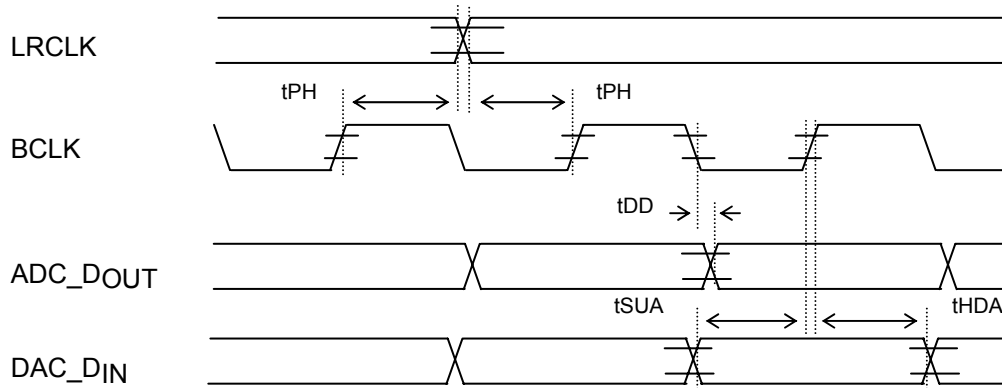
Note 4: The load of output pin: 30pF.

# LC07424LP

## Microcontroller Serial Interface Timing Diagram



## Audio Data Timing Diagram



## Input / Output level

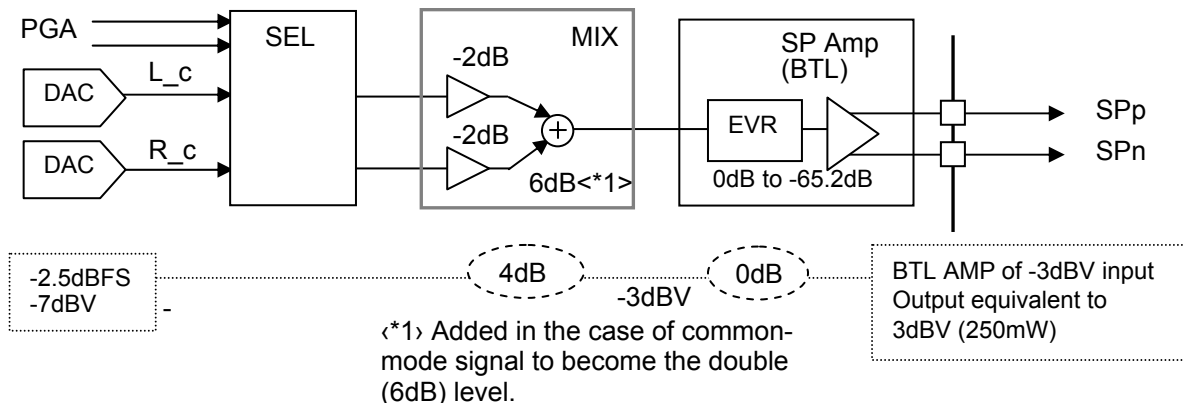
$V_{DDh} = V_{DDvh} = 4.8V$ ,  $V_{DDana} = V_{DDsp} = V_{DDv} = 2.8V$ ,  $V_{DDio} = V_{DDdig} = 1.8V$ , standard setting

DAC analog output full scale (FS) FS = -4.5dBV = 1.68V<sub>p-p</sub> = 2.8V x 0.6

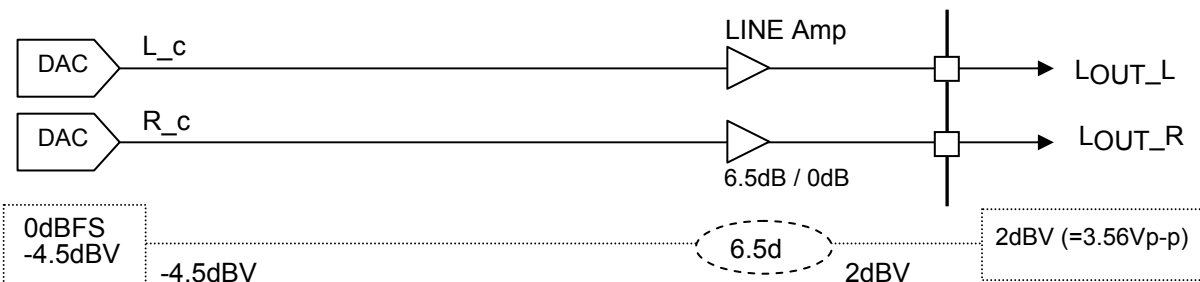
ADC analog input full scale (FS) FS = -4.5dBV = 1.68V<sub>p-p</sub> = 2.8V x 0.6

**dB** : Gain value  
0dBV = 1V<sub>rms</sub> = 2.83V<sub>p-p</sub>

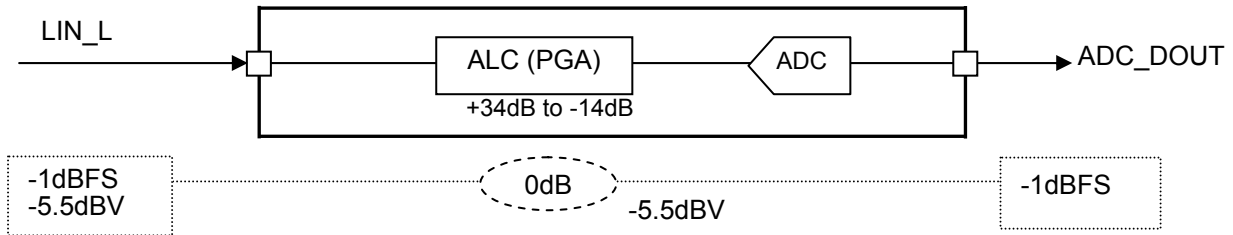
### Speaker output



### Line output



· Digital output



## Outline of operation

### 1. System reset/power-down

When the RESET\_X pin is set to “V<sub>SS</sub>,” the system is reset, and all the circuits go into the power-down mode. After the power is turned on, perform this operation once without fail.

When the system is reset, the contents of the register are initialized. (See register tables.)

For the subsequent startup of each function, refer to the section “Control/start/stop sequence for reducing pop noise.”

### 2. ALC

When the ALC is active, the PGA (programmable gain amplifier) gain value is automatically adjusted so that the audio level becomes the preset value. The PGA gain can be adjusted in a range from +34 to -14dB.

By limiting the gain adjustment range to 0 to -14dB, this adjustment function can be made to work as a limiter function.

The ALC operation can be stopped by a register setting. The ALC is then placed in the manual mode, and the PGA gain is adjusted by the register setting. For details, refer to the section “Description of ALC/limiter operation.”

### 3. A/D converter

The A/D converter converts the analog PGA output signals into digital data, and the digital data is then output as 16-bit serial audio data.

There are three formats supported: I<sup>2</sup>S, left justification and right justification.

The A/D converter incorporates a high-pass filter for canceling DC offset.

The analog input range of the ADC is 0.6V<sub>DDadc</sub>. When V<sub>DDadc</sub> is 2.8V, 0dBfs is 1.68V.

### 4. D/A converter

The D/A converter converts the digital 16-bit serial audio data into analog signals.

There are three formats supported: I<sup>2</sup>S, left justification and right justification.

The D/A converter incorporates a high-pass filter for canceling DC offset.

The analog input range of the ADC is 0.6V<sub>DDadc</sub>. When V<sub>DDadc</sub> is 2.8V, 0dBfs is 1.68V.

### 5. Selector

This selector is for selecting either the DAC or PGA output of the ALC. When the DAC output has been selected, the DAC output signals are output as the Line/speaker amplifier output signals. When the PGA output has been selected, the signals from line input are all turned into analog signals to become the Line/speaker amplifier output signals.

### 6. MIX

This is the mixing circuit for the left- and right-channel audio signals. In other words, this functions as a monaural signal generator circuit to provide a monaural speaker amplifier input. The left- and right-channel signals are mixed on a 1:1 basis and then output through the -2dB amplifier.

If the left- and right-channel signals are identical, the total gain becomes 4dB (= 6dB(doubled) -2dB).

**7. SP AMP**

This is the monaural speaker amplifier. Its maximum output is 250mW (typ  $V_{DD}=2.8V$ ,  $8\Omega$ ,  $THD+N = 10\%$ ). This amplifies the MIX circuit output. EVR (+0dB to -65.2dB) is mounted. A thermal shutdown function is provided. When it is left enabled, the speaker amplifier operation is automatically shut down when the chip temperature has reached a high level.

**8. Video driver**

Either the sag compensation type or DC direct coupling type is selectable. The gain adjustment circuit (6.5dB±1.7dB, 0.1dB/step) is mounted.

**9. Register settings**

This is a 3-line system serial control circuit. The three lines are CS\_X (Chip Select/low active), SCLK (Serial Clock) and SDin (Serial Data). Data can only be written into the register: The register data cannot be read out. The data transfer rate—in other words, the maximum SCLK frequency—depends on the MCLK pin clock. For details, refer to the section “Switching characteristics.”

**10. Master clock**

The master clock frequency is 256fs. This clock signal must be input from the MCLK pin.

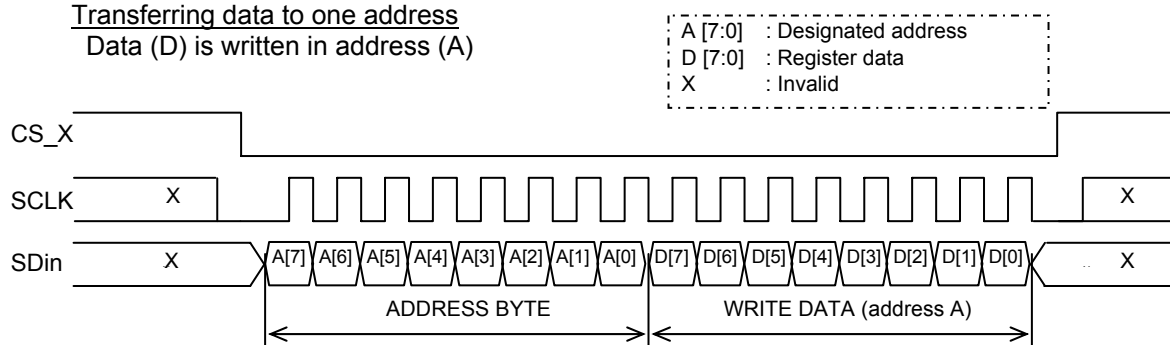
**11. Audio data formats**

I<sup>2</sup>S, left justification and right justification modes are supported. It is possible to select master or slave mode for BCLK and LRCLK. For details, refer to the section “Audio data formats.”

**Microcontroller Serial Interface**

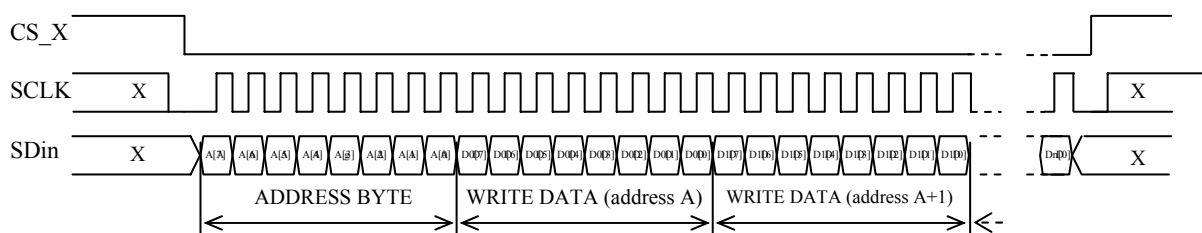
The internal registers values are written by the serial interface consisting of the three CS\_X, SCLK, and SDin lines. When the CS\_X pin is set low, the LC07424LP is switched into the mode that enables operation. The data is received on a byte basis with MSB first. Continuous access (burst access) is also possible, and the addresses incremented by 1 are accessed in sequence with each byte following access to the register specified by the address byte. If the size of data exceeding the highest address (1Dh) is accessed in this process, the data concerned is treated as invalid. In other word, the address never wraps around to 00 (HEX). The maximum data transfer rate (maximum SCLK frequency) depends on the MCLK pin clock. Refer to the section "Switching characteristics."

Transferring data to one address  
Data (D) is written in address (A)



Transferring data to contiguous addresses

Data (D0) is written in address (A), and data (D1) is written into address (A+1).



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## Audio Data Formats

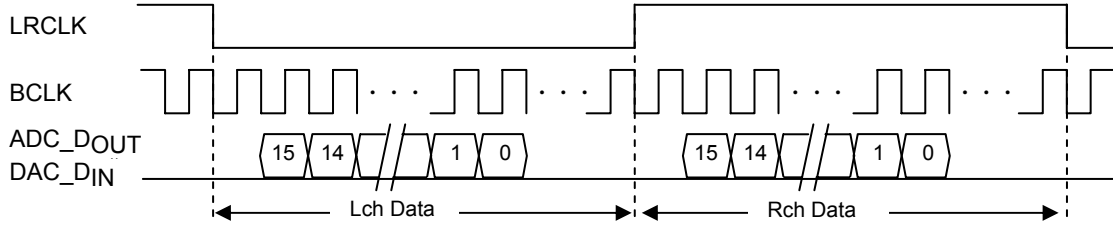
The timing chart is shown below.  
 For all settings, data is MSB-first, 2'S-compliment.

	Slave Mode [ADF_MASTER]=0	Master Mode [ADF_MASTER]=1
MCLK pin	Input	Input
LRCLK pin	Input	Output
BCLK pin	Input	Output

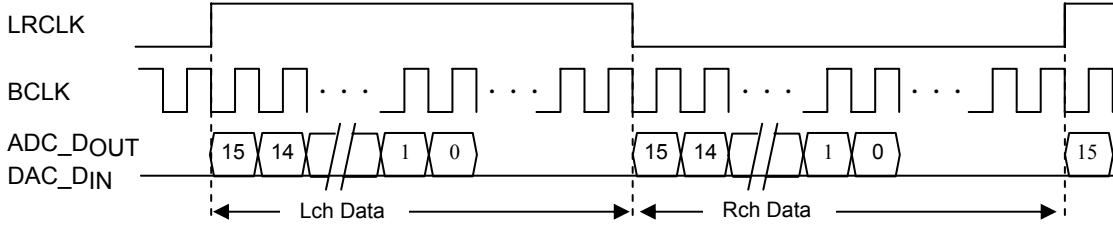
[ADF_MODE]	[ADF_32FS]	
11	-	Set prohibition
10	1	Backward justification 32fs
01	1	Forward justification 32fs
00	1	I <sup>2</sup> S 32fs
10	0	Backward justification 64fs
01	0	Forward justification 64fs
00	0	I <sup>2</sup> S 64fs

### BCLK=64fs

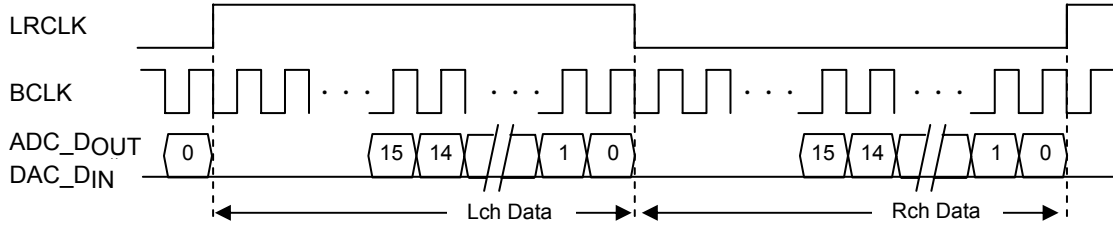
I<sup>2</sup>S mode



Forward justification mode

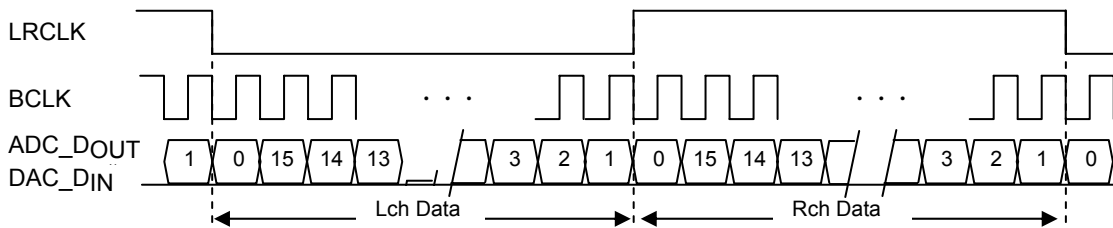


Backward justification mode

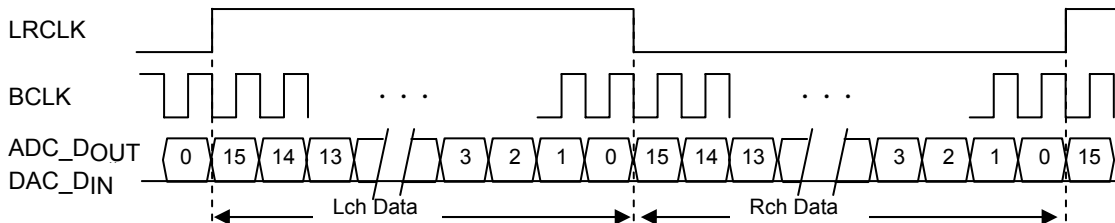


### BCLK=32fs

I<sup>2</sup>S mode



Forward/backward justification mode



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## Register Table

ADRS (Address): displayed in hexadecimal notation

Init (initial value): displayed in hexadecimal notation

"0" settings are used for registers indicated with "0". Registers with gray background are for LSI test.

They are fixed at INIT values.

Set data for all registers (including registers for test).

Function	ADRS [7:0]	INIT [7:0]	Register Data D[7:0]							
			7	6	5	4	3	2	1	0
PM1	00h	00h	VREF_BIAS[1]	VREF_BIAS[0]	SYNC_CLR	SEL_PDX	ALC_PDX	ADC_A_PDX	DAC_A_PDX	VIDEO_PDX
PM2	01h	00h	SP_OUTEN	SP_PDX	MIX_PDX	0	LO_PDX	ADC_D_PDX	DAC_D_PDX	SP_EVR_PDX
ALC1	02h	11h	0	0	0	ALC_LI_L	0	0	0	ALC_LI_R
ALC2	03h	3Dh	ALC_VAL[2]	ALC_VAL[1]	ALC_VAL[0]	ALC_FA[1]	ALC_FA[0]	ALC_FR[2]	ALC_FR[1]	ALC_FR[0]
ALC3	04h	86h	ALC_ZCD	ALC_ZCDTM[1]	ALC_ZCDTM[0]	ALC_FULLEN	ALC_ATLIM[1]	ALC_ATLIM[0]	ALC_RWT[1]	ALC_RWT[0]
ALC4	05h	1Ch	ALC_OFF	ALC_VMAX[6]	ALC_VMAX[5]	ALC_VMAX[4]	ALC_VMAX[3]	ALC_VMAX[2]	ALC_VMAX[1]	ALC_VMAX[0]
ALC5	06h	1Ch	ALC_MUTE_L	ALC_DVL[6]	ALC_DVL[5]	ALC_DVL[4]	ALC_DVL[3]	ALC_DVL[2]	ALC_DVL[1]	ALC_DVL[0]
ALC6	07h	1Ch	ALC_MUTE_R	ALC_DVR[6]	ALC_DVR[5]	ALC_DVR[4]	ALC_DVR[3]	ALC_DVR[2]	ALC_DVR[1]	ALC_DVR[0]
TEST0	08h	00h	TEST0[7]	TEST0[6]	TEST0[5]	TEST0[4]	TEST0[3]	TEST0[2]	TEST0[1]	TEST0[0]
CODEC1	09h	00h	0	0	0	ADF_BCLK	0	0	ADF_MODE[1]	ADF_MODE[0]
CODEC2	0Ah	00h	ADF_DAC_INV	ADF_ADC_INV	0	DE_EN	ADF_FS[1]	ADF_FS[0]	ADF_LB	ADF_MASTER
SEL/MIX	0Bh	A3h	SEL_L[1]	SEL_L[0]	SEL_R[1]	SEL_R[0]	0	0	MIX_MONO[1]	MIX_MONO[0]
SP1	0Ch	00h	0	0	SP_GAIN_L[5]	SP_GAIN_L[4]	SP_GAIN_L[3]	SP_GAIN_L[2]	SP_GAIN_L[1]	SP_GAIN_L[0]
TEST1	0Dh	00h	TEST1[7]	TEST1[6]	TEST1[5]	TEST1[4]	TEST1[3]	TEST1[2]	TEST1[1]	TEST1[0]
SP3	0Eh	2Fh	0	0	SP_ZCD	SP_ZCDTM[1]	SP_ZCDTM[0]	SP_SOFTSW	SP_SSC[1]	SP_SSC[0]
LINE	0Fh	0Fh	0	0	0	0	LO_DET_VDD	LO_GAIN	LO_VREFSW	LO_MUTE
TEST2	10h	00h	TEST2[7]	TEST2[6]	TEST2[5]	TEST2[4]	TEST2[3]	TEST2[2]	TEST2[1]	TEST2[0]
TEST3	11h	00h	TEST3[7]	TEST3[6]	TEST3[5]	TEST3[4]	TEST3[3]	TEST3[2]	TEST3[1]	TEST3[0]
VIDEO1	12h	11h	0	0	VD_Y_GAIN[5]	VD_Y_GAIN[4]	VD_Y_GAIN[3]	VD_Y_GAIN[2]	VD_Y_GAIN[1]	VD_Y_GAIN[0]
VIDEO2	13h	11h	0	0	VD_C_GAIN[5]	VD_C_GAIN[4]	VD_C_GAIN[3]	VD_C_GAIN[2]	VD_C_GAIN[1]	VD_C_GAIN[0]
VIDEO3	14h	02h	0	0	0	0	0	0	VD_SAG_MODE	0
TEST4	15h	11h	TEST4[7]	TEST4[6]	TEST4[5]	TEST4[4]	TEST4[3]	TEST4[2]	TEST4[1]	TEST4[0]
TEST5	16h	02h	TEST5[7]	TEST5[6]	TEST5[5]	TEST5[4]	TEST5[3]	TEST5[2]	TEST5[1]	TEST5[0]
TEST6	17h	00h	TEST6[7]	TEST6[6]	TEST6[5]	TEST6[4]	TEST6[3]	TEST6[2]	TEST6[1]	TEST6[0]
TEST7	18h	05h	TEST7[7]	TEST7[6]	TEST7[5]	TEST7[4]	TEST7[3]	TEST7[2]	TEST7[1]	TEST7[0]
TEST8	19h	00h	TEST8[7]	TEST8[6]	TEST8[5]	TEST8[4]	TEST8[3]	TEST8[2]	TEST8[1]	TEST8[0]
TEST9	1Ah	FFh	TEST9[7]	TEST9[6]	TEST9[5]	TEST9[4]	TEST9[3]	TEST9[2]	TEST9[1]	TEST9[0]
TEST10	1Bh	00h	TEST10[7]	TEST10[6]	TEST10[5]	TEST10[4]	TEST10[3]	TEST10[2]	TEST10[1]	TEST10[0]
TEST11	1Ch	00h	TEST11[7]	TEST11[6]	TEST11[5]	TEST11[4]	TEST11[3]	TEST11[2]	TEST11[1]	TEST11[0]
TEST12	1Dh	00h	TEST12[7]	TEST12[6]	TEST12[5]	TEST12[4]	TEST12[3]	TEST12[2]	TEST12[1]	TEST12[0]

ADRS =Address  
 INIT =Initial value  
 PM =Power Management  
 ALC =Automatic Level Control  
 ADC =AD Converter  
 DAC =DA Converter  
 EVR =Electronic Variable Resistor  
 ADF =Audio Data Format

PGA =Programmable Gain Amplifier  
 Lch =Left channel  
 Rch =Right channel  
 2^n =2<sup>n</sup> (ex. 2<sup>10</sup> = 1024)  
 Nh = N denotes a hexadecimal number.  
 Nb = N denotes a binary number.  
 ABC[n] = Register with a multiple number of bits.  
 ABC is the register name, and "n" is the number of bits.

## LC07424LP

Register Description (Note) This section deals with the outline. Be sure to confirm the description here by referring to the page dealing with the detailed explanation.

ADRS	Bit	Name	INIT	Description
00h	[7]	VREF_BIAS	00b	Setting the common reference voltage circuit
	[6]			11: Normal operation 10: Rapid charging 01: pull-down 00: Power down
	[5]	SYNC_CLR	0b	Digital block synchronous reset control 1: Reset 0: Normal operation
	[4]	SEL_PDX	0b	Selector block power DOWN 1: Normal operation 0: Power down
	[3]	ALC_PDX	0b	ALC block power down 1: Normal operation 0: Power down
	[2]	ADC_A_PDX	0b	ADC Analog block power down 1: Normal operation 0: Power down
	[1]	DAC_A_PDX	0b	DAC Analog block power down 1: Normal operation 0: Power down
	[0]	VIDEO_PDX	0b	VIDEO power down 1: Normal operation 0: Power down
01h	[7]	SP_OUTEN	0b	Speaker out enable 0: Speaker output stop 1: Normal operation
	[6]	SP_PDX	0b	Speaker power down 1: Normal operation 0: Power down
	[5]	MIX_PDX	0b	MIX Power down 1: Normal operation 0: Power down
	[4]	0	0b	0: Fixed
	[3]	LO_PDX	0b	Line out power down 1: Normal operation 0: Power down
	[2]	ADC_D_PDX	0b	ADC logic block power down 1: Normal operation 0: Power down
	[1]	DAC_D_PDX	0b	DAC logic block power down 1: Normal operation 0: Power down
	[0]	SP_EVR_PDX	0b	Speaker EVR power down 1: Normal operation 0: Fixed at [SP_GAIN]=00h
02h	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	0	0b	0: Fixed
	[4]	ADC_LIN_L	1b	Lch line Input selection 0: Non-selection 1: Selection
	[3]	0	0b	0: Fixed
	[2]	0	0b	0: Fixed
	[1]	0	0b	0: Fixed
	[0]	ADC_LIN_R	1b	Rch line Input selection 0: Non-selection 1: Selection
03h	[7]	ALC_VAL	001b	ALC circuit, ALC value (limiter level) setting 111:-10dBFS 110:-9dBFS 101:-8dBFS 100:-7dBFS 011:-6dBFS 010:-5dBFS 001:-4dBFS 000:-3dBFS
	[6]			
	[5]			
	[4]	ALC_FA	11b	ALC circuit, Attack factor setting 11: (1/8)dB 10: (1/4)dB 01: (1/2)dB 00: (1/1)dB
	[3]			
	[2]	ALC_FR	101b	ALC circuit, Recovery factor setting 111: (1/2 <sup>14</sup> )dB 110: (1/2 <sup>13</sup> )dB 101: (1/2 <sup>12</sup> )dB 100: (1/2 <sup>11</sup> )dB 011: (1/2 <sup>10</sup> )dB 010: (1/2 <sup>9</sup> )dB 001: (1/2 <sup>8</sup> )dB 000: (1/2 <sup>7</sup> )dB
	[0]			
04h	[7]	ALC_ZCD	1b	ALC circuit, Gain change in the zero cross timing 1: ON 0: OFF
	[6]	ALC_ZCDTM	00b	ALC circuit, Timeout time setting at detection of zero cross 11: 8192 (1/fs) 10: 4096 (1/fs) 01: 2048 (1/fs) 00: 1024 (1/fs)
	[5]			
	[4]	ALC_FULLEN	0b	ALC circuit, Full-scale detection operation setting 1: ON 0: OFF
	[3]	ALC_ATLIM	01b	ALC circuit, Limit setting for attach operation frequency between zero crosses 11: 16 10: 8 01: 4 00: 2
	[2]			
	[0]	ALC_RWT	10b	ALC circuit, standby time setting during recovery operation 11: 2048 (1/fs) 10: 1024 (1/fs) 01: 512 (1/fs) 00: 256 (1/fs)
05h	[7]	ALC_OFF	0b	ALC circuit 1: ALC function OFF (Manual mode) 0: ALC function ON
	[6]	ALC_VMAX	1Ch	ALC circuit, Maximum gain value setting of PGA when the ALC function is ON
	[5]			7Fh to 61h: Set prohibition
	[4]			60h: +34dB
	[3]			to 0.5dB step
	[2]			1Ch: 0dB
	[0]			to 0.5dB step 00h: -14dB

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ADRS	Bit	Name	INIT	Description
06h	[7]	ALC_MUTE_L	0b	ALC circuit, Lch mute setting 1: ON 0: OFF
	[6]	ALC_DVL	1Ch	ALC circuit, Lch PGA gain value setting in the manual mode 7Fh: MUTE 7Eh to 61h: Set prohibition 60h: +34dB to 0.5dB step 1Ch: 0dB to 0.5dB step 00h: -14dB
	[5]			
	[4]			
	[3]			
	[2]			
	[1]			
	[0]			
07h	[7]	ALC_MUTE_R	0b	ALC circuit, Rch mute setting 1: ON 0: OFF
	[6]	ALC_DVR	1Ch	ALC circuit, Rch PGA gain value setting in the manual mode 7Fh: MUTE 7Eh to 61h: Set prohibition 60h: +34dB to 0.5dB step 1Ch: 0dB to 0.5dB step 00h: -14dB
	[5]			
	[4]			
	[3]			
	[2]			
	[1]			
	[0]			
08h	[7:0]	TEST0	00h	For LSI TEST
09h	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	0	0b	0: Fixed
	[4]	ADF_BCLK	0b	ADF bit clock frequency setting 1: 32fs 0: 64fs
	[3]	0	00b	0: Fixed
	[2]	ADF_MODE	00b	ADF digital audio data format setting 11, 10: Backward justification 01: Forward justification 00: I <sup>2</sup> S
	[1]			
	[0]			
0Ah	[7]	ADF_DAC_INV	0b	DAC input data inverse setting 1: Inverted 0: Non-inversion
	[6]	ADF_ADC_INV	0b	ADC output data inverse setting 1: Inverted 0: Non-inversion
	[5]	0	0b	0: Fixed
	[4]	DE_EN	0b	De-Emphasis Filter Enable setting 1: ON 0: OFF
	[3]	ADF_FS	0b	Sampling frequency setting 11: Set prohibition 10: 44.1kHz 01: 32kHz 00: 48kHz
	[2]			
	[1]	ADF_LB	0b	Loopback mode setting 1: ON 0: OFF
	[0]	ADF_MASTER	0b	BCLK / LRCLK 1: Master mode 0: Slave mode
0Bh	[7]	SEL_L	10b	Select circuit (Lch) ALC / PGA, DAC select setting 10: DAC output selection 01: ALC / PGA output selection 11, 00: Set prohibition
	[6]			
	[5]	SEL_R	10b	Select circuit (Rch) ALC / PGA, DAC select setting 10: DAC output selection 01: ALC / PGA output selection 11, 00: Set prohibition
	[4]			
	[3]	0	0b	0: Fixed
	[2]	0	0b	0: Fixed
	[1]	MIX_MONO	11b	MIX circuit setting 11: Lch+Rch selected 10: Rch selected 01: Lch selected 00: Set prohibition
	[0]			
0Ch	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	SP_GAIN	00h	Speaker circuit EVR gain setting 3Fh: 0dB (about 0.1 to 3.0dB / step) to 00h: -65.2dB
	[4]			
	[3]			
	[2]			
	[1]			
	[0]			

# LC07424LP

ADRS	Bit	Name	INIT	Description
0Dh	[7:0]	TEST1	00h	For LSI TEST
0Eh	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	SP_ZCD	1b	Speaker amplifier circuit, Zero cross detection setting 1: ON 0: OFF
	[4]	SP_ZCDTM	01b	Speaker amplifier circuit, Time setting at the zero cross time
	[3]			11: 1024 (1 / fs) 10: 512 (1 / fs) 01: 256 (1 / fs) 00: 128 (1 / fs)
	[2]	SP_SOFTSW	1b	Speaker amplifier circuit, Soft switch function setting 1: ON 0: OFF
	[1]	SP_SSC	11b	Speaker amplifier circuit, Time setting of soft switch operation
	[0]			11: 200ms 10: 100ms 01: 50ms 00: 10ms
0Fh	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	0	0b	0: Fixed
	[4]	0	0b	0: Fixed
	[3]	LO_DET_VDD	1b	Line output, V <sub>DDH</sub> power detection function 1: ON 0: OFF
	[2]	LO_GAIN	1b	Line output, Gain setting 1: 6.5dB 0: 0dB
	[1]	LO_VREFSW	1b	Line output, pin state control 1: Connected with VREF 0: Not connected with VREF
	[0]	LO_MUTE	1b	Line output, MUTE setting 1: ON 0: OFF
10h	[7:0]	TEST2	00h	For LSI TEST
11h	[7:0]	TEST3	00h	For LSI TEST
12h	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	V <sub>D</sub> _Y_GAIN	11h	Y <sub>1N</sub> pin signal gain setting,
	[4]			3Fh to 23h: Set prohibition
	[3]			22h: 8.2dB
	[2]			to (about 0.1dB / step)
	[1]			11h: 6.5dB
	[0]			to (about 0.1dB / step)
[0]	00h: 4.8dB			
13h	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	V <sub>D</sub> _C_GAIN	11h	C <sub>1N</sub> pin signal gain setting
	[4]			3Fh to 23h: Set prohibition
	[3]			22h: 8.2dB
	[2]			to (about 0.1dB / step)
	[1]			11h: 6.5dB
	[0]			to (about 0.1dB / step)
[0]	00h: 4.8dB			
14h	[7]	0	0b	0: Fixed
	[6]	0	0b	0: Fixed
	[5]	0	0b	0: Fixed
	[4]	0	0b	0: Fixed
	[3]	0	0b	0: Fixed
	[2]	0	0b	0: Fixed
	[1]	V <sub>D</sub> _SAG_MODE	1b	Video driver, Operation setting 1: Sag compensation 0: DC direct coupling
	[0]	0	0b	0: Fixed
15h	[7:0]	TEST4	11h	For LSI TEST
16h	[7:0]	TEST5	02h	For LSI TEST
17h	[7:0]	TEST6	00h	For LSI TEST
18h	[7:0]	TEST7	05h	For LSI TEST
19h	[7:0]	TEST8	00h	For LSI TEST
1Ah	[7:0]	TEST9	FFh	For LSI TEST
1Bh	[7:0]	TEST10	00h	For LSI TEST
1Ch	[7:0]	TEST11	00h	For LSI TEST
1Dh	[7:0]	TEST12	00h	For LSI TEST

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## Detailed Description of Registers

Reference voltage generator circuit

VREF\_BIAS: Voltage REFERENCE BIAS

ADRS	Bit	Name	INIT	Description
00h	[7: 6]	VREF_BIAS[1: 0]	00b	Common reference voltage circuit setting (Vref_H_C and Vref_C pins) 11: Normal operation <*1> 10: VREF Rapid charging<*1> 01: VREF pull-down 00: Power down

"9.1 Reference power supply, Line-out start / stop sequence" on page 31.

<\*1>"VREF rapid charge"setting allows rapid arrival at the target voltage through connection of resistor.

"Normal operation" setting enables power-saving operation through connection of standard resistor.

## Logic synchronization clear

SYNC\_CLR: SYNChronous CLear

ADRS	Bit	Name	INIT	Description
00h	[5]	SYNC_CLR	0b	Digital block synchronized reset control 1: Reset 0: Normal operation This is used if the logic operation should become unstable, and not used normally.

## Power down circuit, Speaker output Control

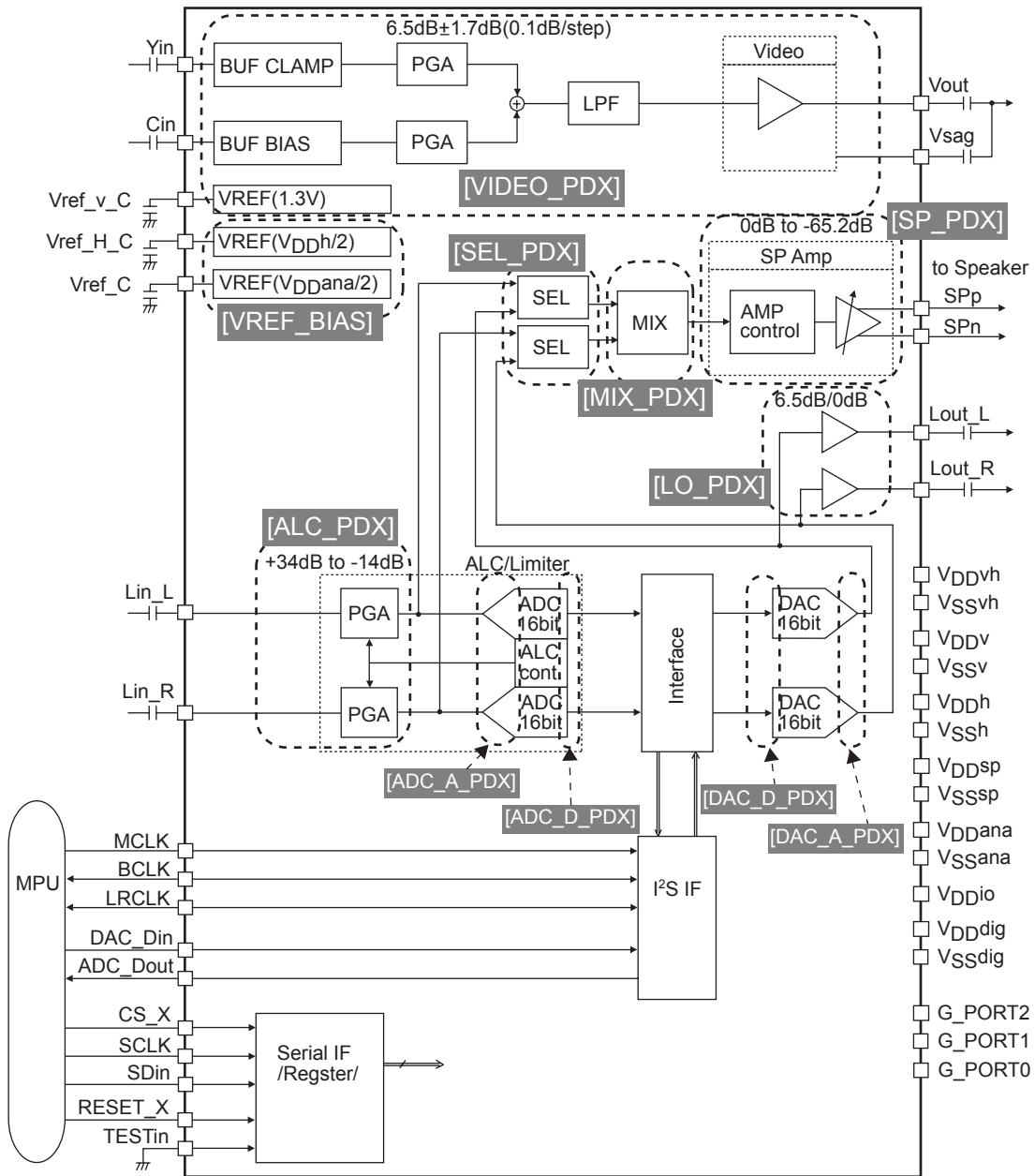
- SEL\_PDX : SElector Power Down (low active)
- ALC\_PDX : ALC Power Down (low active)
- ADC\_A\_PDX : ADC Analog Power Down (low active)
- DAC\_A\_PDX : DAC Analog Power Down (low active)
- VIDEO\_PDX : VIDEO Power Down (low active)
- SP\_OUTEN : SPeaker OUTput ENable
- SP\_PDX : SPeaker amp Power Down (low active)
- MIX\_PDX : MIXer Power Down (low active)
- LO\_PDX : Line Out Power Down (low active)
- ADC\_D\_PDX : ADC Digital Power Down (low active)
- DAC\_D\_PDX : DAC Digital Power Down (low active)
- SP\_EVR\_PDX : SPeaker EVR Power Down (low active)

ADRS	Bit	Name	INIT	Description
00h	[4]	SEL_PDX	0b	Selector block power down 1: Normal operation 0: Power down
	[3]	ALC_PDX	0b	ALC block power down 1: Normal operation 0: Power down
	[2]	ADC_A_PDX	0b	ADC analog block power down 1: Normal operation 0: Power down
	[1]	DAC_A_PDX	0b	DAC analog block power down 1: Normal operation 0: Power down
	[0]	VIDEO_PDX	0b	VIDEO power down 1: Normal operation 0: Power down
01h	[7]	SP_OUTEN	0b	Speaker out enable 0: Speaker output stop 1: Normal operation
	[6]	SP_PDX	0b	Speaker power down 1: Normal operation 0: Power down
	[5]	MIX_PDX	0b	MIX power down 1: Normal operation 0: Power down
	[4]	0	0b	0: Fixed
	[3]	LO_PDX	0b	Line out power down 1: Normal operation 0: Power down
	[2]	ADC_D_PDX	0b	ADC digital block power down 1: Normal operation 0: Power down
	[1]	DAC_D_PDX	0b	DAC digital block power down 1: Normal operation 0: Power down
	[0]	SP_EVR_PDX	0b	Speaker EVR power down 1: Normal operation 0: Fixed at [SP_GAIN]=00h

When the circuit concerned is not used and the power saving function is to be made effective for this circuit, turn ON the power DOWN function.

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Corresponding position diagram between Power Down registers and function blocks (for reference)



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## Line input circuits

ALC\_LI\_L: ACL Line select Left channel

ALC\_LI\_R: ALC Line select Right channel

ADRS	Bit	Name	INIT	Description
02h	[4]	ALC_LI_L	1b	Lch Line input selection 1: Selection 0: Non-selection (L <sub>IN_L</sub> pin enters the OPEN state.)
	[0]	ALC_LI_R	1b	Rch Line input selection 1: Selection 0: Non-selection (L <sub>IN_R</sub> pin enters the OPEN state.)

## ALC circuit settings

ALC\_VAL : ALC VALue  
 ALC\_FA : ALC Factor Attack  
 ALC\_FR : ALC Factor Recovery  
 ALC\_ZCD : ALC Zero Cross Detect  
 ALC\_ZCDTM : ALC Zero Cross Detect TiME out  
 ALC\_FULLEN : ALC FULL scale detect ENable  
 ALC\_ATLIM : ALC ATtack LIMit  
 ALC\_RWT : ALC Recovery Waiting Time  
 ALC\_OFF : ALC operation OFF  
 ALC\_VMAX : ALC Value MAX  
 ALC\_MUTE\_L : ALC MUTE Left channel  
 ALC\_DVL : ALC Digital Value Left channel  
 ALC\_MUTE\_R : ALC MUTE Right channel  
 ALC\_DVR : ALC Digital Value Right channel

ADRS	Bit	Name	INIT	Description
03h	[7:5]	ALC_VAL[2:0]	001b	ALC circuit, ALC value (limiter level) setting □*1□ 111: -10dBFS 110: -9dBFS 101: -8dBFS 100: -7dBFS 011: -6dBFS 010: -5dBFS 001: -4dBFS 000: -3dBFS
	[4:3]	ALC_FA[1:0]	11b	ALC circuit, Attack factor setting Gain DOWN amount at fs cycle □*2□ 11: (1/8)dB 10: (1/4)dB 01: (1/2)dB 00: (1/1)dB
	[2:0]	ALC_FR[2:0]	101b	ALC circuit, Recovery factor setting Gain UP amount at fs cycle □*3□ 111: (1/2 <sup>14</sup> )dB 110: (1/2 <sup>13</sup> )dB 101: (1/2 <sup>12</sup> )dB 100: (1/2 <sup>11</sup> )dB 011: (1/2 <sup>10</sup> )dB 010: (1/2 <sup>9</sup> )dB 001: (1/2 <sup>8</sup> )dB 000: (1/2 <sup>7</sup> )dB

⟨\*1⟩ For example, -10dBFS (dB Full Scale) is on the level 10 dB lower than the Full Scale.

⟨\*2⟩ For example, [ALC\_FA] = 11b causes 1 dB gain DOWN at the eight cycle of fs.

⟨\*3⟩ For example, [ALC\_FR] = 111b causes 1 dB gain UP at the 2<sup>14</sup> (=16384) cycle of fs.

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ADRS	Bit	Name	INIT	Description
04h	[7]	ALC_ZCD	1b	ALC circuit, Gain change in the zero cross timing 1: Gain changed in the zero cross timing 0: Gain changed without waiting for zero cross timing
	[6:5]	ALC_ZCDTM[1:0]	00b	ALC circuit, Time setting for timeout at zero cross detection Effective when [ALC_ZCD]=1 11: 8192 (1 / fs) 10: 4096 (1 / fs) 01: 2048 (1 / fs) 00: 1024 (1 / fs)
	[4]	ALC_FULLEN	0b	ALC circuit, Full scale detection operation setting Rapid level down at detection of full scale 1: ON 0: OFF
	[3:2]	ALC_ATLIM[1:0]	01b	ALC circuit, Limit setting for the attack operation frequency between zero crosses effective when [ALC_ZCD]=1. For the actual reduction for the frequency, See Table 1. 11: 16 10: 8 01: 4 00: 2
	[1:0]	ALC_RWT[1:0]	10b	ALC circuit, Standby time setting during recovery operation. 11: 2048 (1 / fs) 10: 1024 (1 / fs) 01: 512 (1 / fs) 00: 256 (1 / fs)
05h	[7]	ALC_OFF	0b	ALC circuit, Operation stop 1: Operation stop (manual mode) [ALC_DVL] and [ALC_DVR] become effective. 0: Normal operation
	[6:0]	ALC_VMAX[6:0]	1Ch	ALC circuit, PGA maximum gain value setting during ALC operation See Table 8.2.
06h	[7]	ALC_MUTE_L	0b	ALC circuit, PGA MUTE setting (Lch) 1: ON 0: OFF
	[6:0]	ALC_DVL[6:0]	1Ch	ALC circuit, Lch PGA gain value setting in the manual mode See Table 8.2.
07h	[7]	ALC_MUTE_R	0b	ALC circuit, PGA MUTE setting (Rch) 1: ON 0: OFF
	[6:0]	ALC_DVR[6:0]	1Ch	ALC circuit, Rch PGA gain value setting in the manual mode See Table 8.2.

Refer to "Description of ALC operation."

Table 8.1. "Reduction value for the set frequency"

[ALC_ATLIM]	No, of times	[ALC_FA]			
		11b	10b	01b	00b
11b	16	2 dB	4 dB	8 dB	16 dB
10b	8	1 dB	2 dB	4 dB	8 dB
01b	4	0.5 dB	1 dB	2 dB	4 dB
00b	2	0.25 dB	0.5 dB	1 dB	2 dB

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Table 8.2 ALC circuit gain setting table (TYP value) ALC\_VMAX[6: 0] / ALC\_DVL[6: 0] / ALC\_DVL [6: 0]

[6: 0]	gain (dB)	[6: 0]	gain (dB)	[6: 0]	gain (dB)	[6: 0]	gain (dB)	
7Fh	Set prohibition	5Fh	33.5	3Fh	17.5	1Fh	1.5	
7Eh		5Eh	33.0	3Eh	17.0	1Eh	1.0	
7Dh		5Dh	32.5	3Dh	16.5	1Dh	0.5	
7Ch		5Ch	32.0	3Ch	16.0	1Ch	0.0	
7Bh		5Bh	31.5	3Bh	15.5	1Bh	-0.5	
7Ah		5Ah	31.0	3Ah	15.0	1Ah	-1.0	
79h		59h	30.5	39h	14.5	19h	-1.5	
78h		58h	30.0	38h	14.0	18h	-2.0	
77h		57h	29.5	37h	13.5	17h	-2.5	
76h		56h	29.0	36h	13.0	16h	-3.0	
75h		55h	28.5	35h	12.5	15h	-3.5	
74h		54h	28.0	34h	12.0	14h	-4.0	
73h		53h	27.5	33h	11.5	13h	-4.5	
72h		52h	27.0	32h	11.0	12h	-5.0	
71h		51h	26.5	31h	10.5	11h	-5.5	
70h		50h	26.0	30h	10.0	10h	-6.0	
6Fh		4Fh	25.5	2Fh	9.5	0Fh	-6.5	
6Eh		4Eh	25.0	2Eh	9.0	0Eh	-7.0	
6Dh		4Dh	24.5	2Dh	8.5	0Dh	-7.5	
6Ch		4Ch	24.0	2Ch	8.0	0Ch	-8.0	
6Bh		4Bh	23.5	2Bh	7.5	0Bh	-8.5	
6Ah		4Ah	23.0	2Ah	7.0	0Ah	-9.0	
69h		49h	22.5	29h	6.5	09h	-9.5	
68h		48h	22.0	28h	6.0	08h	-10.0	
67h		47h	21.5	27h	5.5	07h	-10.5	
66h		46h	21.0	26h	5.0	06h	-11.0	
65h		45h	20.5	25h	4.5	05h	-11.5	
64h		44h	20.0	24h	4.0	04h	-12.0	
63h		43h	19.5	23h	3.5	03h	-12.5	
62h		42h	19.0	22h	3.0	02h	-13.0	
61h		41h	18.5	21h	2.5	01h	-13.5	
60h		34	40h	18.0	20h	2.0	00h	-14.0

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## Audio data format, Other

- ADF\_BCLK : Audio Data Format BCLK
- ADF\_MODE : Audio Data Format MODE
- ADF\_DAC\_INV : Audio Data Format DAC data INVert
- ADF\_ADC\_INV : Audio Data Format ADC data INVert
- DE\_EN: De-Emphasis filter ENable
- ADF\_FS : Audio Data Format Frequency Sampling
- ADF\_LB : Audio Data Format Loop Back
- ADF\_MASTER : Audio Data Format MASTER mode

ADRS	Bit	Name	INIT	Description
09h	[4]	ADF_BCLK	0b	Bit clock frequency setting of audio data format See Table 8.3.
	[1:0]	ADF_MODE[1:0]	00b	Audio data format setting See Table 8.3.
0Ah	[7]	ADF_DAC_INV	0b	DAC input data inverted setting 1: Inverted 0: Non-inversion
	[6]	ADF_DAC_INV	0b	ADC output data inverted setting 1: Inverted 0: Non-inversion
	[4]	DE_EN	0b	De-Emphasis Filter setting 1: De-Emphasis Filter Effective 0: De-Emphasis Filter Not effective
	[3:2]	ADF_FS[1:0]	00b	Sampling Frequency Setting 11: Set prohibition 10: 44.1kHz 01: 32kHz 00: 48kHz
	[1]	ADF_LB	0b	Loop back mode select. See Fig. 8.1. 1: ON (ADC output data becomes the DAC input data.) 0: OFF (Normal operation. DAC_DIN pin input becomes the DAC input data.)
	[0]	ADF_MASTER	0b	Master / Slave mode setting (IO control of BCLK and LRCLK pins ) 1: Master mode (BCLK and LRCLK pins for output) 0: Slave mode (BCLK and LRCLK pins for input)

"7. Audio data format."

### Loop back function

This function connects internally ADC\_DOUT and DAC\_DIN signals. This will enable the ADC input signal to go through to the DAC output. In this case, the ADC\_DOUT pin output signal is effective, but the DAC\_DIN pin input becomes ineffective.

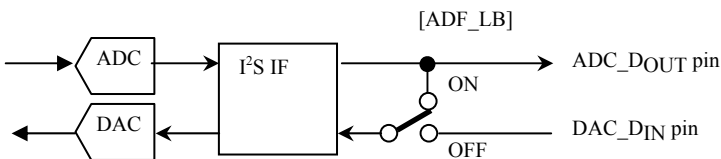


Fig.8.1. Loop back circuit

Table 8.3 ADF setting

[ADF_MODE]	[ADF_BCLK]	
11	-	Set prohibition
10	1	Backward justification 32fs
01	1	Forward justification 32fs
00	1	I²S 32fs
10	0	Backward justification 64fs
01	0	Forward justification 64fs
00	0	I²S 64fs

### Selector, Mixer circuit

- SEL\_L : SELctor Lch
- SEL\_R : SELctor Rch
- MIX\_MONO : MIXer MONO

ADRS	Bit	Name	Init	Description
0Bh	[7:6]	SEL_L	10b	Selector circuit. Lch signal selection 10: DAC output selection 01: ALC / PGA output selection 11, 00: Set prohibition
	[5:4]	SEL_R	10b	Selector circuit. Rch signal selection 10: DAC output selection 01: ALC / PGA output selection 11, 00: Set prohibition
	[1:0]	MIX_MONO	11b	MIX circuit, Setting 11: Lch+Rch setting 10: Rch setting 01: Lch setting 00: Set prohibition

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## Speaker amplifier circuits

SP\_GAIN : SPeaker evr GAIN  
 SP\_ZCD : SPeaker Zero Cross Detect  
 SP\_ZCDTM : SPeaker Zero Cross Detect TiMe out  
 SP\_SOFTSW : SPeaker SOFT SWitch  
 SP\_SSC : SPeaker Soft Switch time Control

ADRS	Bit	Name	Init	Description
0Ch	[5:0]	SP_GAIN	00b	Gain setting for the speaker amplifier circuit and EVR circuit See Table 8.4.
0Eh	[5]	SP_ZCD	1b	Speaker amplifier circuit. Gain change in the zero cross timing. 1: Gain changed in the zero cross timing 0: Gain changed without waiting for the zero cross timing
	[4:3]	SP_ZCDTM	01b	Speaker amplifier circuit. Time setting at zero cross timeout 11:1024 (1 / fs) 10: 512 (1 / fs) 01: 256 (1 / fs) 00: 128 (1 / fs)
	[2]	SP_SOFTSW	1b	Speaker amplifier circuit. Soft switch function setting 1:ON 0:OFF
	[1:0]	SP_SSC	11b	Speaker amplifier circuit. Time setting when soft switch operates 11: 200ms 10: 100ms 01: 50ms 00: 10ms

Table 8.4. Speaker EVR circuit gain setting (TYP value)

[SP_GAIN]	gain (dB)	[SP_GAIN]	gain(dB)	[SP_GAIN]	gain (dB)	[SP_GAIN]	gain (dB)
3Fh	0.0	2Fh	-2.2	1Fh	-8.4	0Fh	-24.6
3Eh	-0.1	2Eh	-2.4	1Eh	-9.2	0Eh	-26.2
3Dh	-0.2	2Dh	-2.6	1Dh	-10.0	0Dh	-28.0
3Ch	-0.3	2Ch	-2.7	1Ch	-10.7	0Ch	-30.4
3Bh	-0.4	2Bh	-2.9	1Bh	-11.5	0Bh	-32.4
3Ah	-0.5	2Ah	-3.3	1Ah	-12.1	0Ah	-35.0
39h	-0.6	29h	-3.6	19h	-12.9	09h	-37.5
38h	-0.7	28h	-3.9	18h	-13.8	08h	-39.7
37h	-0.8	27h	-4.1	17h	-14.9	07h	-42.6
36h	-0.9	26h	-4.4	16h	-15.7	06h	-45.8
35h	-1.0	25h	-5.0	15h	-16.8	05h	-48.7
34h	-1.2	24h	-5.4	14h	-17.8	04h	-51.8
33h	-1.4	23h	-6.0	13h	-18.8	03h	-54.7
32h	-1.6	22h	-6.5	12h	-19.7	02h	-57.8
31h	-1.8	21h	-6.9	11h	-21.3	01h	-60.8
30h	-2.0	20h	-7.6	10h	-22.8	00h	-65.2

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## Line out circuit

LO\_DET\_VDD: Line Out DETct VDDh  
 LO\_GAIN : Line Out GAIN  
 LO\_VREFSW : Line Out Voltage REFerence SWitch  
 LO\_MUTE : Line Out MUTE

ADRS	Bit	Name	Init	Description
0Fh	[3]	LO_DET_VDD	1b	Line output. VDDh power detection function 1: ON 0: OFF
	[2]	LO_GAIN	1b	Line output. Amplifier gain setting 1: 6.5dB 0: 0dB
	[1]	LO_VREFSW	1b	Line output. Effective for pin state control and power DOWN ([LO_PDX]=0) 1: LOUT_L and LOUT_R pins become the VREF level output. 0: LOUT_L and LOUT_R pins become Hi-Z.
	[0]	LO_MUTE	1b	Line output. MUTE setting 1: ON 0: OFF

VDDh power detection function (operation for setting of [LO\_MUTE]=0 and [LO\_PDX]=1)

When VDDh power supply becomes 4.0V (TYP) or less, the line output is automatically set to the state equivalent to "[LO\_MUTE]=1, [LO\_PDX]=0."

When VDDh power supply returns to 4.3V (TYP) or more, the line output is automatically set to the state equivalent to "[LO\_MUTE]=0, [LO\_PDX]=1."

Refer to "1. Reference power supply, line out start/stop sequence."

## Video circuit

VD\_Y\_GAIN : Video Driver Y GAIN  
 VD\_C\_GAIN : Video Driver C GAIN  
 VD\_SAG\_MODE: Video Driver SAG MODE

ADRS	Bit	Name	INIT	Description
12h	[5:0]	VD_Y_GAIN[5:0]	11h	Video driver. YIN pin input gain setting See Table 8.5.
13h	[5:0]	VD_C_GAIN[5:0]	11h	Video driver. CIN pin input gain setting See Table 8.5.
14h	[1]	VD_SAG_MODE	1b	Video driver. VOUT pin output setting 1: Sag compensation type 0: DC direct coupling type

Table 8.5. Video driver circuit gain setting (TYP value) VD\_Y\_GAIN [5: 0] / VD\_C\_GAIN [5: 0]

[5: 0]	gain (dB)	[5: 0]	gain (dB)	[5: 0]	gain (dB)	[5: 0]	gain (dB)	
3Fh	Set prohibition	2Fh	Set prohibition	1Fh	7.9	0Fh	6.3	
3Eh		2Eh		1Eh	7.8	0Eh	6.2	
3Dh		2Dh		1Dh	7.7	0Dh	6.1	
3Ch		2Ch		1Ch	7.6	0Ch	6.0	
3Bh		2Bh		1Bh	7.5	0Bh	5.9	
3Ah		2Ah		1Ah	7.4	0Ah	5.8	
39h		29h		19h	7.3	09h	5.7	
38h		28h		18h	7.2	08h	5.6	
37h		27h		17h	7.1	07h	5.5	
36h		26h		16h	7.0	06h	5.4	
35h		25h		15h	6.9	05h	5.3	
34h		24h		14h	6.8	04h	5.2	
33h		23h		13h	6.7	03h	5.1	
32h		22h		8.2	12h	6.6	02h	5.0
31h		21h		8.1	11h	6.5	01h	4.9
30h		20h		8.0	10h	6.4	00h	4.8

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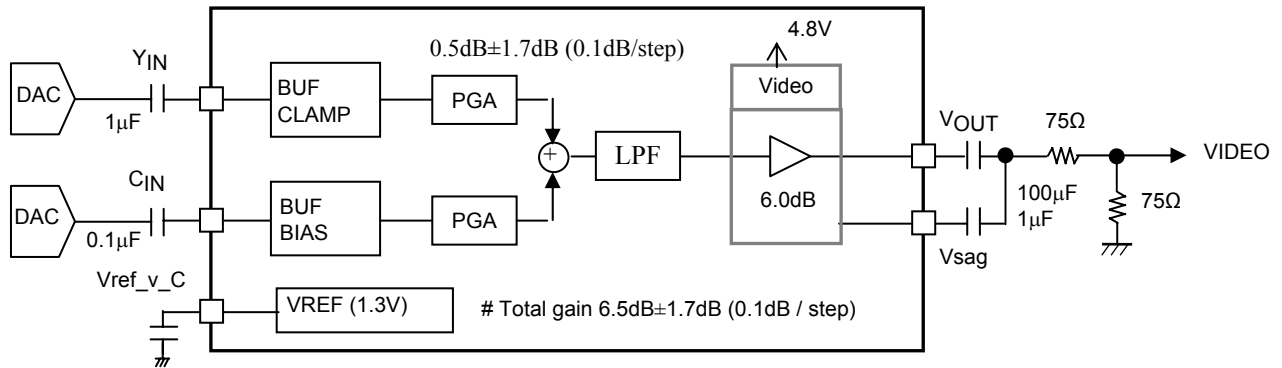
## Sag compensation type ([VD\_SAG\_MODE]=1b)

Value (TYP) when DAC output is 1Vp-p and gain setting is 6dB

	Sync tip level	Video signal level
Y <sub>IN</sub> pin	0.8V	1Vp-p
V <sub>OUT</sub> pin	1.0V (Note 1)	2Vp-p
VIDEO	(Note 2)	1Vp-p

(Note 1) Fluctuation in V cycle because of sag compensation

(Note 2) Fluctuation according to the video signal waveform

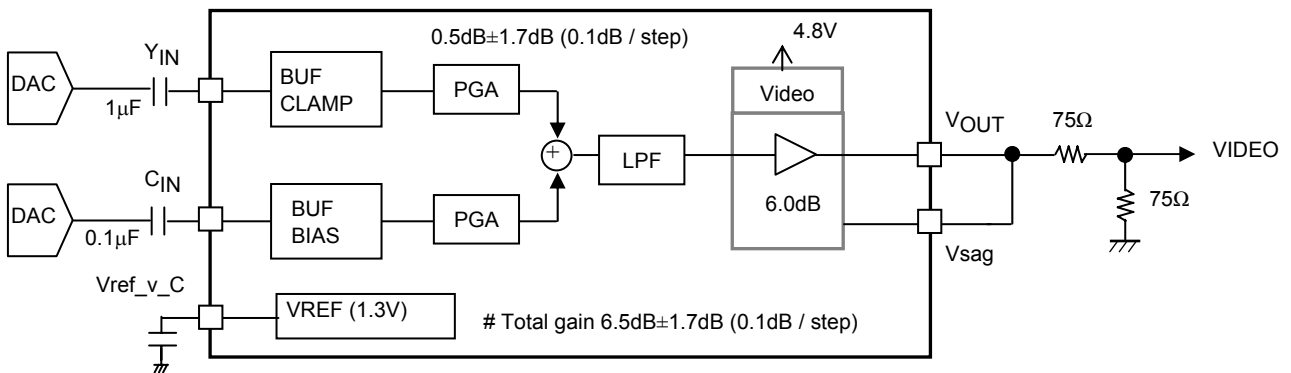


## DC direct coupling type ([VD\_SAG\_MODE]=0b)

Value (TYP) when DAC output is 1Vp-p and gain setting is 6dB (TYP)

	Sync tip level	Video signal level
Y <sub>IN</sub> pin	0.8V	1Vp-p
V <sub>OUT</sub> pin	0.2V (Note 3)	2Vp-p
VIDEO	0.1V	1Vp-p

(Note 3) The sink chip level is lower than the sag compensation type so as to minimize the power dissipation.

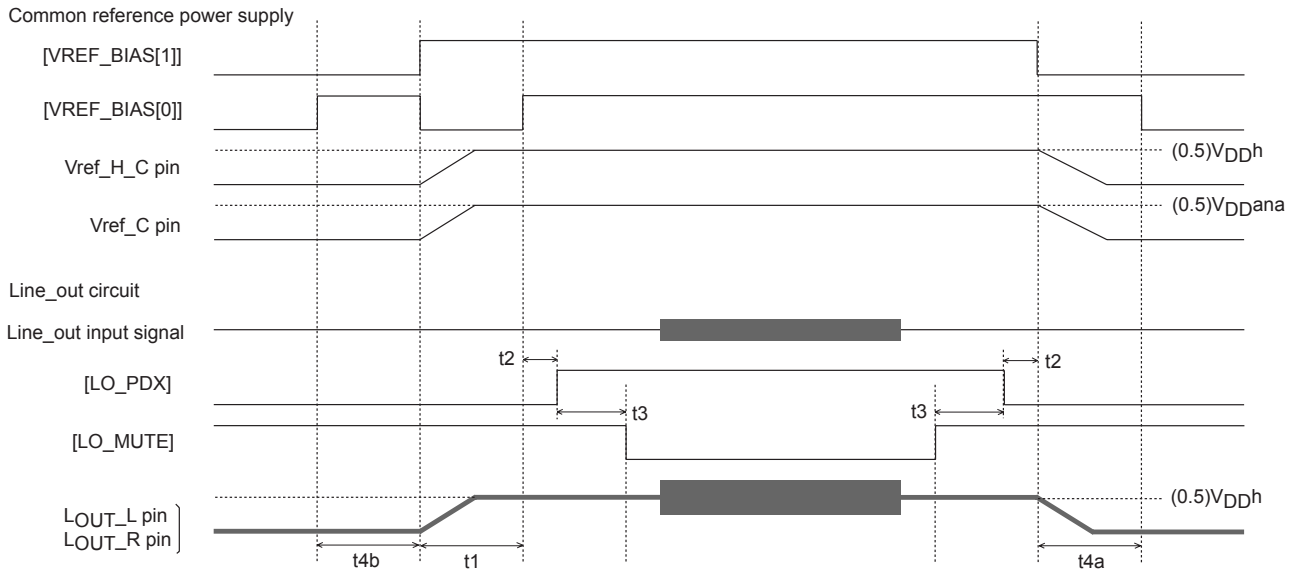


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## Control to reduce the POP sound <Note> [xxxx] is a register name.

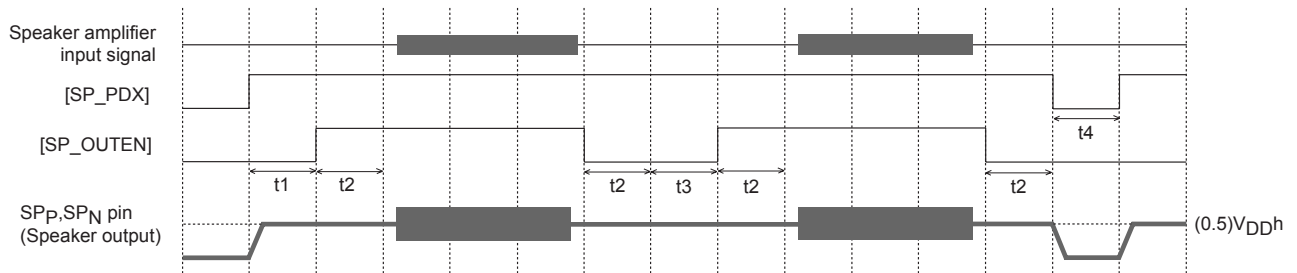
The POP sound can be reduced by performing start/stop in the timing shown below.

### Reference power supply, line out start / stop sequence



- Recommendation value
  - t1 > 300ms (Rapid charge period with the Vref\_H\_C pin connection capacity of 1 $\mu$ F and the Vref\_C pin connection capacity of 4.7 $\mu$ F)
  - t2 > 0ms
  - t3 > 1ms (Waiting time of MUTE ON / OFF)
  - t4a > 300ms (Pull down period)
  - t4b > 1ms (Pull down period, at already when LOUT\_L, LOUT\_R pin is GND level.)
- It makes it to 0Fh: [LO\_VREFSW] = 1, usually.
- [LO\_VREFSW] function at power down ([LO\_PDX] = 0)
  - [LO\_VREFSW] = 1: LOUT\_L, LOUT\_R pin becomes VREF level output
  - [LO\_VREFSW] = 0: LOUT\_L, LOUT\_R pin becomes Hi-Z

### Speaker Amplifier Start / Stop Sequence



- Recommendation value
  - t1 > 1ms (Speaker bias start-up time)
  - t2: [SP\_SSC] set time (200ms / 100ms / 50ms / 10ms)
  - t3 > 1ms
  - t4 > 1ms
- [SP\_OUT\_EN] must be set to 0 when power down ([SP\_PDX] = 0) mode.

## Description of ALC operation ◁ Note ▷ [xxxx] is a register name.

The ALC (Automatic Level Control) function performs automatic adjustment so that the audio level becomes the set value. The amplifier gain of PGA (Programmable Gain Amplifier) is automatically controlled so that the ADC output audio level becomes equal to the ALC value [ALC\_VAL].

The PGA gain variable range is +34dB to -14dB. This range helps setting the maximum value [ALC\_VMAX].

⇒ By setting [ALC\_VMAX] to the maximum value (+34dB), the ALC function can be used to the maximum limit.

⇒ By setting [ALC\_VMAX] to the gain zero (+0dB), there is no gain in the "+" direction. Namely, the operation becomes equivalent to the limiter function.

### ALC settings

- Power down function  
When [ALC\_PDX]=0, the ALC circuit enters the power DOWN mode.
- System operation  
This is done by digitally processing and feeding back the ADC data.  
For this purpose, the ADC function becomes necessary.  
Therefore, to activate the ALC function;  
[ALC\_PDX]=1 (ALC power DOWN mode OFF )  
[ALC\_OFF]=0 (ALC function ON)  
[ADC\_A\_PDX]=1, [ADC\_D\_PDX]=1 (ADC activated)

### Manual mode (ALC Function OFF)

With [ALC\_OFF]=1, the manual mode becomes effective.

The PGA gain becomes the [ALC\_DVL] and [ALC\_DVR] values.

### ALC operating

There are "attack" and "recovery" operations. See the operation chart on the next page.

#### (1) Attack operations

When the PGA output exceeds the ALC value [ALC\_VAL], the PGA gain is lowered in a ratio of the attack factor [ALC\_FA].

With zero cross detection [ALC\_ZCD]=1, the gain reduction between zero crosses is limited by the limit value [ALC\_ATLIM].

#### (2) Recovery operations

When the PGA output is 2dB less than the ALC value [ALC\_VAL] and this state continues for the recovery standby period [ALC\_RWT], the PGA gain is increased in a ratio of the recovery factor [ALC\_FR].

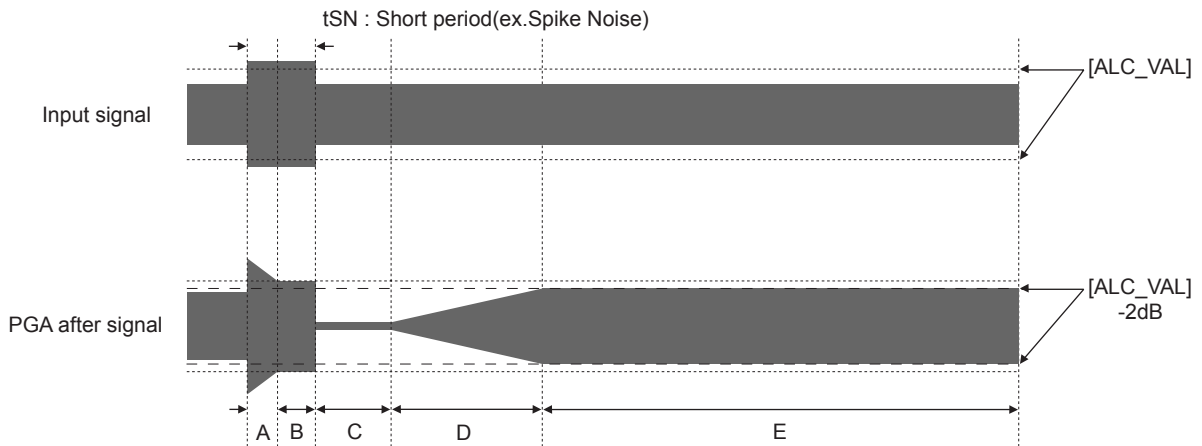
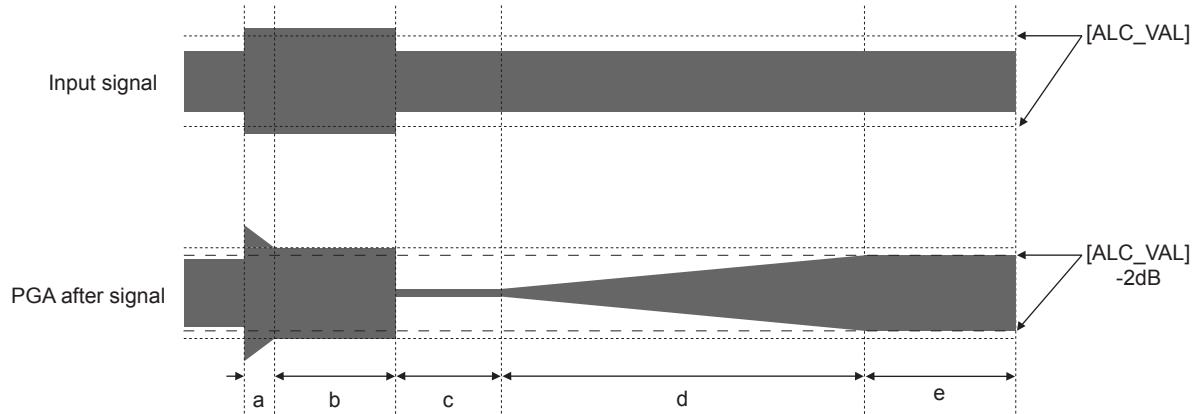
The PGA gain increase continues while the state in which the gain is 2dB less than the ALC value [ALC\_VAL].

The PGA gain increment between zero crosses is maximum 1 dB.

### Functions common to (1) and (2)

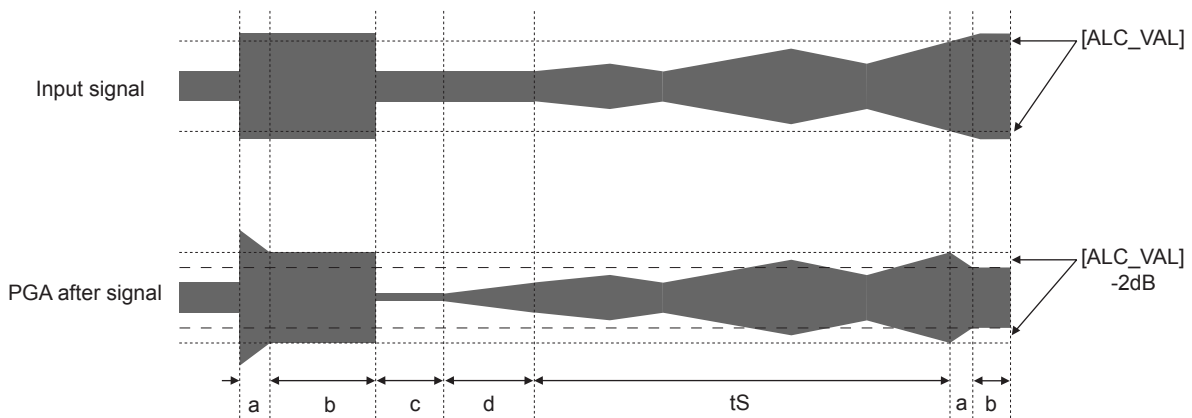
- Zero cross detection  
With [ALC\_ZCD]=1, PGA gain change occurs only when the PGA output is in the zero cross timing.  
With [ALC\_ZCD]=0, PGA gain change is made regardless of whether or not PGA output is zero cross.
- Zero cross timeout  
If the PGA output does not zero cross, the zero cross signal is generated internally if there is no zero cross signal for the period of zero cross timeout value [ALC\_ZCDTM].
- Average output amplitude control  
In the attack operation by spike noise, etc., the average output amplitude becomes small.  
To prevent this, the recover speed is raised automatically above the [ALC\_FR] set value in the case of excessively large input for a short period (tSN).

ALC Wave Forms



Range	Operating	PGA gain	Related registers
a, A	Attack	Rapid reduction	[ALC_FA] Attack factor
b, B	Stable	Constant	[ALC_VAL] ALC value
c, C	Recovery wait time	Constant	[ALC_RWT] Recovery standby time
d,	Recovery	Slow increase	[ALC_FR] Recovery factor
, D	Recovery	Increase faster than d	[ALC_FR] Recovery factor
e, E	Stable	Constant	[ALC_VMAX] PGA gain maximum value

Limiter operation (PGA gain maximum value [ALC\_VMAX]= 0dB set)



In the tS range, the "input" is equivalent to "PGA After" in terms of signal level. (signal level through)

## Checkpoints

!! The user is responsible for ascertaining whether this IC can be adopted for the mass production sets, including the various conditions for mounting in the set.

## Power supply

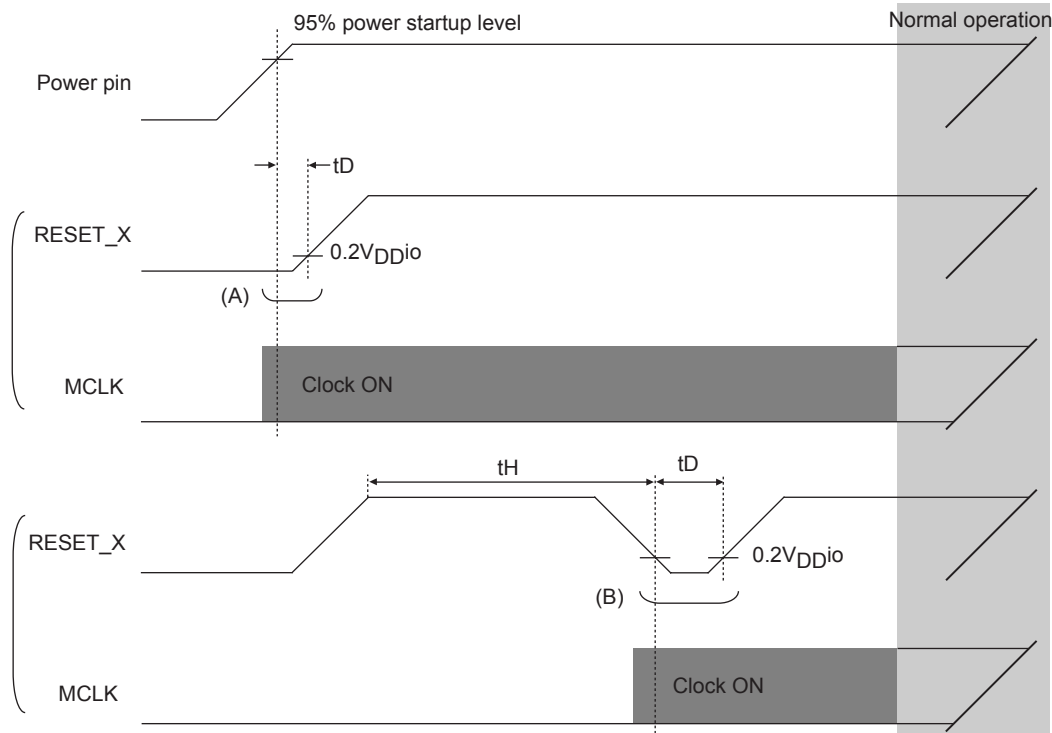
- Power pins are 4.8V, 2.8V, and 1.8V systems.
  - 4.8V system: Analog power supplies ( $V_{DDh}$ ,  $V_{DDvh}$ )
  - 2.8V system: Analog power supplies ( $V_{DDana}$ ,  $V_{DDsp}$ ,  $V_{DDv}$ )
  - 1.8V system: Digital power supply ( $V_{DDdig}$ ), digital I/O power supply ( $V_{DDio}$ )
- Connect the decoupling capacitor near the power pin. Refer to our reference substrate data.
- Power ON
  - Simultaneous rise and fall while maintaining the voltage sequence.
  - Alternatively, raise starting from the higher voltage (4.8 V system) side and fall starting from the low voltage (1.8 V system) side.
  - The voltage sequence is 4.8V system  $\geq$  2.8V system  $\geq$  1.8V system.

## Register control

- Set data for all registers including those for the test. Refer to our recommended register data file.
- Registers designated as "registers for LSI test" are fixed at the initial value (INIT).

## Resetting

- When power has been applied, be sure to reset.
  - (A) or (B) is executed as shown in the figure below.
  - (A) is reset at the same time as the power is first applied.
  - (B) is reset immediately after the power is first applied.
- The circuit state is uncertain if the reset is not made. It is recommended to set "th" as short as possible.
- The RESET\_X pin input circuit is subject to clock synchronizing processing.
- Accordingly, the MCLK pin clock input is always necessary even during periods (A) and (B).



$t_D > 10\mu s$  (note that the MCLK input clock frequency is 8MHz or more)

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