

# MC14598B

## 8-Bit Bus-Compatible Latches

The MC14598B is an 8-bit latch addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2.

All 8 outputs from the latches are available in parallel when  $\overline{\text{Enable}}$  is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

### Features

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin ( $\overline{\text{Enable}}$ ) TTL Compatible Input
- Open Drain Full Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except  $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range With Fanout as Follows: 1 TTL Load  
4 LSTTL Loads
- Pb-Free Package is Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input Voltage Range, enable (DC or Transient)	$V_{in}$	-0.5 to $V_{DD}$ +0.5	V
Input Voltage Range, all Other Inputs (DC or Transient)	$V_{in}$	-0.5 to $V_{DD}$ +12	V
Output Voltage Range, (DC or Transient)	$V_{out}$	-0.5 to $V_{DD}$ +0.5	V
Input or Output Current (DC or Transient) per Pin	$I_{in}, I_{out}$	$\pm 10$	mA
Power Dissipation per Package (Note 1)	$P_D$	500	mW
Ambient Temperature Range	$T_A$	-55 to +125	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Lead Temperature (8-Second Soldering)	$T_L$	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

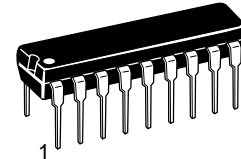
1. Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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PDIP-18  
P SUFFIX  
CASE 707

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedance
0	$D_n$

$D_n$  = State of nth latch  
NC = NO CONNECTION

### ORDERING INFORMATION

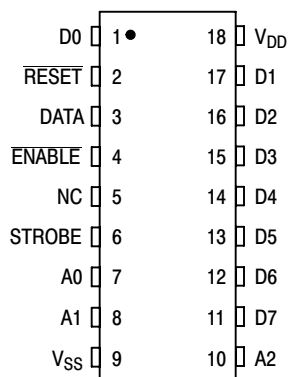
Device	Package	Shipping
MC14598BCP	PDIP-18	20 Units/Rail
MC14598BCPG	PDIP-18 (Pb-Free)	20 Units/Rail

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

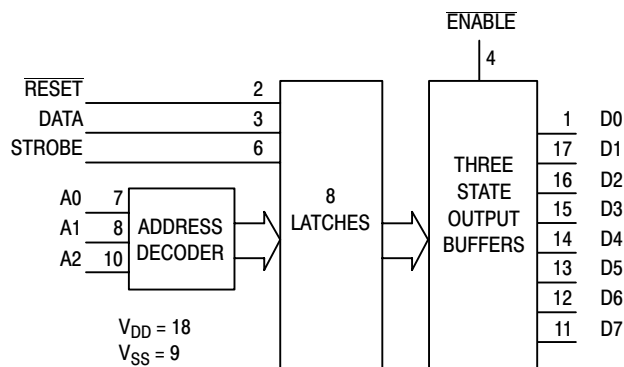
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

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## PIN ASSIGNMENT



## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
Input Voltage (Note 3), Enable (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	-	0.8	-	1.1	0.8	-	0.8	Vdc
			10	-	1.6	-	2.2	1.6	-	1.6	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	V <sub>IH</sub>	5.0	2.0	-	2.0	1.9	-	2.0	-	Vdc
			10	6.0	-	6.0	3.1	-	6.0	-	
Input Voltage Other Inputs (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
Output Drive Current (Full — Sink Only) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-1.0	-	-1.0	-2.0	-	-1.0	-	mAdc
			10	-	-	-	-6.0	-	-	-	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	1.6	-	1.6	3.2	-	1.6	-	mAdc
			10	-	-	-	6.0	-	-	-	
			15	-	-	-	12	-	-		
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
3-State Leakage Current	I <sub>TL</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±3.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current at an External Load Capacitance of 130 pF (Note 3)	I <sub>T</sub>	5.0	I <sub>T</sub> = (2.0 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (4.0 μA/kHz) f + I <sub>DD</sub>								
			I <sub>T</sub> = (6.0 μA/kHz) f + I <sub>DD</sub>								

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.

# MC14598B

## SWITCHING CHARACTERISTICS (Note 4) ( $T_A = 25^\circ\text{C}$ , $C_L = 130\text{ pF} + 1\text{ TTL Load}$ )

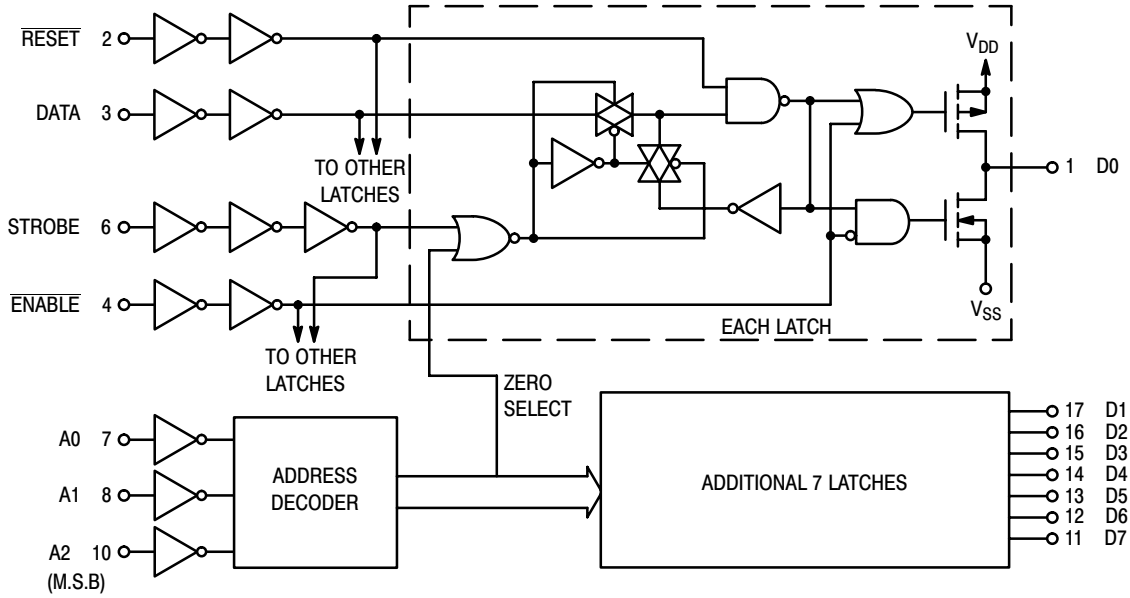
Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (Note 5)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (0.5\text{ ns/pF}) C_L + 35\text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.2\text{ ns/pF}) C_L + 25\text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.16\text{ ns/pF}) C_L + 20\text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Enable to Output	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	– – –	160 125 100	320 250 200	ns
Strobe to Output		5.0 10 15	– – –	200 100 80	400 200 160	
$\overline{\text{Reset}}$ to Output		5.0 10 15	– – –	175 90 70	350 180 140	
Pulse Width Enable	$t_{WH}$ , $t_{WL}$	5.0 10 15	320 240 160	160 120 80	– – –	ns
Strobe		5.0 10 15	200 100 80	100 50 40	– – –	
Increment		5.0 10 15	200 100 80	100 50 40	– – –	
$\overline{\text{Reset}}$		5.0 10 15	300 160 100	150 80 50	– – –	
Setup Time Data	$t_{su}$	5.0 10 15	100 50 35	50 25 20	– – –	ns
Address		5.0 10 15	200 100 70	100 50 35	– – –	
Hold Time Data	$t_h$	5.0 10 15	100 50 35	50 25 20	– – –	ns
Address		5.0 10 15	100 50 35	50 25 20	– – –	
$\overline{\text{Reset}}$ Removal Time	$t_{rem}$	5.0 10 15	20 20 20	–25 –15 –10	– – –	ns

4. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

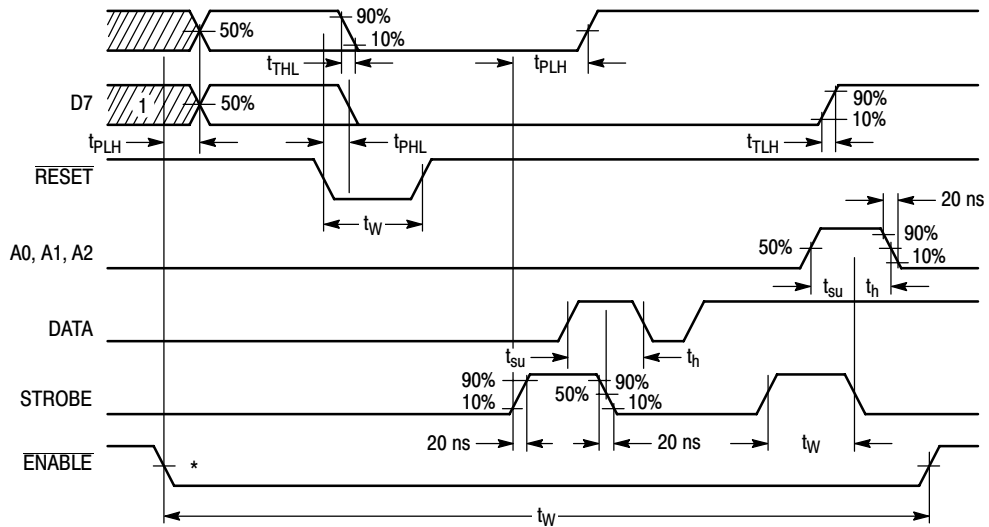
5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14598B

## MC14598B FUNCTION DIAGRAM



## MC14598B TIMING DIAGRAM



\*1.4 V with  $V_{DD} = 5.0$  V

### NOTES:

1. High-impedance output state (another device controls bus).
2. Output Load as for MC14597B.

# MC14598B



**LATCH TRUTH TABLE**

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

\*= No change in state of latch

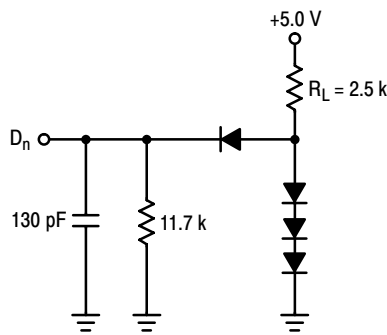
X = Don't care

**TRUTH TABLE FOR MC14597B**

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
	X	1	Count Up	-
	X	1	No Change	-
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

## TEST LOAD, ALL OUTPUTS



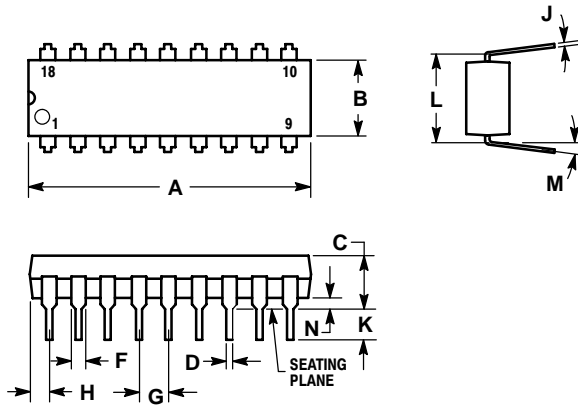
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# MC14598B

## PACKAGE DIMENSIONS


PDIP-18  
CASE 707-02  
ISSUE D



### NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

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