MC1488

Quad Line EIA-232D Driver

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA−232D.

Features

- Current Limited Output
  ±10 mA typical
- Power−Off Source Impedance
  300 Ω minimum
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All ON Semiconductor DTL and TTL Logic Families
- Pb−Free Packages are Available

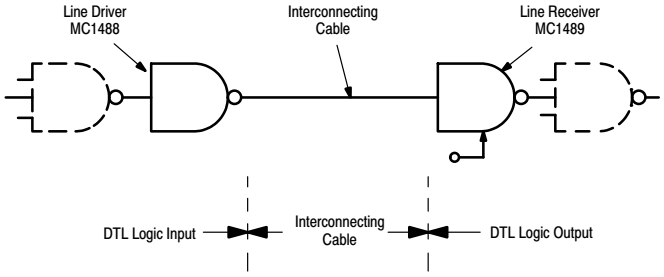
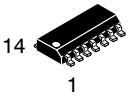


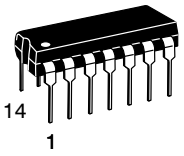
Figure 1. Simplified Application

ON Semiconductor®

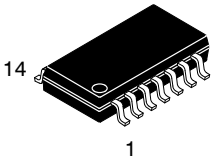
http://onsemi.com



SOIC−14
D SUFFIX
CASE 751A

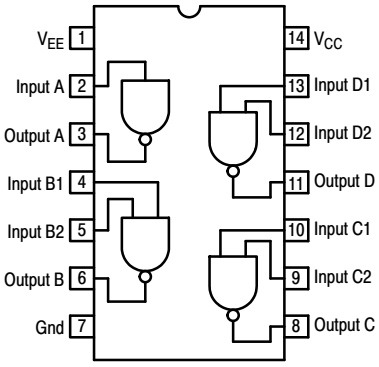


PDIP−14
P SUFFIX
CASE 646



SOEIAJ−14
M SUFFIX
CASE 965

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

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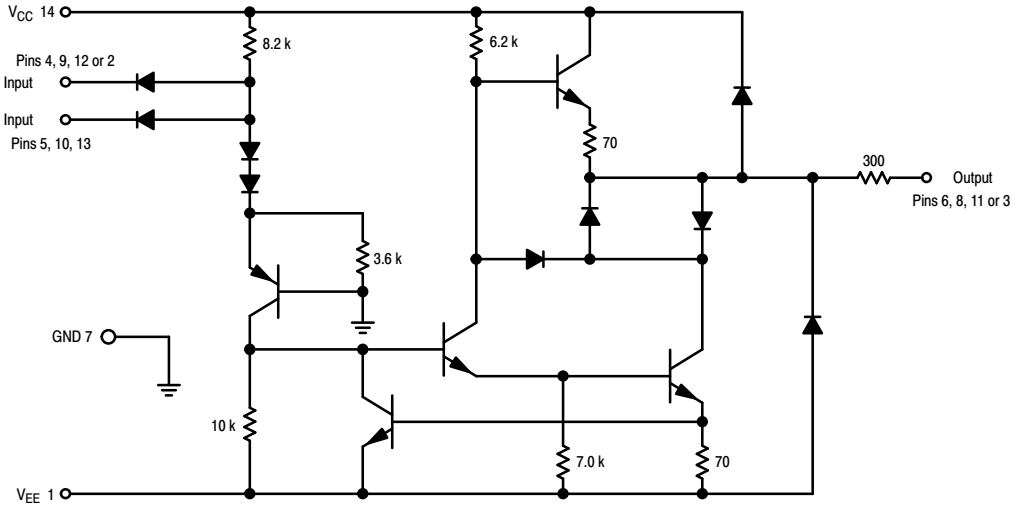


Figure 2. Circuit Schematic
(1/4 of Circuit Shown)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+ 15 − 15	Vdc
Input Voltage Range	V_{IR}	− 15 ≤ V_{IR} ≤ 7.0	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, SO−14 and Plastic Dual−In−Line Package) Derate above T_A = + 25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	− 65 to + 175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = + 9.0 ± 1% Vdc, V_{EE} = −9.0 ± 1% Vdc, T_A = 0 to 75°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current − Low Logic State (V_{IL} = 0)	I_{IL}	−	1.0	1.6	mA
Input Current − High Logic State (V_{IH} = 5.0 V)	I_{IH}	−	−	10	μA
Output Voltage − High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = − 13.2 Vdc)	V_{OH}	 + 6.0 + 9.0	 +7.0 +10.5	 − −	Vdc
Output Voltage − Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = − 13.2 Vdc)	V_{OL}	 − 6.0 − 9.0	 − 7.0 − 10.5	 − −	Vdc
Positive Output Short−Circuit Current, Note 1	I_{OS+}	+ 6.0	+ 10	+ 12	mA
Negative Output Short−Circuit Current, Note 1	I_{OS-}	− 6.0	− 10	− 12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ± 2.0 V)	r_o	300	−	−	Ohms
Positive Supply Current (R_l = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = + 9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = + 12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = + 15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = + 15 Vdc)	I_{CC}	 − − − − − −	 + 15 + 4.5 + 19 + 5.5 − −	 + 20 + 6.0 + 25 + 7.0 + 34 + 12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = − 9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = − 12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = − 15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = − 15 Vdc)	I_{EE}	 − − − − − −	 − 13 − − 18 − − −	 − 17 − 500 − 23 − 500 − 34 − 2.5	 mA μA mA μA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = − 9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = − 12 Vdc)	P_C	 − −	 − −	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = −9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_l = 3.0 k and 15 pF)	t_{PLH}	−	275	350	ns
Fall Time (z_l = 3.0 k and 15 pF)	t_{THL}	−	45	75	ns
Propagation Delay Time (z_l = 3.0 k and 15 pF)	t_{PHL}	−	110	175	ns
Rise Time (z_l = 3.0 k and 15 pF)	t_{TLH}	−	55	100	ns

1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

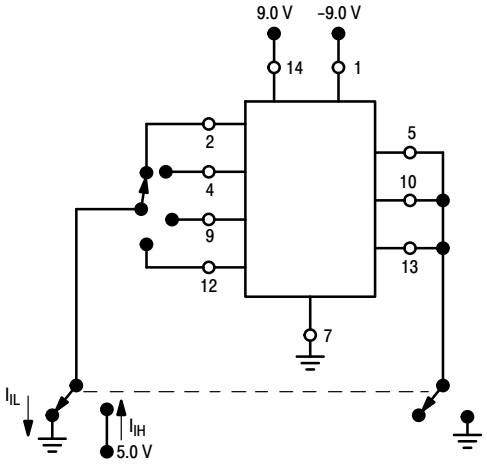


Figure 3. Input Voltage

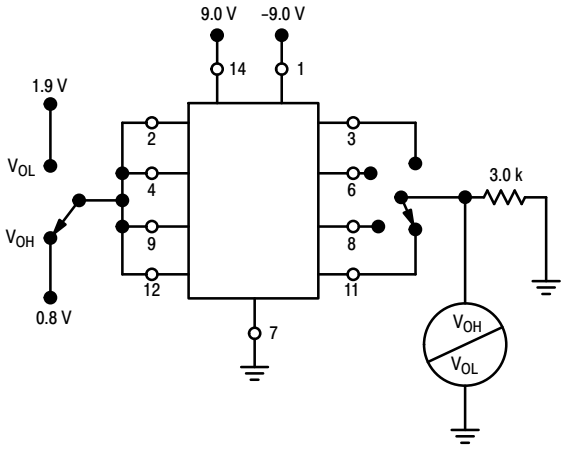


Figure 4. Output Current

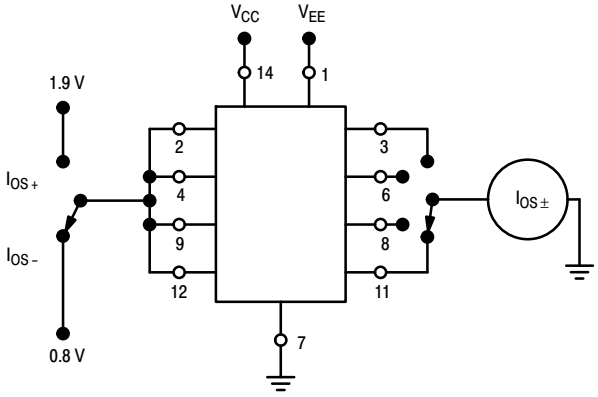


Figure 5. Output Short−Circuit Current

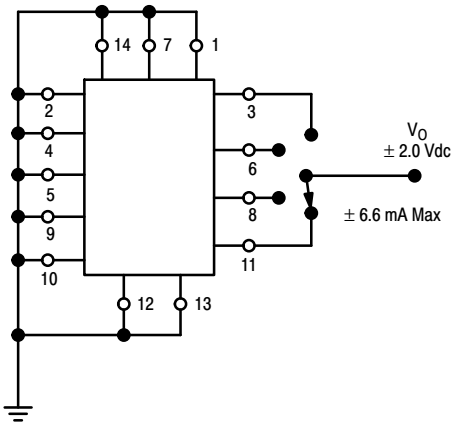


Figure 6. Output Resistance (Power Off)

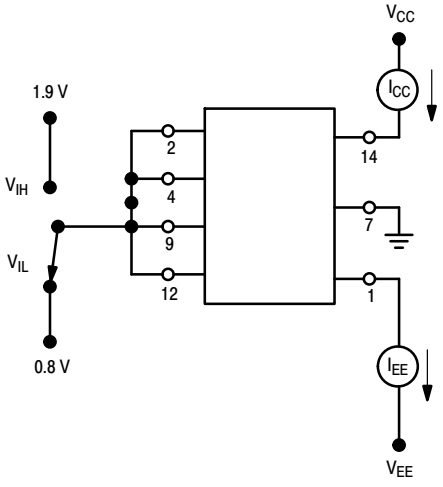


Figure 7. Power Supply Currents

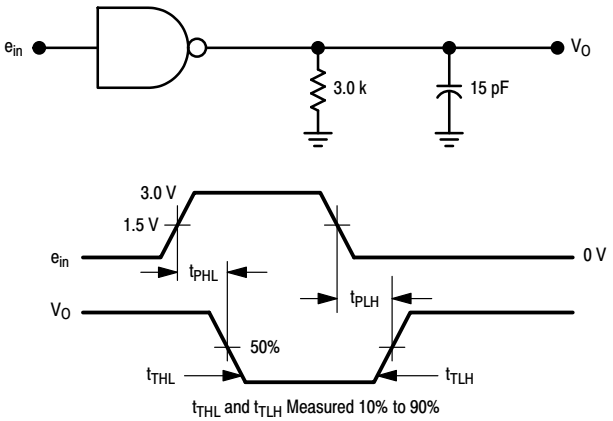


Figure 8. Switching Response

TYPICAL CHARACTERISTICS
(T_A = +25°C, unless otherwise noted.)

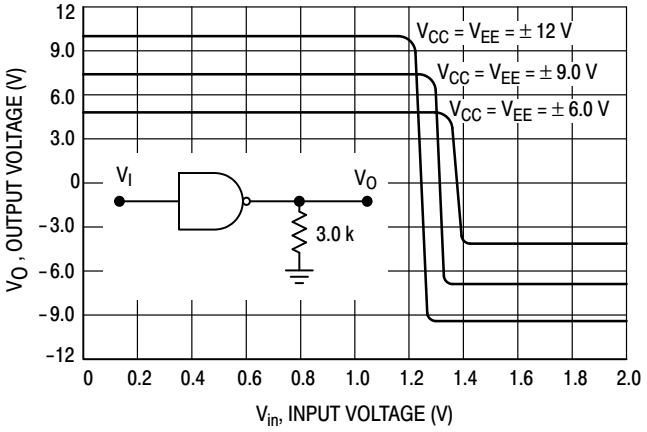


Figure 9. Transfer Characteristics versus Power Supply Voltage

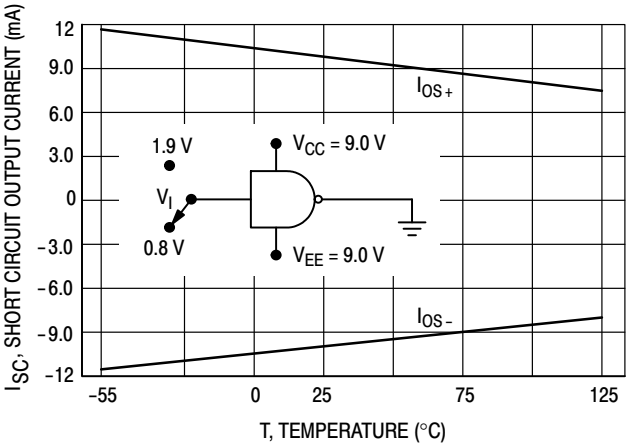


Figure 10. Short Circuit Output Current versus Temperature

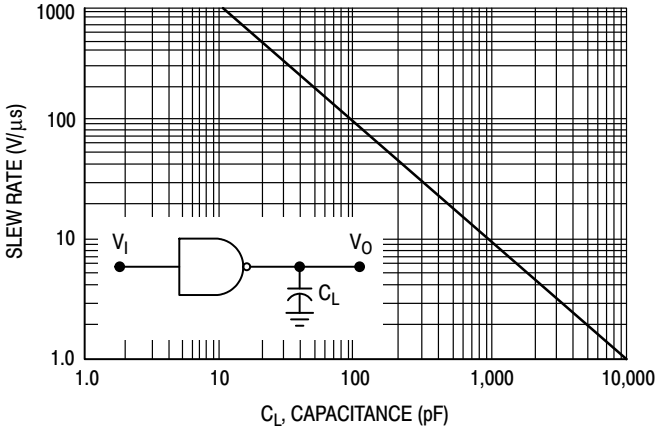


Figure 11. Output Slew Rate versus Load Capacitance

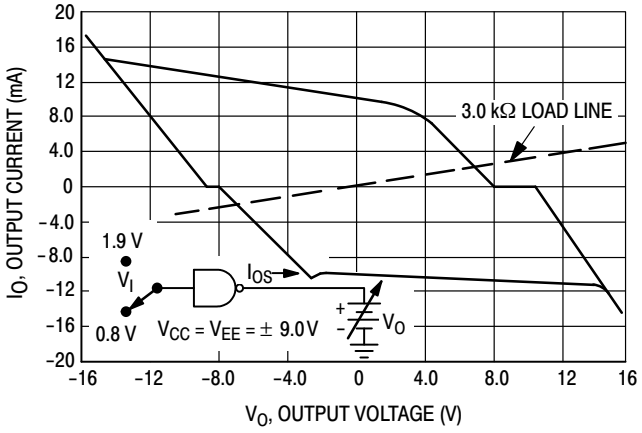


Figure 12. Output Voltage and Current−Limiting Characteristics

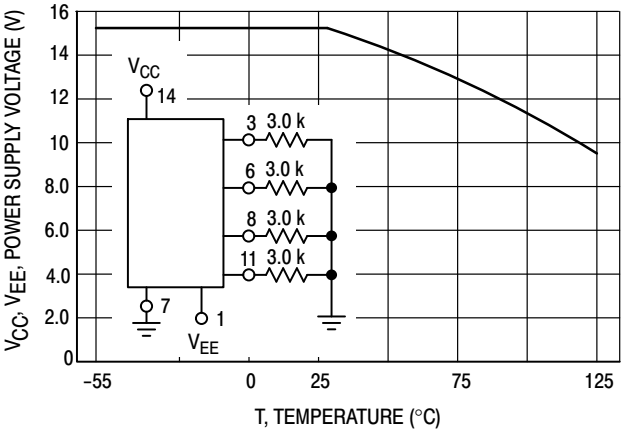


Figure 13. Maximum Operating Temperature versus Power Supply Voltage

APPLICATIONS INFORMATION

The Electronic Industries Association EIA−232D specification details the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA−232D defined levels. The EIA−232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5.0 and 15 V in magnitude and are positive for a Logic "0" and negative for a Logic "1." These voltages are so defined when the drivers are terminated with a 3000 to 7000 Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA−232D levels with one stage of inversion.

The EIA−232D specification further requires that during transitions, the driver output slew rate must not exceed 30 V per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 14 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per microsecond.

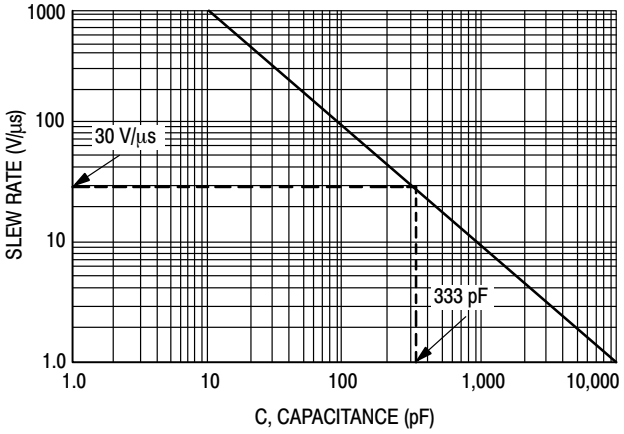


Figure 14. Slew Rate versus Capacitance for I_{SC} = 10 mA

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power supply voltages are greater than 9.0 V (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power supply designs, a loss of system power causes a low impedance on the power supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 Ω output resistors to ground. If all four outputs were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power supplies of the drivers, a diode should be placed in each power supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 15, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25 V limits specified in the earlier Standard EIA−232B.) The addition of the diodes also permits the MC1488 to withstand faults with power supplies of less than the 9.0 V stated above.

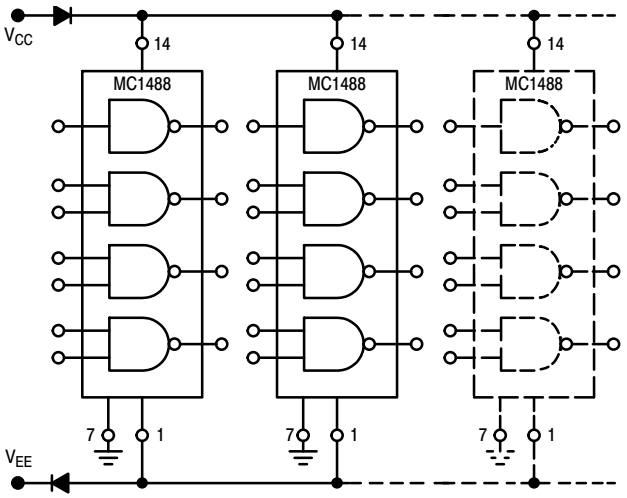


Figure 15. Power Supply Protection to Meet Power Off Fault Conditions

The maximum short circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting − this enables the circuit designer to define the output voltage levels independent of power supplies and can be accomplished by diode clamping of the output pins. Figure 16 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum 7.0 V (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately – 2.5 V to the minimum specified – 15 V. The MC1488 will drive the output to within 2.0 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA–232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 17 shows one such combination.

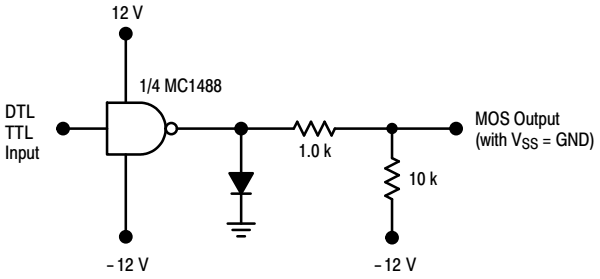


Figure 16. DTL/TTL–to–MOS Translator

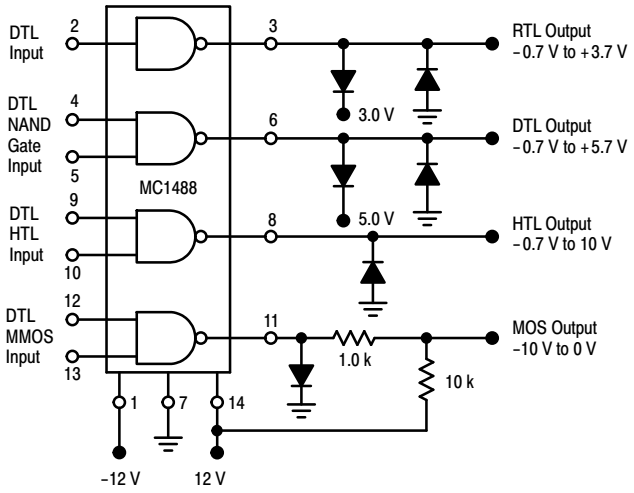


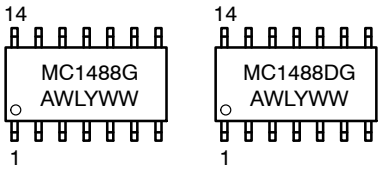
Figure 17. Logic Translator Applications

ORDERING INFORMATION

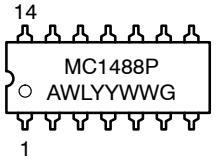
Device	Package	Operating Temperature Range	Shipping
MC1488D	SOIC−14	T_A = 0 to +75°C	55 Units/Rail
MC1488DG	SOIC−14 (Pb−Free)		
MC1488DR2	SOIC−14		2500/Tape & Reel
MC1488DR2G	SOIC−14 (Pb−Free)		
MC1488P	PDIP−14		25 Units/Rail
MC1488PG	PDIP−14 (Pb−Free)		
MC1488M	SOEIAJ−14		50 Units/Rail
MC1488MG	SOEIAJ−14 (Pb−Free)		
MC1488MEL	SOEIAJ−14		2000/Tape & Reel
MC1488MELG	SOEIAJ−14 (Pb−Free)		

MARKING DIAGRAMS

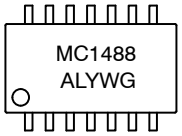
SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646



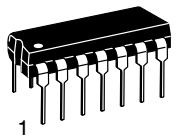
SOEIAJ−14
M SUFFIX
CASE 965



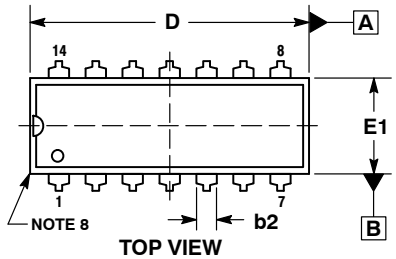
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

PDIP−14
CASE 646−06
ISSUE S

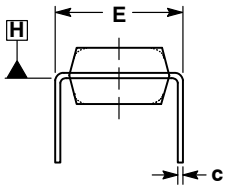
DATE 22 APR 2015



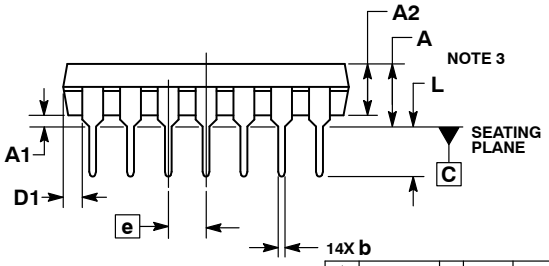
SCALE 1:1



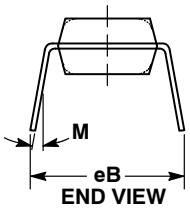
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

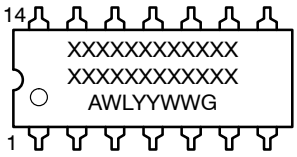


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

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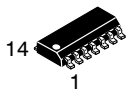

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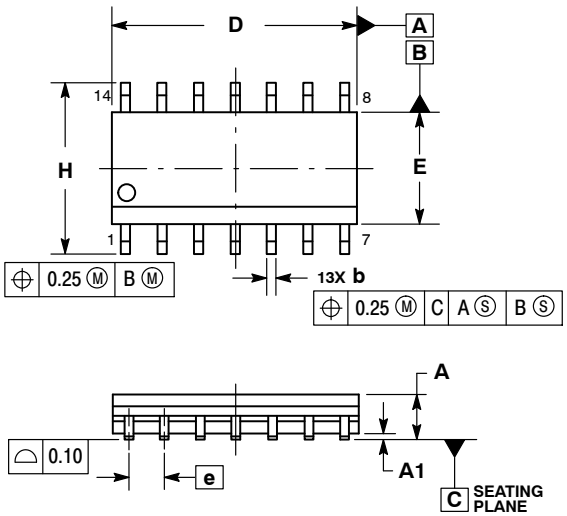
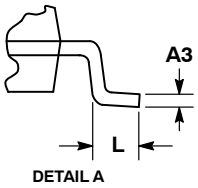
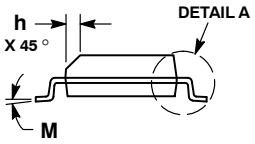
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



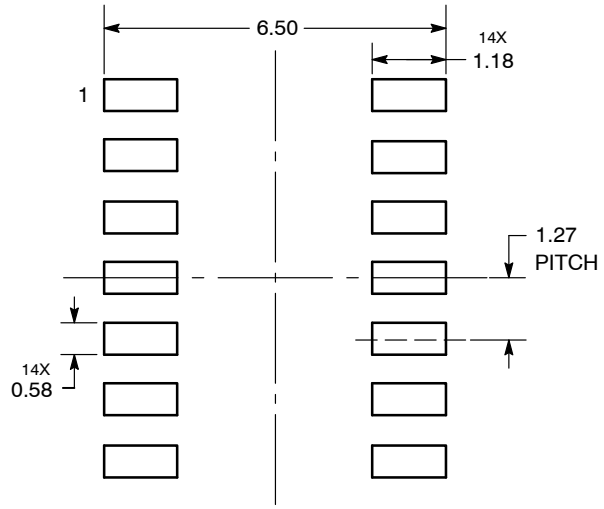




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

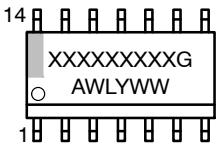
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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SOEIAJ−14
CASE 965−01
ISSUE B

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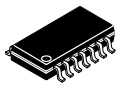

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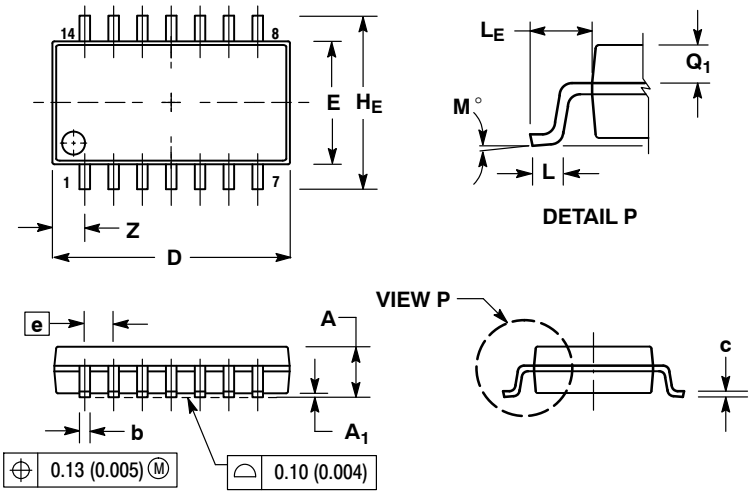

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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