MC74HC4316A

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

High−Performance Silicon−Gate CMOS

The MC74HC4316A utilizes silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF−channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power−supply range (from V_{CC} to V_{EE}).

The HC4316A is similar in function to the metal−gate CMOS MC14016 and MC14066, and to the High−Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal−gate CMOS analog switches. Logic−level translators are provided so that the On/Off Control and Enable logic−level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active−low) is high, all four analog switches are turned off.

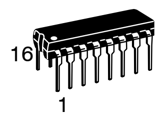
Features

- Logic−Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power−Supply Voltage Range (V_{CC} − V_{EE}) = 2.0 to 12.0 V
- Digital (Control) Power−Supply Voltage Range (V_{CC} − GND) = 2.0 V to 6.0 V, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

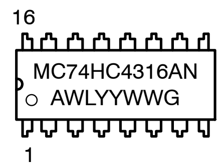
ON Semiconductor®

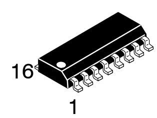
http://onsemi.com

MARKING DIAGRAMS

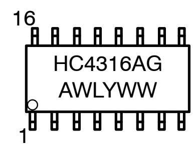


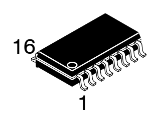
PDIP−16
N SUFFIX
CASE 648



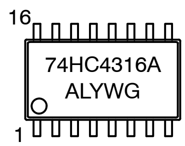


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4316ANG	PDIP−16 (Pb−Free)	500 Units / Box
MC74HC4316ADR2G	SOIC−16 (Pb−Free)	2500/Tape&Reel
MC74HC4316AFELG	SOEIAJ−16 (Pb−Free)	50/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

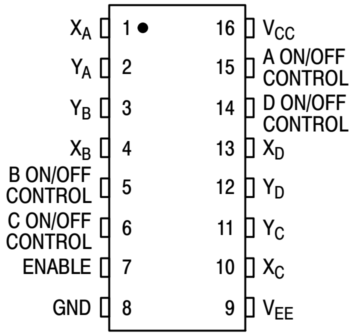


Figure 1. Pin Assignment

FUNCTION TABLE

Inputs		State of Analog Switch
Enable	**On/Off Control**	
L	H	On
L	L	Off
H	X	Off

X = Don't Care.

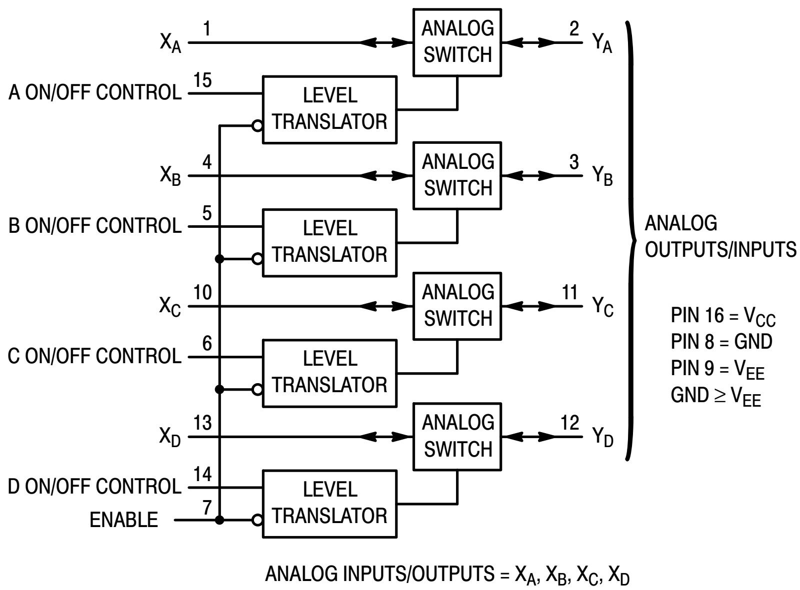


Figure 2. Logic Diagram

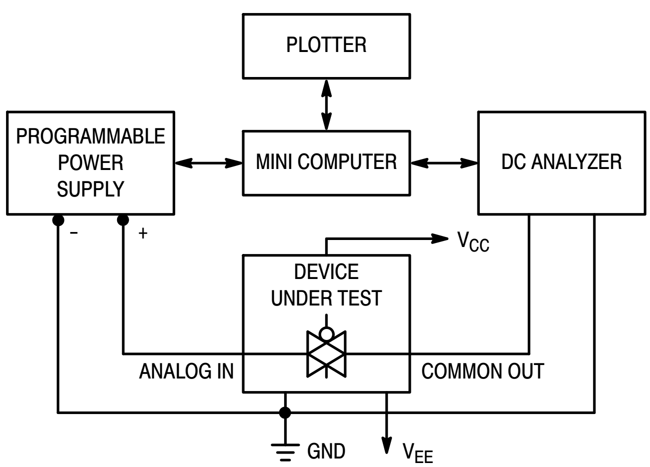


Figure 3. On Resistance Test Set−Up

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air Plastic DIP* EIAJ/SOIC Package* TSSOP Package*	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*Derating – Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)	2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 6.0	GND	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	–	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 2.0 V (Control or Enable Inputs) V_{CC} = 3.0 V (Figure 10) V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High−Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 4	 20 40	 40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA (Figure 3)	2.0* 4 5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 160 90 90	– 200 110 110	– 240 130 130	Ω
		V_{in} = V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA (Figure 3)	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 90 70 70	– 115 90 90	– 140 105 105	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) I_S ≤ 2.0 mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 20 15 15	– 25 20 20	– 30 25 25	Ω
I_{off}	Maximum Off−Channel Leakage Current, Any One Channel	V_{in} = V_{IL} V_{IO} = V_{CC} or V_{EE} Switch Off (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	μA
I_{on}	Maximum On−Channel Leakage Current, Any One Channel	V_{in} = V_{IH} V_{IS} = V_{CC} or V_{EE} (Figure 5)	6.0	– 6.0	0.1	0.5	1.0	μA

*At supply voltage (V_{CC} – V_{EE}) approaching 2.0 V the analog switch−on resistance becomes extremely non−linear. Therefore, for low−voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 9 and 10)	2.0	40	50	60	ns
		4.5	6	8	9	
		6.0	5	7	8	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 11 and 12)	2.0	130	160	200	ns
		4.5	40	50	60	
		6.0	30	40	50	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 11 and 12)	2.0	140	175	250	ns
		4.5	40	50	60	
		6.0	30	40	50	
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	–	10	10	10	pF
	Control Input = GND: Analog I/O	–	35	35	35	
	Control Input = GND: Feedthrough	–	1.0	1.0	1.0	

Symbol	Parameter	Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 14)*	15	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25	– 2.25	150	MHz
			4.50	– 4.50	160	
			6.00	– 6.00	160	
–	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25	– 2.25	– 50	dB
			4.50	– 4.50	– 50	
			6.00	– 6.00	– 50	
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25	– 2.25	– 40	
			4.50	– 4.50	– 40	
			6.00	– 6.00	– 40	
–	Feedthrough Noise, Control to Switch (Figure 8)	V_{in} ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25	– 2.25	30	mV_{PP}
			4.50	– 4.50	65	
			6.00	– 6.00	100	
		R_L = 10 kΩ, C_L = 10 pF	2.25	– 2.25	60	
			4.50	– 4.50	130	
			6.00	– 6.00	200	
–	Crosstalk Between Any Two Switches (Figure 13)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25	– 2.25	– 70	dB
			4.50	– 4.50	– 70	
			6.00	– 6.00	– 70	
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25	– 2.25	– 80	
			4.50	– 4.50	– 80	
			6.00	– 6.00	– 80	
THD	Total Harmonic Distortion (Figure 15)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{Measured}$ − THD_{Source}				%
		V_{IS} = 4.0 V_{PP} sine wave	2.25	– 2.25	0.10	
		V_{IS} = 8.0 V_{PP} sine wave	4.50	– 4.50	0.06	
		V_{IS} = 11.0 V_{PP} sine wave	6.00	– 6.00	0.04	

*Limits not tested. Determined by design and verified by qualification.

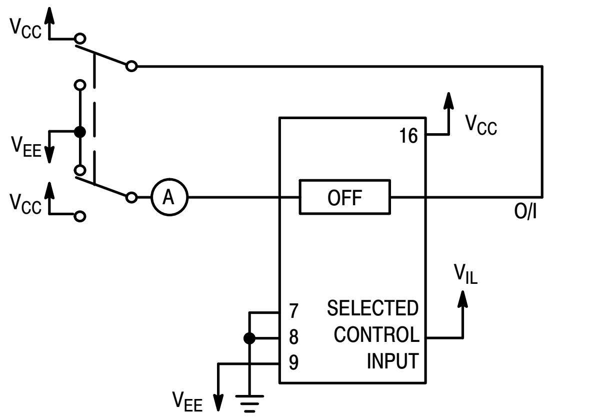


Figure 4. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up

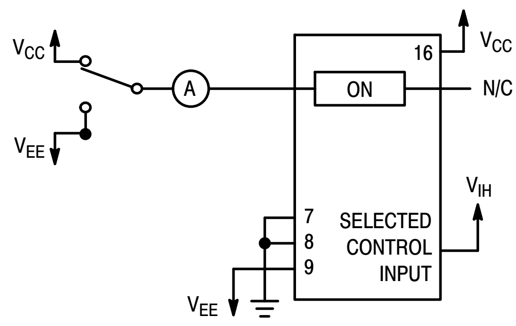
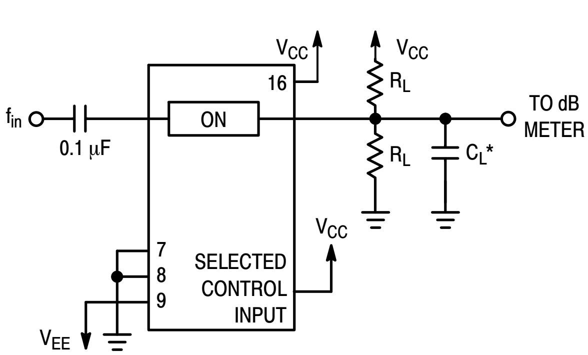
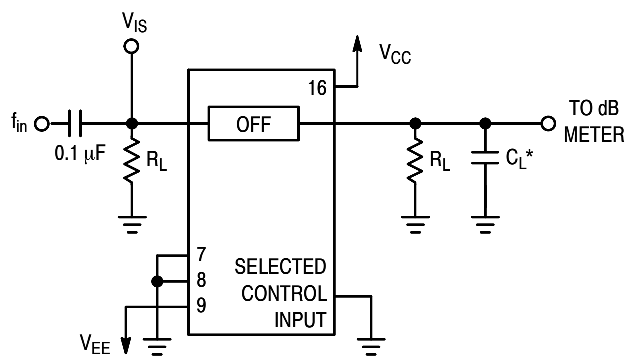


Figure 5. Maximum On Channel Leakage Current, Test Set−Up



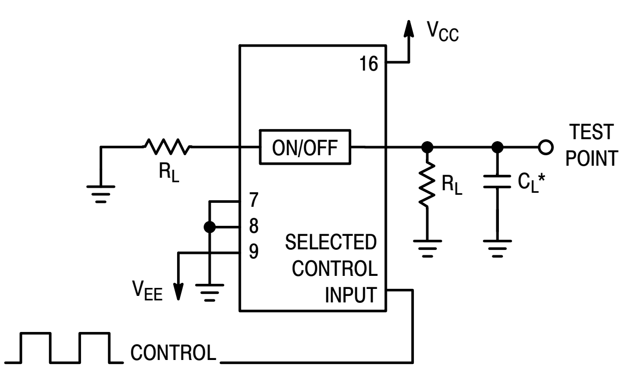
*Includes all probe and jig capacitance.

Figure 6. Maximum On−Channel Bandwidth Test Set−Up



*Includes all probe and jig capacitance.

Figure 7. Off−Channel Feedthrough Isolation, Test Set−Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Control to Analog Out, Test Set−Up

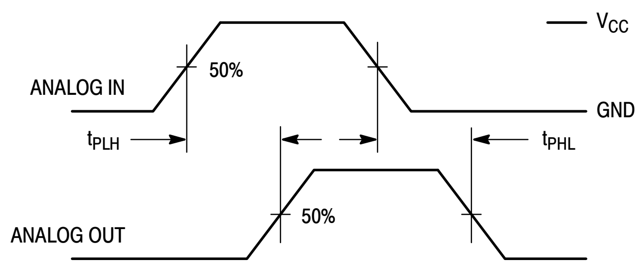
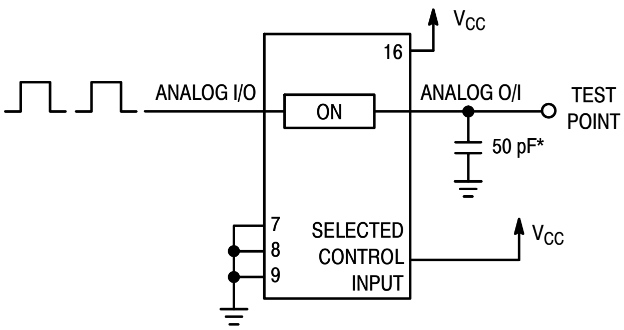


Figure 9. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10. Propagation Delay Test Set−Up

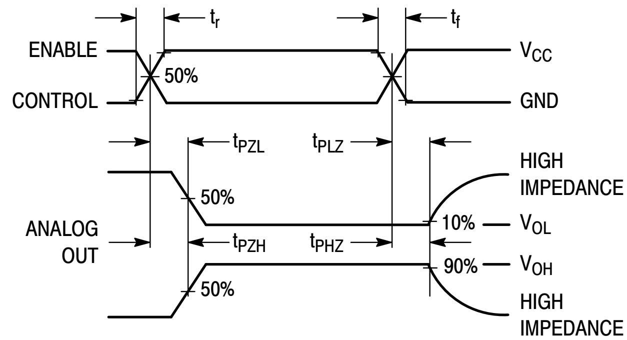
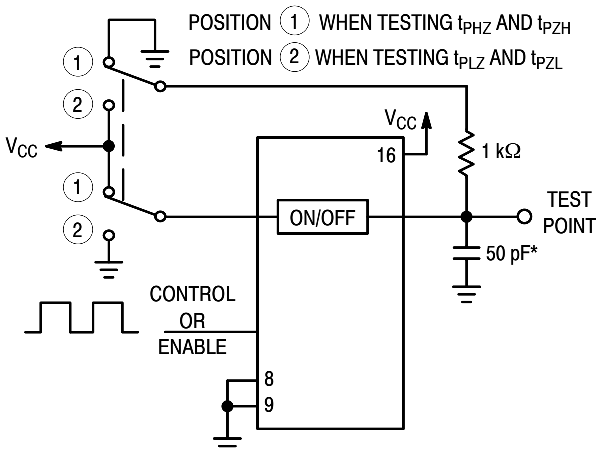
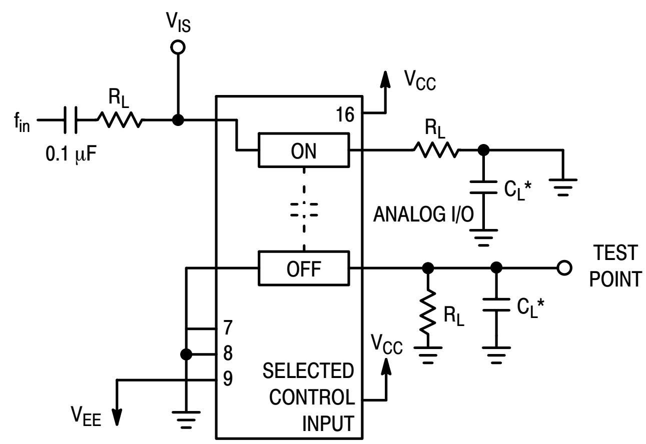


Figure 11. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 12. Propagation Delay Test Set−Up



*Includes all probe and jig capacitance.

Figure 13. Crosstalk Between Any Two Switches, Test Set−Up (Adjacent Channels Used)

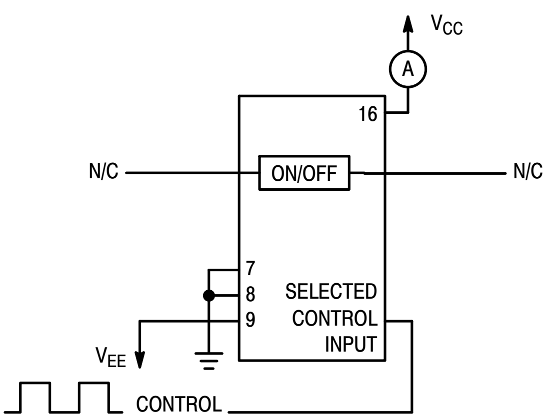
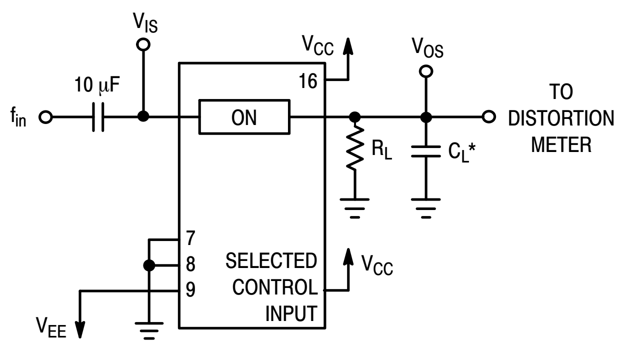


Figure 14. Power Dissipation Capacitance Test Set−Up



*Includes all probe and jig capacitance.

Figure 15. Total Harmonic Distortion, Test Set−Up

APPLICATIONS INFORMATION

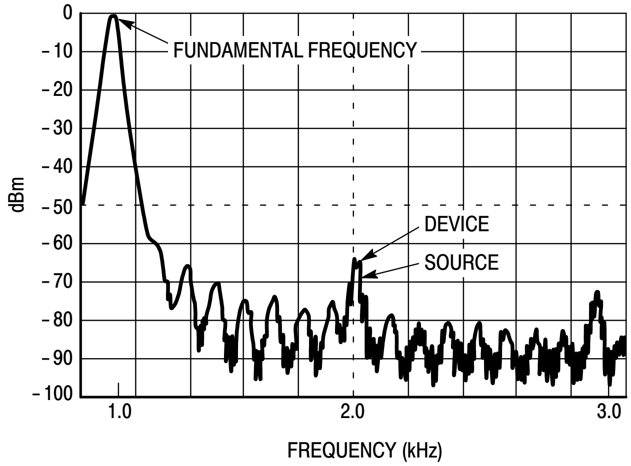


Figure 16. Plot, Harmonic Distortion

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is 12 V. Therefore, using the configuration in Figure 17, a maximum analog signal of twelve volts peak−to−peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 18. These diodes should be small signal, fast turn−on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MOSORBs (MOSORB™ is an acronym for high current surge protectors). MOSORBs are fast turn−on devices ideally suited for precise dc protection with no inherent wear out mechanism.

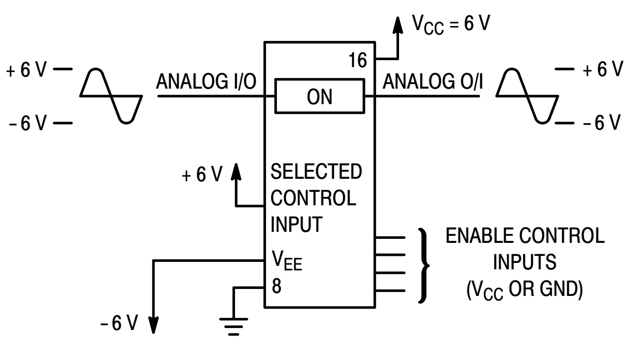


Figure 17.

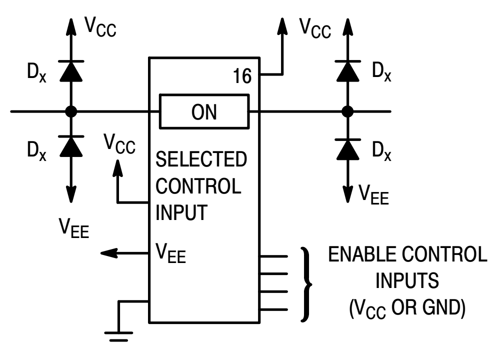
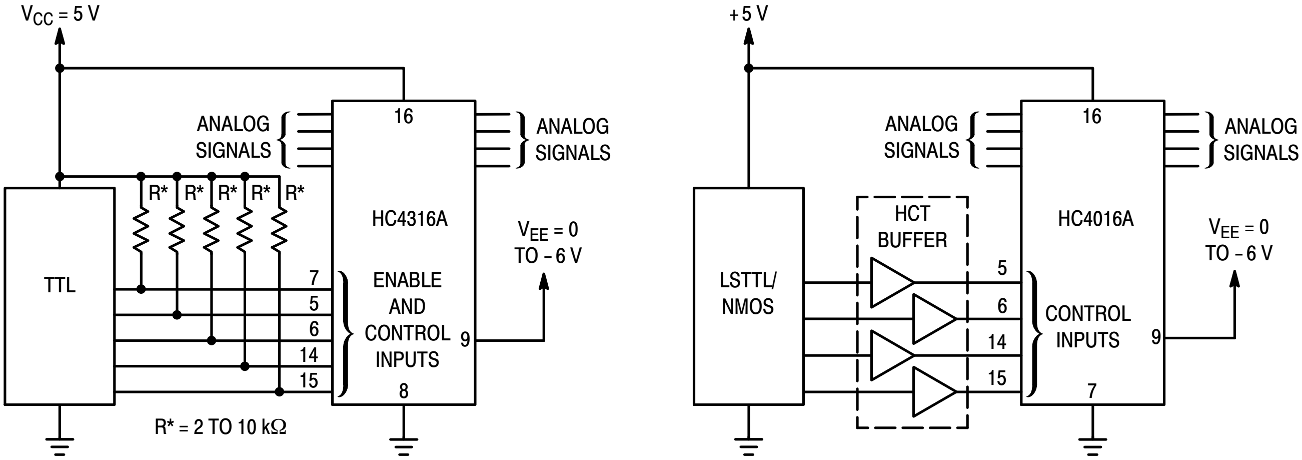


Figure 18. Transient Suppressor Application



a. Using Pull−Up Resistors **b. Using HCT Buffer**

Figure 19. LSTTL/NMOS to HCMOS Interface

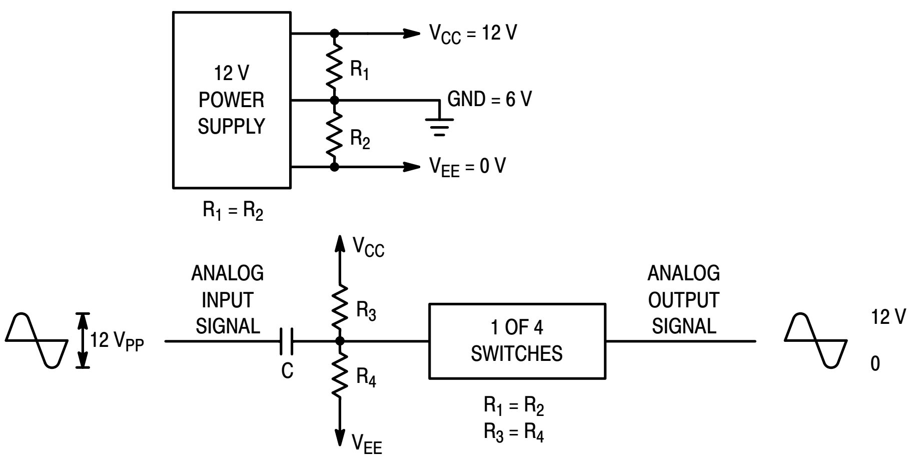


Figure 20. Switching a 0−to−12 V Signal Using a Single Power Supply (GND ≠ 0 V)

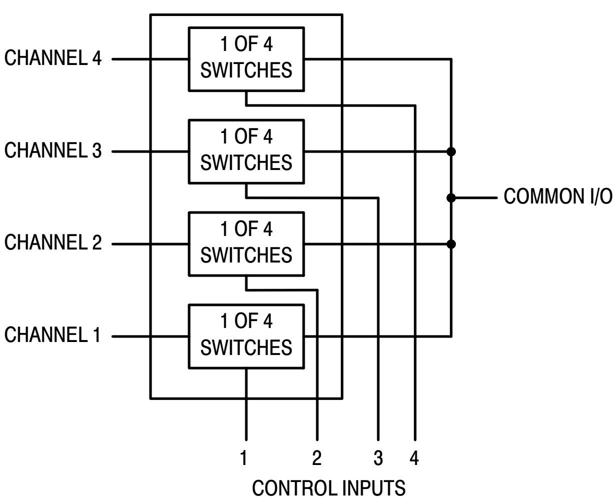


Figure 21. 4−Input Multiplexer

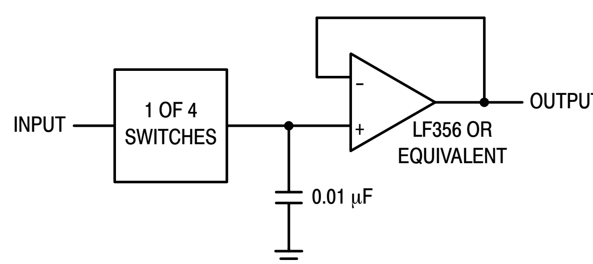
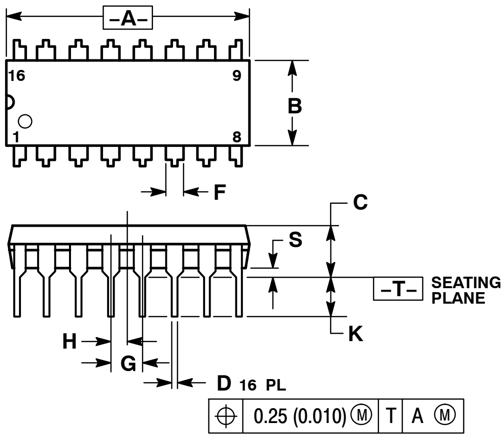
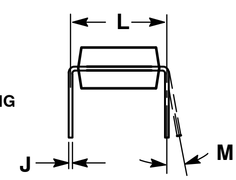


Figure 22. Sample/Hold Amplifier

PACKAGE DIMENSIONS

PDIP−16
N SUFFIX
CASE 648−08
ISSUE T

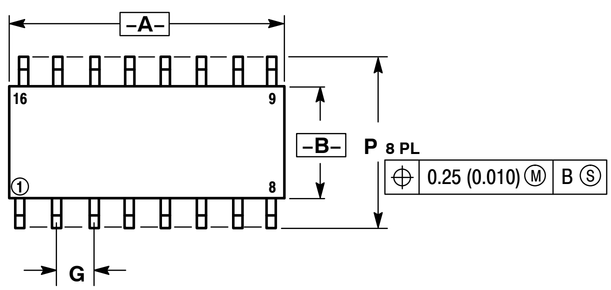


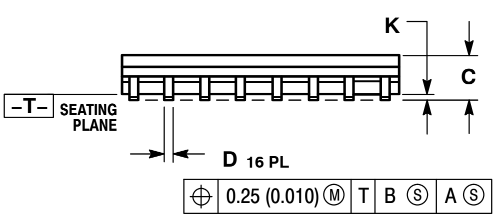


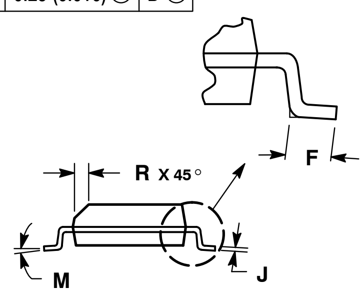
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE K



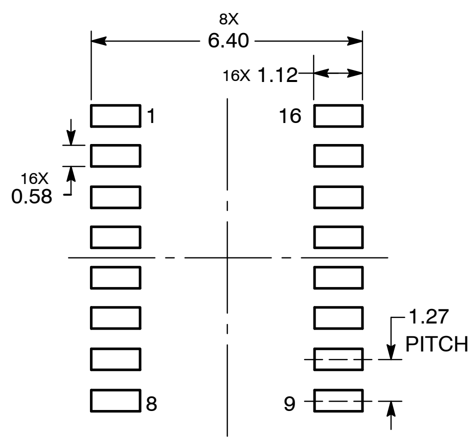




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

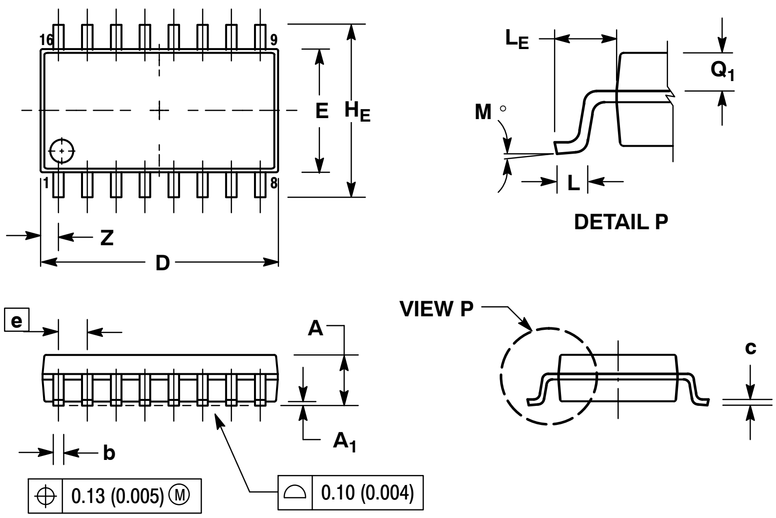
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOEIAJ−16
F SUFFIX
CASE 966−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative