MN3762MAE

8mm (1/2 inch) 710H CCD Area Image Sensor

■ Overview

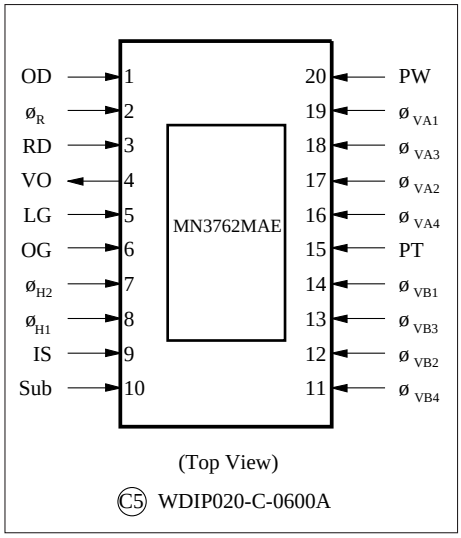
The MN3762MAE is a 8mm (1/2 inch) frame interline Transfer CCD (FIT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 450K pixels (758 horizontal × 585 vertical) and provides stable and clear images with a resolution of 530 horizontal TV-lines and 420 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3762MAE	8mm (1/2 inch)	CCIR	B/W

■ Pin Assignments



(Top View)

C5 WDIP020-C-0600A

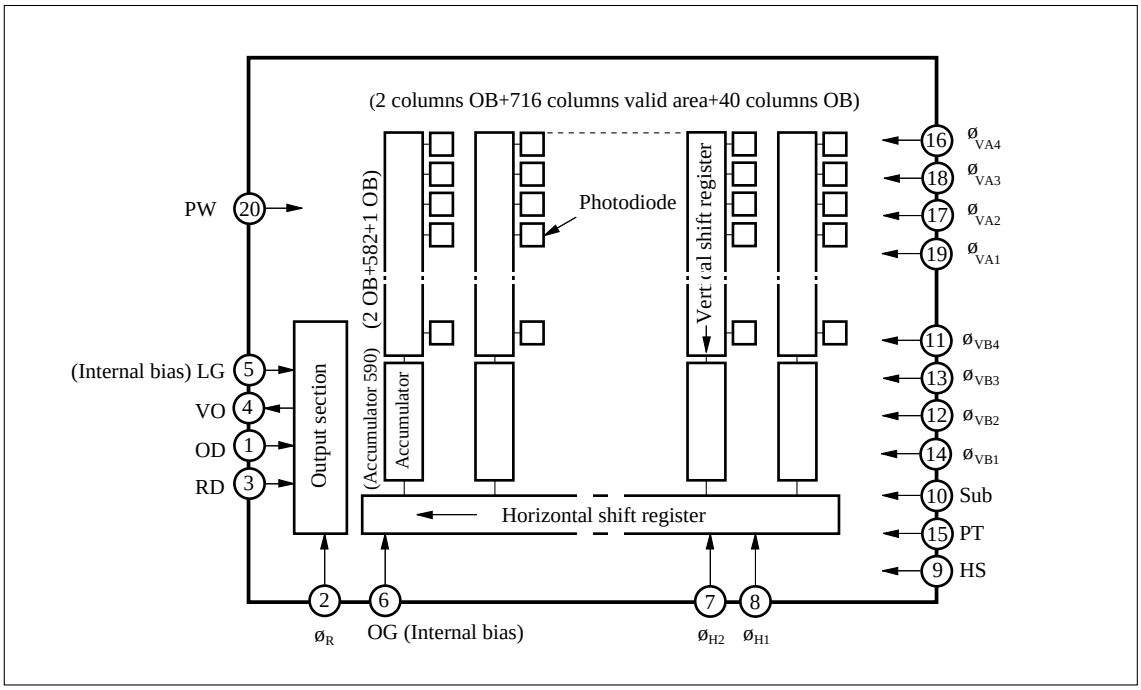
■ Features

- Total number of pixels: 758 (horizontal) × 585 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 20 Pin DIL ceramic package

■ Applications

- Cameras for broadcasting
- Cameras for commercial use

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	11	$ø_{VB4}$	Vertical shift register clock pulse (B4)
2	$ø_R$	Reset pulse	12	$ø_{VB2}$	Vertical shift register clock pulse (B2)
3	RD	Reset drain	13	$ø_{VB3}$	Vertical shift register clock pulse (B3)
4	VO	Video output	14	$ø_{VB1}$	Vertical shift register clock pulse (B1)
5	LG	Output load transistor gate	15	PT	P-well for protection circuit
6	OG	Output gate	16	$ø_{VA4}$	Vertical shift register clock pulse (A4)
7	$ø_{H2}$	Horizontal register clock pulse (2)	17	$ø_{VA2}$	Vertical shift register clock pulse (A2)
8	$ø_{H1}$	Horizontal register clock pulse (1)	18	$ø_{VA3}$	Vertical shift register clock pulse (A3)
9	IS	Input source	19	$ø_{VA1}$	Vertical shift register clock pulse (A1)
10	Sub	Substrate	20	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

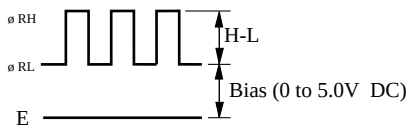
Parameter	Symbol	Rating Note 2)		Operating condition Note 1)			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD}	– 0.2	18	14.5	15.0	15.5	V
Output drain voltage	V_{OD}	– 0.2	18	14.5	15.0	15.5	V
Output load transistor gate voltage Note 3)	V_{LG}	(Supplied internally)					V
Output gate voltage Note 3)	V_{OG}	(Supplied internally)					V
Input source voltage	V_{IS}	– 0.2	18	14.5	15.0	15.5	V
Protection P well voltage	V_{PT}	–10.0	0.2	$ø_{V(L)}$ –1.2	$ø_{V(L)}$ –1.0	$ø_{V(L)}$ – 0.7	V
P well voltage	V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage H-L	$V_{ø R (H-L)}$ * 1	—	18	4.7	5.0	5.3	V
Reset pulse voltage Bias	$V_{ø R (Bias)}$ * 1	– 0.2	—	0	Fixed * 3	5.0	V
Horizontal register clock pulse voltage 1	$V_{ø H1 (H)}$	—	18	4.7	5.0	5.3	V
	$V_{ø H1 (L)}$	– 0.2	—	– 0.2	0	0.3	V
Horizontal register clock pulse voltage 2	$V_{ø H2 (H)}$	—	18	4.7	5.0	5.3	V
	$V_{ø H2 (L)}$	– 0.2	—	– 0.2	0	0.3	V
Vertical shift register clock pulse voltage	$V_{ø V1A, ø V3A (H)}$	—	18	14.5	15.0	15.5	V
	$V_{ø V1A, ø V3A (M)}$	—	—	– 0.1	0	0.1	V
	$V_{ø V1A, ø V3A (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage	$V_{ø V2A,4A (M)}$	—	15	1.7	2.0	2.3	V
	$V_{ø V2A,4A (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage	$V_{ø V1B (H)}$	—	15	6.7	7.0	7.3	V
	$V_{ø V1B (M)}$	—	—	– 0.1	0	0.1	V
	$V_{ø V1B (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage	$V_{ø V3B (M)}$	—	15	– 0.1	0	0.1	V
	$V_{ø V3B (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage	$V_{ø V2B,4B (M)}$	—	15	1.7	2.0	2.3	V
	$V_{ø V2B,4B (L)}$	–9	—	–7.3	–7.0	–6.7	V
Substrate voltage	V_{Sub} * 2	– 0.2	45	0	Adjust	14.0	V
	$øV_{Sub}$ * 2			24.2	25	25.8	V
Operating temperature	T_{opr}	–10	70	—	25	—	˚C
Storage temperature	T_{stg}	–30	70	—	—	—	˚C

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/8 using a light source of 2856K and 920nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500 (t=2.5mm) in the light path.
If any blooming is present at the minimum operating condition of V_{Sub}, it should be adjusted to the minimum voltage at which there is no FPN picture.

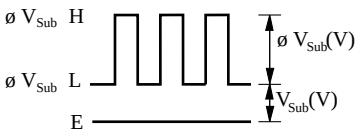
Note 2) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55$ (V)
$-0.2 < V_{øV} - V_{PT} < +28$ (V)

Note 3) The LG and OG pins should each be grounded via a capacitor of 0.047µF or more.

* 1



* 2 V_{Sub} when using electronic shutter function



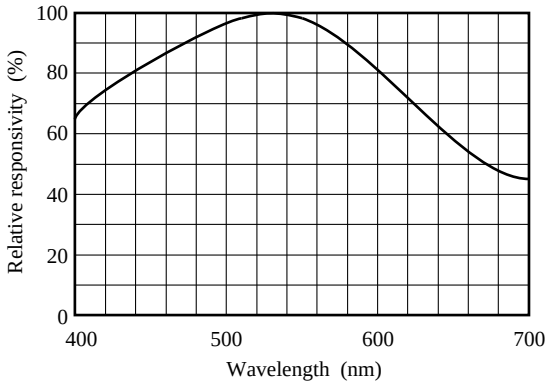
* 3 If there are any parameters not specified here but need to be stipulated, the decision will be made in consultation with the customer.

■ Optical Characteristics

Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MN3762MAE	B/W	716	582	60	1,100	400	0.001	0	530	420

■ Graphs of Characteristics

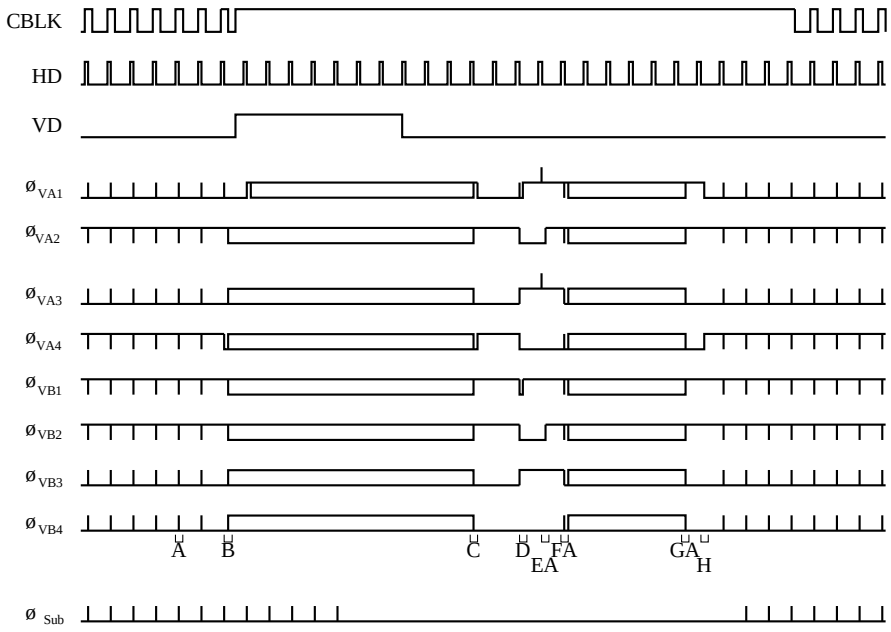
CCD Spectral Characteristics



■ Example of Recommended Driving Pulses

• V Rate timing

< Field A >



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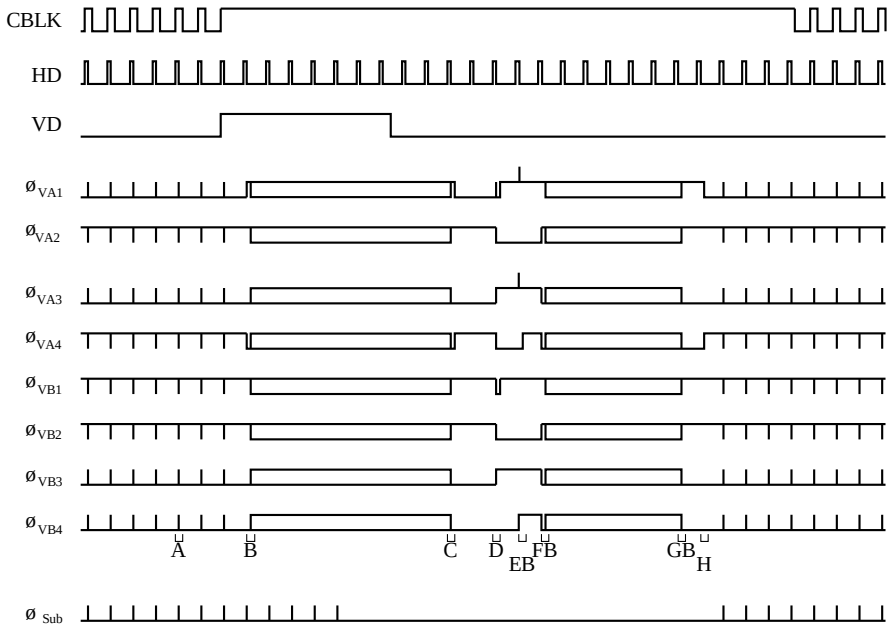

• H Rate timing