

2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

74ALVT16841

FEATURES

- High speed parallel latches
- 5V I/O Compatible
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16841 Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity. It is designed for V_{CC} operation from 2.5V to 3.0V with I/O compatibility to 5V.

The 74ALVT16841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable (nOE) is Low. When nOE is High the output is in the High-impedance state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nQx	$C_L = 50pF$	2.8	2.3	ns
C_{IN}	Input capacitance DIR, OE	$V_I = 0V$ or V_{CC}	3	3	pF
C_{Out}	Output pin capacitance	$V_{IO} = 0V$ or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ALVT16841 DL	AV16841 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVT16841 DGG	AV16841 DGG	SOT364-1

PIN DESCRIPTION

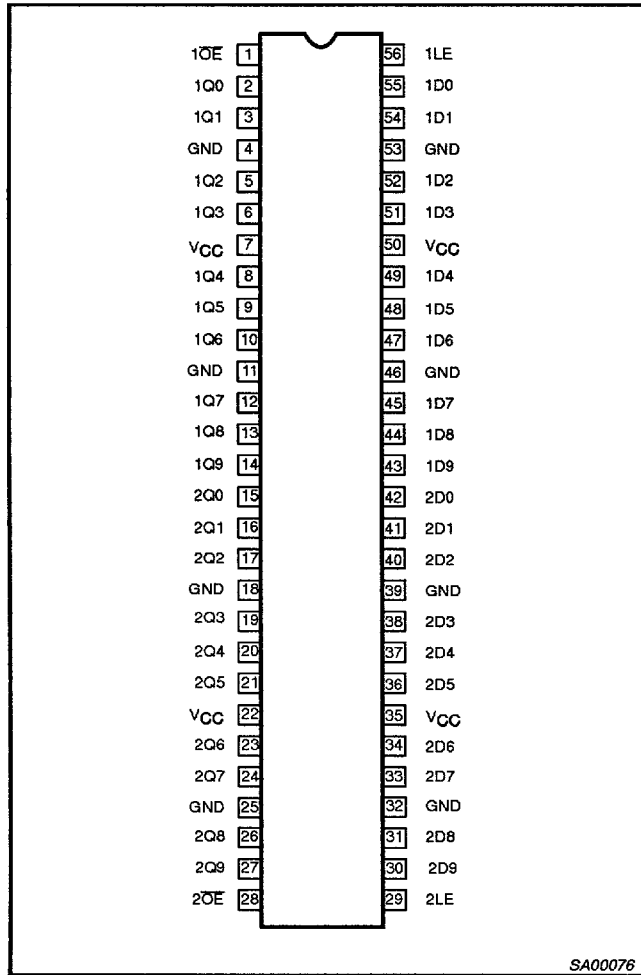
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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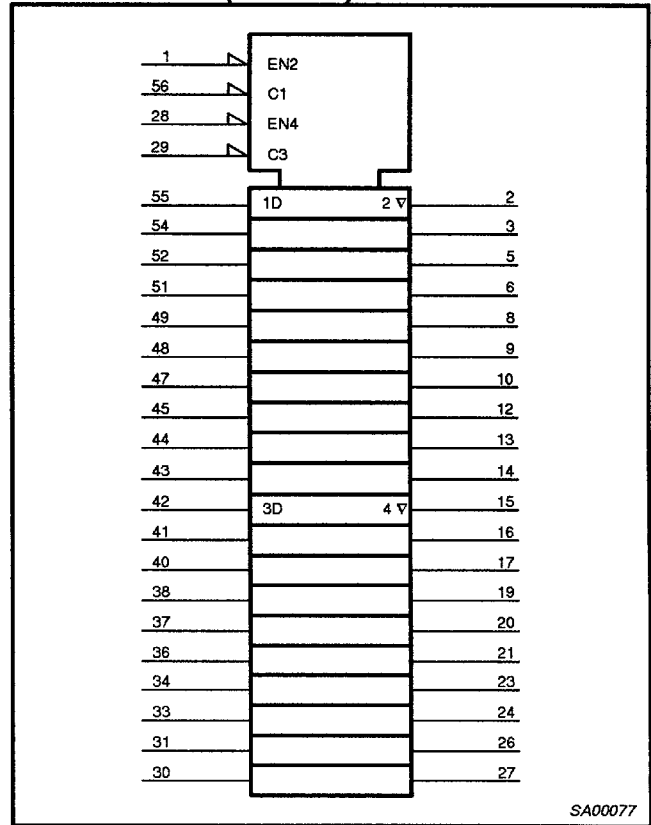
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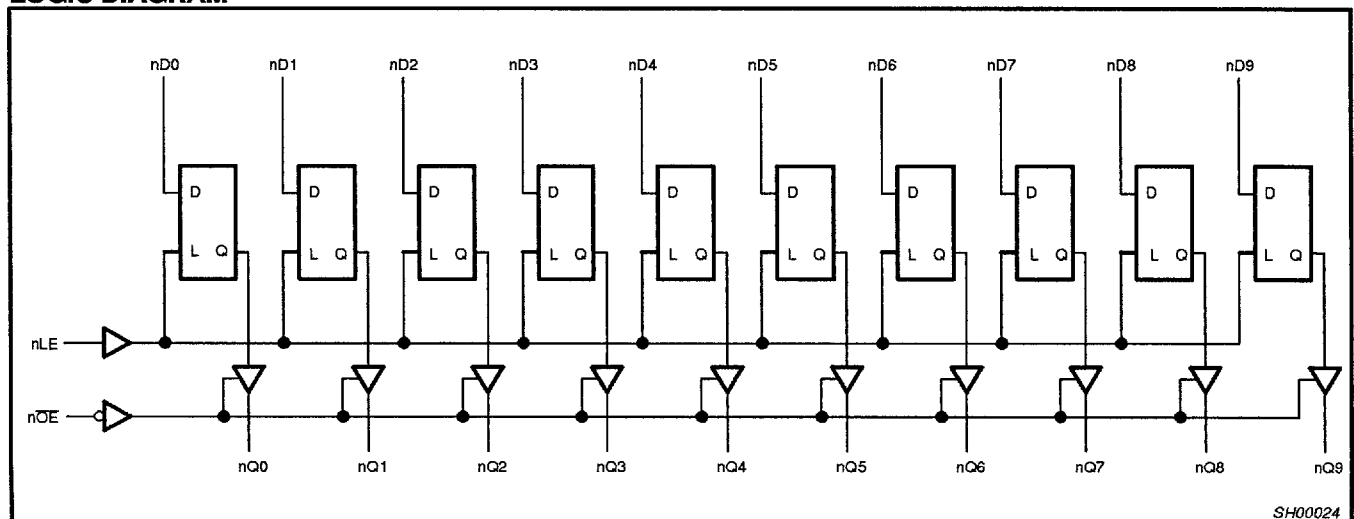
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



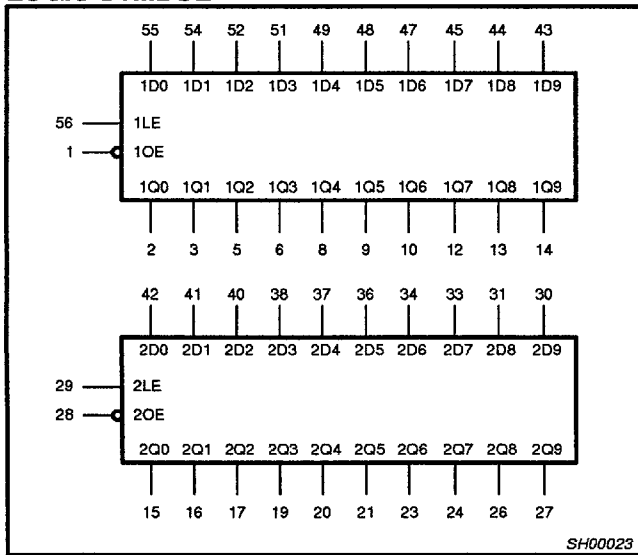
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LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
nOE	nLE	nDx	nQ0 - nQ9	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
 h = High voltage level one set-up time prior to the High-to-Low LE transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the High-to-Low LE transition
 ↓ = High-to-Low LE transition
 NC = No change
 X = Don't care
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IH}	High-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{OH}	High-level output current		-8		-32	mA
I _{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
Δt/ΔV	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V_{IK}	Input clamp voltage	$V_{CC} = 3.0V; I_{IK} = -18mA$		-0.85	-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 3.0$ to $3.6V; I_{OH} = -100\mu A$	$V_{CC}-0.2$	V_{CC}		V
		$V_{CC} = 3.0V; I_{OH} = -32mA$	2.0	2.3		
V_{OL}	Low-level output voltage	$V_{CC} = 3.0V; I_{OL} = 100\mu A$		0.07	0.2	V
		$V_{CC} = 3.0V; I_{OL} = 16mA$		0.25	0.4	
		$V_{CC} = 3.0V; I_{OL} = 32mA$		0.3	0.5	
		$V_{CC} = 3.0V; I_{OL} = 64mA$		0.4	0.55	
I_I	Input leakage current	$V_{CC} = 3.6V; V_I = V_{CC}$ or GND	Control pins	0.1	±1	μA
		$V_{CC} = 0$ or $3.6V; V_I = 5.5V$		0.1	10	
		$V_{CC} = 3.6V; V_I = 5.5V$	I/O Data pins ⁴	0.1	20	
		$V_{CC} = 3.6V; V_I = V_{CC}$		0.5	10	
		$V_{CC} = 3.6V; V_I = 0$		0.1	-5	
I_{OFF}	Output off current	$V_{CC} = 0V; V_I$ or $V_O = 0$ to $4.5V$		0.1	±100	μA
I_{HOLD}	Bus Hold current	$V_{CC} = 3V; V_I = 0.8V$	75	130		μA
	A or B outputs	$V_{CC} = 3V; V_I = 2.0V$	-75	-140		μA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	$V_O = 5.5V; V_{CC} = 3.0V$		50	125	μA
I_{PUPD}	Power up/down 3-State output current ³	$V_{CC} \leq 1.2V; V_O = 0.5V$ to $V_{CC}; V_I = GND$ or V_{CC} OE/OE = Don't care		40	±100	μA
I_{OZH}	3-State output High current	$V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL}$ or V_{IH}		0.5	5	μA
I_{OZL}	3-State output Low current	$V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL}$ or V_{IH}		0.5	-5	μA
I_{CCH}	Quiescent supply current	$V_{CC} = 3.6V; \text{Outputs High, } V_I = GND$ or $V_{CC}, I_O = 0$		0.07	0.09	mA
I_{CCL}		$V_{CC} = 3.6V; \text{Outputs Low, } V_I = GND$ or $V_{CC}, I_O = 0$		3.2	5	
I_{CCZ}		$V_{CC} = 3.6V; \text{Outputs Disabled; } V_I = GND$ or $V_{CC}, I_O = 0^5$		0.07	0.09	
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 3V$ to $3.6V; \text{One input at } V_{CC}-0.6V,$ Other inputs at V_{CC} or GND		0.04	0.2	mA

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μ sec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.0 1.0	1.7 1.8	2.8 3.0	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.5	2.1 2.3	3.6 3.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.5 1.5	2.3 2.3	3.8 4.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.5	2.7 2.7	4.2 4.0	ns

AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$		
			Min	Typ	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nLE	3	1.0 0.8		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nLE	3	1.2 0.5		ns
$t_w(\text{H})$	nLE pulse width High	1	1.5		ns

AC CHARACTERISTICS (2.5V ± 0.2V RANGE)GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.2 1.2	2.0 2.4	3.8 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.8 1.8	2.6 2.8	5.4 5.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	2.0 2.0	3.1 3.4	5.9 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.0 2.0	3.5 3.1	5.6 5.2	ns

AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$		
			Min	Typ	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nLE	3	1.0 1.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nLE	3	1.8 0.4		ns
$t_w(\text{H})$	nLE pulse width High	1	1.5		ns

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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = -40°C to +85°C				
			MIN	TYP ¹	MAX		
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA		-0.85	-1.2	V	
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2			V	
		V _{CC} = 2.3V; I _{OH} = -8mA	1.7				
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100μA		0.07	0.2	V	
		V _{CC} = 2.3V; I _{OL} = 24mA		0.3	0.5		
I _I	Input leakage current	V _{CC} = 2.7V; V _I = GND	Control pins	0.1	±1	μA	
		V _{CC} = 0 or 2.7V; V _I = 2.7V			0.1		10
		V _{CC} = 2.7V; V _I = 2.7V	I/O Data pins ⁴		0.1		20
		V _{CC} = 2.7V; V _I = V _{CC}			0.1		10
		V _{CC} = 2.7V; V _I = 0			0.1		-5
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA	
I _{HOLD} ⁶	Bus Hold current A or B outputs	V _{CC} = 2.5V; V _I = 0.8V		90		μA	
		V _{CC} = 2.5V; V _I = 2.0V		75		μA	
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		50	125	μA	
I _{PUPD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care		40	100	μA	
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	μA	
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	μA	
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.09	mA	
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		2.3	4.5		
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.09		
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.01	0.2	mA	

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.

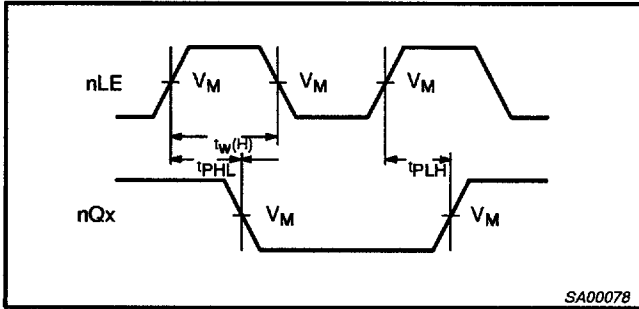
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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

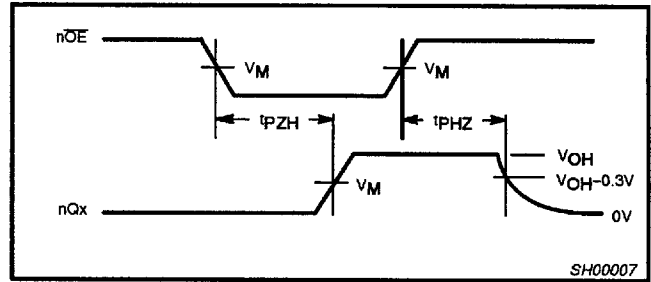
74ALVT16841

AC WAVEFORMS

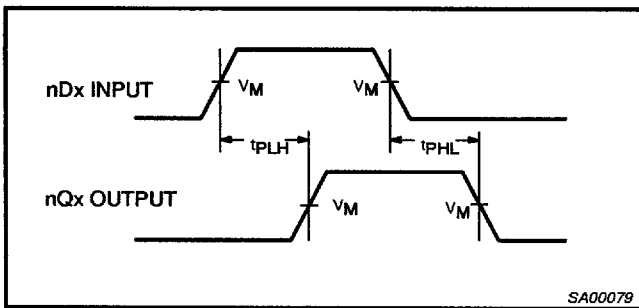
For all waveforms $V_M = 1.5V$ or $V_{CC} / 2$, whichever is less



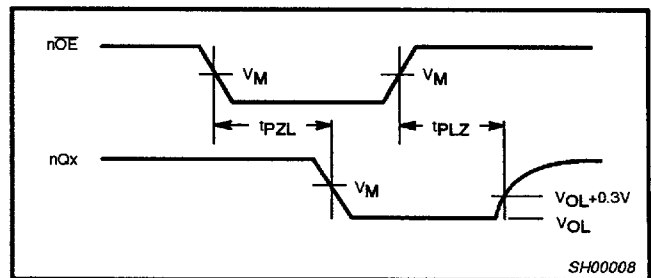
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



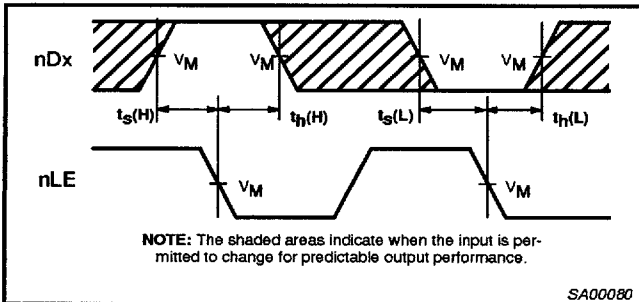
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



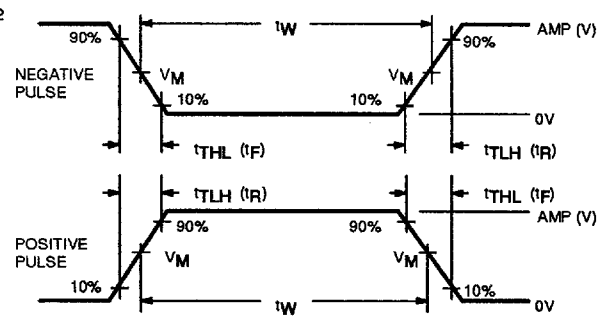
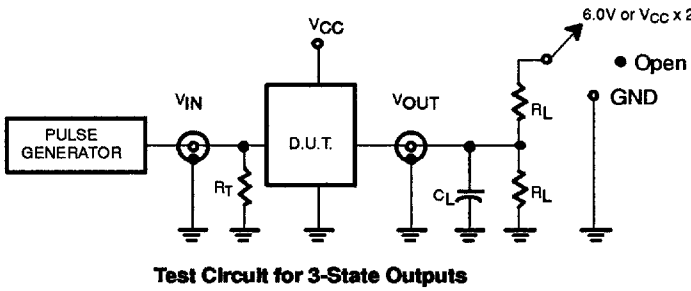
Waveform 3. Data Setup and Hold Times

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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

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TEST CIRCUIT AND WAVEFORM



$V_M = 1.5V$ or $V_{CC}/2$ whichever is less

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

SW00025

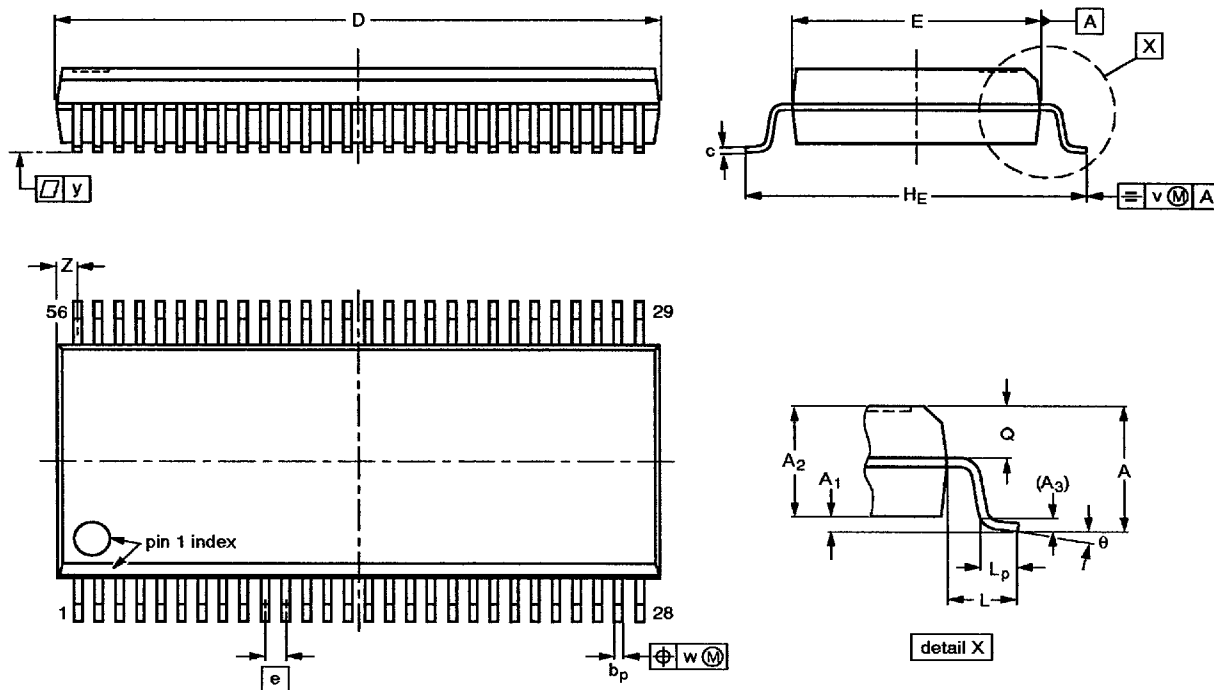
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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT371-1		MO-118AB			93-11-02 95-02-04

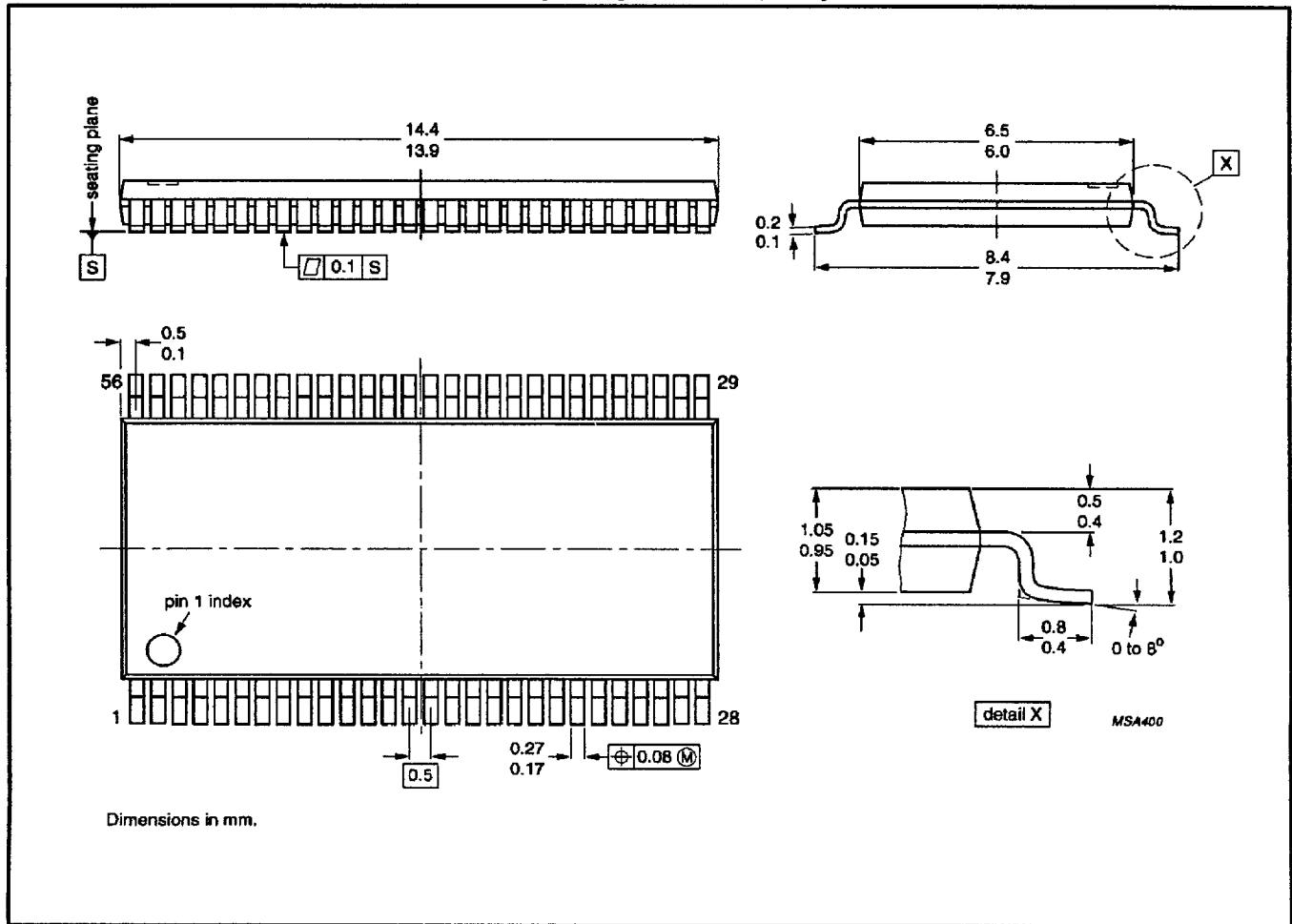
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2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

74ALVT16841

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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