Silicon Diffused Power Transistor — BUT11AX

GENERAL DESCRIPTION

High-voltage, high-speed glass-passivated npn power transistor in a plastic full-pack envelope intended for use in converters, inverters, switching regulators, motor control systems, etc.

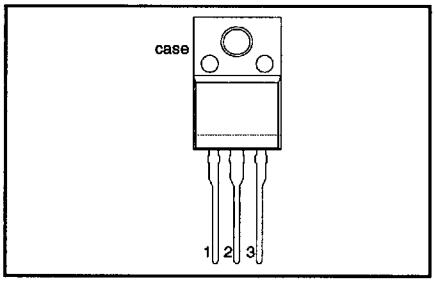
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CESM}	Collector-emitter voltage peak value	V_{BE} = 0 V	-	1000	V
V_{CEO}	Collector-emitter voltage (open base)		-	450	V
I_C	Collector current (DC)		-	5	A
I_{CM}	Collector current peak value		-	10	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	-	32	W
V_{CEsat}	Collector-emitter saturation voltage		-	1.5	V
I_{Csat}	Collector saturation current		2.5	-	A
t_f	Fall time		150	-	ns

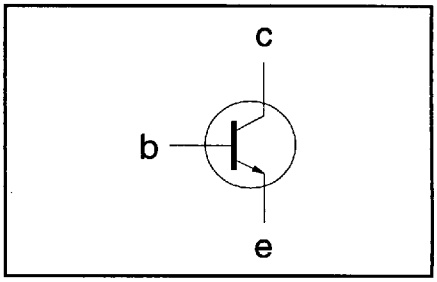
PINNING - SOT186A

PIN	DESCRIPTION
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	Collector-emitter voltage peak value	V_{BE} = 0 V	-	1000	V
V_{CEO}	Collector-emitter voltage (open base)		-	450	V
I_C	Collector current (DC)		-	5	A
I_{CM}	Collector current peak value		-	10	A
I_B	Base current (DC)		-	2	A
I_{BM}	Base current peak value		-	4	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	-	32	W
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction temperature		-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Junction to heatsink	with heatsink compound	-	3.95	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	55	-	K/W

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	Collector cut-off current [1]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	-	-	1.0	mA
I_{CES}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$; T_j = 125 °C	-	-	2.0	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 9 V; I_C = 0 A	-	-	10	mA
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0 A; I_C = 100 mA; L = 25 mH	450	-	-	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 2.5 A; I_B = 0.5 A	-	-	1.5	V
V_{BEsat}	Base-emitter saturation voltage	I_C = 2.5 A; I_B = 0.5 A	-	-	1.3	V
h_{FE}	DC current gain	I_C = 5 mA; V_{CE} = 5 V	10	18	35	
h_{FE}		I_C = 500 mA; V_{CE} = 5 V	10	20	35	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
	Switching times (resistive load)	I_{Con} = 2.5 A; I_{Bon} = $-I_{Boff}$ = 0.5 A			
t_{on}	Turn-on time		0.6	-	µs
t_s	Turn-off storage time		3.5	-	µs
t_f	Turn-off fall time		0.6	-	µs
	Switching times (inductive load)	I_{Con} = 2.5 A; I_{Bon} = 0.5 A; L_B = 1 µH; $-V_{BB}$ = 5 V			
t_s	Turn-off storage time		1.5	-	µs
t_f	Turn-off fall time		150	-	ns
	Switching times (inductive load)	I_{Con} = 2.5 A; I_{Bon} = 0.5 A; L_B = 1 µH; $-V_{BB}$ = 5 V; T_j = 100 °C			
t_s	Turn-off storage time		1.8	-	µs
t_f	Turn-off fall time		170	-	ns

1 Measured with half sine-wave voltage (curve tracer).

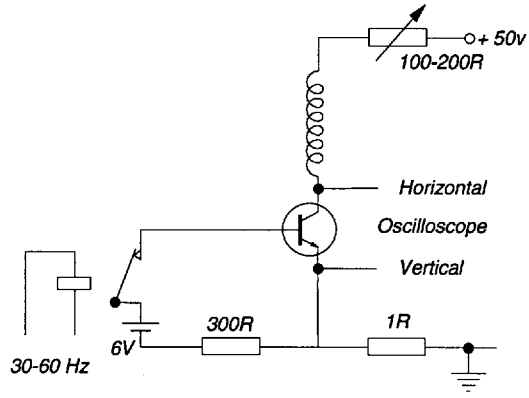


Fig.1. Test circuit for $V_{CEOsust}$.

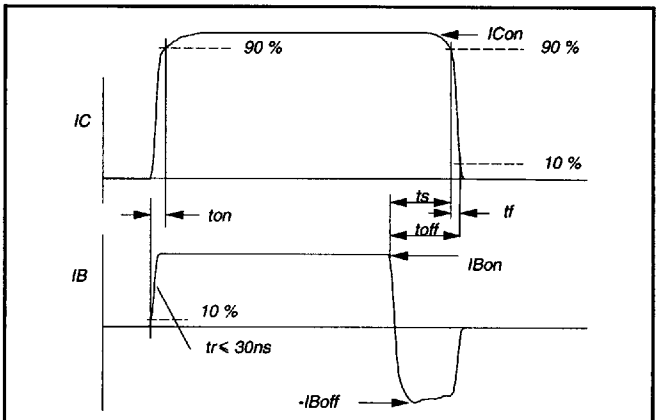


Fig.4. Switching times waveforms with resistive load.

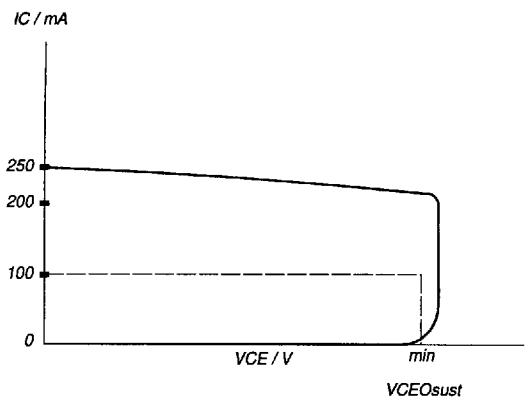


Fig.2. Oscilloscope display for $V_{CEOsust}$.

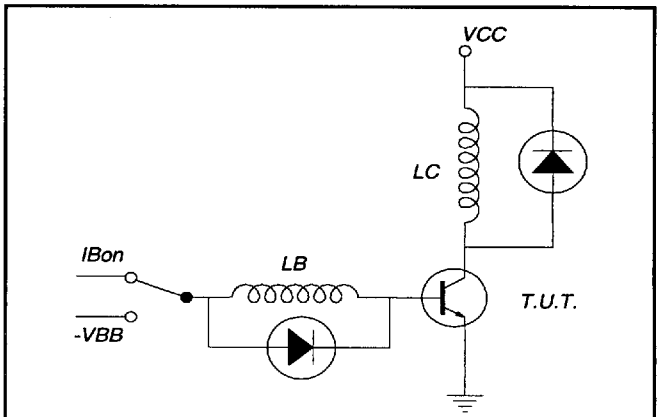


Fig.5. Test circuit inductive load.
V_{CC} = 300 V; $-V_{BE}$ = 5 V; L_C = 200 uH; L_B = 1 uH

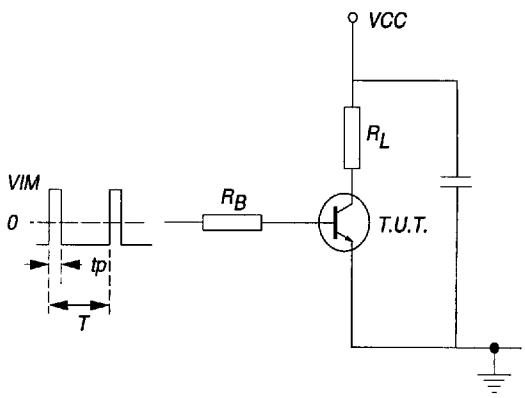


Fig.3. Test circuit resistive load. V_{IM} = -6 to +8 V
V_{CC} = 250 V; t_p = 20 μs; δ = t_p / T = 0.01.
R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

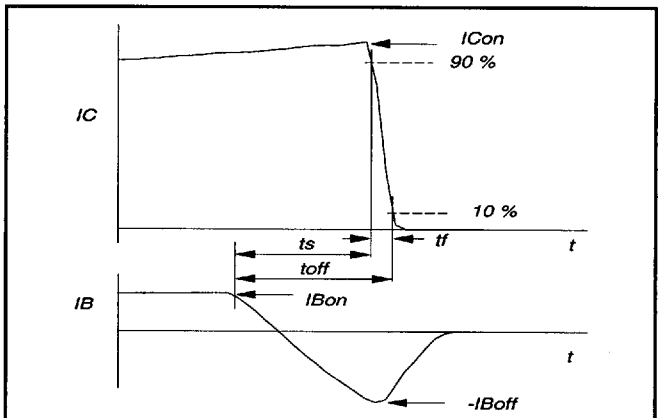


Fig.6. Switching times waveforms with inductive load.

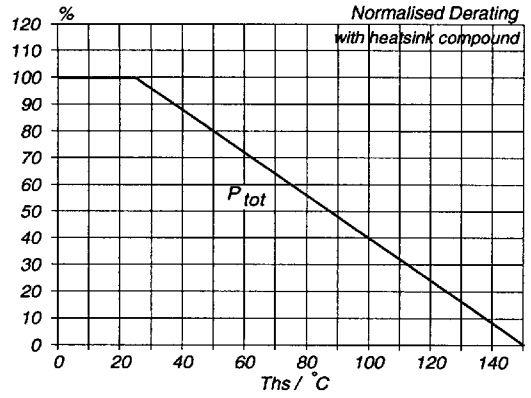


Fig.7. Normalised power derating and second breakdown curves.

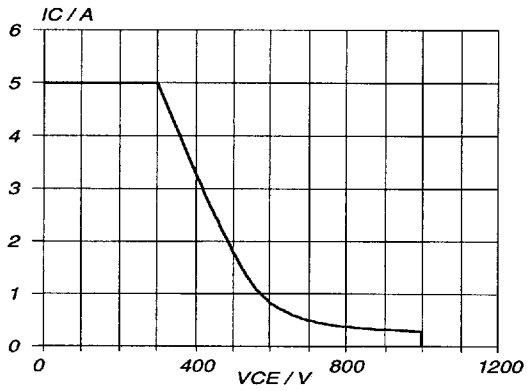


Fig.8. Reverse bias safe operating area. $T_j \leq T_{j\,max}$

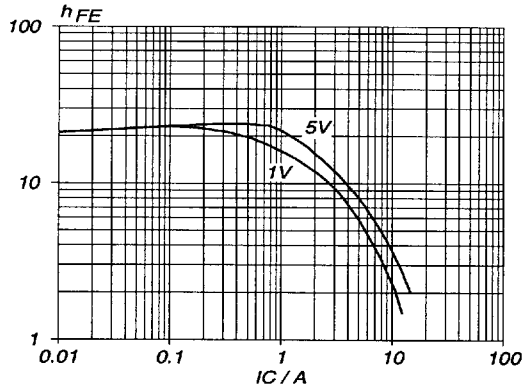


Fig.9. Typical DC current gain. $h_{FE} = f(I_C)$; parameter V_{CE}

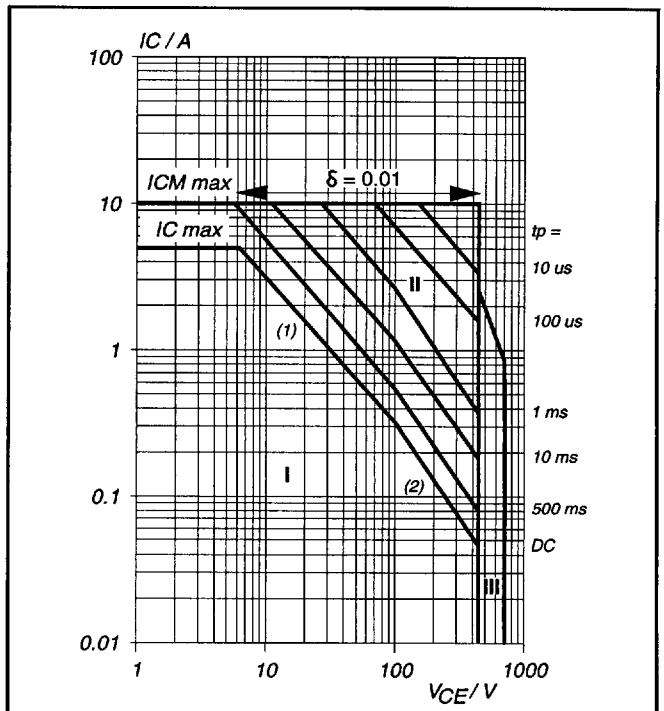


Fig.10. Forward bias safe operating area. $T_{hs} \leq 25$ °C

(1) P_{tot} max and P_{tot} peak max lines.
(2) Second breakdown limits.
I Region of permissible DC operation.
II Extension for repetitive pulse operation.
III Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\,\Omega$ and $t_p \leq 0.6\,\mu s$.
NB: Mounted with heatsink compound and 30 ± 5 newton force on the centre of the envelope.

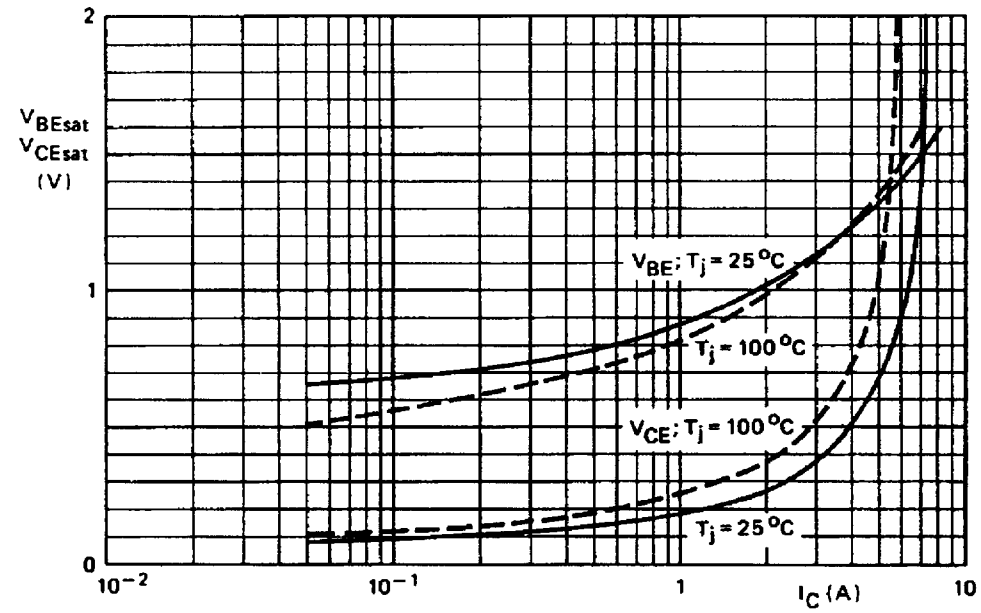


Fig.11. Typical base-emitter and collector-emitter saturation voltages.
$V_{BEsat} = f(I_C)$; $V_{CEsat} = f(I_C)$; $I_C/I_B = 5$

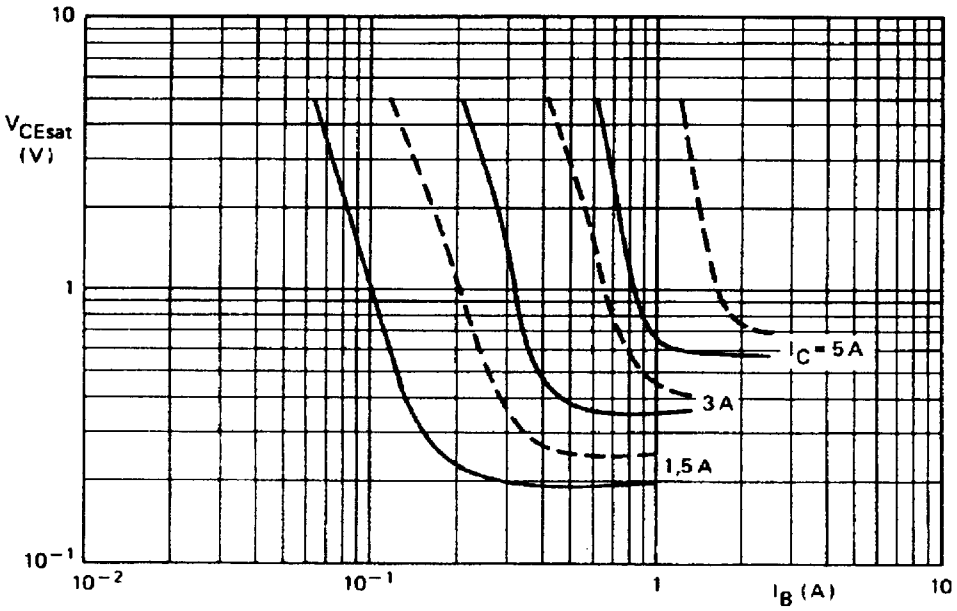


Fig.12. Collector-emitter saturation voltage. Solid lines = typ values, dotted lines = max values. $V_{CEsat} = f(I_B)$; parameter I_C

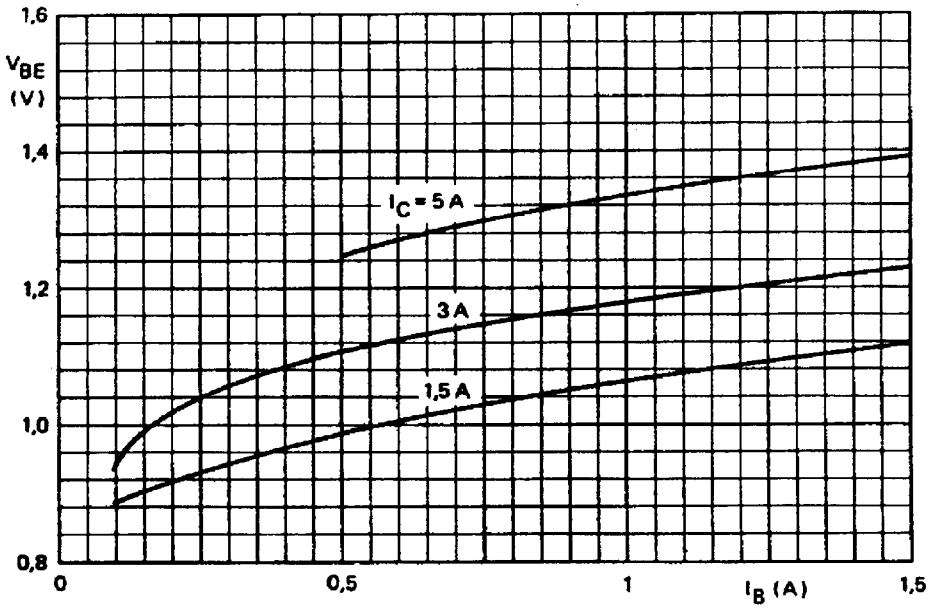


Fig.13. Typical base-emitter saturation voltage.
V_{BEsat} = f(I_B); parameter I_C

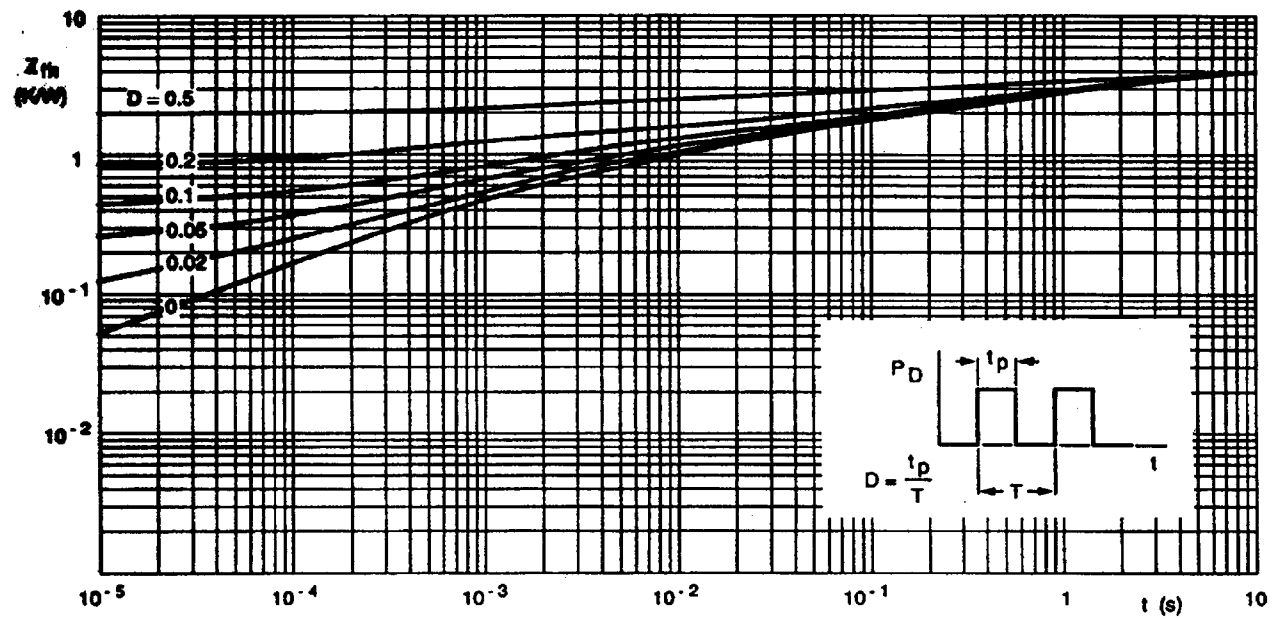


Fig.14. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

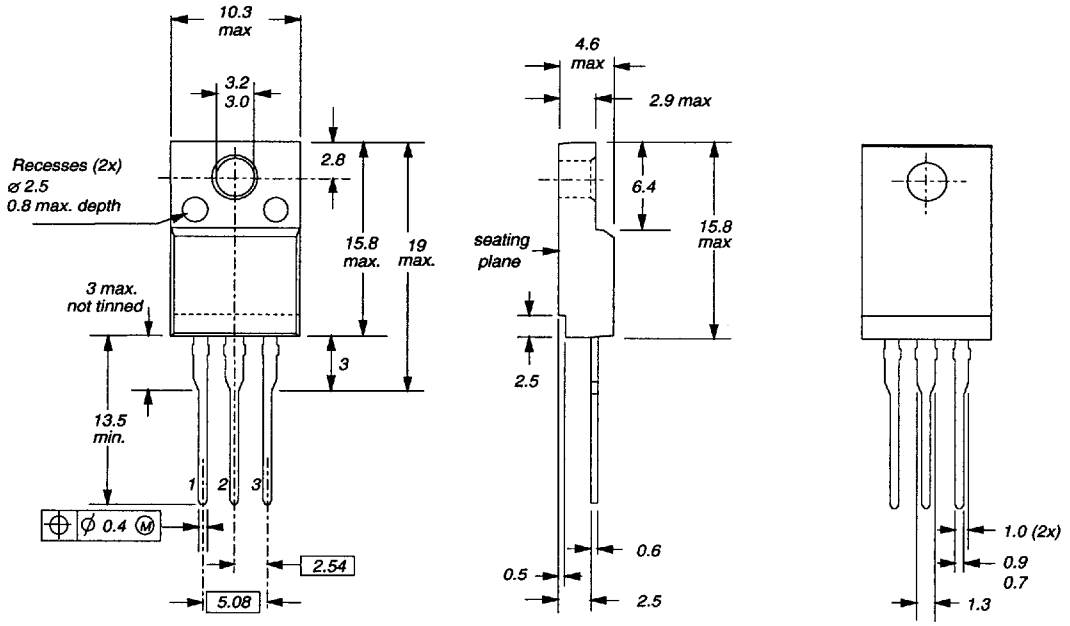


Fig.15. SOT186A; The seating plane is electrically isolated from all terminals.

Notes
1. Refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".