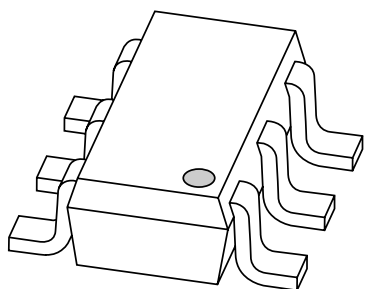


DATA SHEET



BZA456A

Quadruple ESD transient voltage
suppressor

Product specification
Supersedes data of 1998 Oct 30

1999 May 25

Quadruple ESD transient voltage suppressor

BZA456A

FEATURES

- ESD rating >8 kV, according to IEC1000-4-2
- SOT457 surface mount package
- Common anode configuration
- Non-clamping range –0.5 to 5.6 V
- Maximum reverse peak power dissipation:
24 W at $t_p = 1$ ms
- Maximum clamping voltage at peak pulse current:
8 V at $I_{ZSM} = 3$ A.

APPLICATIONS

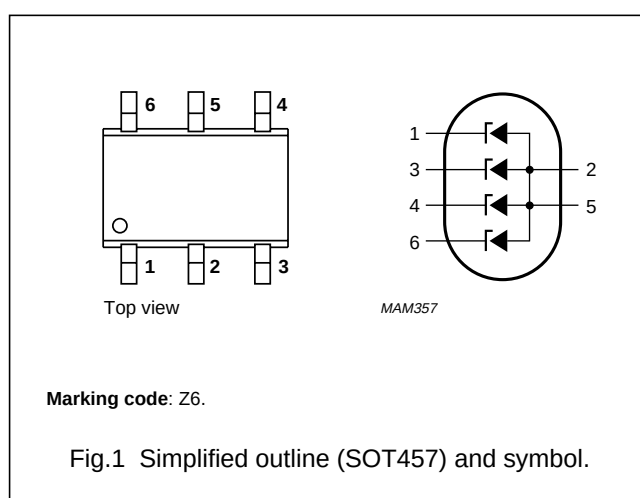
- Computers and peripherals
- Audio and video equipment
- Communication systems
- Medical equipment.

DESCRIPTION

Monolithic transient voltage suppressor diode in a six lead SOT457 (SC-74) package for 4-bit wide ESD transient suppression at 5.6 V level.

PINNING

PIN	DESCRIPTION
1	cathode 1
2	common
3	cathode 2
4	cathode 3
5	common
6	cathode 4



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
I_Z	working current	$T_s = 60$ °C; note 1	–	note 2	mA
I_F	continuous forward current	$T_s = 60$ °C	–	100	mA
I_{FSM}	non-repetitive peak forward current	$t_p = 1$ ms; square pulse	–	3.75	A
I_{ZSM}	non-repetitive peak reverse current	$t_p = 1$ ms; square pulse; see Fig.2	–	3	A
P_{tot}	total power dissipation	$T_s = 60$ °C; see Fig.3	–	720	mW
P_{ZSM}	non repetitive peak reverse power dissipation	square pulse; $t_p = 1$ ms; see Fig.4	–	24	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C

Notes

1. T_s is the temperature at the soldering point of the anode pin.
2. DC working current limited by $P_{tot\ max}$.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	one or more diodes loaded	125	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per diode						
V_Z	working voltage	$I_Z = 1\text{ mA}$	5.32	5.6	5.88	V
V_F	forward voltage	$I_F = 200\text{ mA}$	–	–	1.3	V
V_{ZSM}	non-repetitive peak reverse voltage	$I_{ZSM} = 3\text{ A}$; $t_p = 1\text{ ms}$	–	–	8	V
I_R	reverse current	$V_R = 3\text{ V}$	–	–	2	μA
r_{dif}	differential resistance	$I_Z = 250\text{ }\mu\text{A}$	–	–	1600	Ω
		$I_Z = 1\text{ mA}$	–	–	400	Ω
S_Z	temperature coefficient of working voltage	$I_Z = 5\text{ mA}$	–	1.2	–	mV/K
C_d	diode capacitance	see Fig.5 $V_R = 0$; $f = 1\text{ MHz}$	–	–	240	pF
		$V_R = 3\text{ V}$; $f = 1\text{ MHz}$	–	–	140	pF

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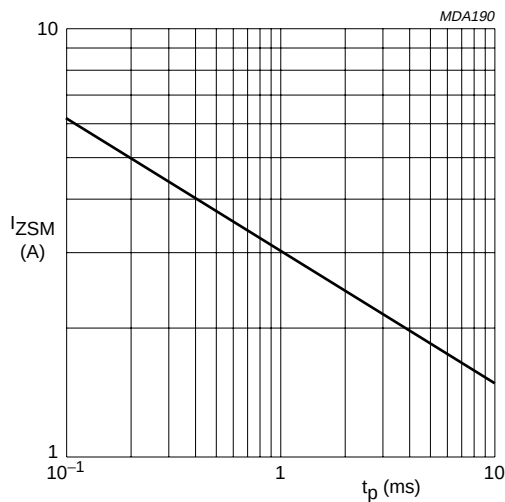
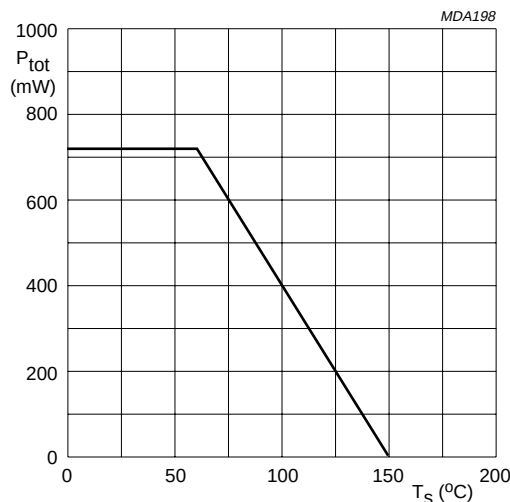
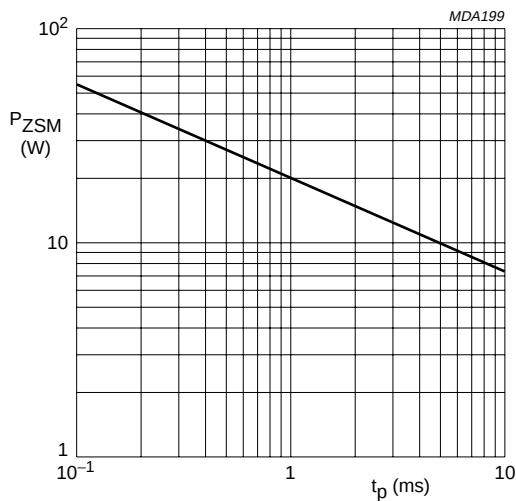


Fig.2 Maximum non-repetitive peak reverse current as a function of pulse time.



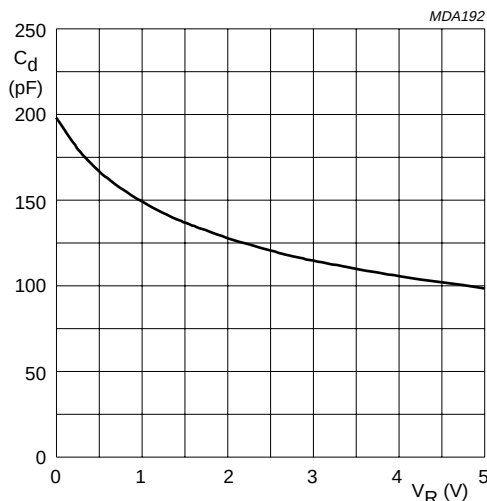
All diodes loaded.

Fig.3 Power derating curve.



$P_{ZSM} = V_{ZSM} \times I_{ZSM}$.
 V_{ZSM} is the non-repetitive peak reverse voltage at I_{ZSM} .

Fig.4 Maximum non-repetitive peak reverse power dissipation as a function of pulse duration (square pulse).

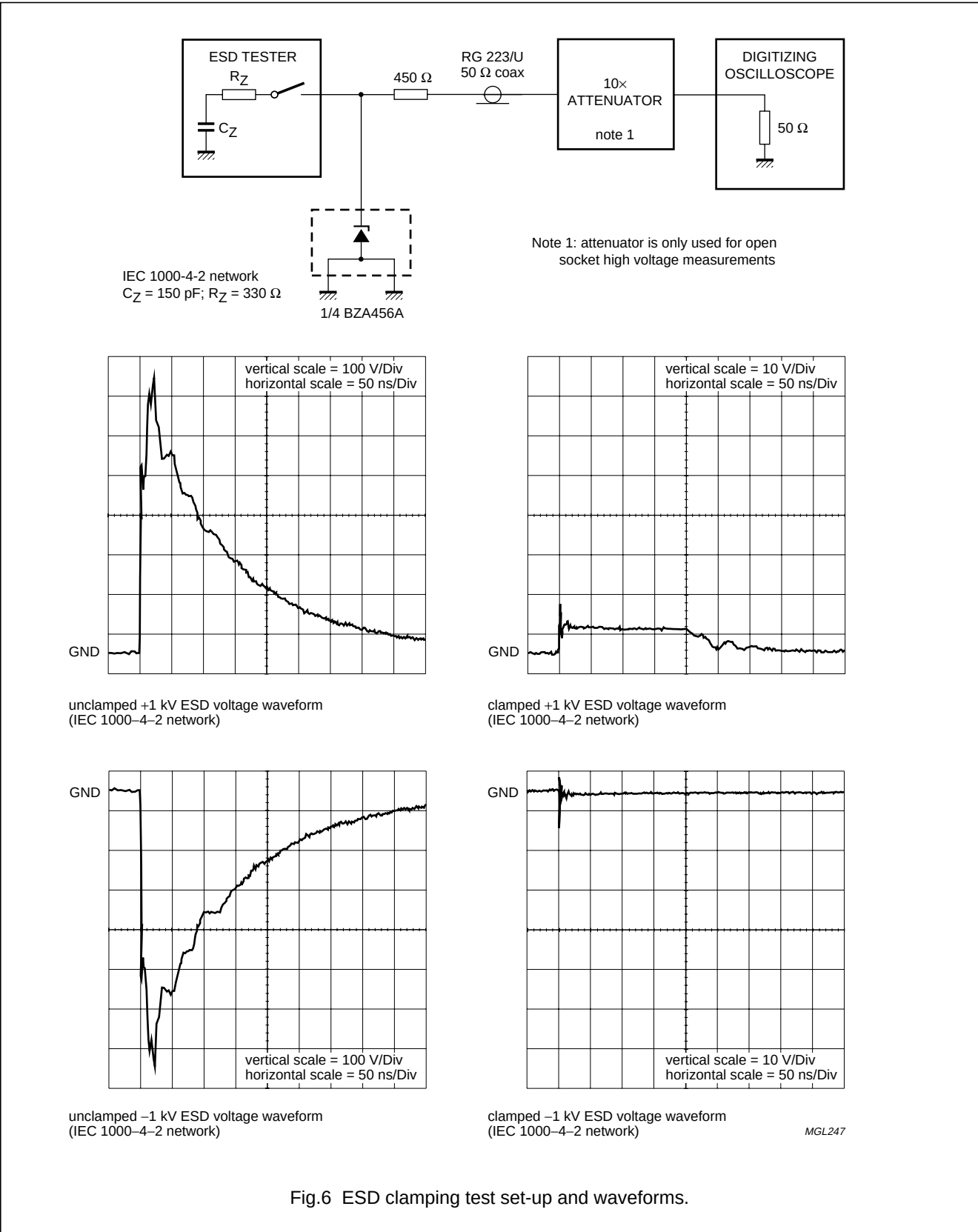


$T_j = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ MHz}$.

Fig.5 Diode capacitance as a function of reverse voltage; typical values.

Quadruple ESD transient voltage suppressor

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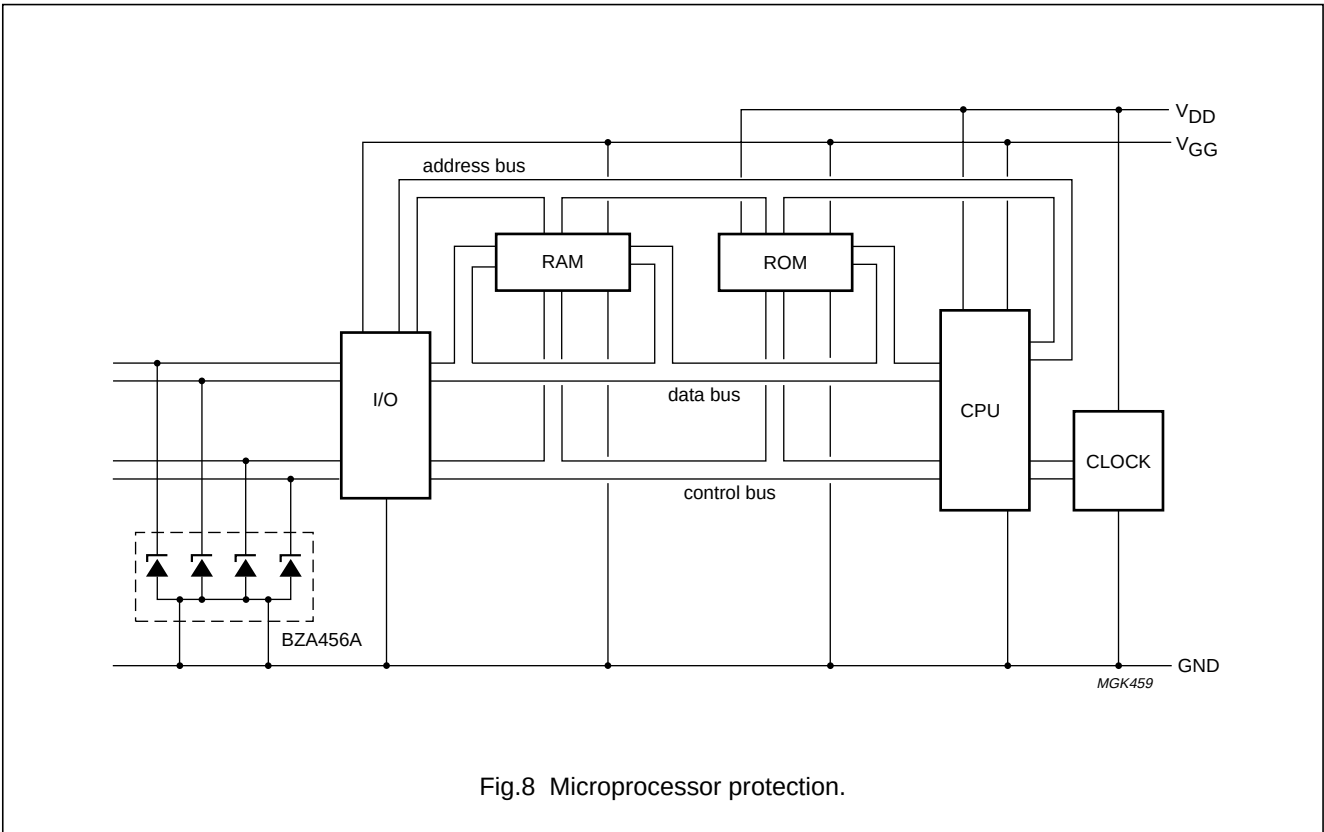
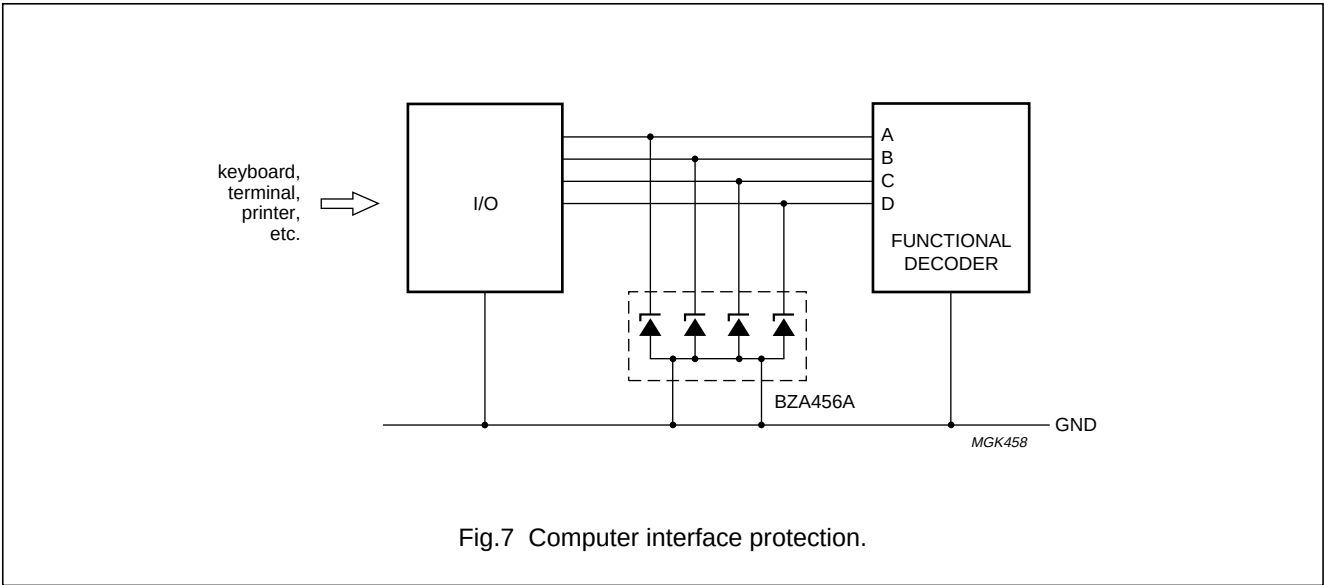
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APPLICATION INFORMATION

Typical common anode application

A quadruple transient suppressor in a SOT457 package makes it possible to protect four separate lines using only one package. Two simplified examples are shown in Figs 7 and 8.



Quadruple ESD transient voltage suppressor

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Device placement and printed-circuit board layout

Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA456A is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage ($V = L di/dt$) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors.
2. Keep parallel signal paths to a minimum.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.

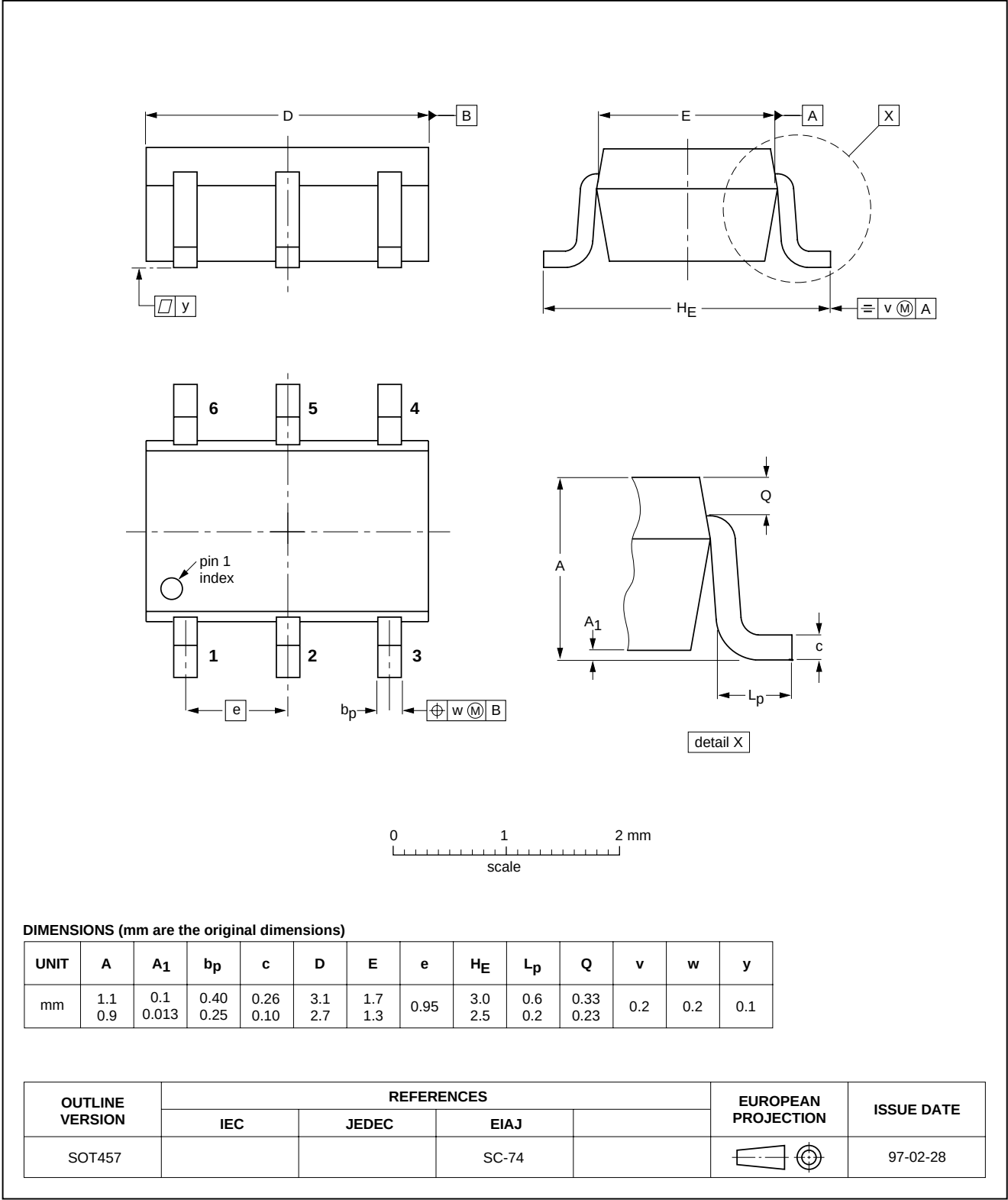
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



Quadruple ESD transient voltage suppressor

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

Quadruple ESD transient voltage suppressor

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NOTES

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Printed in The Netherlands

115002/00/03/pp12

Date of release: 1999 May 25

Document order number: 9397 750 05953

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