

CD4078B Types

CMOS 8-Input NOR/OR Gate

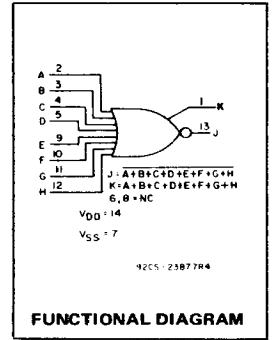
High-Voltage Types (20-Volt Rating)

The RCA-CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-Speed Operation:
t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V
2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|---------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) (Voltages referenced to V _{SS} Terminal) | -0.5 to +20 V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5 to V _{DD} +0.5 V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10 mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -40 to +60°C (PACKAGE TYPE E) | 500 mW |
| For T _A = +60 to +85°C (PACKAGE TYPE E) | Derate Linearly at 12 mW/°C to 200 mW |
| For T _A = -55 to +100°C (PACKAGE TYPES D, F, K) | 500 mW |
| For T _A = +100 to +125°C (PACKAGE TYPES D, F, K) | Derate Linearly at 12 mW/°C to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100 mW |
| OPERATING-TEMPERATURE RANGE (T _A): | |
| PACKAGE TYPES D, F, K, H | -55 to +125°C |
| PACKAGE TYPE E | -40 to +85°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65 to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. | +265°C |

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | Min. | Max. | Units |
|---|------|------|-------|
| Supply Voltage Range (For T _A Full Package Temperature Range) | 3 | 18 | V |

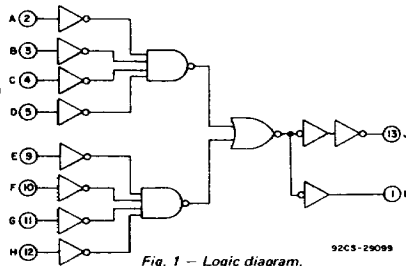


Fig. 1 - Logic diagram.

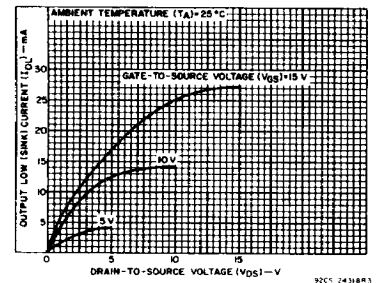


Fig. 2 - Typical output low (sink) current characteristics.

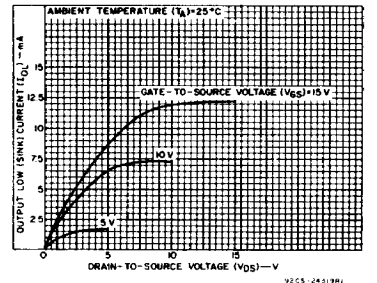


Fig. 3 - Minimum output low (sink) current characteristics.

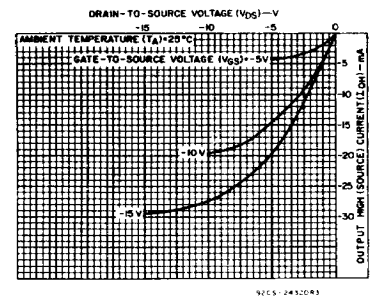


Fig. 4 - Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

| CHARACTERISTIC | TEST CONDITIONS | ALL TYPES LIMITS | | UNITS | |
|--|-----------------|-----------------------|------|-------|------|
| | | V _{DD} VOLTS | TYP. | | MAX. |
| Propagation Delay Time, t _{PHL} , t _{PLH} | | 5 | 150 | 300 | ns |
| | | 10 | 75 | 150 | |
| | | 15 | 55 | 110 | |
| Transition Time, t _{THL} , t _{TLH} | | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Input Capacitance, C _{IN} | Any Input | | 5 | 7.5 | pF |

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STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | +25 | | | | | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | - | 0.01 | 0.25 | μA |
| | - | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | - | 0.01 | 0.5 | |
| | - | 0,15 | 15 | 1 | 1 | 30 | 30 | - | 0.01 | 1 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | | | 0.05 | | | 0 | 0.05 | V |
| | - | 0,10 | 10 | | | 0.05 | | | 0 | 0.05 | |
| | - | 0,15 | 15 | | | 0.05 | | | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | | | 4.95 | | | 4.95 | 5 | V |
| | - | 0,10 | 10 | | | 9.95 | | | 9.95 | 10 | |
| | - | 0,15 | 15 | | | 14.95 | | | 14.95 | 15 | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | | | 1.5 | | | - | 1.5 | V |
| | 1.9 | - | 10 | | | 3 | | | - | 3 | |
| | 1.5, 13.5 | - | 15 | | | 4 | | | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | | | 3.5 | | | 3.5 | - | V |
| | 1.9 | - | 10 | | | 7 | | | 7 | - | |
| | 1.5, 13.5 | - | 15 | | | 11 | | | 11 | - | |
| Input Current I _{IY} Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |

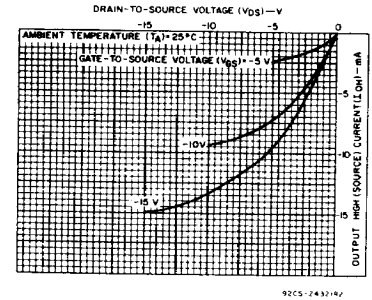


Fig. 5 - Minimum output high (source) current characteristics.

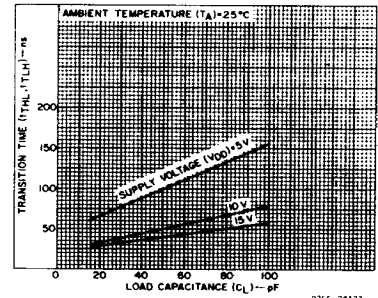


Fig. 6 - Typical transition time as a function of load capacitance.

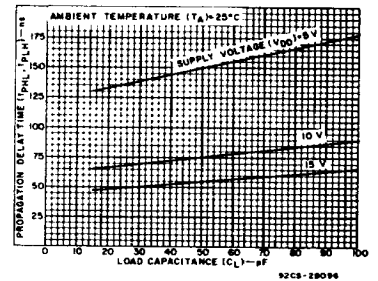


Fig. 7 - Typical propagation delay time as a function of load capacitance.

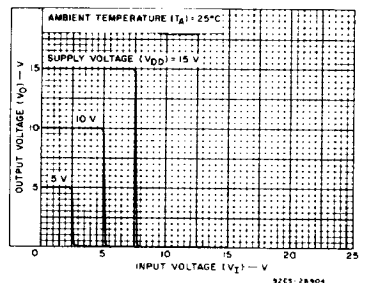


Fig. 9 - Typical voltage transfer characteristics (NOR output).

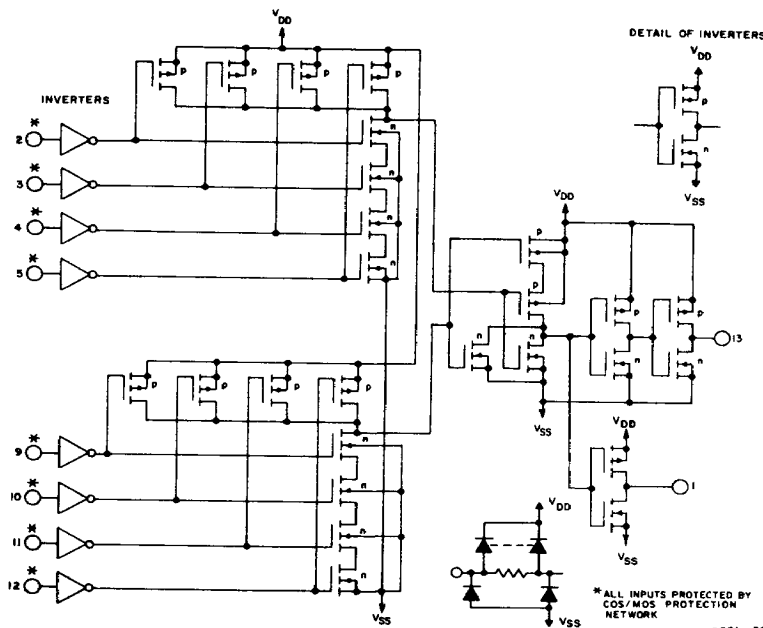


Fig. 8 - Schematic diagram.

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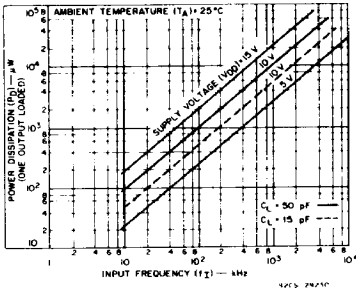


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

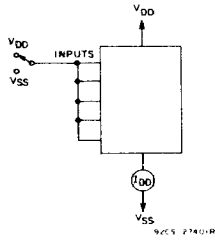


Fig. 11 – Quiescent-device-current test circuit.

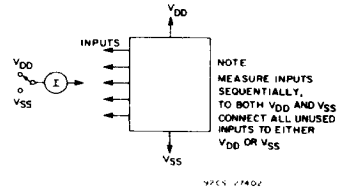


Fig. 12 – Input current test circuit.

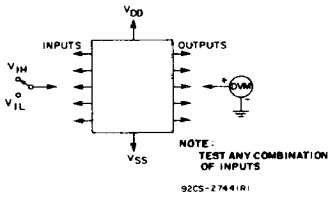


Fig. 13 – Input-voltage test circuit.

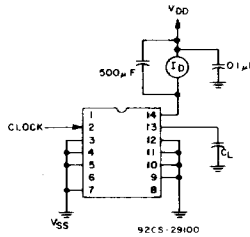
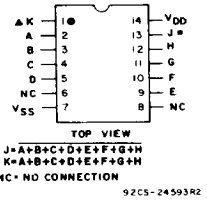
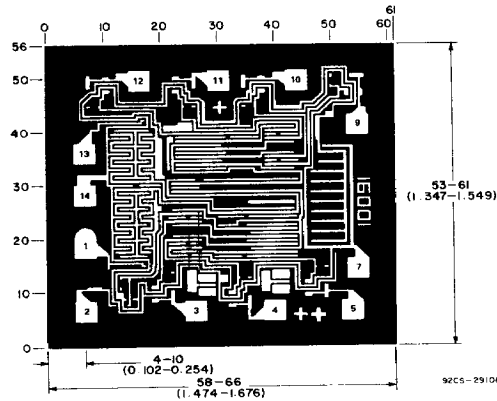


Fig. 14 – Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.