

HS-508BRH, HS-508BEH

Radiation Hardened 8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FN4824
Rev 3.00
November 17, 2011

The HS-508BRH, HS-508BEH are dielectrically isolated, radiation hardened, CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10V greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521 for further information on the HS-508BRH, HS-508BEH multiplexers in general.

The HS-508BRH, HS-508BEH have been specifically designed to meet exposure to radiation environments. Operation from -55°C to +125°C is guaranteed.

Features

- Electrically Screened to SMD # [5962-96742](#)
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
 - Gamma Dose (γ) 3×10^5 Rad (Si)
 - Dielectrically Isolated Device Islands
 - SEP >100 Mev-mg/cm²
- Analog/Digital Overvoltage Protection
- ESD Rated to 3kV
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- (Typ) DTL/TTL and CMOS Compatible Threshold
- Analog Signal Range. $\pm 15V$
- Fast Access Time
- Supply Current at 1MHz Address Toggle 4mA (Typ)
- Standby Power 7.5mW (Typ)
- Pb-Free (RoHS Compliant)

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

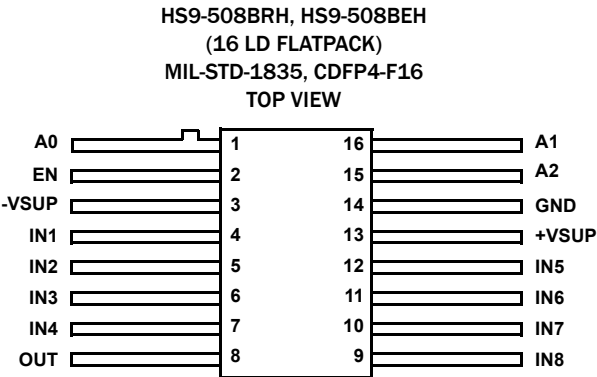
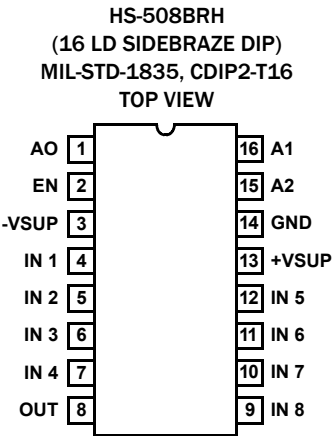
Detailed Electrical Specifications for these devices are contained in SMD [5962-96742](#).

Ordering Information

ORDERING NUMBER (Note)	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG.
5962F9674202QEC	HS1-508BRH-8	Q 5962F96 74202QEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9674202QXC	HS9-508BRH-8	Q 5962F96 74202QXC	-55 to +125	16 Ld Flatpack	K16.A
5962F9674202VEC	HS1-508BRH-Q	Q 5962F96 74202VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9674202VXC	HS9-508BRH-Q	Q 5962F96 74202VXC	-55 to +125	16 Ld Flatpack	K16.A
HS1-508BRH/PROTO	HS1-508BRH/PROTO	HS1- 508BRH /PROTO	-55 to +125	16 Ld SBDIP	D16.3
HS9-508BRH/PROTO	HS9-508BRH/PROTO	HS9- 508BRH /PROTO	-55 to +125	16 Ld Flatpack	K16.A
5962F9674203VXC	HS9-508BEH-Q	Q 5962F96 74203VXC	-55 to +125	16 Ld Flatpack	K16.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pin Configurations



Functional Diagram

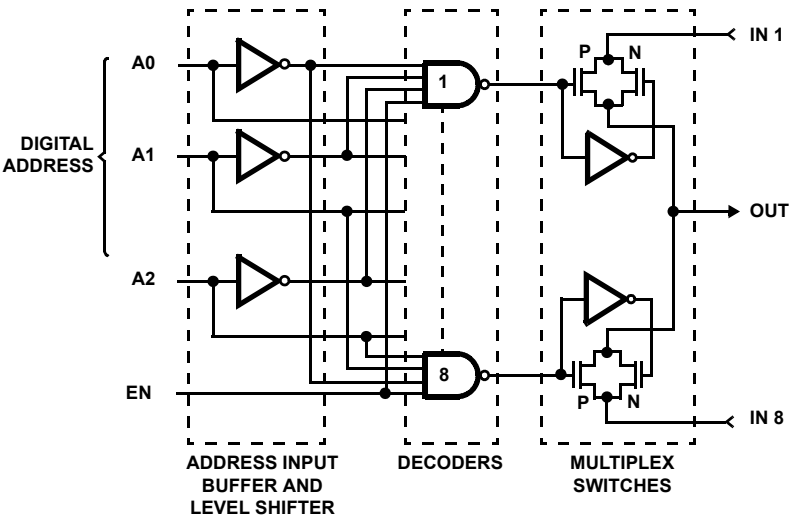


TABLE 1. TRUTH TABLE

A2	A1	A0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Die Characteristics

DIE DIMENSIONS

120 mils x 93 mils x 19 mils

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)

Thickness: $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Top Metallization

Type: AlSiCu

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

Substrate

Rad Hard Silicon Gate

Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density

$6.68\text{e}04 \text{ A/cm}^2$

Transistor Count

506

Metallization Mask Layout

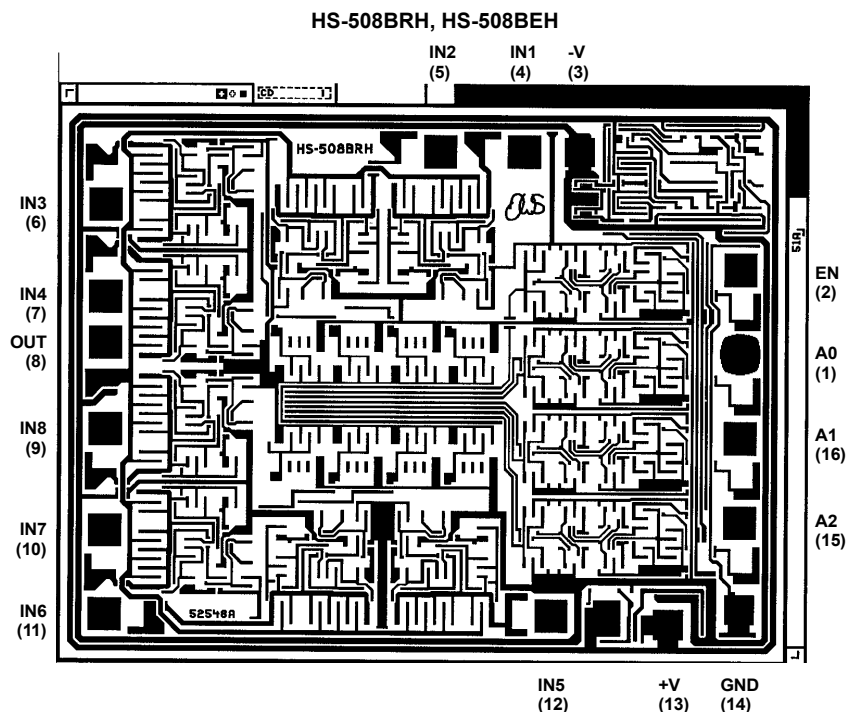


TABLE 2. HS-508BRH, HS-508BEH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	A0	0	0
2	EN	-342	0
3	V-	-818	-653
4	IN1	-818	-879
5	IN2	-818	-1221
6	IN3	-598	-2579
7	IN4	-224	-2579
8	OUT	-38	-2579
9	IN8	314	-2579
10	IN7	724	-2579
11	IN6	1066	-2579
12	-IN5	1066	-761
13	V+	1100	-287
14	GND	1038	0
15	A2	684	0
16	A1	342	0

NOTE: Dimensions in microns

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