ISL54222A

High-Speed USB 2.0 (480Mbps) Multiplexer

FN6902
Rev 1.00
February 4, 2010

The Intersil ISL54222A is a single supply dual 2:1 multiplexer that can operate from a single 1.8V to 3.3V supply. It contains two SPDT (Single Pole/Double Throw) switches configured as a DPDT. The part was designed for switching or routing of USB High-Speed signals and/or USB Full-speed signals in portable battery powered products.

The 4.4Ω switches can swing rail-to-rail and were specifically designed to pass USB full speed data signals that range from 0V to 3.3V and USB high-speed data signals that range from 0V to 400mV with a single supply as low as 1.8V. They have high bandwidth and low capacitance to pass USB high speed data signals with minimal distortion.

The digital logic inputs are 1.8V logic compatible when operated with a 1.8V to 3.3V supply. The ISL54222A has an output enable pin to open all the switches and put the part in a low power state.

The ISL54222A is available in 10 Ld 1.8mmx1.4mm µTQFN, 10 Ld 2.1mmx1.6mm µTQFN, 10 Ld TDFN and 10 Ld MSOP packages. It operates over a temperature range of -40° to +85°C.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN1450 “ISL54222AIRUEVAL1Z Evaluation Board User’s Manual”

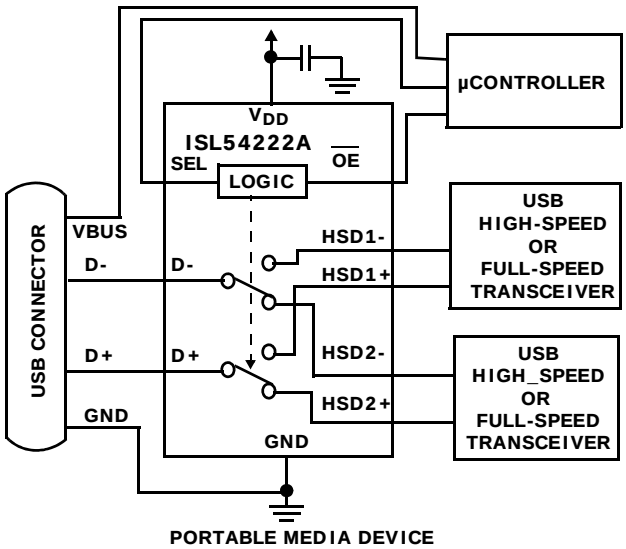
Features

- High-Speed (480Mbps) and Full-Speed (12Mbps) Signaling Capability per USB 2.0
- 1.8V Logic Compatible
- Low Power All Off State
- Power OFF Protection
- D-/D+ Pins Overvoltage Tolerant to 5.5V
- -3dB Frequency 780MHz
- Low ON Capacitance @ 240MHz 4.2pF
- Low ON-Resistance @ V_{DD} = 3V 4.4Ω
- Low ON-Resistance @ V_{DD} = 1.8V. 5.7Ω
- Single Supply Operation (V_{DD}) . . . . . 1.8V to 3.3V
- Available in µTQFN, TDFN, MSOP Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit and Overvoltage Requirements Without Additional External Components
- HBM ESD Performance I/O to GND . . . . . >12kV

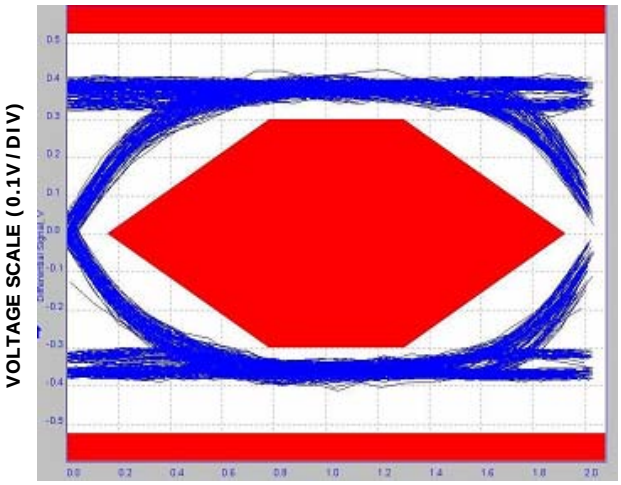
Applications* (see page 15)

- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDAs
- Digital Cameras and Camcorders
- USB Switching

Application Block Diagram

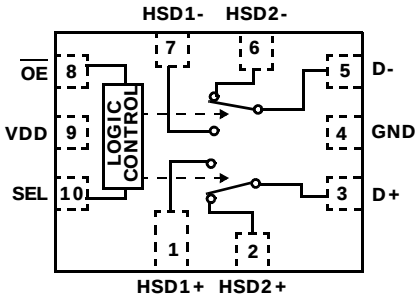


USB 2.0 HS Eye Pattern With Switches In The Signal Path

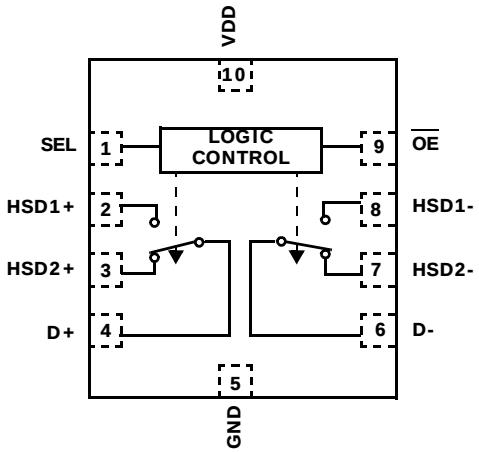


Pin Configurations

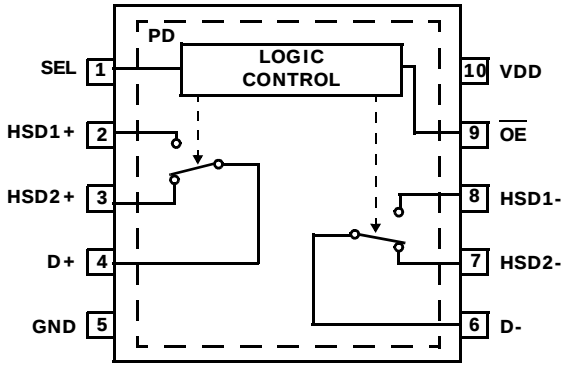
ISL54222A
(10 LD 1.8X1.4 µTQFN)
TOP VIEW



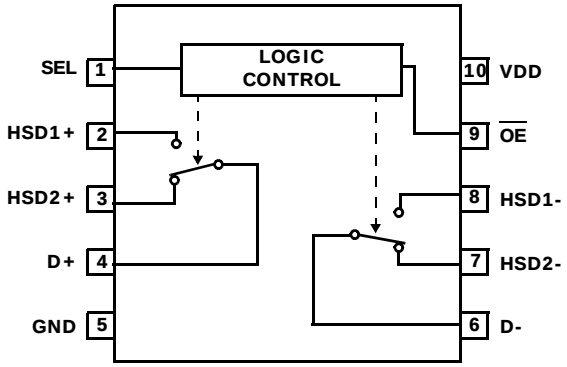
ISL54222A
(10 LD 2.1X1.6 µTQFN)
TOP VIEW



ISL54222A
(10 LD 3X3 TDFN)
TOP VIEW



ISL54222A
(10 LD MSOP)
TOP VIEW



NOTE:

1. Switches Shown for SEL = Logic “1” and $\overline{OE}$ = Logic “0”.

Truth Table

$\overline{OE}$	SEL	HSD1-, HSD1+	HSD2-, HSD2+
0	0	ON	OFF
0	1	OFF	ON
1	X	OFF	OFF

NOTE: Logic “0” when ≤ 0.5V, Logic “1” when ≥ 1.4V with a 1.8V to 3.3V Supply.

Pin Descriptions

TDFN	MSOP	µTQFN 1.8x1.4	µTQFN 2.1x1.6	NAME	FUNCTION
10	10	9	10	VDD	Power Supply (1.8V to 3.3V)
1	1	10	1	SEL	Select Logic Control Input
2	2	1	2	HSD1+	USB Data Port (Channel 1 Positive Input)

Pin Descriptions (Continued)

TDFN	MSOP	µTQFN 1.8x1.4	µTQFN 2.1x1.6	NAME	FUNCTION
3	3	2	3	HSD2+	USB Data Port (Channel 2 Positive Input)
4	4	3	4	D+	USB Data Common Positive Port
5	5	4	5	GND	Ground Connection
6	6	5	6	D-	USB Data Common Negative Port
7	7	6	7	HSD2-	USB Data Port (Channel 2 Negative Input)
8	8	7	8	HSD1-	USB Data Port (Channel 1 Negative Input)
9	9	8	9	$\overline{OE}$	Bus Switch Enable
PD	-	-	-	PD	Thermal Pad. Tie to Ground or Float

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54222AIRUZ-T (Notes 2, 4)	X	-40 to +85	10 Ld 1.8x1.4mm µTQFN (Tape and Reel)	L10.1.8x1.4A
ISL54222AIRU1Z-T (Notes 2, 4)	GS	-40 to +85	10 Ld 2.1x1.6mm µTQFN (Tape and Reel)	L10.2.1x1.6A
ISL54222AIRTZ (Note 3)	222A	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54222AIRTZ-T (Notes 2, 3)	222A	-40 to +85	10 Ld 3x3 TDFN (Tape and Reel)	L10.3x3A
ISL54222AIUZ (Note 3)	4222A	-40 to +85	10 Ld MSOP	M10.118
ISL54222AIUZ-T (Notes 2, 3)	4222A	-40 to +85	10 Ld MSOP (Tape and Reel)	M10.118
ISL54222AIRUEVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54222A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to 3.5V
Input Voltages
HSD2x, HSD1x (Note 6) . . . . . - 0.3V to 6V
SEL, $\overline{OE}$ (Note 6) . . . . . -0.3 to ((V_{DD}) + 0.3V)
Output Voltages
D+, D- (Note 6) . . . . . -0.3V to 6V
Continuous Current (HSD2x, HSD1x) . . . . . ±40mA
Peak Current (HSD2x, HSD1x)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model . . . . . >8kV
Human Body Model, (I/O pins to GND) . . . . . >12kV
Machine Model . . . . . >500V
Charged Device Model . . . . . >2.2kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld TDFN (Notes 8, 9)	55	18
10 Ld MSOP (Notes 7, 10)	165	65
10 Ld 2.1x1.6 µTQFN (Notes 7, 10)	160	100
10 Ld 1.8x1.4 µTQFN (Notes 7, 10)	160	105

Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
V_{DD} Supply Voltage Range . . . . . 1.8V to 3.3V
Logic Control Input Voltage . . . . . 0V to V_{DD}
Analog Signal Range . . . . . 0V to 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on HSD1x, HSD2x, D+,D- exceeding GND by specified amount are clamped. Signals on $\overline{OE}$ and SEL exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
9. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
10. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications - 1.8V to 3.3V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON} (High-Speed)	V_{DD} = 1.8V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 40mA, V_{HSD1x} or $V_{HSD2\ x}$ = 0V to 400mV (see Figure 3, Note 16)	25	-	5.7	8	Ω
		Full	**-**	-	**10**	Ω
r_{ON} Matching Between Channels, Δr_{ON} (High-Speed)	V_{DD} = 1.8V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 40mA, V_{HSD1x} or $V_{HSD2\ x}$ = Voltage at max r_{ON}, (Notes 15, 16)	25	-	0.072	0.5	Ω
		Full	**-**	-	**0.55**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$ (High-Speed)	V_{DD} = 1.8V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 40mA, V_{HSD1x} or $V_{HSD2\ x}$ = 0V to 400mV, (Notes 14, 16)	25	-	0.60	0.9	Ω
		Full	**-**	-	**1**	Ω
OFF Leakage Current, $I_{HSD1x(OFF)}$	V_{DD} = 3.3V, SEL = V_{DD} and $\overline{OE}$ = 0V or $\overline{OE}$ = V_{DD}, V_{Dx} = 0.3V, 3V, V_{HSD1X} = 3V, 0.3V, V_{HSD2x} = 0.3V, 3V	25	-15	0.35	15	nA
		Full	**-20**	-	**20**	nA
ON Leakage Current, $I_{HSD1x(ON)}$	V_{DD} = 3.3V, SEL = $\overline{OE}$ = 0V, V_{Dx} = 0.3V, 3V, V_{HSD1X} = 0.3V, 3V, V_{HSD2x} = 3V, 0.3V	25	-20	5	20	nA
		Full	**-25**	-	**25**	nA
OFF Leakage Current, $I_{HSD2x(OFF)}$	V_{DD} = 3.3V, SEL = $\overline{OE}$ = 0V or $\overline{OE}$ = V_{DD}, V_{Dx} = 3V, 0.3V, V_{HSD2x} = 0.3V, 3V, V_{HSD1X} = 3V, 0.3V	25	-15	0.26	15	nA
		Full	**-20**	-	**20**	nA

Electrical Specifications - 1.8V to 3.3V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ON Leakage Current, $I_{HSD2x(ON)}$	V_{DD} = 3.3V, SEL = V_{DD}, $\overline{OE}$ = 0V, V_{Dx}= 0.3V, 3V, V_{HSD2x} = 0.3V, 3V, V_{HSD1X} = 3V, 0.3V	25	-20	4.4	20	nA
		Full	**-25**	-	**25**	nA
Power OFF Leakage Current, I_{OFF}	V_{DD} = 0V, V_{D+} = 0V to 5.25V, V_{D-}= 0V to 5.25V	25	-	0.008	0.025	µA
		Full	**-**	-	**0.65**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 500Ω, C_L = 50pF (Figure 1)	25	-	25	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 500Ω, C_L = 50pF (Figure 1)	25	-	17	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 500Ω, C_L = 50pF (Figure 2)	25	-	17	-	ns
Turn-ON Enable Time, t_{ENABLE}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 15KΩ, C_L = 50pF, Time out of All-Off state	25	-	37	-	ns
Turn-OFF Disable Time, $t_{DISABLE}$	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 15kΩ, C_L = 50pF, Time into All-Off state, Time is highly dependent on the load (R_L, C_L) time constant.	25	-	96	-	ns
Skew, ($t_{SKEWOUT}$ - t_{SKEWIN})	V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps, (Duty Cycle = 50%) (Figure 6)	25	-	50	-	ps
Rise/Fall Degradation (Propagation Delay), t_{PD}	V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, R_L = 45Ω, C_L = 10pF, (Figure 6)	25	-	250	-	ps
Crosstalk	V_{DD} = 3.3V, R_L = 50Ω, f = 240MHz (see Figure 5)	25	-	-31	-	dB
OFF-Isolation	V_{DD} = 3.3V, $\overline{OE}$ = 3.3V, R_L = 50Ω, f = 240MHz	25	-	-28	-	dB
-3dB Bandwidth	Signal = 0dBm, 0.2VDC offset, R_L = 50Ω	25	-	780	-	MHz
OFF Capacitance, C_{HSxOFF}	f = 1MHz, V_{DD} = 3.3V, SEL = 0V, $\overline{OE}$ = 3.3V, V_{HSD1x} or V_{HSD2x} = V_{Dx} = 0V (Figure 4)	25	-	2.6	-	pF
COM ON Capacitance, $C_{DX(ON)}$	f = 1MHz, V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, V_{HSD1x} or V_{HSD2x} = V_{Dx} = 0V (Figure 4)	25	-	6.7	-	pF
COM ON Capacitance, $C_{DX(ON)}$	f = 240MHz, V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, V_{HSD1x} or V_{HSD2x} = V_{Dx} = 0V (Figure 4)	25	-	4.2	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**1.8**		**3.3**	V
Positive Supply Current, I_{DD}	V_{DD} = 3.3V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V	25	-	32	43	µA
		Full	**-**	-	**50**	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.3V, SEL = 0V or V_{DD}, $\overline{OE}$ = V_{DD}	25	-	0.77	1	µA
		Full	**-**	-	**1.5**	µA

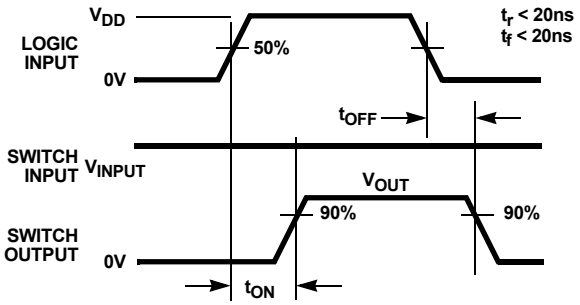
Electrical Specifications - 1.8V to 3.3V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Positive Supply Current, I_{DD}	V_{DD} = 1.8V, SEL = 0V, $\overline{OE}$ = 0V	25	-	5.8	7.8	µA
		Full	-	-	**8.3**	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 1.8V, SEL = 0V, $\overline{OE}$ = V_{DD}	25	-	0.12	0.3	µA
		Full	-	-	**1**	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{SELL}, $V_{\overline{OE}L}$	V_{DD} = 1.8V to 3.3V	Full	-	-	**0.5**	V
Input Voltage High, V_{SELH}, $V_{\overline{OE}H}$	V_{DD} = 1.8V to 3.3V	Full	**1.4**	-	**V_{DD}**	V
Input Current, I_{SELL}, $I_{\overline{OE}L}$	V_{DD} = 3.3V, SEL = 0V, $\overline{OE}$ = 0V	Full	-	170	-	nA
Input Current, I_{SELH}	V_{DD} = 3.3V, SEL = 3.3V	Full	-	-1.4	-	nA
Input Current, $I_{\overline{OE}H}$	V_{DD} = 3.3V, $\overline{OE}$ = 3.3V	Full	-	-1.4	-	nA

NOTES:

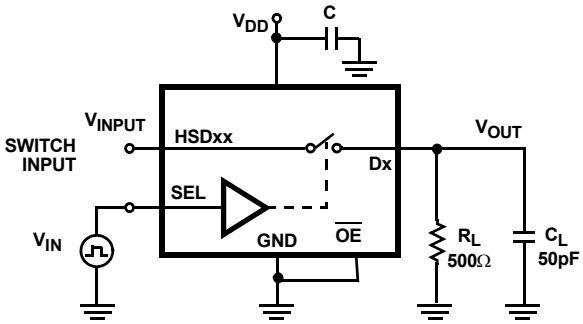
11. V_{LOGIC} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
15. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between HSD2+ and HSD2- or between HSD1+ and HSD1-.
16. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

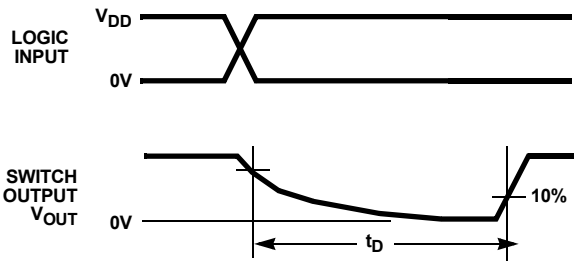
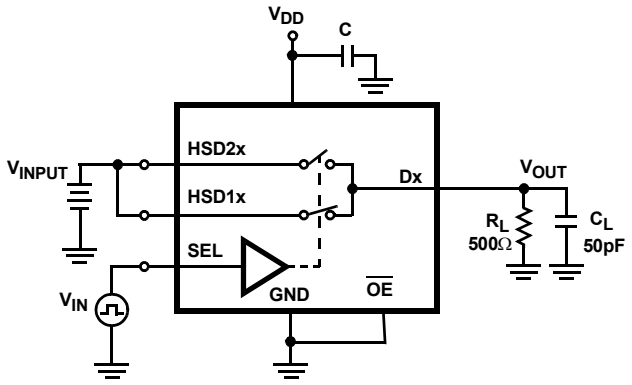


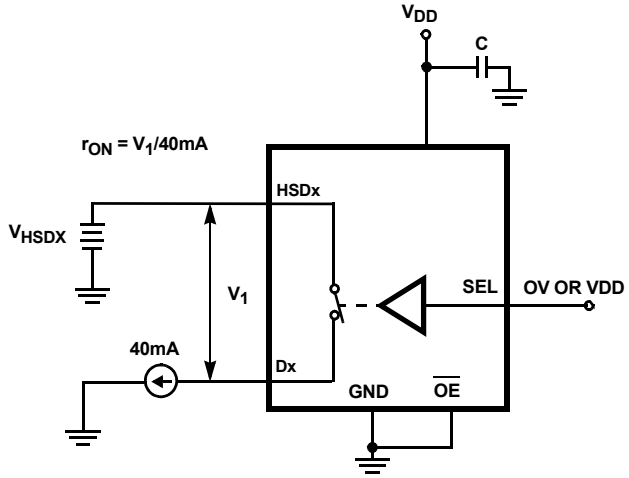
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

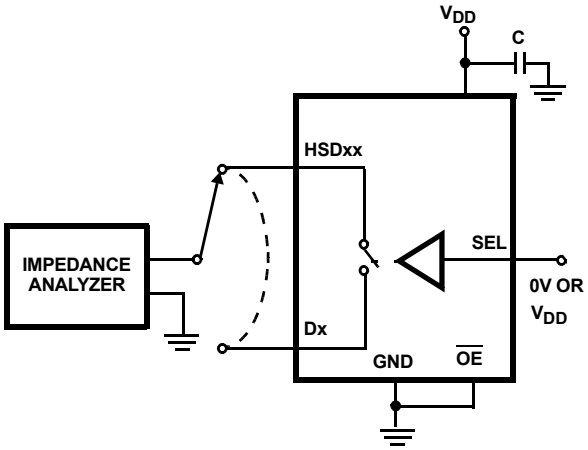
FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

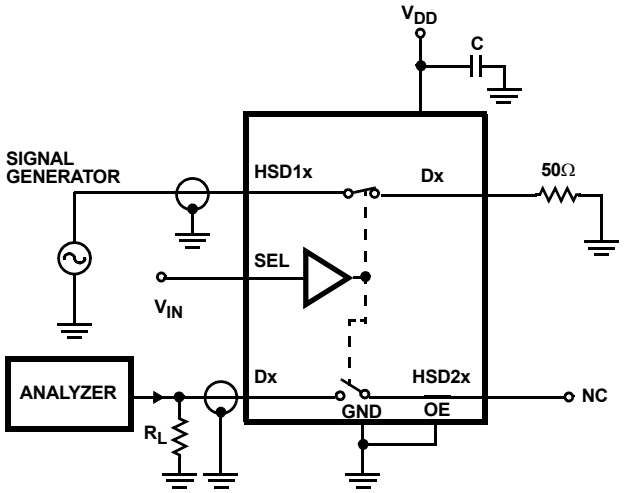
FIGURE 3. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 4. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 5. CROSSTALK TEST CIRCUIT

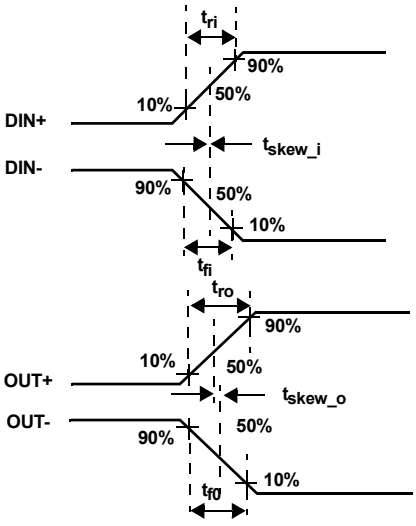
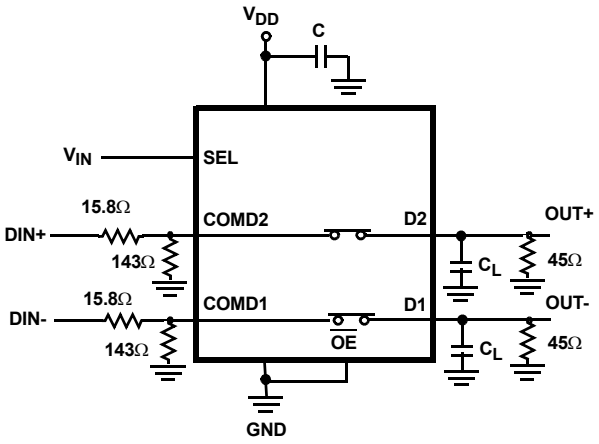


FIGURE 6A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

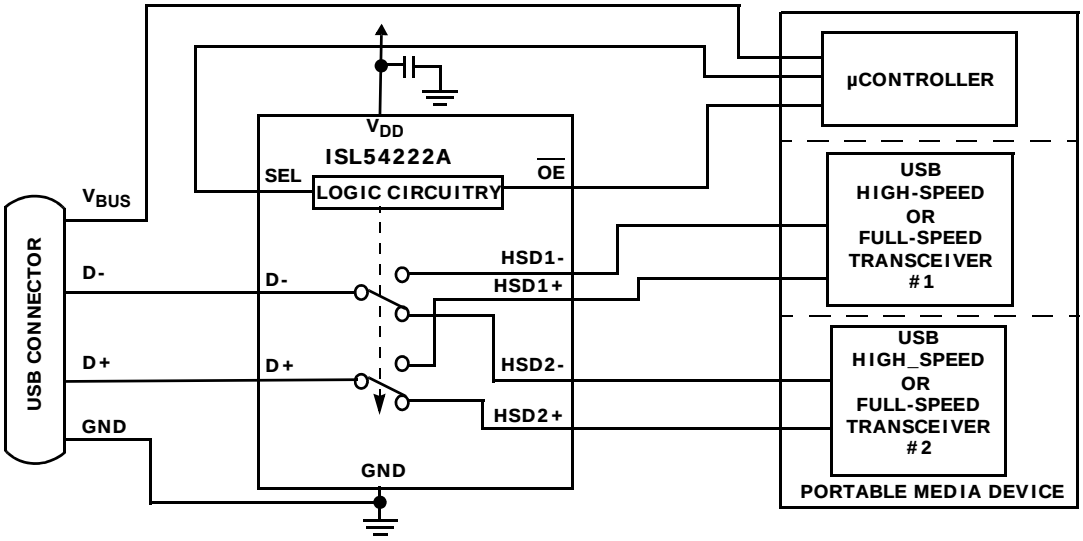
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 6B. TEST CIRCUIT

FIGURE 6. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54222A device is a dual single pole/double throw (SPDT) analog switch configured as a DPDT that operates from a single DC power supply in the range of 1.8V to 3.3V.

It was designed to function as a dual 2-to-1 multiplexer to select between two USB high-speed differential data signals in portable battery powered products. It is offered in MSOP, TDFN and small µTQFN packages for use in MP3 players, cameras, PDAs, cell phones, and other personal media players.

The part consists of four 4.4Ω high-speed (HSx) switches. These switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion. They can also swing from 0V to 3.3V to pass USB full speed (12Mbps) differential data signals with minimal distortion.

The device has an enable pin to open all switches and put the part in a low power down state. It can be used to facilitate proper bus disconnect and connection when switching between the USB sources.

The ISL54222A was designed for MP3 players, cameras, cell phones, and other personal media player applications that have multiple high-speed or full-speed transceivers sections and need to multiplex between these USB sources to a single USB host (computer). A typical application block diagram of this functionality is shown on page 9.

A detailed description of the HS switches is provided in the following section.

High-Speed (HSx) Switches

The HSx switches (HSD1-, HSD1+, HSD2-, HSD2+) are bi-directional switches that can pass 0V to 3.3V signals. When powered with a 1.8V supply, these switches have a nominal r_{ON} of 5.7Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.60Ω. The r_{ON} matching between the HSD1 and HSD2 switches over this signal range is only 0.072Ω, ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. With supply of 1.8V, the switch resistance with the signal level at the rail is nominally 12Ω. See Figures 7, 8, 9, 10, 11 and 12 in the “Typical Performance Curves” beginning on page 11.

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals in the range of 0V to 400mV. They have low capacitance (4.2pF) and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high-speed signal quality specifications. See Figure 13 in the “Typical Performance Curves” on page 12 for USB High-speed Eye Pattern taken with switches in the differential signal paths.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figures 14 and 15 in the “Typical Performance Curves” on page 13 for USB Full-speed Eye Patterns taken with switches in the differential signal paths.

The maximum normal operating signal range for the HSx switches is from 0V to 3.3V. The signal voltage should not be allowed to exceed 3.3V or go below ground by more than -0.3V for normal operation.

However, in the event that the USB 5.25V V_{BUS} voltage gets shorted to one or both of the D-/D+ pins, the ISL54222A has special fault protection circuitry to prevent damage to the ISL54222A part. The fault circuitry allows the signal pins (D-, D+, HSD1-, HSD1+, HSD2-, HSD2+) to be driven up to 5.5V while the V_{DD} supply voltage is in the range of 0V to 3.3V. In this condition, the part draws < 300µA of I_{DD} current and causes no stress to the IC. In addition, when V_{DD} is at 0V (ground) all switches are OFF and the fault voltage is isolated from the other side of the switch. When V_{DD} is

in the range of 1.8V to 3.3V, the fault voltage will pass through to the output of an active switch channel. During the fault condition normal operation is not guaranteed until the fault is removed. See the following “USB 2.0 VBUS Short Requirements” on page 10.

The HS1 channel switches are active (turned ON) whenever the SEL voltage is logic”0”(Low) and the $\overline{OE}$ voltage is logic”0”(Low).

The HS2 channel switches are active (turned ON) whenever the SEL voltage is logic “1” (High) and the $\overline{OE}$ voltage is logic “0” (Low).

ISL54222A Operation

The following will discuss using the ISL54222A shown in the “Application Block Diagram” on page 9.

POWER

The power supply connected at the VDD pin provides the DC bias voltage required by the ISL54222A part for proper operation. The ISL54222A can be operated with a V_{DD} voltage in the range of 1.8V to 3.3V.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

LOGIC CONTROL

The state of the ISL54222A device is determined by the voltage at the SEL pin and the $\overline{OE}$ pin. SEL is only active when the $\overline{OE}$ pin is logic “0” (Low). Refer to “Truth Table” on page 2.

The ISL54222A logic pins are designed to minimize current consumption when the logic control voltage is lower than the V_{DD} supply voltage. With V_{DD} = 3.3V and logic pins at 1.4V, the part typically draws only 6.6µA. With V_{DD} = 1.8V and logic pins at 1.4V, the part typically draws only 0.2µA. Driving the logic pins to the V_{DD} supply rail minimizes power consumption. The logic pins must be driven High or Low and must not float.

LOGIC CONTROL VOLTAGE LEVELS

With V_{DD} supply voltage in the range of 1.8V to 3.3V the logic levels are:

$\overline{OE}$ = Logic “0” (Low) when $V_{\overline{OE}} \leq 0.5V$
$\overline{OE}$ = Logic “1” (High) when $V_{\overline{OE}} \geq 1.4V$
SEL = Logic “0” (Low) when $V_{SEL} \leq 0.5V$
SEL = Logic “1” (High) when $V_{SEL} \geq 1.4V$

HSD1 USB CHANNEL

If the SEL pin = Logic “0” and the $\overline{OE}$ pin = Logic “0”, high-speed Channel 1 will be ON. The HSD1- and HSD1+ switches are ON and the HSD2- and HSD2+ switches are OFF (high impedance).

When a computer or USB hub is plugged into the common USB connector and Channel 1 is active, a link will be established between the USB 1 transceiver section of the media player and the computer. The device transceiver 1 will be able to transmit and receive data from the computer.

HSD2 USB Channel

If the SEL pin = Logic “1” and the $\overline{OE}$ pin = Logic “0”, high-speed Channel 2 will be ON. The HSD2- and HSD2+ switches are ON and the HSD1- and HSD1+ switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common USB connector and the part has Channel 2 active, a link will be established between the USB 2 transceiver section of the media player and the computer. The device transceiver 2 will be able to transmit and receive data from the computer.

ALL SWITCHES OFF/LOW POWER MODE

If the SEL pin = Logic “0” or Logic “1” and the $\overline{OE}$ pin = Logic “1”, all of the switches will turn OFF (high impedance) and the part will be put in a low power mode. In this mode the part draws only 1.5µA (max) of current across the operating temperature range.

The all OFF state can be used to switch between the two USB sections of the media player. When disconnecting from one USB device to the other USB device, you can momentarily put the ISL54222A switch in the “all off” state in order to get the computer to disconnect from the one device so it can properly connect to the other USB device when that channel is turned ON.

USB 2.0 V_{BUS} Short Requirements

The USB 2.0 specification in chapter 7, section 7.1.1 states a USB device must be able to withstand a V_{BUS} short to the D+ or D- signal lines when the device is either powered off or powered on for at least 24 hours. The ISL54222A part has special fault protection circuitry to meet these short circuit requirements.

The fault protection circuitry allows the signal pins (D-, D+, HSD1-, HSD1+, HSD2-, HSD2+) to be driven up to 5.5V while the V_{DD} supply voltage is in the range of 0V to 3.3V. In this overvoltage condition, the part draws < 300µA of I_{DD} current and causes no stress or damage to the IC.

In addition, when V_{DD} is at 0V (ground), all switches are OFF and the shorted V_{BUS} voltage is isolated from the other side of the switch.

When V_{DD} is in the range of 1.8V to 3.3V, the shorted V_{BUS} voltage will pass through to the output of an active (turned ON) switch channel but not through a turned OFF channel. Any components connected on the active channel must be able to withstand the overvoltage condition.

Note: During the fault condition, normal operation of the USB channel is not guaranteed until the fault condition is removed.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

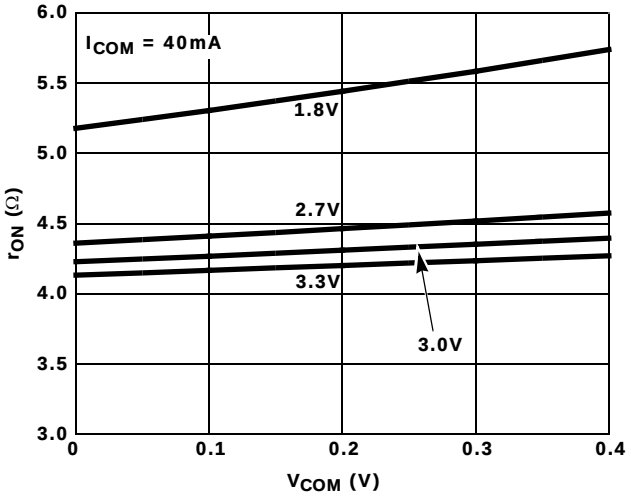


FIGURE 7. ON-RESIDTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

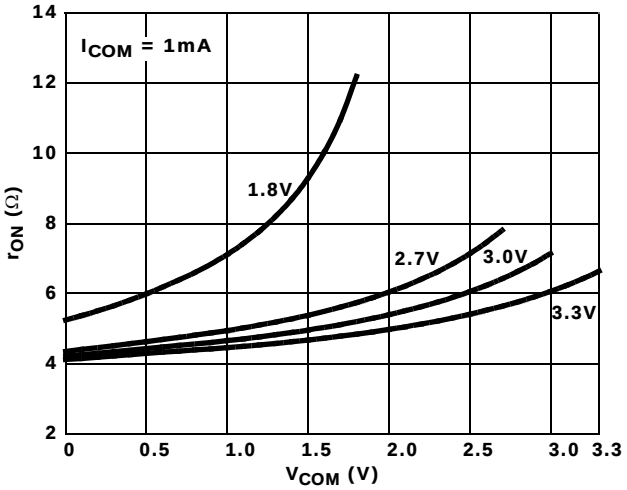


FIGURE 8. ON-RESIDTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

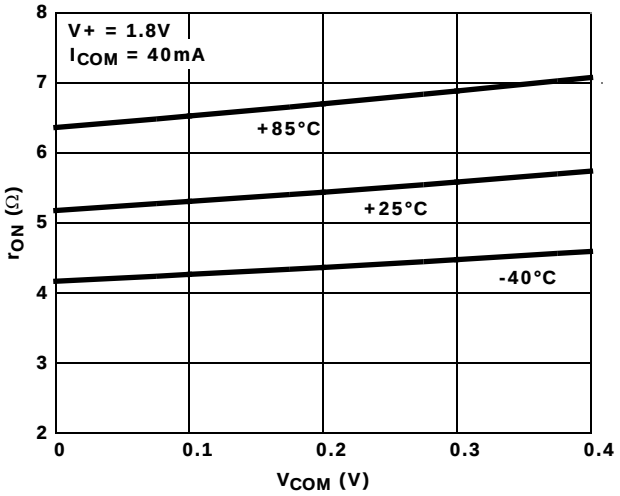


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

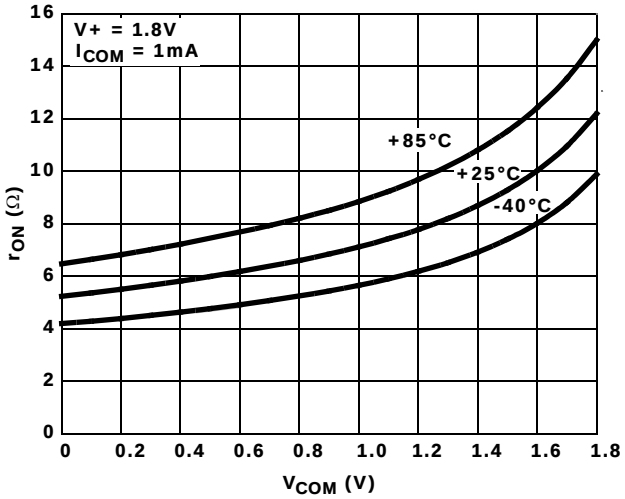


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

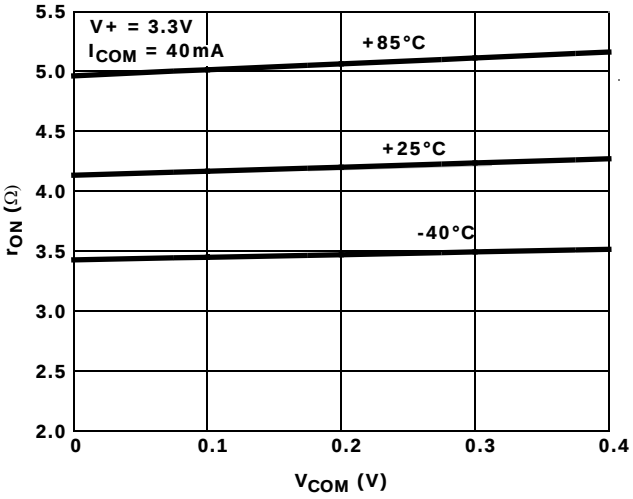


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

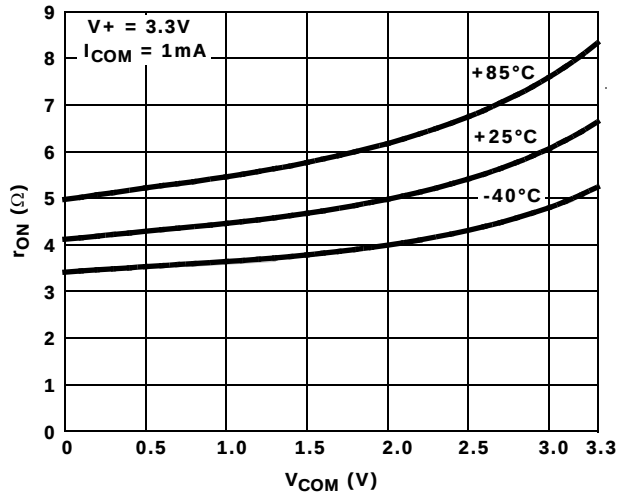


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

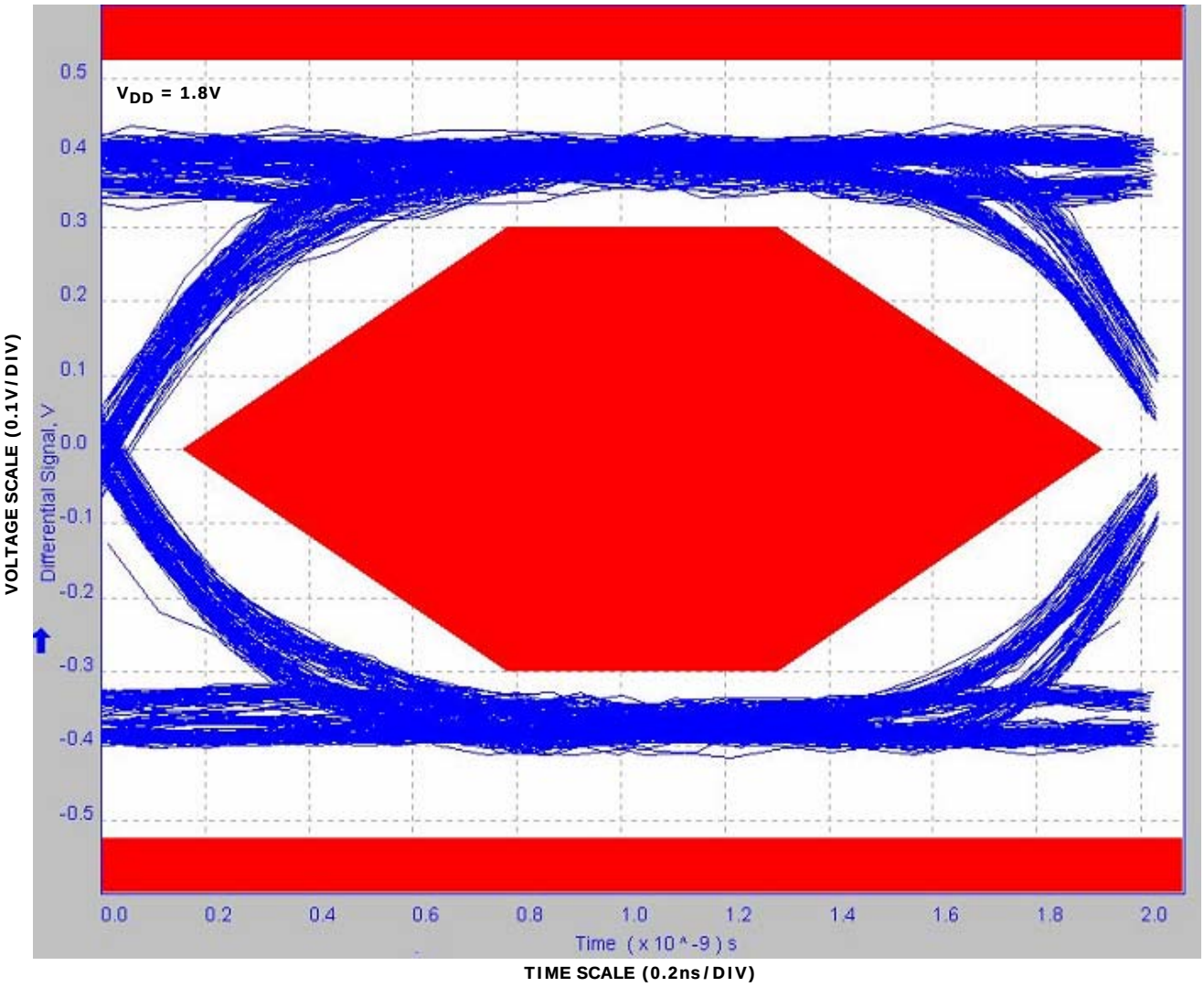


FIGURE 13. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

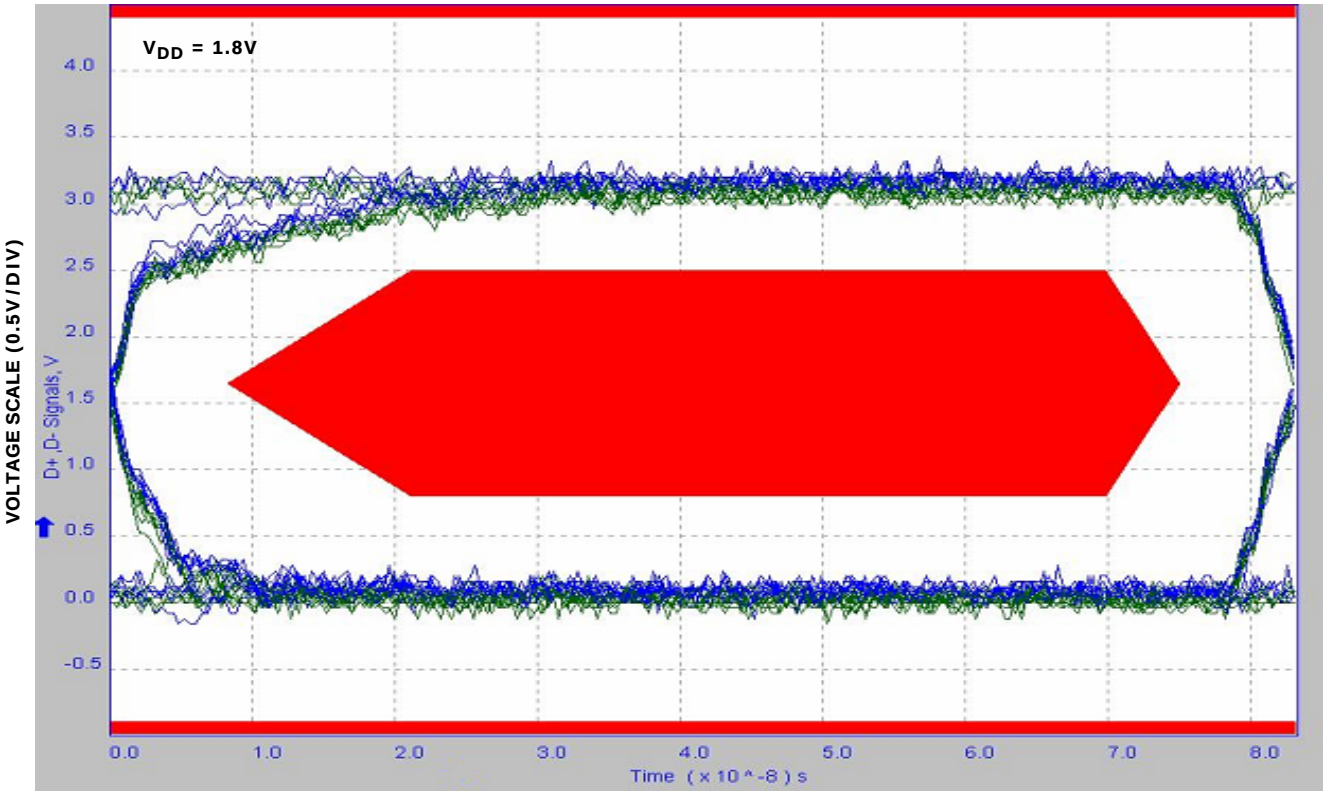


FIGURE 14. EYE PATTERN: 12Mbps WITH USB SWITCHES IN THE SIGNAL PATH

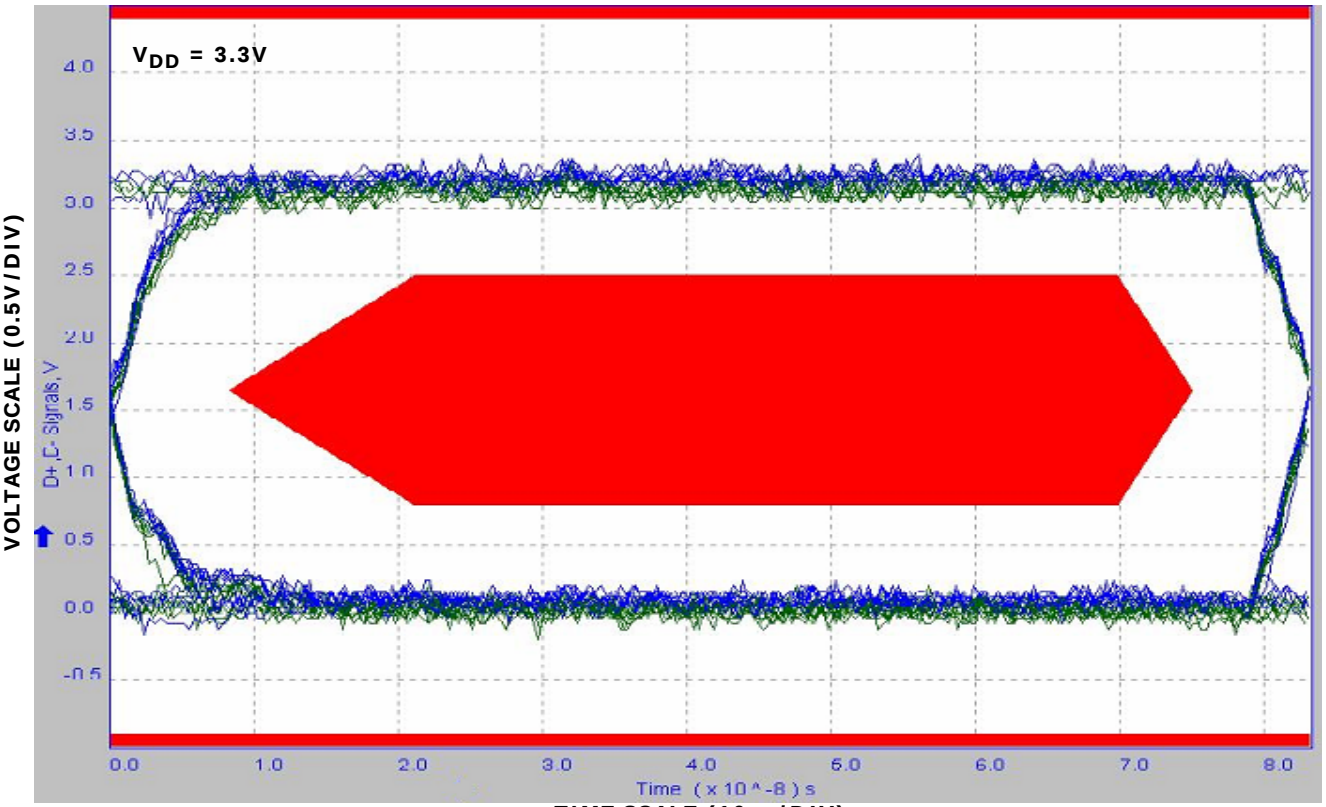


FIGURE 15. EYE PATTERN: 12Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

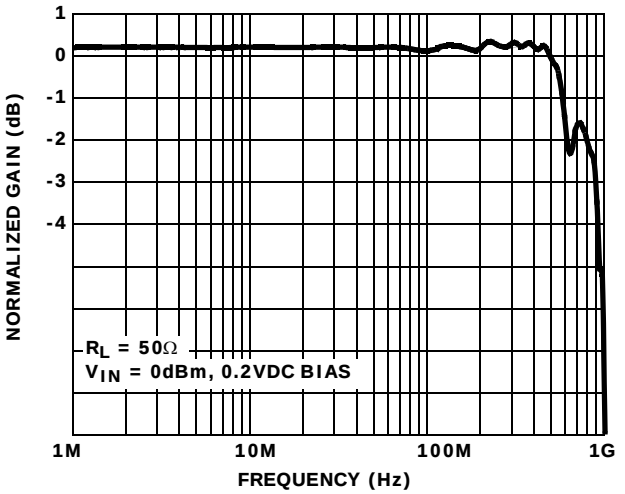


FIGURE 16. FREQUENCY RESPONSE

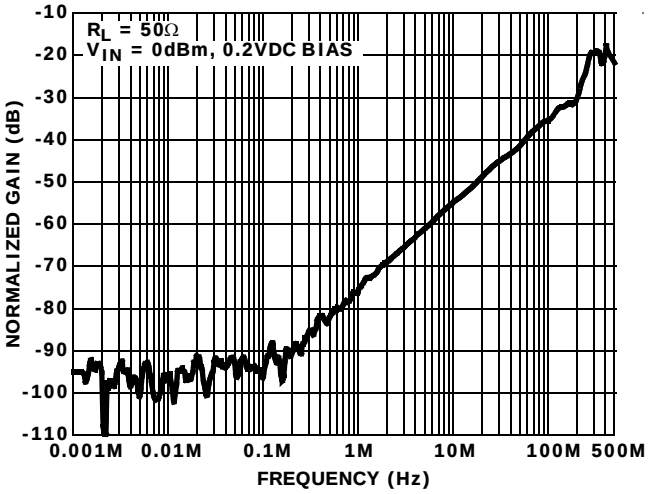


FIGURE 17. OFF-ISOLATION

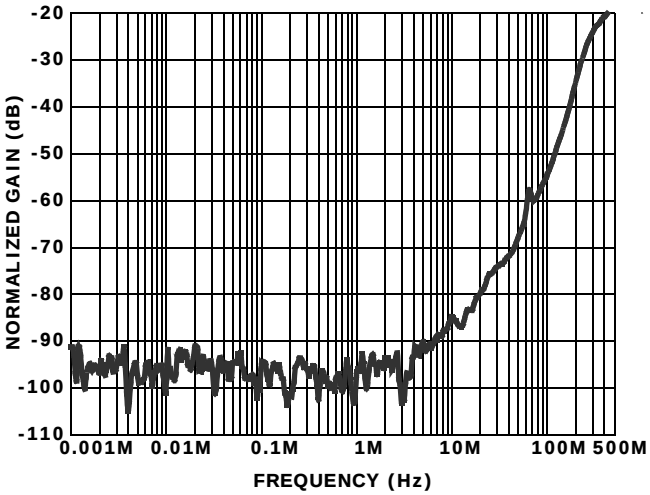


FIGURE 18. CROSSTALK

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

325

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
2/4/10	FN6902.1	Updated to new Intersil data sheet format. Page 1 Updated with Related Literature and Marketing graphics. Added to Pin Configurations 10 Ld MSOP. Updated Pin Description Table by adding columns reflecting package option, pin names and Functions. Updated ordering information by numbering all notes and adding MSL note, now a new standard. Added Latchup to Abs Max Ratings Added to Thermal Resistance 10 Ld 1.8x1.4 uTQFN Tja 160 and Tjc of 105 with corresponding notes Added to Thermal Resistance Tjc of 100 and corresponding note for MSOP package Changed Tja for 10 Ld 2.1x1.6 uTQFN from 155 to 160. Added Tjc and corresponding note. Updated package outline drawings L10.1.8x1.4A and L10.3x3A to most recent revisions. Changes to L10.1.8x1.4A were to add solder footprint. Changes to L10.3x3A were to change tolerance in top view from 0.15 to 0.10. Page 1 in Features section changed "Low On Capacitance 6.7pF" to "Low On Capacitance @ 240MHz 4.2pF" Page 1 in Features section changed "Low On Resistance 5.7ohms" to "Low On Resistance @ 1.8V 5.7ohms" Added in Features section "Low On Resistance @ VDD = 3V 4.4ohms" Electrical Specification table: added COM On Capacitance at 240MHz
5/13/09	FN6902.0	Initial Release.

Products

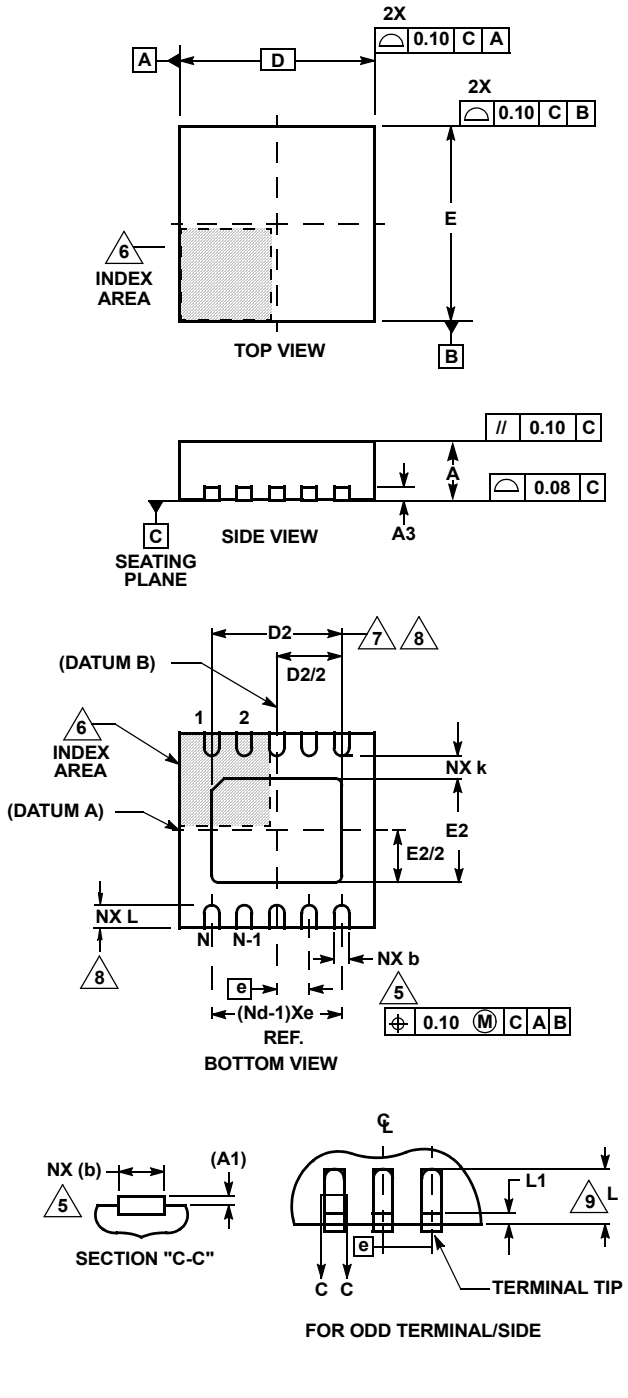
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54222A

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

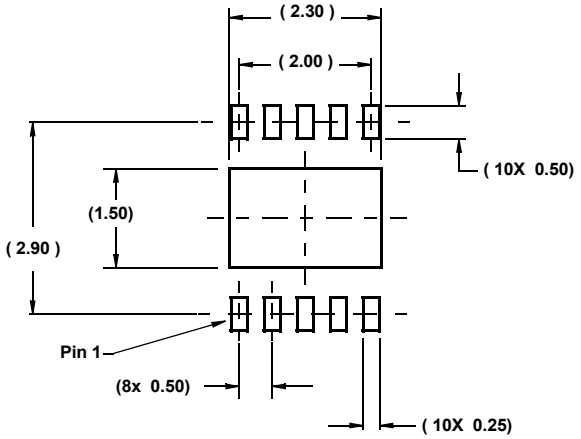
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 4 8/09

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.



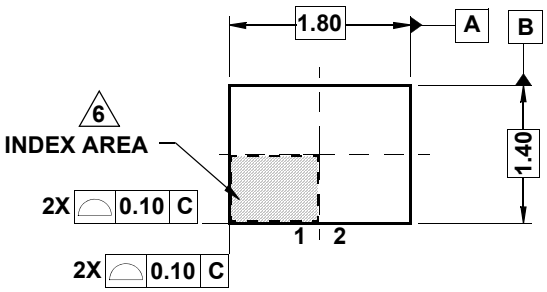
TYPICAL RECOMMENDED LAND PATTERN

Package Outline Drawing

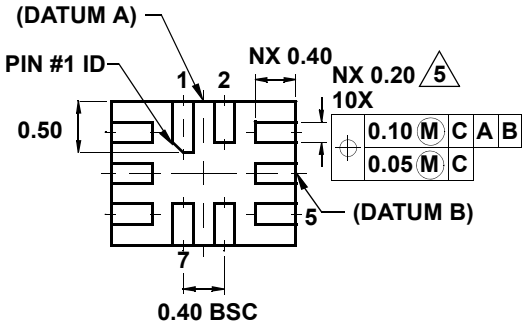
L10.1.8x1.4A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

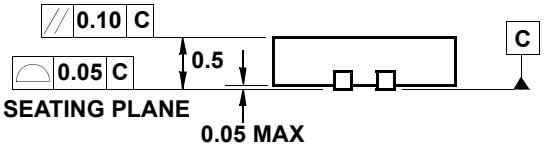
Rev 4, 9/09



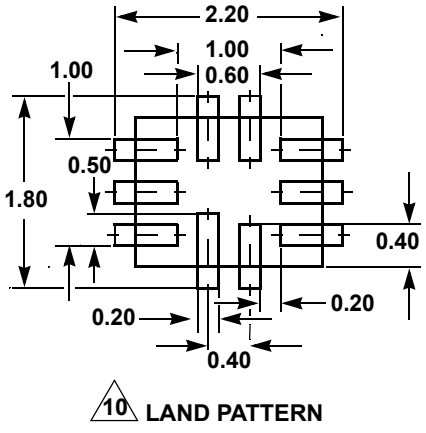
TOP VIEW



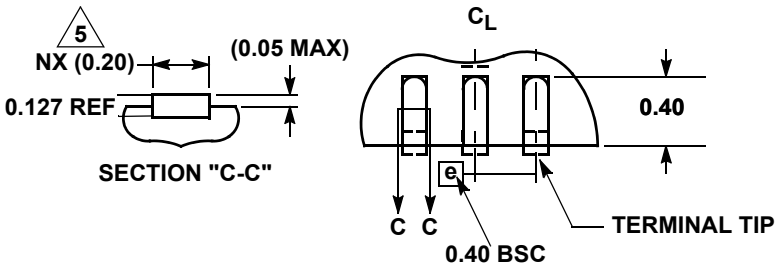
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

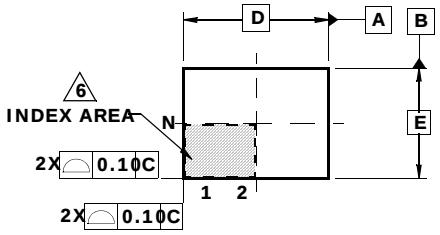


DETAIL "X"

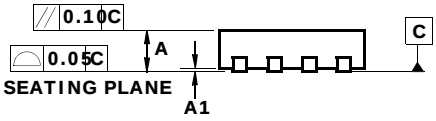
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals. Total 10 leads.
3. Nd and Ne refer to the number of terminals on D (4) and E (6) side, respectively.
4. All dimensions are in millimeters. Tolerances ±0.05mm unless otherwise noted. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

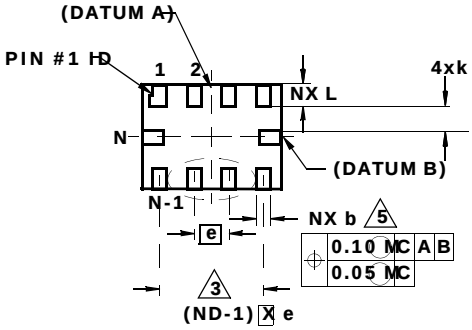
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



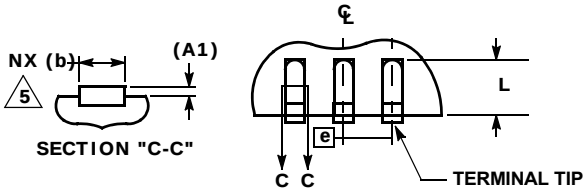
TOP VIEW



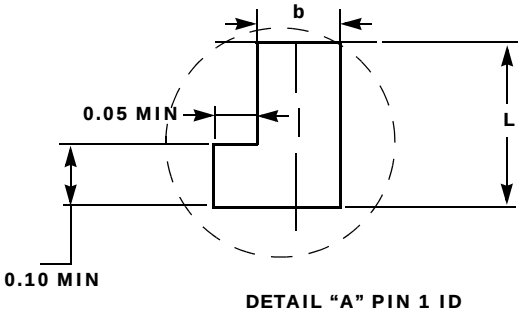
SIDE VIEW



BOTTOM VIEW



FOR ODD TERMINAL/SIDE



DETAIL "A" PIN 1 ID

L10.2.1x1.6A

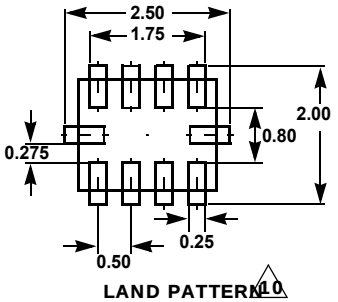
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMI-NAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		10		2
Nd		4		3
Ne		1		3
θ	0	-	12	4

Rev. 3 6/06

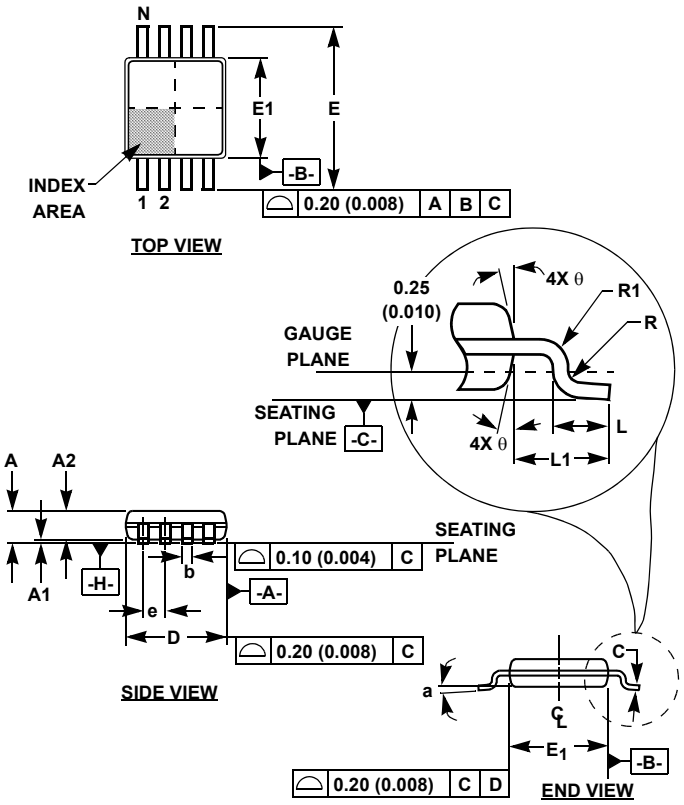
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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