ISL6314

Single-Phase Buck PWM Controller with Integrated MOSFET Drivers for Intel VR11 and AMD Applications

FN6455
Rev 2.00
Oct 8, 2009

The ISL6314 single-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. This controller IC maintains the same features as the multi-phase product family, but reduces the output to a single-phase, for lower current systems. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

One outstanding feature of this controller IC is its multi-processor compatibility, allowing it to work with both Intel and AMD microprocessors. Included are programmable VID codes for Intel VR11 as well as AMD 5-bit and 6-bit DAC tables. A circuit is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

Another unique feature of the ISL6314 is the addition of a circuit that allows optimizing compensation to be added for flatter load transient response and well controlled dynamic VID response.

The ISL6314 also includes advanced control loop features for optimal transient response to load apply and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming. Active Pulse Positioning (APP) and Adaptive Phase Alignment (APA) are two other unique features, allowing for quicker initial response to high di/dt load transients; the number of output bulk capacitors can be reduced, helping to reduce cost.

Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Furthermore, the ISL6314 includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

Features

- Integrated-driver Single-Phase Power Conversion
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over-Temperature
  - Adjustable Reference-Voltage Offset
- Optimal Transient Response
  - Adaptive Phase Alignment (APA)
  - Active Pulse Positioning (APP) Modulation
- Fully Differential, Continuous DCR Current Sensing
  - Accurate Load Line Programming
- Variable Gate Drive Bias: 5V to 12V
- Multi-Processor Compatible
  - Intel VR11 Mode of Operation
  - AMD Mode of Operation
- Microprocessor Voltage Identification Inputs
  - 8-Bit DAC
  - Selectable Between Intel VR11, AMD 5-bit, and AMD 6-bit DAC Tables
  - Dynamic VID Technology
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.0MHz
- Pb-Free (RoHS compliant)

Ordering Information

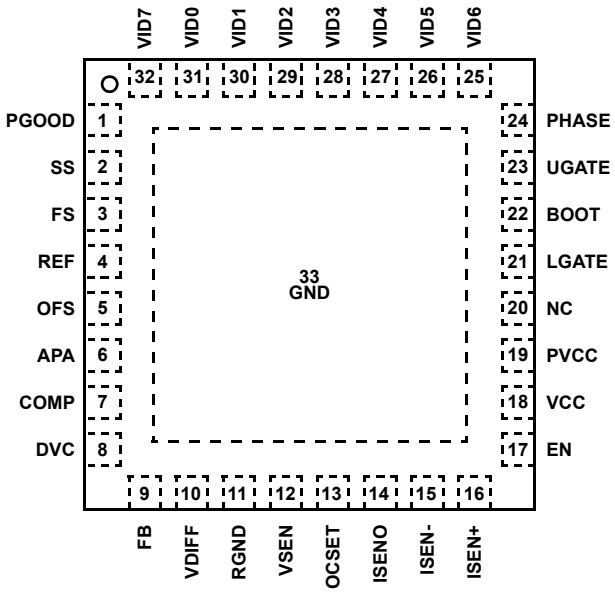
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6314CRZ*	ISL6314 CRZ	0 to +70	32 Ld 5x5 QFN	L32.5x5B
ISL6314IRZ*	ISL6314 IRZ	-40 to +85	32 Ld 5x5 QFN	L32.5x5B

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

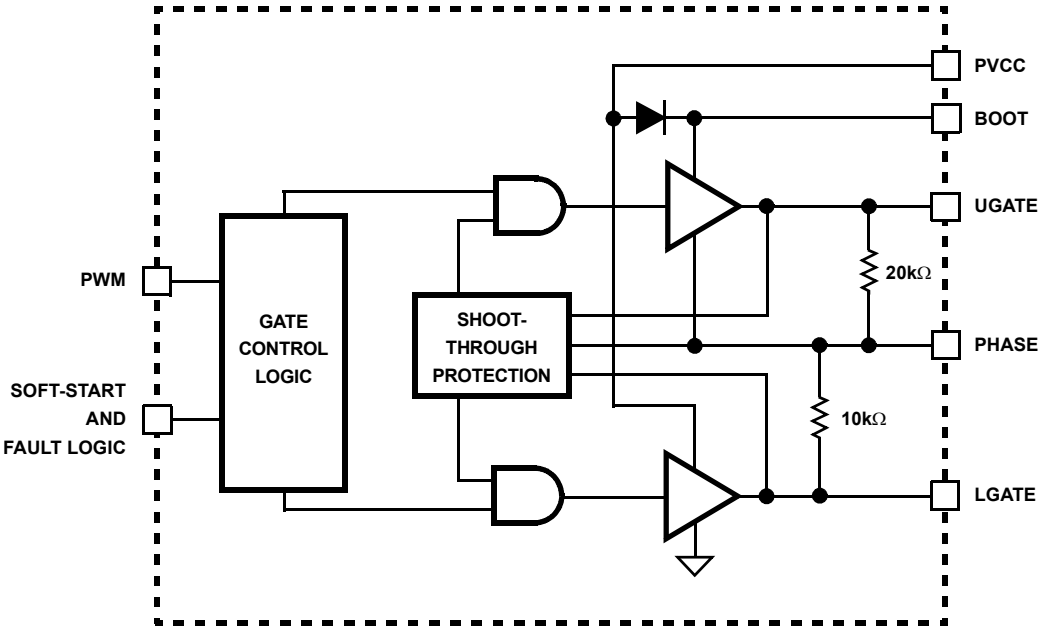
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

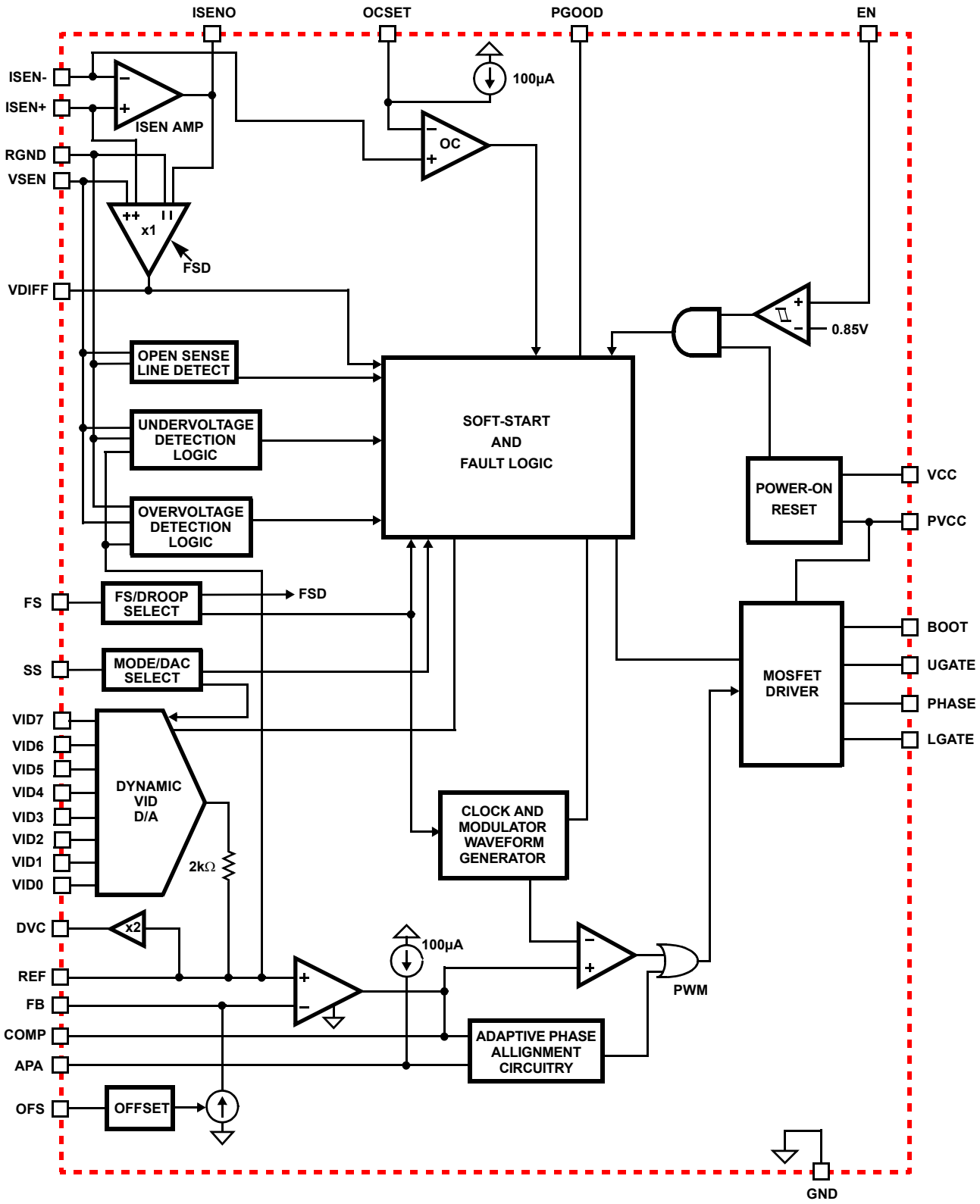
ISL6314
(32 LD QFN)
TOP VIEW



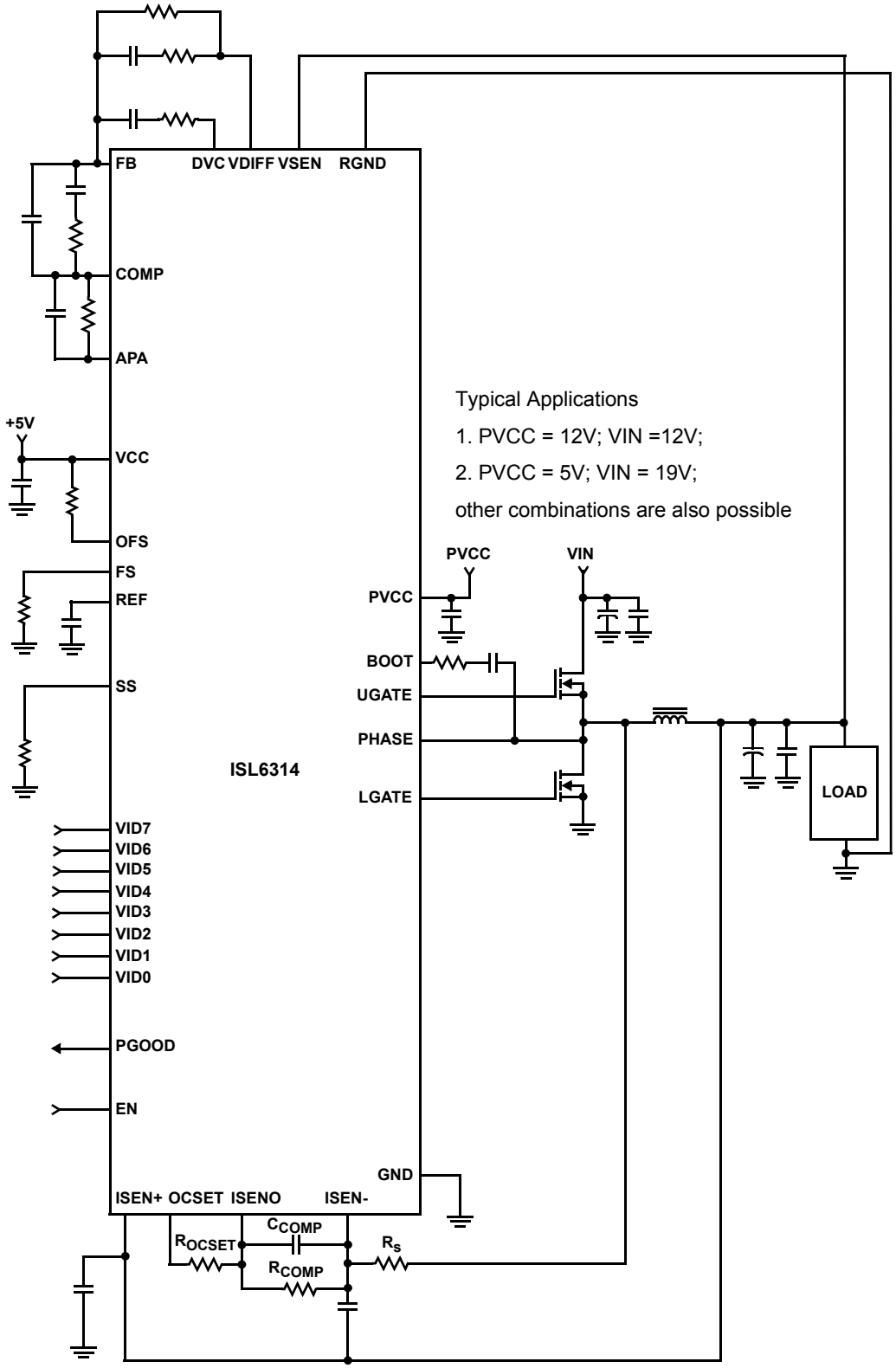
ISL6314 Integrated Driver Block Diagram



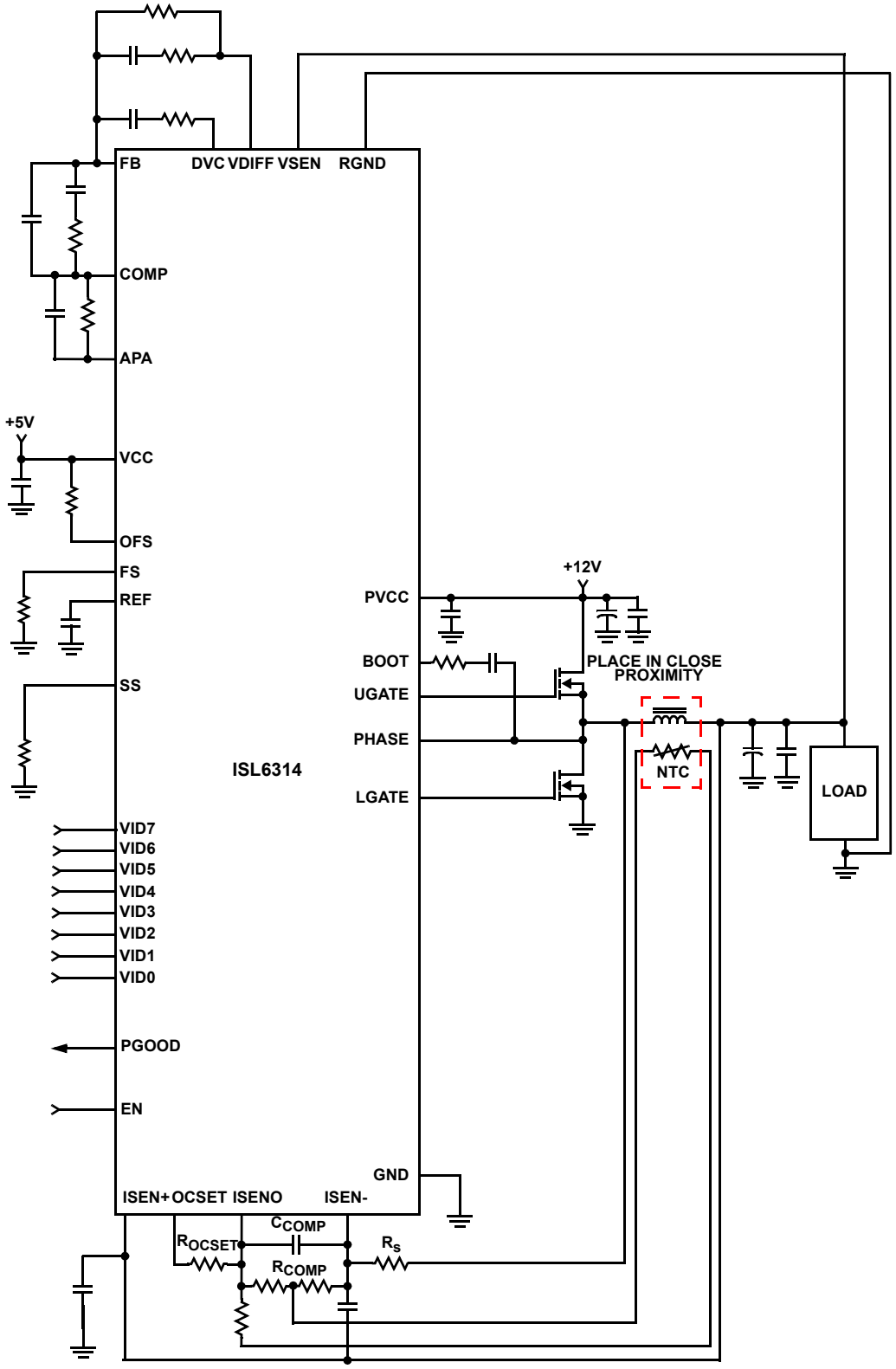
Block Diagram



Typical Application - ISL6314



Typical Application - ISL6314 with NTC Thermal Compensation



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
Absolute Boot Voltage, V_{BOOT} . . . . . GND - 0.3V to GND + 36V
Phase Voltage, V_{PHASE} . . . . . GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT-PHASE}$ = 5V)
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE} . . . . . GND - 0.3V to PVCC + 0.3V GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	32	3.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature
ISL6314CRZ . . . . . 0°C to +70°C
ISL6314IRZ . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLIES					
Input Bias Supply Current	I_{VCC}; V_{CC} = 5V; EN = high, not switching;	9	11.4	16	mA
Gate Drive Bias Current - PVCC Pin	I_{PVCC}; PVCC = 12V; EN = high, high, not switching	1	2	4	mA
V_{CC} POR (Power-On Reset) Threshold	V_{CC} rising	4.25	4.38	4.50	V
	V_{CC} falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC rising	4.25	4.38	4.50	V
	PVCC falling	3.75	3.88	4.00	V
PWM MODULATOR					
Oscillator Frequency Accuracy, f_{SW} (ISL6314CRZ)	R_T = 100kΩ (± 0.1%)	225	250	275	kHz
Oscillator Frequency Accuracy, f_{SW} (ISL6314IRZ)	R_T = 100kΩ (± 0.1%)	215	250	280	kHz
Adjustment Range of Switching Frequency	(Note 3)	0.08	-	1.0	MHz
Oscillator Ramp Amplitude, V_{P-P}	(Note 3)	-	1.50	-	V
CONTROL THRESHOLDS					
EN Rising Threshold		0.84	0.86	0.88	V
EN Hysteresis		-	110	-	mV
REFERENCE AND DAC					
System Accuracy (1.000V to 1.600V)		-0.5	-	0.5	%
System Accuracy (0.600V to 1.000V)		-1.0	-	1.0	%
System Accuracy (0.375V to 0.600V)		-2.0	-	2.0	%
VIDx Input Low Voltage (INTEL)	Pins VID0 to VID7	-	-	0.4	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIDx Input High Voltage (INTEL)	Pins VID0 to VID7	0.8	-	-	V
VIDx Input Low Voltage (AMD)	Pins VID0 to VID7	-	-	0.8	V
VIDx Input High Voltage (AMD)	Pins VID0 to VID7	1.4	-	-	V
VIDx Pull-Up Current (INTEL)	Pins VID0 to VID7; VIDx = 0V	-	-40	-	µA
VIDx Pull-Down Current (AMD)	Pins VID0 to VID7; VIDx = 0.5V	-	20	-	µA
PIN-ADJUSTABLE OFFSET					
OFS Sink Current Accuracy (Negative Offset)	R_{OFS} = 32.4kΩ from OFS to VCC	47.0	49.4	53.0	µA
OFS Source Current Accuracy (Positive Offset)	R_{OFS} = 6.04kΩ from OFS to GND	47.0	49.7	53.0	µA
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground, (Note 3)	-	96	-	dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10k to ground, (Note 3)	-	40	-	MHz
Slew Rate	C_L = 100pF, load = ±400µA, (Note 3)	-	20	-	V/µs
Maximum Output Voltage	Load = 1mA	3.90	4.20	-	V
Minimum Output Voltage	Load = -1mA	-	1.20	1.4	V
SOFT-START RAMP					
Soft-Start Ramp Rate	VR11, R_{SS} = 100kΩ	-	1.25	-	mV/µs
	AMD, R_{SS} = 100kΩ	-	1.25	-	mV/µs
Adjustment Range of Soft-Start Ramp Rate (Note 3)		0.156	-	6.25	mV/µs
OVERCURRENT PROTECTION					
OCSET Trip Current (ISL6314CRZ)		94	100	106	µA
OCSET Trip Current (ISL6314IRZ)		93	100	107	µA
OCSET Accuracy	OCSET and ISUM Difference	-5	0	5	mV
ISENO Offset		-1.7	0	1.7	mV
PROTECTION					
Undervoltage Threshold	VSEN falling	VDAC - 325	VDAC - 350mV	VDAC - 375	V
Undervoltage Hysteresis	VSEN rising	-	100	-	mV
Overvoltage Threshold During Soft-Start	VR11 and AMD	1.24	1.27	1.30	V
Overvoltage Threshold (Default)	VR11, VSEN rising	VDAC + 150mV	VDAC + 175mV	VDAC + 200mV	V
	AMD, VSEN rising	VDAC + 200mV	VDAC + 225mV	VDAC + 250mV	V
Overvoltage Hysteresis	VSEN falling	-	100	-	mV
PGOOD Output Sink Current	PGOOD = 0.4V	-	7.5	-	mA
OVER-TEMPERATURE SHUTDOWN (Note 3)					
Thermal Shutdown Setpoint		-	160	-	°C
Thermal Recovery Setpoint		-	100	-	°C

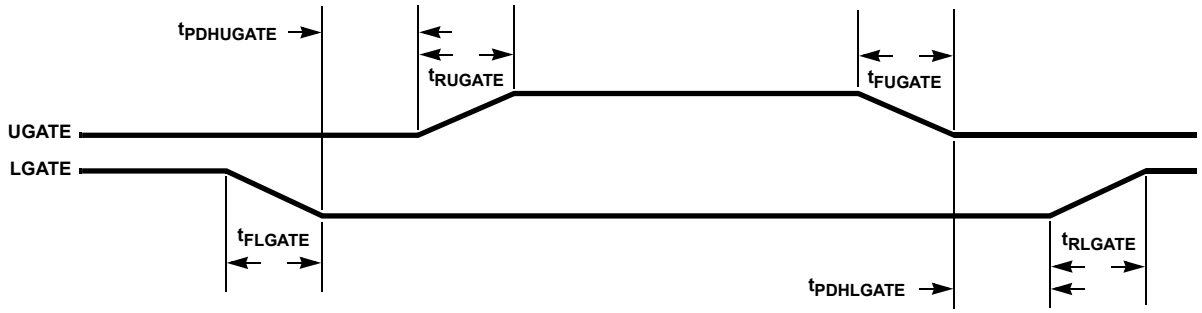
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING TIME (Note 3)					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 12V, 3nF load, 10% to 90%	-	26	-	ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 12V, 3nF load, 10% to 90%	-	18	-	ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%	-	12	-	ns
UGATE Turn-On Non-Overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF load, adaptive	-	10	-	ns
LGATE Turn-On Non-Overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF load, adaptive	-	10	-	ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA source current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA sink current	0.9	1.65	3.0	Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA source current	0.85	1.25	2.2	Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA sink current	0.60	0.80	1.35	Ω

NOTE:

3. Limits should be considered typical and are not production tested.

Timing Diagram



Functional Pin Description

VCC (Pin 18)

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1µF ceramic capacitor.

PVCC (Pin 19)

This pin is the power supply pin for the channel MOSFET drivers, and can be connected to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple this pin with a quality 1.0µF ceramic capacitor.

GND (Pin 33 = Metal Pad)

GND is the bias and reference ground for the IC, connected to the metal pad under the IC.

EN (Pin 17)

This pin is a threshold-sensitive (approximately 0.85V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

FS (Pin 3)

A resistor, R_T, tied to this pin sets the channel switching frequency of the controller. Refer to Equation 42 for proper resistor calculation.

The FS pin also controls whether the droop voltage (as described under pins ISENO, ISEN-, ISEN+) is added to the differential remote-sense amplifier's output (VDIFF). Tying the R_T resistor to ground connects droop voltage, allowing the converter to incorporate output voltage droop proportional to the output current. Tying the R_T resistor to VCC disconnects the droop voltage.

VID0, VID1, VID2, VID3, VID4, VID5, VID6, and VID7 (Pins 31, 30, 29, 28, 27, 26, 25, 32)

These are the inputs for the internal DAC that provide the reference voltage for output regulation. These pins respond to TTL logic thresholds. These pins are internally pulled high, to approximately 1.2V, by 40µA internal current sources for Intel modes of operation, and pulled low by 20µA internal current sources for AMD modes of operation. The internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

VSEN (Pin 12)

This pin senses the microprocessor's CORE voltage. Connect this pin to the CORE voltage sense pin or point of the microprocessor.

RGND (Pin 11)

This pin senses the local ground voltage of the microprocessor. Connect this pin to the Ground sense pin or point of the microprocessor.

FB and COMP (Pins 9, 7)

These pins are the internal error amplifier inverting input and output respectively. The FB pin, COMP pin, and the VDIFF pins are tied together through external R-C networks to compensate the regulator.

DVC (Pin 8)

A series resistor and capacitor can be connected from the DVC pin to the FB pin to compensate and smooth dynamic VID transitions.

OCSET (Pin 13)

This is the overcurrent set pin. Placing a resistor from OCSET pin to ISENO allows a 100µA current to flow out of this pin, producing a voltage reference. Internal circuitry compares the voltage at OCSET to the voltage at ISEN-, and if ISEN- ever exceeds OCSET, the overcurrent protection activates.

APA (Pin 6)

This is the Adaptive Phase Alignment set pin. A 100µA current flows out the APA pin and by tying a resistor from this pin to COMP the trip level for the Adaptive Phase Alignment circuitry can be set.

REF (Pin 4)

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 2kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during soft-start and Dynamic VID transitions. This pin can also be returned to RGND if desired.

NC (Pin 20)

This pin is presently NC (No Connect), but is reserved for a future function.

OFS (Pin 5)

The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity is selected by connecting the resistor to GND (for positive offset) or to VCC (for negative offset). For no offset, the OFS pin should be left unconnected.

UGATE (Pin 23)

Connect this pin to the corresponding upper MOSFET gate. This pin is used to control the upper MOSFET and is monitored for shoot-through prevention purposes.

BOOT (Pin 22)

This pin provides the bias voltage for the upper MOSFET drive. Connect this pin to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pin provides the necessary bootstrap charge.

PHASE (Pin 24)

Connect this pin to the source of the upper MOSFET. This pin is the return path for the upper MOSFET drive.

LGATE (Pin 21)

This pin is used to control the lower MOSFET. Connect this pin to the lower MOSFET gate.

SS (Pin 2)

A resistor, R_{SS}, placed from SS to VCC or GND will set the soft-start ramp slope. Refer to Equations 16 and 17 for proper resistor calculation.

The state of the SS pin also selects which of the available DAC tables will be used to decode the VID inputs and puts the controller into the corresponding mode of operation. For Intel VR11 mode of operation the R_{SS} resistor should be tied to GND. AMD compliance is selected if the R_{SS} resistor is tied to VCC (once in AMD mode, the VID7 bit selects 5-bit DAC if set to a logic high, or 6-bit DAC if set to a logic low).

PGOOD (Pin 1)

For Intel mode of operation, PGOOD indicates whether VSEN is within specified overvoltage and undervoltage limits after a fixed delay from the end of soft-start. If VSEN exceeds these limits, or if an overcurrent event occurs, or if the part is disabled, PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

For AMD modes of operation, PGOOD will always be high as long as VSEN is within the specified undervoltage/overvoltage window and soft-start has ended. PGOOD only goes low if VSEN is outside this window.

ISENO, ISEN-, and ISEN+ (Pins 14, 15, 16)

ISEN-, ISEN+, and ISENO are the DCR current sense amplifier's negative input, positive input, and output respectively. For accurate DCR current sensing, connect a resistor from the phase node to ISEN- and connect ISEN+ to the output inductor, roughly VOUT. A parallel R-C feedback circuit connected between ISEN- and ISENO will then create a voltage from ISEN+ to ISENO proportional to the voltage drop across the inductor DCR. This voltage is referred to as the droop voltage and is added to the differential remote-sense amplifier's output.

An optional 0.001µF to 0.01µF ceramic capacitor can be placed from the ISEN+ pin to the ISEN- pin to help reduce common mode noise that might be introduced by the layout.

VDIFF (Pin 10)

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND (VOUT) added to the difference between ISEN+ and ISENO (droop). VDIFF therefore represents the VOUT voltage plus the droop voltage. The state of the FS pin determines whether the droop voltage is added or not.

Operation

Power Conversion

The ISL6314 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The "Block Diagram" on page 3 provides a top level view of the single-phase power conversion using the ISL6314 controller.

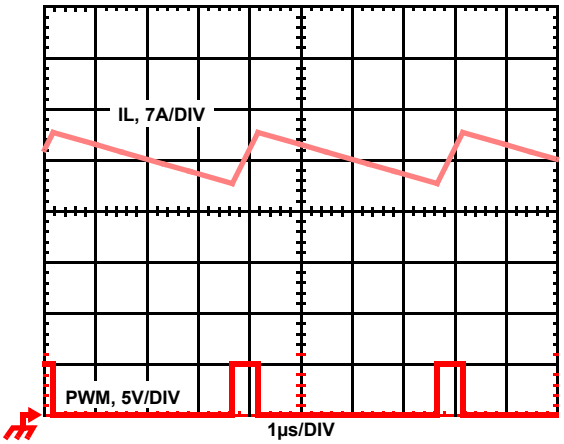


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 1-PHASE CONVERTER

Output Ripple

Figure 1 illustrates the output ripple. The PWM current forms the AC ripple current and the DC load current. The peak-to-peak current about 7A, and the DC components of the inductor current feeds the load.

To understand the ripple current amplitude, examine Equation 1 representing a single channel peak-to-peak inductor current.

$$I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors. Equation 2 shows the approximation for the output voltage ripple.

$$V_{P\text{-}P} = I_{P\text{-}P} \cdot ESR \quad \text{(EQ. 2)}$$

Adaptive Phase Alignment (APA)

To improve the transient response, the ISL6314 implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on the channel during large current step transient events.

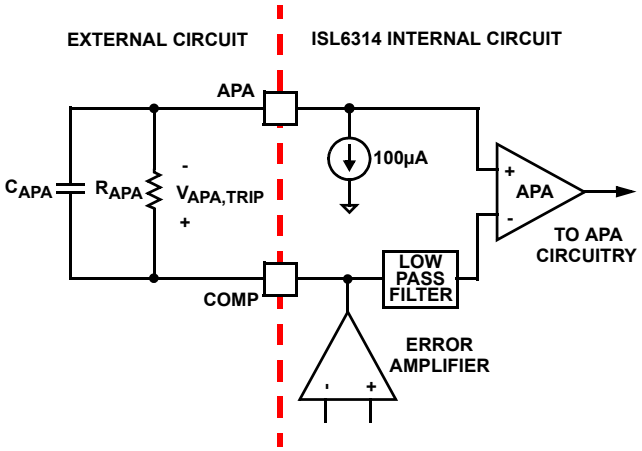


FIGURE 2. ADAPTIVE PHASE ALIGNMENT DETECTION

As Figure 2 shows, the APA circuitry works by monitoring the voltage on the APA pin and comparing it to a filtered copy of the voltage on the COMP pin. The voltage on the APA pin is a copy of the COMP pin voltage that has been negatively offset. If the APA pin exceeds the filtered COMP pin voltage an APA event occurs and the channel is forced on.

The APA trip level is the amount of DC offset between the COMP pin and the APA pin. This is the voltage excursion that the APA and COMP pin must have during a transient event to activate the Adaptive Phase Alignment circuitry. This APA trip level is set through a resistor, R_{APA}, that connects from the APA pin to the COMP pin. A 100µA current flows across R_{APA} into the APA pin to set the APA trip level as described in Equation 3. An APA trip level of 500mV is recommended for most applications. A 1000pF capacitor, C_{APA}, should also be placed across the R_{APA} resistor to help with noise immunity.

$$V_{APA,\,TRIP} = R_{APA} \cdot 100 \times 10^{-6} \qquad \text{(EQ. 3)}$$

Active Pulse Positioning (APP) Modulated PWM Operation

The ISL6314 uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel's driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor connected to the FS pin. The advantage of Intersil's proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because is allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, as illustrated in Figure 3. At the beginning of each PWM time interval, this V_{COMP} signal is compared to the internal modulator waveform. As long as the V_{COMP} voltage is lower then the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the V_{COMP} voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the V_{COMP} voltage crosses the modulator ramp again. When this occurs, the PWM signal will transition low again.

During each PWM time interval, the PWM signal can only transition high once. Once PWM transitions high, it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

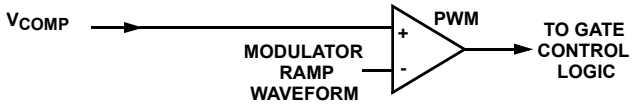


FIGURE 3. CHANNEL PWM FUNCTION

Output Voltage Setting

The ISL6314 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the logic signals into one of the discrete voltages shown in Tables 2, 3 or 4. In the Intel VR11 mode of operation, each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA), which decreases to 0A as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. In AMD modes of operation, the VID pins are pulled low by a weak 20µA current source. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6314 accommodates three different DAC ranges: Intel VR11, AMD K8/K9 5-bit, and AMD 6-bit. The state of the SS and VID7 pins decide which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

TABLE 1. ISL6314 DAC SELECT AND FUNCTION TABLE

DAC VERSION	SS PIN	VID7 PIN
INTEL VR11	R_{SS} resistor tied to GND	-
AMD 5-BIT	R_{SS} resistor tied to VCC	high
AMD 6-BIT	R_{SS} resistor tied to VCC	low
TIE RESISTOR to VCC	**OPEN**	**TIE RESISTOR to GND**
R_{SS}: AMD Tables	-	R_{SS}: Intel Table
R_{OFS}: Negative	No Offset	R_{OFS}: Positive
R_T: No Droop	-	R_T: Droop

TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000

TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000

TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000

TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000

TABLE 2. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

TABLE 3. AMD 5-BIT VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825

TABLE 3. AMD 5-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 4. AMD 6-BIT VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000

TABLE 4. AMD 6-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000

TABLE 4. AMD 6-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Voltage Regulation

In order to regulate the output voltage to a specified level, the ISL6314 uses the integrating compensation network shown in Figure 4. This compensation network insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6314 to include the combined tolerances of each of these elements.

The ISL6314 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The droop voltage, V_{DROOP}, also feeds into the remote-sense amplifier. The remote-sense output, V_{DIFF}, is therefore equal to the sum of the output voltage, V_{OUT}, and the droop voltage. V_{DIFF} is connected to the inverting input of the error amplifier through an external resistor.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 4)}$$

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signal. The PWM signal controls the timing of the Internal MOSFET drivers and regulates the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 4. The internal and external circuitry that controls voltage regulation is illustrated in Figure 4.

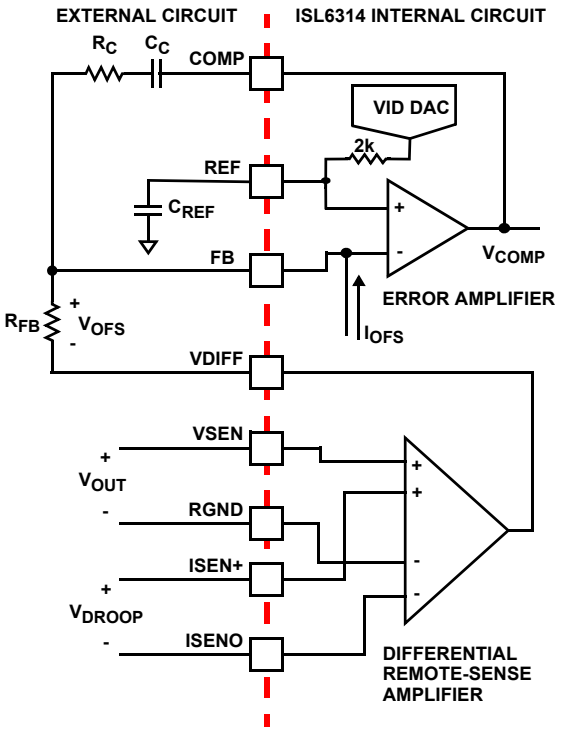


FIGURE 4. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely-controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

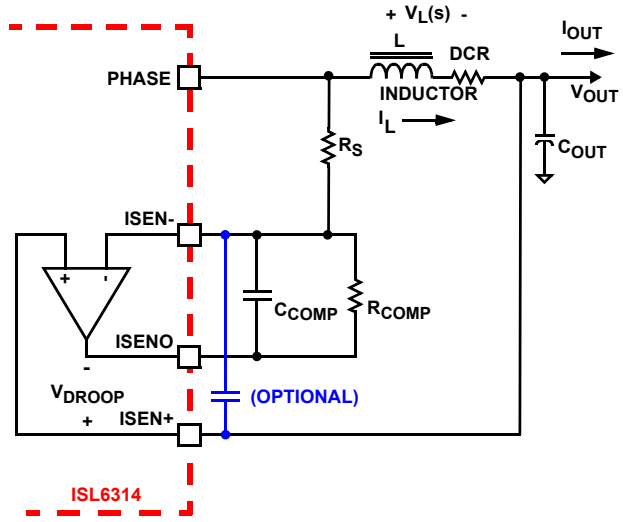


FIGURE 5. DCR SENSING CONFIGURATION

As shown in Figure 5, a voltage, V_{DROOP}, proportional to the current in the channel, I_{OUT}, feeds into the differential remote-sense amplifier. The resulting voltage at the output of the remote-sense amplifier is the sum of the output voltage and the droop voltage. Equation 5 shows that feeding this voltage into the compensation network causes the regulator to adjust the output voltage so that it’s equal to the reference voltage minus the droop voltage.

The droop voltage, V_{DROOP}, is created by sensing the current through the output inductors. This is accomplished by using a continuous DCR current sensing method.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 5. The channel current, I_L, flowing through the inductor, passes through the DCR. Equation 5 shows the S-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

The inductor DCR is important because the voltage dropped across it is proportional to the channel current. By using a simple R-C network and a current sense amplifier, as shown in Figure 5, the voltage drop across the inductor’s DCR can be extracted. The output of the current sense amplifier, V_{DROOP}, can be shown to be proportional to the channel current I_L, shown in Equation 6.

$$V_{DROOP}(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_{COMP} \cdot C_{COMP} + 1)} \cdot \frac{R_{COMP}}{R_S} \cdot (I_L) \cdot DCR \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the R-C time constant matches the inductor L/DCR time constant, then V_{DROOP} is equal to the voltage drop across the DCR, multiplied by a gain. As Equation 7 shows, V_{DROOP} is therefore proportional to the total output current, I_{OUT}.

$$V_{DROOP} = \frac{R_{COMP}}{R_S} \cdot I_{OUT} \cdot DCR \quad \text{(EQ. 7)}$$

By simply adjusting the value of R_S, the load line can be set to any level, giving the converter the right amount of droop at all load currents. It may also be necessary to compensate for any changes in DCR due to temperature. These changes cause the load line to be skewed, and cause the R-C time constant to not match the L/DCR time constant. If this becomes a problem a simple negative temperature coefficient resistor network can be used in the place of R_{COMP} to compensate for the rise in DCR due to temperature.

Note: An optional 10nF ceramic capacitor from the ISEN+ pin to the ISEN- pin is recommended to help reduce any noise affects on the current sense amplifier due to layout

Output-Voltage Offset Programming

The ISL6314 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into the OFS pin and out of the FB pin, providing a negative offset. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.3V, and I_{OFS} flows into the FB pin and out of the OFS pin, providing a positive offset. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 6 and 7.

Once the desired output offset voltage has been determined, use the following formulas in Equations 8 and 9 to set R_{OFS}:

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.6 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 8)}$$

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.3 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 9)}$$

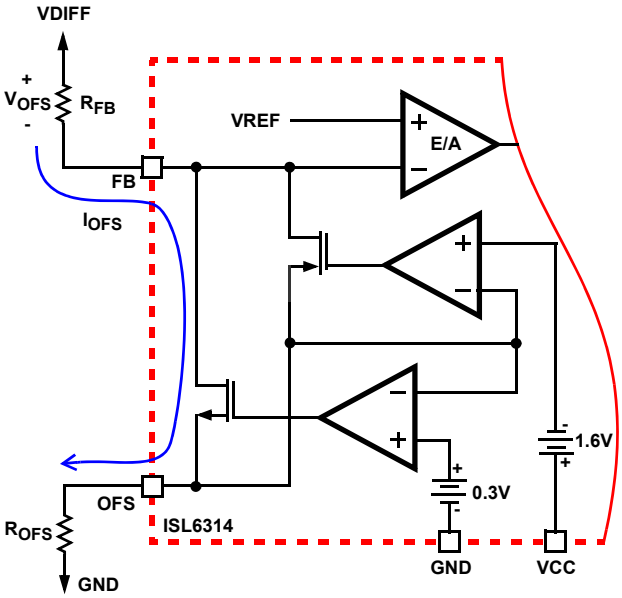


FIGURE 6. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

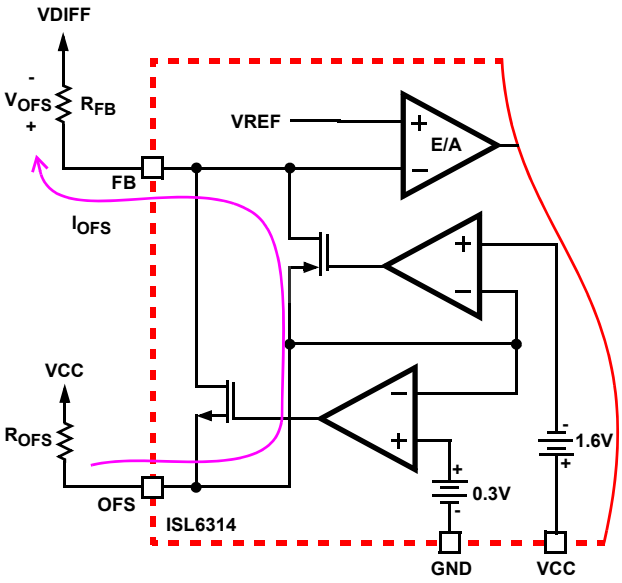


FIGURE 7. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the ISL6314 to do this by making changes to the VID inputs. The ISL6314 is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The DAC mode, ISL6314 is operating in, determines how the controller responds to a dynamic VID change.

INTEL DYNAMIC VID TRANSITIONS

When in Intel VR11 mode the ISL6314 checks the VID inputs on the positive edge of an internal 5.5MHz clock. If a new code is established and it remains stable for three consecutive readings (0.36µs to 0.54µs), the ISL6314 recognizes the new code and changes the internal DAC reference directly to the new level. The Intel processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VR11 mode, the ISL6314 will immediately change the internal DAC reference to the new requested value as soon as the request is validated, which means the fastest recommended rate at which a bit change can occur is once every 1µs. If the VID code is changed by more then one step at a time, the DAC will try to track it at a 5.5MHz step rate. This will likely cause an overcurrent or overvoltage fault.

AMD DYNAMIC VID TRANSITIONS

When running in AMD 5-bit or 6-bit modes of operation, the ISL6314 responds differently to a dynamic VID change. In the AMD modes the ISL6314 still checks the VID inputs on the positive edge of an internal 5.5MHz clock. In these modes the VID code can be changed by more than a 1-bit step at a time. If a new code is established and it remains stable for three consecutive readings (0.36µs to 0.54µs), the ISL6314 recognizes the change and begins slewing the DAC in 6.25mV steps at a stepping frequency of 345kHz until the VID and DAC are equal. Thus, the total time required for a VID change, t_{DVID}, is dependent only on the size of the VID change (ΔV_{VID}).

The time required for a ISL6314-based converter in AMD 5-bit DAC configuration to make a 1.1V to 1.5V reference voltage change is about 186µs, as calculated using Equation 10.

$$t_{DVID} = \frac{1}{345 \times 10^3} \cdot \left(\frac{\Delta V_{VID}}{0.00625}\right) \qquad \text{(EQ. 10)}$$

VID "OFF" DAC CODES

Both the Intel VR11 and the AMD 5-bit VID tables include "Off" DAC codes, which indicate to the controller to disable all regulation. Recognition of these codes is slightly different in that they must be stable for four consecutive readings of a 5.5MHz clock (0.54µs to 0.72µs) to be recognized. Once an "Off" code is recognized the ISL6314 latches off, and must be reset by dropping the EN pin.

Compensating Dynamic VID Transitions

During a VID transition, the resulting change in voltage on the FB pin and the COMP pin causes an AC current to flow through the error amplifier compensation components from the FB to the COMP pin. This current then flows through the feedback resistor, R_{FB}, and can cause the output voltage to overshoot or undershoot at the end of the VID transition. In order to ensure the smooth transition of the output voltage during a VID change, a VID-on-the-fly compensation network is required. This network is composed of a resistor and capacitor in series, R_{DVC} and C_{DVC}, between the DVC and the FB pin, as shown in Figure 8.

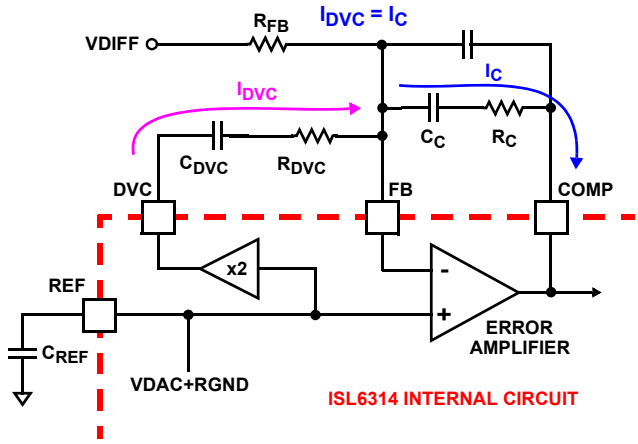


FIGURE 8. VID-ON-THE-FLY COMPENSATION NETWORK

This VID-on-the-fly compensation network works by sourcing AC current into the FB node to offset the effects of the AC current flowing from the FB to the COMP pin during a VID transition. To create this compensation current the ISL6314 sets the voltage on the DVC pin to be 2x the voltage on the REF pin. Since the error amplifier forces the voltage on the FB pin and the REF pin to be equal, the resulting voltage across the series RC between DVC and FB is equal to the REF pin voltage. The RC compensation components, R_{DVC} and C_{DVC}, can then be selected to create the desired amount of compensation current.

The amount of compensation current required is dependant on the modulator gain of the system, K1, and the error amplifier R-C components, R_C and C_C, that are in series between the FB and COMP pins. Use Equations 11, 12, and 13 to calculate the RC component values, R_{DVC} and C_{DVC}, for the VID-on-the-fly compensation network. For these equations: V_{IN} is the input voltage for the power train; V_{P-P} is the oscillator ramp amplitude (1.5V); and R_C and C_C are the error amplifier R-C components between the FB and COMP pins.

$$K1 = \frac{V_{IN}}{V_{PP}} \qquad A = \frac{K1}{K1 - 1} \qquad \text{(EQ. 11)}$$

$$R_{DVC} = A \times R_C \quad \text{(EQ. 12)}$$

$$C_{DVC} = \frac{C_C}{A} \quad \text{(EQ. 13)}$$

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

Internal Bootstrap Device

The integrated driver features an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

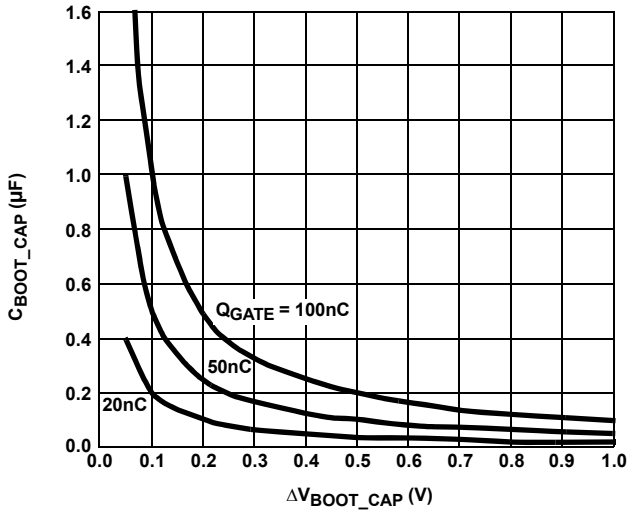


FIGURE 9. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

The bootstrap capacitor must have a maximum voltage rating above PVCC + 4V and its capacitance value can be chosen from Equation 14: where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Typical curves are shown in Figure 9.

$$C_{BOOT_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT_CAP}} \quad \text{(EQ. 14)}$$

$$Q_{GATE} = \frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}$$

Gate Drive Voltage Versatility

The ISL6314 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

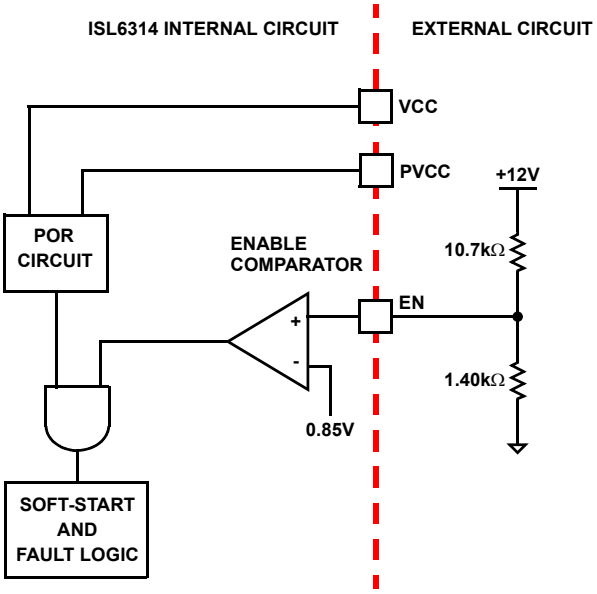


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

Enable and Disable

While in shutdown mode, the LGATE and UGATE signals are held low to assure the MOSFETs remain off. The following input conditions must be met, for both Intel and AMD modes of operation, before the ISL6314 is released from shutdown mode to begin the soft-start start-up sequence:

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6314 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6314 will not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 6).
2. The voltage on EN must be above 0.85V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6314 in shutdown until the voltage at EN rises above 0.85V. The enable comparator has 110mV of hysteresis to prevent bounce.
3. The driver bias voltage applied at the PVCC pin must reach the internal power-on reset (POR) rising threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6314 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see “Electrical Specifications” on page 6).

For Intel VR11 and AMD 6-bit modes of operation these are the only conditions that must be met for the controller to immediately begin the soft-start sequence, as shown in Figure 10. If running in AMD 5-bit mode of operation there is one more condition that must be met:

4. The VID code must not be 11111 in AMD 5-bit mode. This code signals the controller that no load is present. The controller will not allow soft-start to begin if this VID code is present on the VID pins.

Once all of these conditions are met the controller will begin the soft-start sequence and will ramp the output voltage up to the user designated level.

Intel Soft-Start

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. The soft-start sequence for the Intel modes of operation is slightly different than the AMD soft-start sequence.

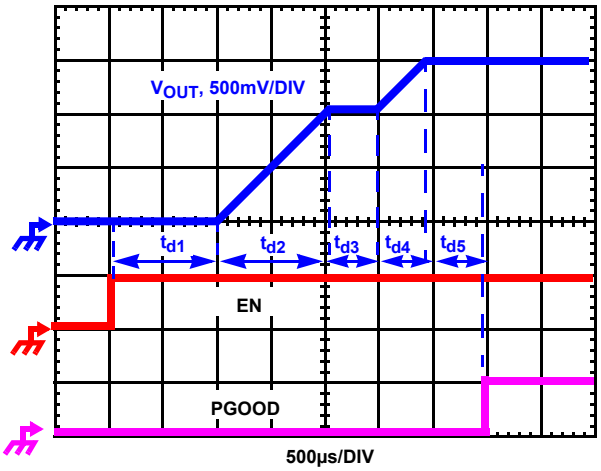


FIGURE 11. INTEL SOFT-START WAVEFORMS

For the Intel VR11 mode of operation, the soft-start sequence is composed of four periods, as shown in Figure 11. Once the ISL6314 is released from shutdown and soft-start begins (as described in “Enable and Disable” on page 20), the controller will have fixed delay period t_{d1}, typically 1.1ms. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V VBOOT voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed period t_{d3}, typically 93µs. At the end of t_{d3} period, ISL6314 will read the VID signals. It is recommended that the VID codes be set no later then 50µs into period t_{d3}. If the VID code is valid, ISL6314 will initiate the second soft-start ramp until the output voltage reaches the VID voltage plus/minus any offset or droop voltage.

The soft-start time is the sum of the 4 periods as shown in Equation 15.

$$t_{SS} = t_{d1} + t_{d2} + t_{d3} + t_{d4} \quad \text{(EQ. 15)}$$

During t_{d2} and t_{d4}, ISL6314 digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{SS} from SS pin to GND. The second soft-start ramp time t_{d2} and t_{d4} can be calculated based on Equations 16 and 17:

$$t_{d2} = 1.1 \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 16)}$$

$$t_{d4} = |V_{VID} - 1.1| \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 17)}$$

For example, when VID is set to 1.5V and the R_{SS} is set at 100kΩ, the first soft-start ramp time t_{d2} will be 880µs and the second soft-start ramp time t_{d4} will be 320µs.

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay t_{d5}. The typical value for t_{d5} is 93µs.

AMD Soft-Start

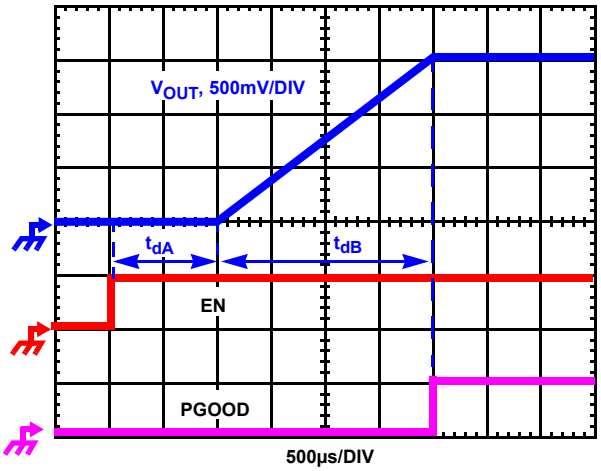


FIGURE 12. AMD SOFT-START WAVEFORMS

For the AMD 5-bit and 6-bit modes of operation, the soft-start sequence is composed of two periods, as shown in Figure 12. At the beginning of soft-start, the VID code is immediately obtained from the VID pins, followed by a fixed delay period t_{dA} of typically 1.1ms. After this delay period the ISL6314 will begin ramping the output voltage to the desired DAC level at a fixed rate of 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{SS} on the SS pin. The amount of time required to ramp the output voltage to the final DAC voltage is referred to as t_{dB}, and can be calculated as shown in Equation 18.

$$t_{dB} = V_{VID} \cdot R_{SS} \cdot 8 \cdot 10^{-3} (\mu s) \quad \text{(EQ. 18)}$$

At the end of soft-start, PGOOD will immediately go high if the VSEN voltage is within the undervoltage and overvoltage limits.

Table 5 is a summary table of the typical soft-start timing for both modes. The times listed are fixed delays; the variable ones (defined by the equations) depend on the slope of the ramp (1.25 mV/µs for a nominal 100kΩ R_{SS} resistor), and the amount of voltage excursion.

TABLE 5. ISL6314 SOFT_START TIMING SUMMARY

MODE	TIME SLOT	TIME
VR11	t_{d1}	1.1ms
VR11	t_{d2}	Equation 16
VR11	t_{d3}	93µs
VR11	t_{d4}	Equation 17
VR11	t_{d5}	93µs
AMD	t_{dA}	1.1ms
AMD	t_{dB}	Equation 18

Pre-Biased Soft-Start

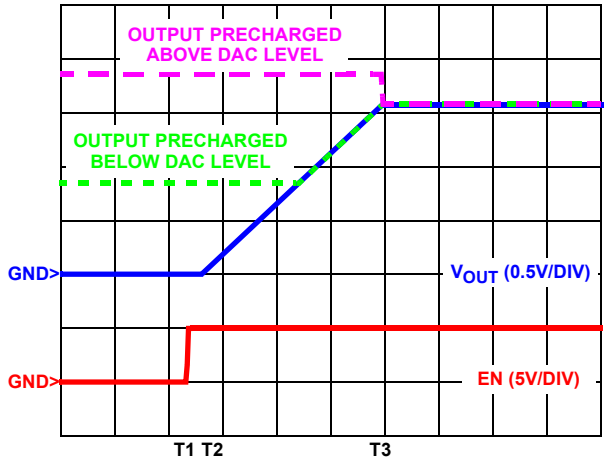


FIGURE 13. SOFT-START WAVEFORMS FOR ISL6314-BASED CONVERTER

The ISL6314 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level. See Figure 13.

Fault Monitoring and Protection

The ISL6314 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 14 outlines the interaction between the fault monitors and the power-good signal.

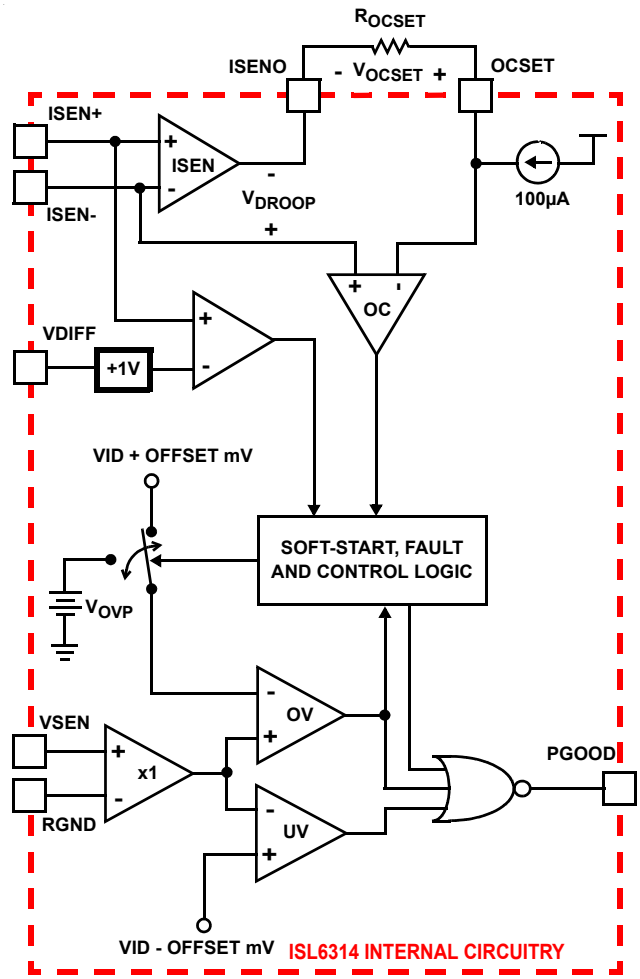


FIGURE 14. POWER-GOOD AND PROTECTION CIRCUITRY

Power-Good Signal

The power-good pin (PGOOD) is an open-drain logic output that signals whether or not the ISL6314 is regulating the output voltage within the proper levels, and whether any fault conditions exist. This pin should be tied through a resistor to a voltage source that's equal to or less than VCC.

For Intel mode of operation, PGOOD indicates whether VSEN is within specified overvoltage and undervoltage limits after a fixed delay from the end of soft-start. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from EN, POR, or one of the no-CPU VID codes. In the event of an overvoltage or overcurrent condition, or a no-CPU VID code, the controller latches off and PGOOD will not return high until EN is toggled and a successful soft-start is completed. In the case of an undervoltage event, PGOOD will return high when the output voltage rises above the undervoltage hysteresis level. PGOOD is always low prior to the end of soft-start.

For AMD modes of operation, PGOOD will always be high as long as VSEN is within the specified undervoltage/overvoltage window and soft-start has ended. PGOOD only goes low if VSEN is outside this window. Even if the controller is shut down the PGOOD signal will still stay high until VSEN falls below the undervoltage threshold.

Overvoltage Protection

The ISL6314 constantly monitors the difference between the VSEN and RGND voltages to detect if an overvoltage event occurs. During soft-start, while the DAC is ramping up, the overvoltage trip level is the higher of a fixed voltage 1.27V or DAC + 175mV for Intel modes of operation and DAC + 225mV for AMD modes of operation. Upon successful soft-start, the overvoltage trip level is only DAC + 175mV or DAC + 225mV depending on whether the controller is running in Intel or AMD mode. When the output voltage rises above the OVP trip level actions are taken by the ISL6314 to protect the microprocessor load.

At the inception of an overvoltage event, LGATE is commanded high and the PGOOD signal is driven low. This turns on the lower MOSFETs and pulls the output voltage below a level that might cause damage to the load. The LGATE output remains high until VSEN falls 100mV below the OVP threshold that tripped the overvoltage protection circuitry. The ISL6314 will continue to protect the load in this fashion as long as the overvoltage condition recurs. Once an overvoltage condition ends, the ISL6314 latches off, and must be reset by toggling EN, or through POR, before a soft-start can be reinitiated.

There is an OVP condition that exists that will not latch off the ISL6314. During a soft-start sequence, if the VSEN voltage is above the OVP threshold an overvoltage event will occur, but will be released once VSEN falls 100mV below the OVP threshold. If VSEN then rises above the OVP trip threshold a second time, the ISL6314 will be latched off and cannot be restarted until the controller is reset.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL6314 is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor. In the event that during normal operation the PVCC or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Undervoltage Detection

The undervoltage threshold is set at DAC - 350mV of the VID code. When the output voltage (V_{SEN} - R_{GND}) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above DAC - 250mV.

Open Sense Line Protection

In the case that either of the remote sense lines (VSEN or RGND) become open, the ISL6314 is designed to prevent the controller from regulating. This is accomplished by means of a small 5µA pull-up current on VSEN, and a pull-down current on RGND. If the sense lines are opened at any time, the voltage difference between V_{SEN} and R_{GND} will increase until an overvoltage event occurs, at which point overvoltage protection activates and the controller stops regulating. The ISL6314 will be latched off and cannot be restarted until the controller is reset.

Overcurrent Protection

The ISL6314 detects overcurrent events by comparing the droop voltage, V_{DROOP}, to the OCSET voltage, V_{OCSET}, as shown in Figure 14. The droop voltage, set by the external current sensing circuitry, is proportional to the output current as shown in Equation 19. A constant 100µA flows through R_{OCSET}, creating the OCSET voltage. When the droop voltage exceeds the OCSET voltage, the overcurrent protection circuitry activates. Since the droop voltage is proportional to the output current, the overcurrent trip level, I_{MAX}, can be set by selecting the proper value for R_{OCSET}, as shown in Equation 20.

$$V_{DROOP} = \frac{R_{COMP}}{R_S} \cdot I_{OUT} \cdot DCR \quad \text{(EQ. 19)}$$

$$R_{OCSET} = \frac{I_{MAX} \cdot R_{COMP} \cdot DCR}{100\mu A \cdot R_S} \quad \text{(EQ. 20)}$$

Once the output current exceeds the overcurrent trip level, V_{DROOP} will exceed V_{OCSET}, and a comparator will trigger the converter to begin overcurrent protection procedures.

At the beginning of an overcurrent shutdown, the controller turns off both upper and lower MOSFETs and lowers PGOOD. The controller will then immediately attempt to soft-start (which includes the 1.1ms delay of either t_{d1} or t_{dA}). If the overcurrent fault remains, the trip-retry cycles will continue until either the controller is disabled or the fault is cleared. But if five overcurrent events occur without successfully completing soft-start, the controller will latch off after the fifth try and must be reset by toggling EN before a soft-start can be reinitiated. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard. Figure 15 shows an example.

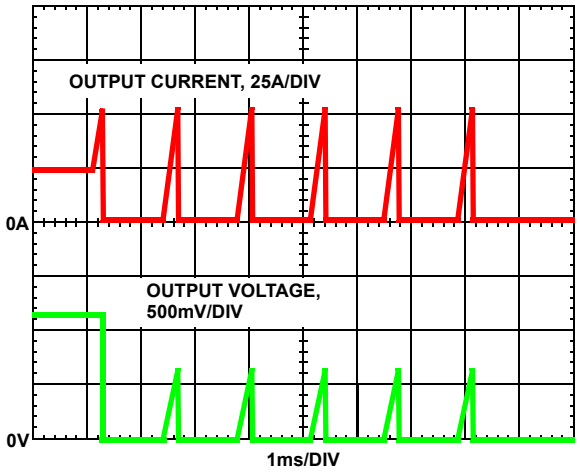


FIGURE 15. OVERCURRENT BEHAVIOR IN HICCUP MODE

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stage

The first step in designing a power converter using the ISL6314 is to determine if one phase is sufficient (if not, Intersil offers other parts, such as the ISL6313, which has two phases with similar features). This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which the output handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 21, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 1), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW(1)} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot (1-d) + \frac{I_{L(P-P)}^2 \cdot (1-d)}{12}\right] \quad \text{(EQ. 21)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively. Note that the dead times t_{d1} and t_{d2} in Equation 22 are NOT related to the soft-start timing delays.

$$P_{LOW(2)} = V_{D(ON)} \cdot f_S \cdot \left[\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right) \cdot t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right) \cdot t_{d2}\right] \quad \text{(EQ. 22)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW(1)}$ and $P_{LOW(2)}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 23, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP(1)}$.

$$P_{UP(1)} \approx V_{IN} \cdot \left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right) \cdot \left(\frac{t_1}{2}\right) \cdot f_S \quad \text{(EQ. 23)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 24, the approximate power loss is $P_{UP(2)}$.

$$P_{UP(2)} \approx V_{IN} \cdot \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right) \cdot \left(\frac{t_2}{2}\right) \cdot f_S \quad \text{(EQ. 24)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP(3)}$, as shown in Equation 25.

$$P_{UP(3)} = V_{IN} \cdot Q_{rr} \cdot f_S \quad \text{(EQ. 25)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 26 as $P_{UP(4)}$.

$$P_{UP(4)} \approx r_{DS(ON)} \cdot d \cdot \left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{P-P}^2}{12}\right] \quad \text{(EQ. 26)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 23, 24, 25 and 26. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there is one set of drivers in the controller package, the total power dissipated by it must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the 5x5 QFN package is approximately 3W at room temperature. See “Layout Considerations” on page 29 for thermal transfer improvement suggestions.

When designing the ISL6314 into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver’s internal circuitry and their corresponding average driver current can be estimated with Equations 27 and 28, respectively.

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q \cdot VCC \qquad \text{(EQ. 27)}$$

$$P_{Qg_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot F_{SW} \cdot N_{Q1}$$

$$P_{Qg_Q2} = Q_{G2} \cdot PVCC \cdot F_{SW} \cdot N_{Q2}$$

$$I_{DR} = \left(\frac{3}{2} \cdot Q_{G1} \cdot N_{Q1} + Q_{G2} \cdot N_{Q2}\right) \cdot F_{SW} + I_Q \qquad \text{(EQ. 28)}$$

In Equations 27 and 28, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs respectively. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

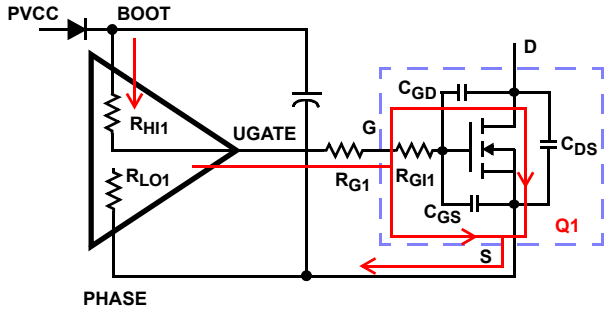


FIGURE 16. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

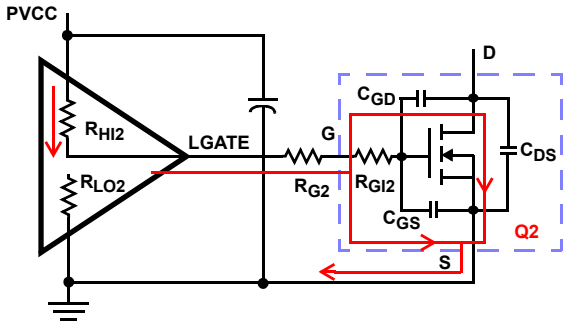


FIGURE 17. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance, P_{DR_UP}, the lower drive path resistance, P_{DR_UP}, and in the boot strap diode, P_{BOOT}. The rest of the power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 16 and 17 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated as shown in Equation 29:

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + P_{BOOT} + (I_Q \cdot VCC) \qquad \text{(EQ. 29)}$$

$$P_{BOOT} = \frac{P_{Qg_Q1}}{3}$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \cdot \frac{P_{Qg_Q1}}{3}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \cdot \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

Inductor DCR Current Sensing Component Selection

For accurate load line regulation, the ISL6314 senses the total output current by detecting the voltage across the output inductor DCR (as described in “Load-Line (Droop) Regulation” on page 16). As Figure 18 illustrates, an R-C network is required to accurately sense the inductor DCR voltage and convert this information into a “droop” voltage, which is proportional to the total output current.

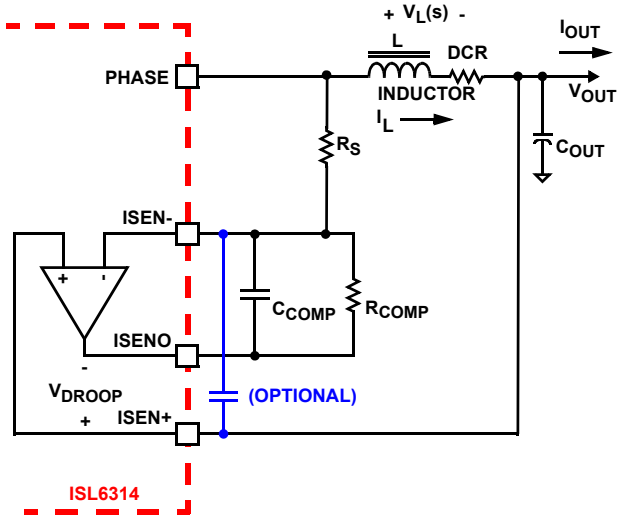


FIGURE 18. DCR SENSING CONFIGURATION

Choosing the components for this current sense network is a two step process. First, R_{COMP} and C_{COMP} must be chosen so that the time constant of this R_{COMP} - C_{COMP} network matches the time constant of the inductor L/DCR. Then the resistor R_S must be chosen to set the current sense network gain, obtaining the desired full load droop voltage. Follow the steps outlined in the following to choose the component values for this R-C network.

1. Choose an arbitrary value for C_{COMP}. The recommended value is 0.01µF.
2. Plug the inductor L and DCR component values, and the values for C_{COMP} chosen in Step 1, into Equation 30 to calculate the value for R_{COMP}.

$$R_{COMP} = \frac{L}{DCR \cdot C_{COMP}} \quad \text{(EQ. 30)}$$

3. Use the new value for R_{COMP} obtained from Equation 30, as well as the desired full load current, I_{FL}, full load droop voltage, V_{DROOP}, and inductor DCR in Equation 31 to calculate the value for R_S.

$$R_S = \frac{I_{FL}}{V_{DROOP}} \cdot R_{COMP} \cdot DCR \quad \text{(EQ. 31)}$$

Due to errors in the inductance or DCR it may be necessary to adjust the value of R_1 to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 19. Follow the steps outlined in the following to ensure the R-C and inductor L/DCR time constants are matched accurately.

1. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
2. Record ΔV1 and ΔV2 as shown in Figure 19.
3. Select new values, $R_{1,NEW}$, for the time constant resistor based on the original value, $R_{1,OLD}$, using Equation 32.

$$R_{1,NEW} = R_{1,OLD} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 32)}$$

4. Replace R_1 with the new value and check to see that the error is corrected. Repeat the procedure if necessary.

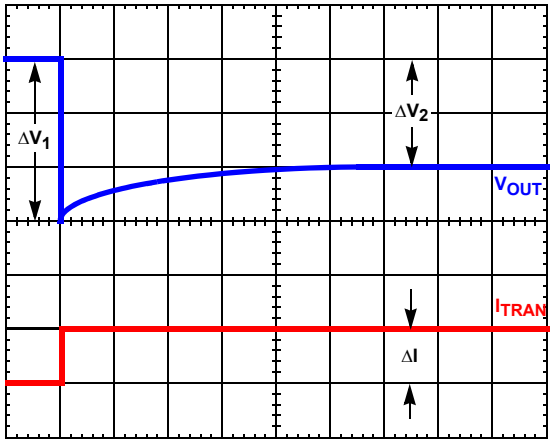


FIGURE 19. TIME CONSTANT MISMATCH BEHAVIOR

Loadline Regulation Resistor

If loadline regulation is desired, the resistor on the FS pin, R_T, should be connected to Ground (the value of R_T separately selects the switching frequency, as per Equation 42). The desired loadline, R_{LL}, can be calculated by Equation 33 where V_{DROOP} is the desired droop voltage at the full load current I_{FL}.

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \quad \text{(EQ. 33)}$$

Based on values for Equation 31, the desired loadline can also be calculated from Equation 34.

$$R_{LL} = \frac{R_{COMP} \cdot DCR}{R_S} \quad \text{(EQ. 34)}$$

If no loadline regulation is required, the resistor on the FS pin, R_T, should be connected to the VCC pin (the value of R_T separately selects the switching frequency, as per Equation 42).

APA Pin Component Selection

A 100µA current flows out of the APA pin and across R_{APA} to set the APA trip level. A 1000pF capacitor, C_{APA}, should also be placed across the R_{APA} resistor to help with noise immunity. An APA trip level of 500mV is recommended for most applications. Use Equation 35 to set R_{APA} to get the desired APA trip level.

$$R_{APA} = \frac{V_{APA,TRIP}}{100 \times 10^{-6}} = \frac{500mV}{100 \times 10^{-6}} = 5k\Omega \quad \text{(EQ. 35)}$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in Load-Line Regulation, there are two distinct methods for achieving these goals.

COMPENSATION WITH LOAD-LINE REGULATION

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C, as shown in Figure 20.

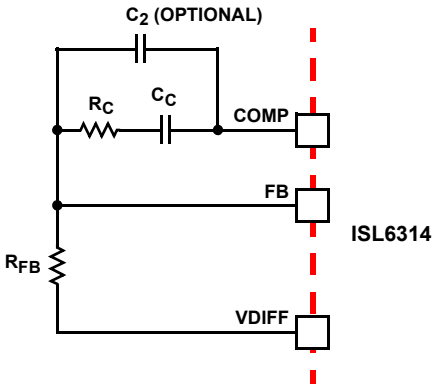


FIGURE 20. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6314 CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

In Equation 36, L is the filter inductance; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and V_{P-P} is the peak-to-peak sawtooth signal amplitude, as described in the “Electrical Specifications” on page 6.

Once selected, the compensation values in Equation 36 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 36 unless some performance issue is noted.

Case 1:
$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} > f_0$$
$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{P-P}\cdot\sqrt{L\cdot C}}{V_{IN}}$$
$$C_C = \frac{V_{IN}}{2\cdot\pi\cdot V_{P-P}\cdot R_{FB}\cdot f_0}$$

Case 2:
$$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} \le f_0 < \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$
$$R_C = R_{FB}\cdot\frac{V_{P-P}\cdot(2\cdot\pi)^2\cdot f_0^2\cdot L\cdot C}{V_{IN}} \qquad \text{(EQ. 36)}$$
$$C_C = \frac{V_{IN}}{(2\cdot\pi)^2\cdot f_0^2\cdot V_{P-P}\cdot R_{FB}\cdot\sqrt{L\cdot C}}$$

Case 3:
$$f_0 > \frac{1}{2\cdot\pi\cdot C\cdot ESR}$$
$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{P-P}\cdot L}{V_{IN}\cdot ESR}$$
$$C_C = \frac{V_{IN}\cdot ESR\cdot\sqrt{C}}{2\cdot\pi\cdot V_{P-P}\cdot R_{FB}\cdot f_0\cdot\sqrt{L}}$$

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 20). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted. For the solutions in Equation 36, R_{FB} is selected arbitrarily, typically in the 1kΩ to 5kΩ range.

COMPENSATION WITHOUT LOAD-LINE REGULATION

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 21, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

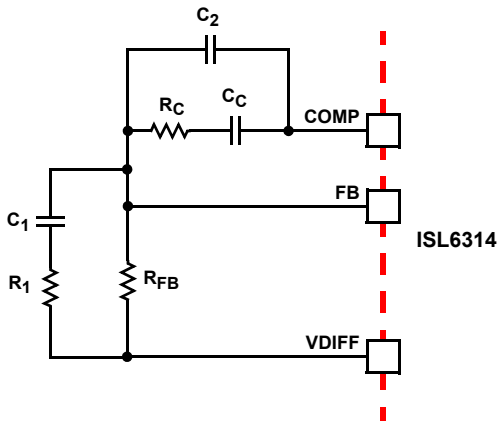


FIGURE 21. COMPENSATION CIRCUIT WITHOUT LOAD-LINE REGULATION

$$R_1 = R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR}$$

$$C_1 = \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}}$$

$$C_2 = \frac{V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P\text{-}P}} \quad \text{(EQ. 37)}$$

$$R_C = \frac{V_{PP} \cdot (2\pi)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}$$

$$C_C = \frac{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P\text{-}P}}$$

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 37, R_{FB} is selected arbitrarily, typically in the 1kΩ to 5kΩ range. The remaining compensation components are then selected according to Equation 37.

In Equation 37, L is the filter inductance; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and $V_{P\text{-}P}$ is the peak-to-peak sawtooth signal amplitude as described in the "Electrical Specifications" on page 6.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductor increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, Equation 38 shows the output voltage initially deviates by an amount as expressed in Equation 38:

$$\Delta V \approx ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \quad \text{(EQ. 38)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Output Ripple" on page 10 and Equation 39), a voltage develops across the bulk capacitor ESR equal to $I_{C(P\text{-}P)}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P\text{-}P(MAX)}$, determines the lower limit on the inductance.

$$L \geq ESR \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{P\text{-}P(MAX)}} \quad \text{(EQ. 39)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductor must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 40 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 41 addresses the leading edge. Normally, the trailing edge

dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the inductance, and C is the total output capacitance.

$$L \leq \frac{2 \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 40)}$$

$$L \leq \frac{1.25 \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 41)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in “MOSFETs” on page 23, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T. Figure 22 and Equation 42 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.61 - (1.035 \cdot \log(f_S))]} \quad \text{(EQ. 42)}$$

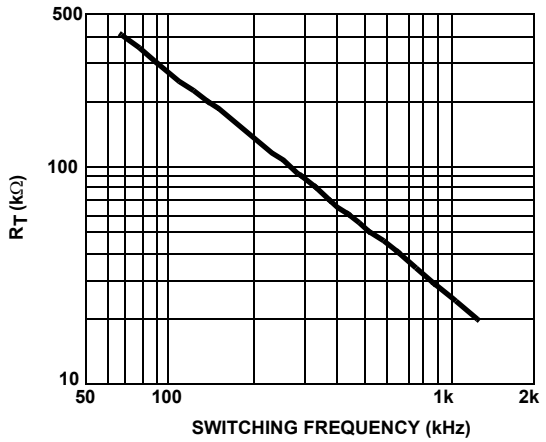


FIGURE 22. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

Use Figure 23 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L(P-P)}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage.

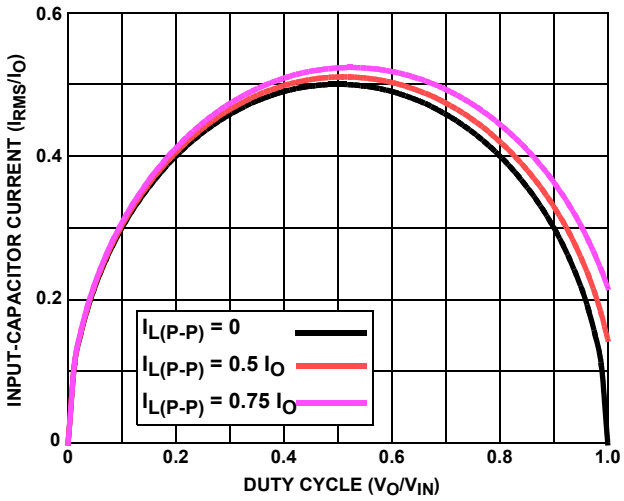


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR SINGLE-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turn-off, the upper MOSFET was carrying channel current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL6314 controller. The power components are the most critical because they switch large amounts of energy. Next, are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductor. Keep the gate drive traces short, resulting in low trace impedances.

When placing the MOSFETs try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input Bulk capacitors should be placed close to the drain of the upper FETs and the source of the lower FETs. Locate the output inductor and output capacitors between the MOSFETs and the load. The high-frequency input and output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next to, or on the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC and PVCC bypass capacitors as close to the ISL6314 as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multi-layer printed circuit board is recommended. Figure 24 shows the connections of the critical components for the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer.

Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase node. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE, and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL6314 regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISEN+ and ISEN- pins on the ISL6314 as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed on the bottom of the board, away from the noisy switching components located on the top of the board. These traces should be routed side by side, and they should be very thin traces. It’s important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6314 to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

© Copyright Intersil Americas LLC 2007-2009. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

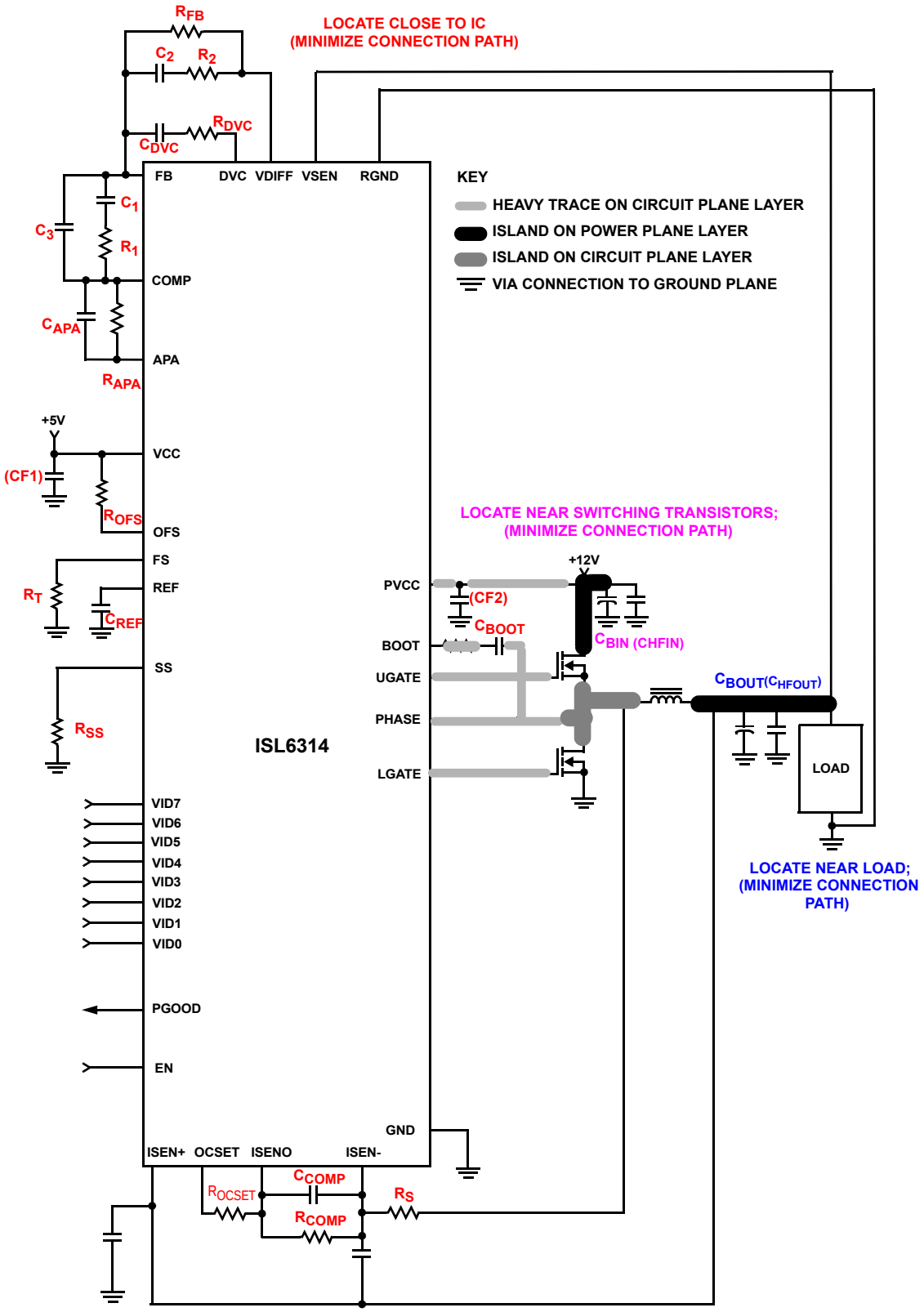
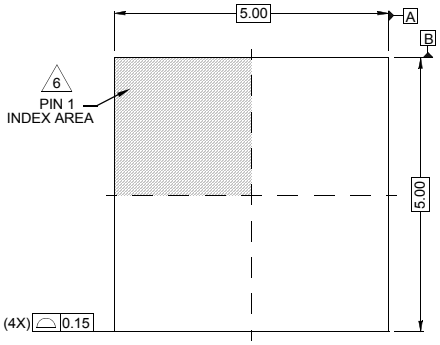


FIGURE 24. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

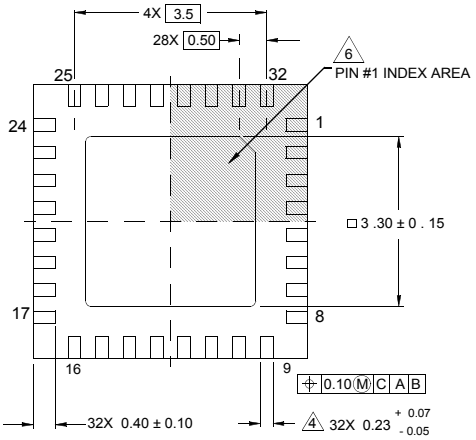
Package Outline Drawing

L32.5x5B

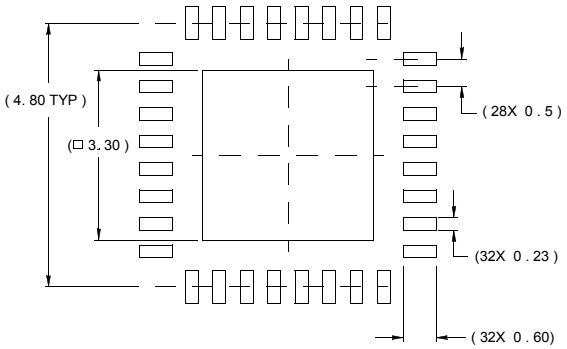
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 11/07



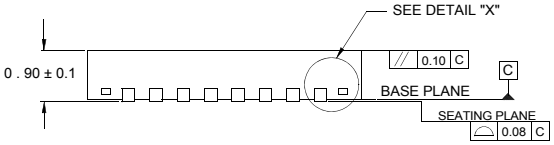
TOP VIEW



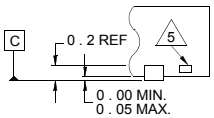
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.