ZL8800

Dual Channel/Dual Phase PMBus ChargeMode Control DC/DC Digital Controller

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The ZL8800 is a dual output or dual phase digital DC/DC controller. Each output can operate independently or be used together in a dual phase configuration for high current applications.

The ZL8800 supports a wide range of output voltages (0.54V to 5.5V) operating from input voltages as low as 4.5V up to 14V.

With the fully digital ChargeMode™ control, the ZL8800 will respond to a transient load step within a single switching cycle. This unique compensation-free modulation technique allows designs to meet transient specifications with minimum output capacitance, thus saving cost and board space.

The proprietary single wire Digital-DC™ (DDC) serial bus enables the ZL8800 to communicate between other Intersil ICs. By using the DDC, the ZL8800 achieves complex functions such as inter-IC phase current balancing, sequencing, and fault spreading, eliminating complicated power supply managers with numerous external discrete components.

The ZL8800 features cycle-by-cycle output overcurrent protection. The input voltage, output voltages, and DrMOS/MOSFET driver supply voltages are overvoltage and undervoltage protected. One internal temperature sensor and two external temperature sensors are available for temperature monitoring, one of which is used for under-temperature and over-temperature protection. A snapshot parametric capture feature allows users to take a snapshot of operating and fault data during normal or fault conditions.

Integrated Low Dropout (LDO) regulators allow the ZL8800 to operate from a single input supply, eliminating the need for additional linear regulators. The LDO output can be used to power external drivers or DrMOS devices.

With full PMBus™ compliance, the ZL8800 is capable of measuring and reporting input voltage, input current, output voltage, and output current as well as the device's internal temperature, two external temperatures, and an auxiliary voltage input.

Features

- Unique compensation-free design, which is always stable
- Output voltage range: 0.54V to 5.5V
- Input voltage range: 4.5V to 5.5V or 6.5V to 14V
- 1% output voltage accuracy over line, load, and temperature
- ChargeMode control achieves fast transient response and reduced output capacitance and provides output stability without compensation
- Switching frequency range: 200kHz to 1.33MHz
- Proprietary single wire DDC serial bus enables voltage sequencing and fault spreading with other Intersil ICs
- External power supply tracking
- Cycle-by-cycle inductor peak current protection
- Digital fault protection for output voltage UV/OV, input voltage UV/OV, temperature, and MOSFET driver voltage
- 10-bit average output current measurement with adjustable gain settings for sensing with high current, low DCR inductors
- 10-bit monitor ADC measures input voltage, input current, output voltage, internal and external temperature, and driver voltage
- Configurable to use standalone MOSFET drivers or integrated Driver-MOSFET (DrMOS) devices
- Nonvolatile memory for storing operating parameters and fault events
- PMBus compliant

Applications

- Servers and storage equipment
- Telecom and datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

Related Literature

- For a full list of related documents, visit our website
  - ZL8800 product page

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	DUAL OUTPUT	DUAL PHASE	DDC CURRENT SHARE	SPS SUPPORT
ZL8800	Yes	Yes	No	No
ZL8801	No	Yes	Yes	No
ZL8802	Yes	Yes	Yes	Yes

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Simplified Applications

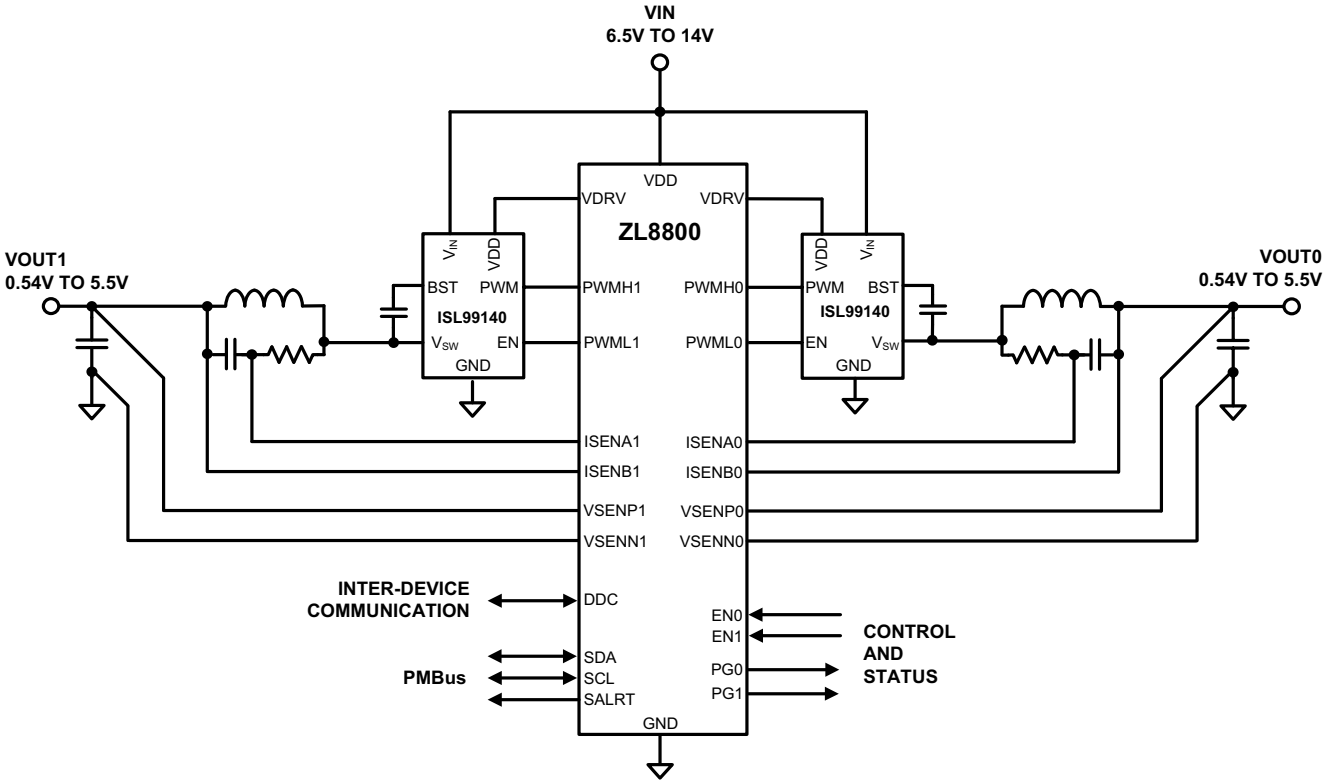


FIGURE 1. SIMPLIFIED TWO OUTPUT DRMOS APPLICATION

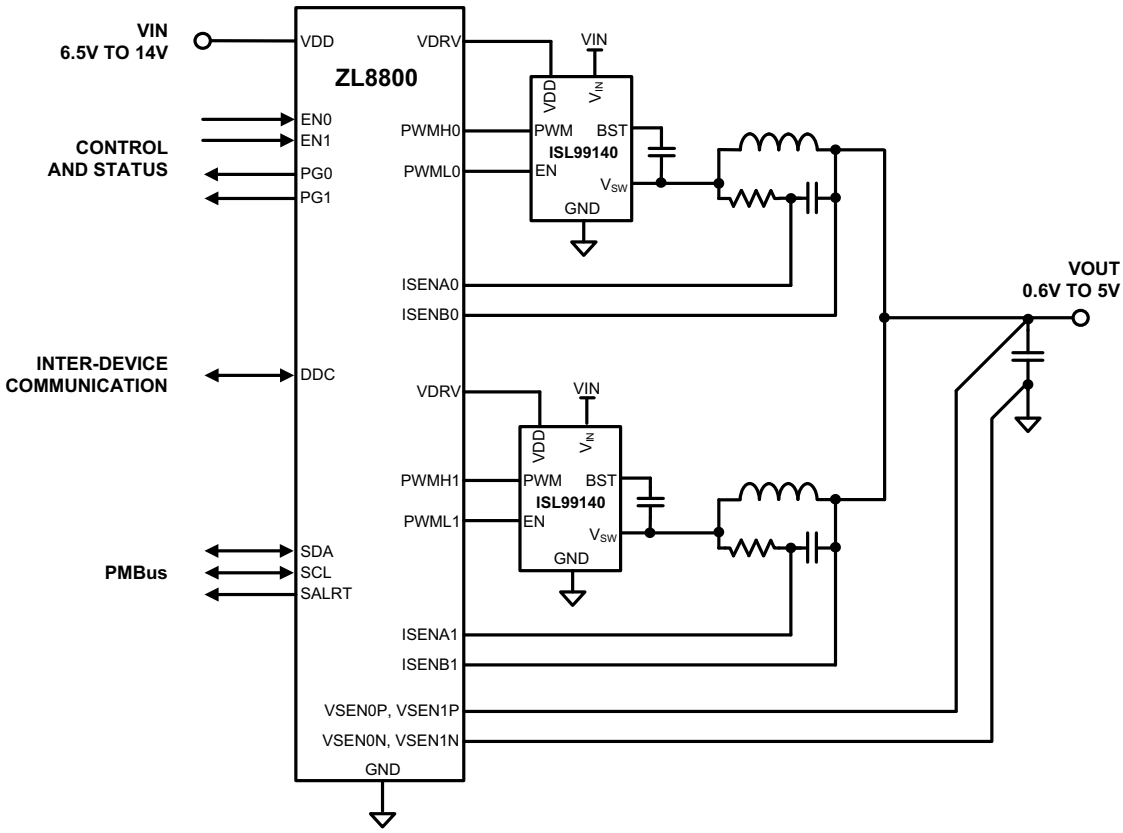


FIGURE 2. SIMPLIFIED TWO PHASE DRMOS APPLICATION

Block Diagram

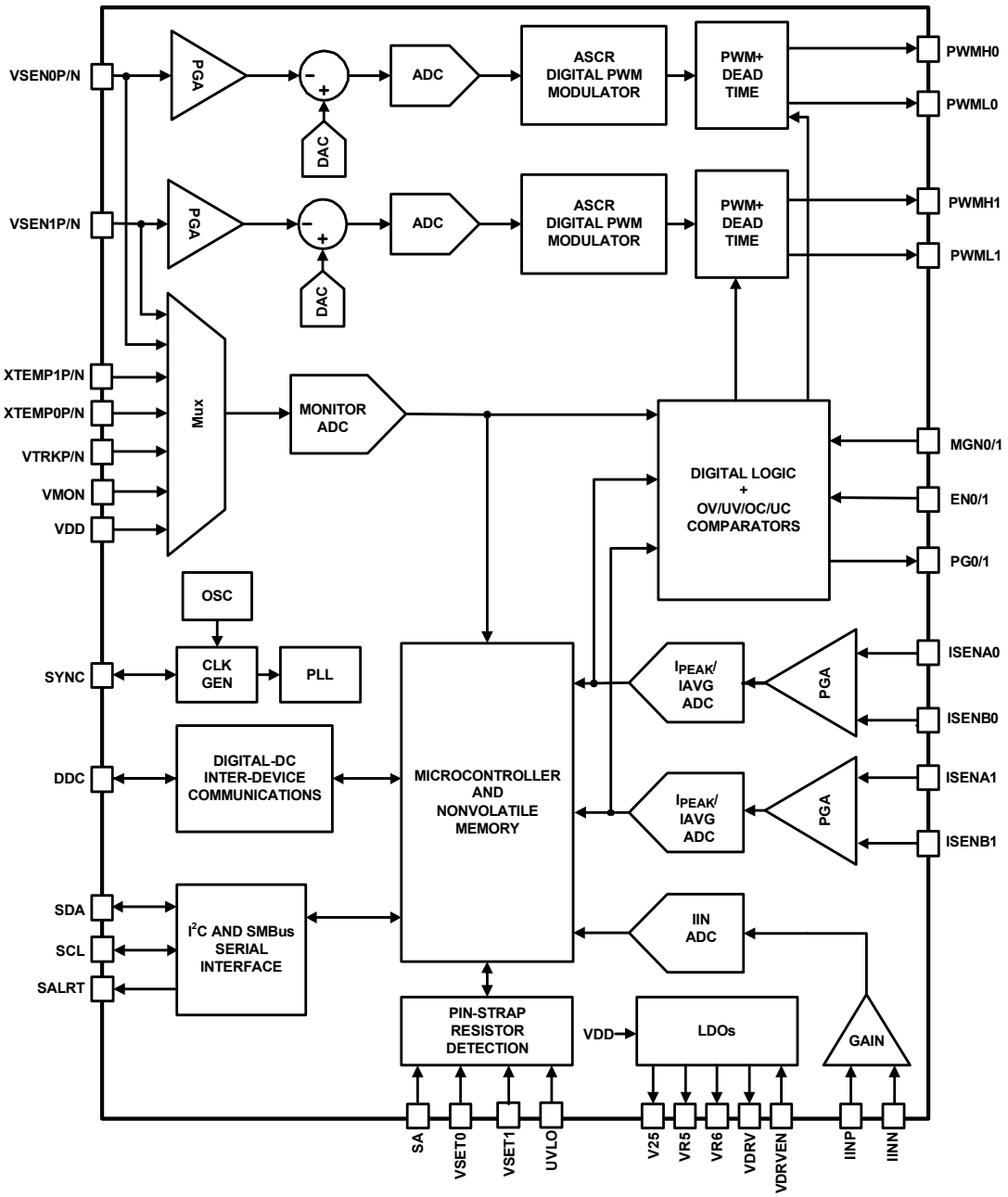


FIGURE 3. BLOCK DIAGRAM

Schematic

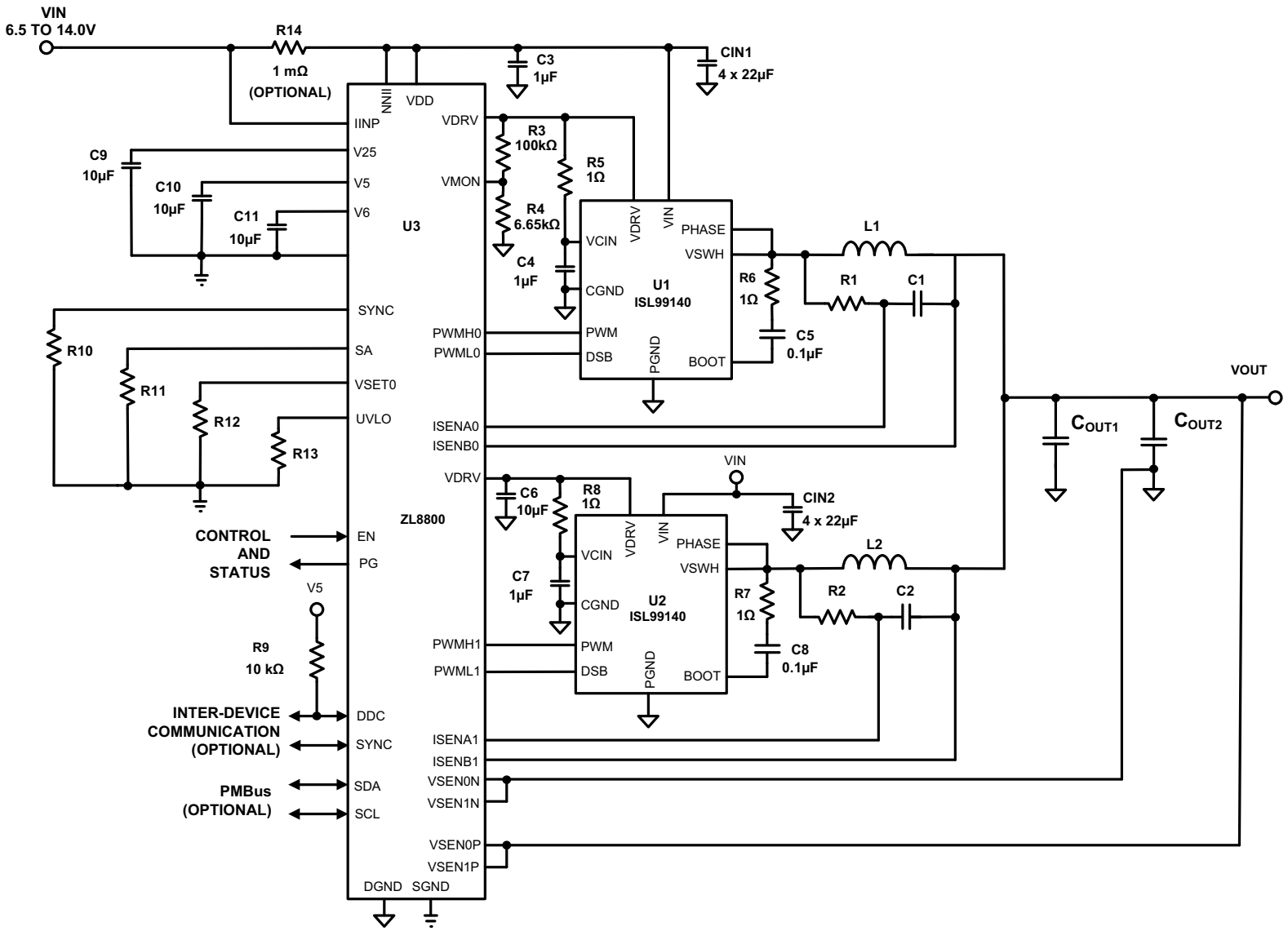
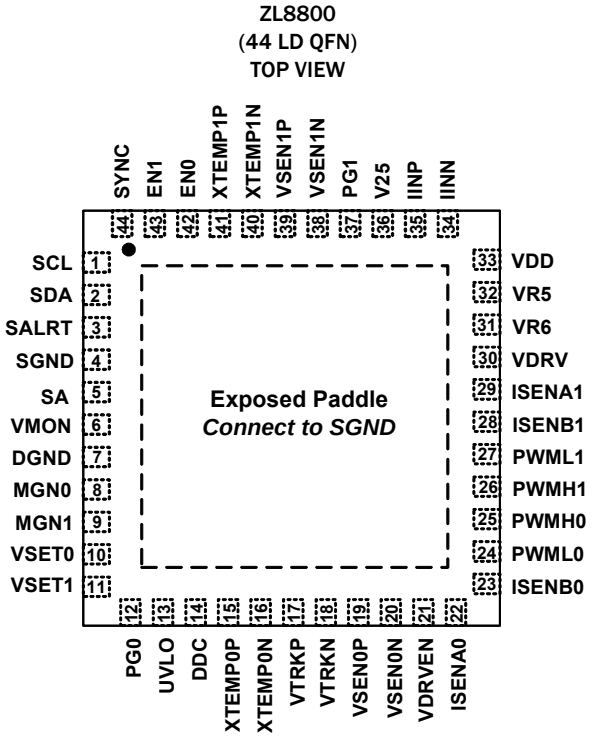


FIGURE 4. TWO PHASE SCHEMATIC

Pin Configuration



Pin Description

PIN	LABEL	TYPE (Note 1)	DESCRIPTION
1	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V source (VR5 recommended. Do not use V25). Pull-up supply must be from an “always on” source or VR5.
2	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V source (VR5 recommended. Do not use V25). Pull-up supply must be from an “always on” source or VR5.
3	SALRT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5V to 5.5V source (VR5 recommended. Do not use V25). Leave floating if not used.
4	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND. All pin-strap resistors should be connected to SGND. SGND must be connected to DGND and PGND using a single point connection.
5	SA	M	Serial address select pin. Used to assign unique address for each individual device or to enable certain management features. See Table 3 on page 13 for PMBus address options. Connect resistor to SGND.
6	VMON	I	External voltage monitoring (can be used for external driver bias (VDRV) monitoring). Requires an external 16:1 resistor divider network. 6.65k/100k recommended.
7	DGND	PWR	Digital ground. Connect to low impedance ground plane.
8	MGN0	I	Channel 0 margin pin.
9	MGN1	I	Channel 1 margin pin.
10	VSET0	M	Channel 0 output voltage selection pin. Used to set V_{OUT0} and V_{OUT0} max. See Table 4 on page 13 for V_{OUT} pin-strap options. Default V_{OUT} max is 115% of V_{OUT} setting, but this can be overridden through the PMBus interface with the VOUT_MAX command. Connect resistor to SGND.
11	VSET1	M	Channel 1 output voltage selection pin. Used to set V_{OUT1} and V_{OUT1} max. See Table 4 on page 13 for V_{OUT} pin-strap options. Default V_{OUT} max is 115% of V_{OUT} setting, but this can be overridden through the PMBus interface with the VOUT_MAX command. Connect resistor to SGND. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode.
12	PG0	O	Channel 0 Power-good output.

Pin Description (Continued)

PIN	LABEL	TYPE (Note 1)	DESCRIPTION
13	UVLO	M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}. See Table 6 on page 14 for UVLO setting options. Pin-strapped (configured) values can be overridden by the PMBus interface. Connect resistor to SGND. If enabling the device by tying the EN0 and/or EN1 pins high (self-enabling), set the UVLO level to 16V with a 100k resistor so the device will not turn on until after a configuration file has been loaded.
14	DDC	I/O	Single wire DDC bus (current sharing, inter device communication). Pull up to VRS.
15	XTEMP0P	I	External temperature sensor input for channel 0. Connect to external 2N3904 (base emitter junction) or equivalent embedded thermal diode. If not used, connect to SGND.
16	XTEMP0N	I	External temperature sensor input for channel 0 return. If not used, connect to SGND.
17	VTRKP	I	Tracking sense positive input. Used to track an external voltage source. If not used, connect to SGND.
18	VTRKN	I	Tracking sense negative input (return). If not used, connect to SGND.
19	VSEN0P	I	Differential output channel 0 voltage sense feedback. Connect to positive output regulation point.
20	VSEN0N	I	Differential output channel 0 voltage sense feedback. Connect to negative output regulation point.
21	VDRVEN	I	VDRV (MOSFET driver bias supply) Enable. Leave unconnected (float) or pull-up to VR5 to enable, tie to ground to disable.
22	ISENA0	I	Positive differential voltage input for channel 0 DCR current sensing.
23	ISENB0	I	Negative differential voltage input for channel 0 DCR current sensing.
24	PWML0	O	PWM0 low signal/DrMOS enable.
25	PWMH0	O	PWM0 high signal.
26	PWMH1	O	PWM1 high signal.
27	PWML1	O	PWM1 low signal/DrMOS enable.
28	ISENB1	I	Negative differential voltage input for channel 1 DCR current sensing.
29	ISENA1	I	Positive differential voltage input for channel 1 DCR current sensing.
30	VDRV	PWR	MOSFET driver bias supply regulator output. 10µF recommended.
31	VR6	PWR	Internal 6V reference used to power internal circuitry. 10µF recommended.
32	VR5	PWR	Internal 5V reference used to power internal circuitry. 10µF recommended.
33	VDD	PWR	Supply voltage.
34	IINN	I	Input current monitor negative input.
35	IINP	I	Input current monitor positive input.
36	V25	PWR	Internal 2.5V reference used to power internal circuitry.
37	PG1	O	Channel 1 Power-good output.
38	VSEN1N	I	Differential output channel 1 voltage sense feedback. Must be connected to negative output regulation point in 2-channel or 2-phase mode.
39	VSEN1P	I	Differential output channel 1 voltage sense feedback. Must be connected to positive output regulation point in 2-channel or 2-phase mode.
40	XTEMP1N	I	External temperature sensor input for channel 1 return. If not used connect to SGND.
41	XTEMP1P	I	External temperature sensor input for channel 1. Connect to external 2N3904 (base emitter junction) or equivalent embedded thermal diode. If not used connect to SGND.
42	EN0	I	Enable channel 0. Active signal enables PWM0 switching. Recommended to be tied low during device configuration.
43	EN1	I	Enable channel 1. Active signal enables PWM1 switching. Recommended to be tied low during device configuration.
44	SYNC	M/I/O	Clock synchronization input. Used to set the frequency of the internal clock, to sync to an external clock, or to output to an internal clock.
PAD	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTE:

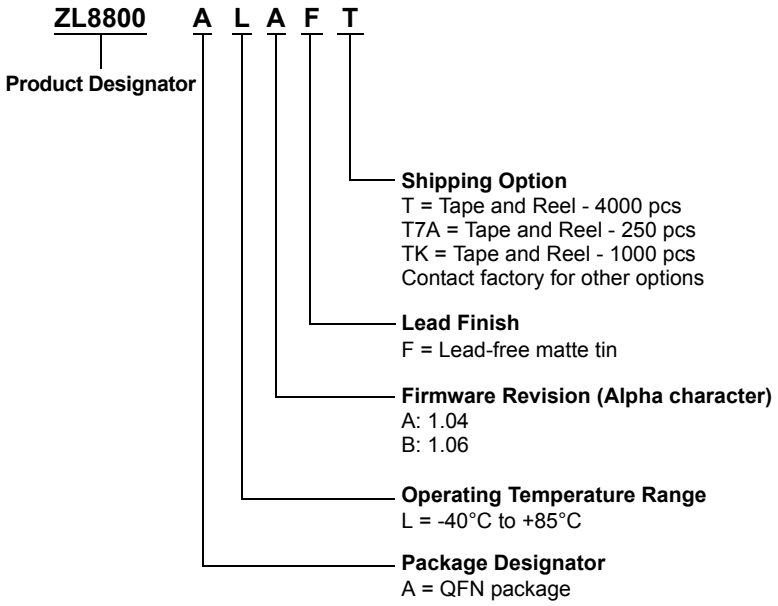
1. I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	FIRMWARE REVISION (Note 5)	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #	RECOMMENDED FOR NEW DESIGNS
ZL8800ALAFTK	8800	1.04	-40 to +85	1k	44 Lead QFN	L44.7x7B	N
ZL8800ALAFT	8800	1.04	-40 to +85	4k	44 Lead QFN	L44.7x7B	N
ZL8800ALAFT7A	8800	1.04	-40 to +85	250	44 Lead QFN	L44.7x7B	N
ZL8800ALBFT	8800	1.06	-40 to +85	4k	44 Lead QFN	L44.7x7B	Y
ZL8800ALBFTK	8800	1.06	-40 to +85	1k	44 Lead QFN	L44.7x7B	Y
ZL8800ALBFT7A	8800	1.06	-40 to +85	250	44 Lead QFN	L44.7x7B	Y
ZL8800-2CH-DEM01Z	Demonstration Board, 2 independent 30A synchronous buck converters with compensation-free ChargeMode control						
ZL8800-2PH-DEM01Z	Demonstration Board, 2-phase 60A synchronous buck converter with compensation-free ChargeMode control						

NOTES:

2. Refer to TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), refer to the ZL8800 product information page. For more information about MSL, refer to TB363.
5. See "Firmware Revision History" on page 86. Only the latest firmware revision is recommended for new designs.



Absolute Maximum Ratings

DC Supply Voltage: VDD . . . . . -0.3V to 17V
Logic I/O Voltage: DDC, EN0, EN1, MGN0, MGN1, PG0, PG1, SA, VDRVEN, SALRT, SCL, SDA, SYNC, UVLO, VMON, VSET0, VSET1 . . . . . -0.3V to 6.0V
Analog Input Voltages: VSEN0P, VSEN0N, VSEN1P, VSEN1N, VTRKP, VTRKN, ISENA0, ISENA1, ISENB0, ISENB1 . . . . . -0.3V to 6.5V
XTEMP0P, XTEMP1P . . . . . -0.3V to 6.0V
XTEMP0N, XTEMP1N . . . . . -0.3V to 0.3V
IINN, IINP . . . . . -0.3V to 17V
Logic Reference: V25 . . . . . -0.3V to 3V
Bias Supplies: VR5, VR6, VDRV . . . . . -0.3V to 6.5V
PWM Logic OUTPUTS, PWMH0, PWMH1, PWML0, PWML1 . . . -0.3V to 6.5V
Ground Voltage Differential (VDGND-VSGND) . . . . . -0.3V to +0.3V
ESD Ratings
Human Body Model (Tested per JESD22-A114E) 3000V
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C1010-D) 1000V
Latch-Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld QFN Package (Notes 7, 8)	25	1.5

Storage Temperature range . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Supply Voltage Range, V_{DD} . . . . . 4.5V to 14V
Output Voltage Range, V_{OUT} . . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C
Ambient Temperature Range, T_A . . . . . -40°C to +85°C
5V (VR5) Supply Total Supplied Current (Note 9) 5mA
5V LDO Supply (VDRV) (Note 6) . . . . . 0 to 80mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Output current is limited by device thermal dissipation.
7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. Refer to TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
9. Total of current used by pull-ups to SDA, SCL, SALRT, DDC, EN, and PG (including push-pull configuration).

Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C**

PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
IC INPUT AND BIAS SUPPLY CHARACTERISTICS					
IDD Supply Current	f_{SW} = 200kHz	-	26	**50**	mA
	f_{SW} = 1.33MHz	-	50	**80**	mA
IDD Device Disabled Current	EN = 0V, SMBus inactive, V_{DD} = 12V, f_{SW} = 400kHz	-	20	**30**	mA
VR5 Reference Output Voltage	V_{DD} > 6V, I < 5mA	**4.5**	5.0	**5.5**	V
V25 Reference Output Voltage	For reference only, VR > 3V	**2.25**	2.5	**2.75**	V
VR6 Reference Output Voltage	For reference only, V_{DD} = 12V	**5.5**	6.1	**6.6**	V
VDRV 5V Output Voltage (Note 10)	V_{DD} > 6.0V; 0-80mA	**4.5**	5.25	**5.5**	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range	V_{IN} > V_{OUT} + 1.8V	**0.54**	-	**5.5**	V
Output Voltage Set-Point Accuracy (Note 12)	Across line, load, temperature variation 0.72 < V_{OUT} < 5.50	**-1**	-	**1**	% V_{OUT}
Output Voltage Set-Point Resolution (Note 11)	Set using PMBus command	-	±0.025	-	% V_{OUT}
Output Voltage Positive Sensing Bias Current	VSEN[0,1] P = 4V (negative = sinking)	**-100**	20	**100**	µA
Output Voltage Negative Sensing Bias Current	VSEN[0,1] N = 0V	-	20	-	µA
LOGIC INPUT/OUTPUT CHARACTERISTICS					
Logic Input Leakage Current	Logic I/O - multimode pins	**-100**	-	**100**	nA
Logic Input Low, V_{IL}		-	-	**0.8**	V
Logic Input High, V_{IH}		**2**	-	-	V
Logic Output Low, V_{OL}	2mA sinking	-	-	**0.5**	V
Logic Output High, V_{OH}	2mA sourcing	**2.25**	-	-	V

Electrical Specifications V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
PWM INPUT/OUTPUT CHARACTERISTICS					
PWM Output Low	2mA sinking	-	-	**0.5**	V
PWM Output High	2mA sourcing	**4.25**	-	-	V
PWM Tri-State Input Bias Current (PWMH0,1)	V_{PWM} = 2.5V	-	-	**10**	µA
OSCILLATOR AND SWITCHING CHARACTERISTICS					
Switching Frequency Range		**200**	-	**1334**	kHz
Switching Frequency Set-point Accuracy		**-5**	-	**5**	%
Minimum SYNC Pulse Width	50% to 50%	**150**	-	-	ns
Input Clock Frequency Drift Tolerance	Maximum allowed drift of external clock	**-10**	-	**10**	%
PMBus Clock Frequency (Note 13)		**100**	-	**400**	kHz
POWER MANAGEMENT					
SOFT-START/ RAMP CHARACTERISTICS					
T_{ON} Delay/T_{OFF} Delay	Factory default	-	5	-	ms
T_{ON} Delay/T_{OFF} Delay Range	Set using PMBus command	**2**		**5000**	ms
Ramp Delay/T_{OFF} Delay Accuracy	Turn-on, turn-off delay	-	-0/+2	-	ms
Soft-Start/T_{ON} Ramp/T_{OFF} Ramp Duration	Factory default	-	5	-	ms
Soft-Start/T_{ON} Ramp/T_{OFF} Ramp Duration Range	Set using PMBus command	**0.5**		**100**	ms
Soft-Start/T_{ON} Ramp/T_{OFF} Ramp Duration Accuracy		-	±250	-	µs
TRACKING					
VTRK Input Bias Current	VTRK = 5V	-	70	**200**	µA
VTRK Regulation Accuracy (Note 16)	100% tracking, V_{OUT} – VTRK	**-2**	-	**2**	% V_{OUT}
POWER-GOOD					
Power-Good V_{OUT} Threshold	Factory default	-	90	-	% V_{OUT}
Power-Good V_{OUT} Hysteresis	Factory default	-	5	-	%
Power-Good Delay Applies to Turn-On Only (LOW to HIGH transition)	Factory default	-	1	-	ms
	Set using PMBus command	**0**	-	**5000**	ms
MONITORING AND FAULT MANAGEMENT					
INPUT VOLTAGE MONITOR AND FAULT DETECTION					
V_{DD}/V_{IN} UVLO Threshold Range		**2.85**	-	**16**	V
V_{DD}/V_{IN} Monitor Accuracy	Full Scale (FS) = 14V	-	±2	-	% FS
V_{DD}/V_{IN} Monitor Resolution	Full Scale (FS) = 14V	-	±0.15	-	% FS
V_{IN} UV/OV Fault Response Delay		-	100	-	µs
INPUT CURRENT					
Input Current Sense Differential Input Voltage	V_{IINP} - V_{IINN}	**0**	-	**20**	mV
Input Current Sense Input Offset Voltage	V_{IINP} - V_{IINN}	-	±100	-	µV
Input Current Sense Accuracy	% of full scale (20mV)	-	±5	-	% FS
OUTPUT VOLTAGE MONITOR AND FAULT DETECTION					
V_{OUT} Monitor Accuracy	FS = V_{SET} voltage (V_O)	**-2**	-	**2**	% FS
V_{OUT} Monitor Resolution	FS = V_{SET} voltage (V_O)	-	±0.15	-	% FS
V_{OUT} UV/OV Fault Response Delay		-	10	-	µs

Electrical Specifications V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP	MAX (Note 15)	UNIT
OUTPUT CURRENT					
OUTPUT CURRENT-SENSE RESOLUTION					
Low Range	±25mV full scale	-	37.5	-	µV
Medium Range	±35mV full scale	-	56.25	-	µV
High Range	±50mV full scale	-	75.0	-	µV
OUTPUT CURRENT-SENSE INPUT BIAS CURRENT					
V_{OUT} Referenced	ISENA0 or ISENA1	**-100**	-	**100**	nA
	ISENB0 or ISENB1	**-25**	-	**25**	µA
OUTPUT CURRENT-SENSE MONITOR AND FAULT DETECTION					
Output Current DCR Monitor Temperature Compensation	Factory default		3900		ppm/°C
	Configurable using PMBus	**100**		**12700**	ppm/°C
VMON BIAS MONITOR AND FAULT DETECTION					
VMON UVLO Threshold Range	Using VMON pin with 16:1 resistor divider	**2.85**	-	**5**	V
VMON Accuracy (Note 14)	Full Scale (FS) = 1.15V	**-2**	-	**2**	% FS
VMON Resolution	Full Scale (FS) = 1.15V	-	±0.15	-	% FS
VMON UV/OV Fault Response Delay		-	200	-	µs
TEMPERATURE SENSING					
INTERNAL TEMPERATURE SENSOR					
Internal Temperature Accuracy	Tested at +100°C	-5	–	5	°C
Internal Temperature Resolution		-	1	-	°C
Thermal Protection Threshold (Junction Temperature)	Factory default	-	125	-	°C
	Configurable using PMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		-	15	-	°C
EXTERNAL TEMPERATURE SENSOR: XTEMP0 and XTEMP1					
External Temperature Accuracy	Filter capacitance <100pF	-	±5	-	°C
External Temperature Resolution		-	1	-	°C
Thermal Protection Threshold	Factory default	-	125	-	°C
	Configurable using PMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		-	15	-	°C

NOTES:

10. Output current is limited by device thermal dissipation.
11. Percentage of Full Scale (FS) with temperature compensation applied.
12. V_{OUT} measured at the termination of the VSENxP and VSENxN sense points.
13. For operation at 400kHz, see PMBus Power System Management Protocol Specification Part 1, Section 5.2.6.2 for timing parameter limits.
14. Does not include errors due to resistor divider tolerances.
15. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
16. Only one output voltage can track the VTRK input: Channel 0, Channel 1, or the output of a 2-phase configuration.

ZL8800 Overview

Digital-DC Architecture Overview

The ZL8800 is an innovative mixed-signal power conversion and power management IC based on patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

The ZL8800 DC/DC controller is a dual channel, dual phase controller based on an architecture that does not require loop compensation. Adaptive algorithms enable the power converter to automatically change the operating state to increase efficiency and overall performance with no user interaction needed.

The ZL8800's full digital loop achieves precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. The ChargeMode control algorithm responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers. An extensive set of power management functions is fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal Nonvolatile Memory (NVM). Additionally, all functions can be configured and monitored through the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility. The ZL8800 is compliant with the PMBus Power System Management Protocol Specification Part I and II version 1.2.

When enabled, the ZL8800 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available through PMBus commands if desired, and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated subregulation circuitry enables single supply operation from any supply between 4.5V and 14V with no bias supplies needed.

The ZL8800 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of online tools and application notes are available to help simplify the design process. A demonstration board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. A Windows-based Graphical User Interface (GUI) enables full configuration and monitoring capability through the SMBus interface and the included USB cable.

Power Management Overview

The ZL8800 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL8800 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL8800 can continuously monitor input voltage and current, output voltage and current, internal temperature, and the temperature of two external thermal diodes. A Power-good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques described in this document or through the SMBus interface using PMBus commands. Monitoring parameters can also be preconfigured to provide alerts for specific conditions. The "PMBus Command Summary" on page 25 contains a listing of all the PMBus commands supported by the ZL8800 and a detailed description of the use of each of these commands.

Multimode Pins

To simplify circuit design, the ZL8800 incorporates patented multimode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multimode pins can respond to four different connections as shown in Table 2. These pins are sampled when power is applied.

Pin-strap Settings: This is the simplest implementation method, because no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings (excluding VDRVEN, which should be left floating). Using a single pin, one of three settings can be selected.

TABLE 2. MULTIMODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	< 0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0 VDC
Resistor to SGND	Set by resistor value

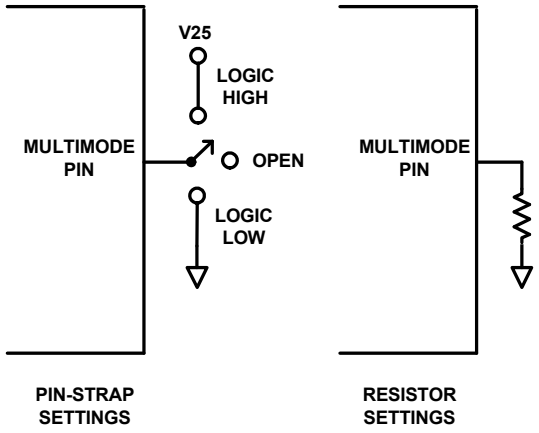


FIGURE 5. PIN-STRAP AND RESISTOR SETTINGS

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multimode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

SMBus: Almost any ZL8800 function can be configured through the SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be reconfigured and/or verified through SMBus. The "PMBus Command Detail" on page 29 section of this document explains the use of the PMBus commands in detail.

Configurable Pins

Four operating parameters can be set using the pin-strap or resistor setting method: SMBus address (pin 5, SA), output voltage (pins 10 and 11, VSET0,1), switching frequency (pin 44, SYNC), and input voltage undervoltage lockout (pin 13, UVLO).

The SMBus device address and the output voltage are the only parameters that **must** be set by external pins. All other device parameters can be set through PMBus. The device address is set using the SA pin. The output voltage is set using the VSET0 and VSET1 pins.

SMBus Device Address Selection (SA)

When communicating with multiple SMBus devices using the SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 3. Because the ZL8800 is a 2-channel device, the next higher sequential address after the selected ZL8800 address should not be used by any device on the SMBus. For example, if Address 0x26 is used, 0x27 should not be used by any device sharing the same SMBus (see the "DDC_CONFIG (D3h)" command for details). The SMBus address cannot be changed with a PMBus command.

TABLE 3. SMBus DEVICE ADDRESS SELECTION

RSA (kΩ)	SMBus ADDRESS	RSA (kΩ)	SMBus ADDRESS
LOW	0x26h	42.2	0x28h
OPEN	0x28h	46.4	0x29h
10	0x19h	51.1	0x2Ah
11	0x1Ah	56.2	0x2Bh
12.1	0x1Bh	61.9	0x2Ch
13.3	0x1Ch	68.1	0x2Dh
14.7	0x1Dh	75	0x2Eh
16.2	0x1Eh	82.5	0x2Fh
17.8	0x1Fh	90.9	0x30h
19.6	0x20h	100	0x31h
21.5	0x21h	110	0x32h
23.7	0x22h	121	0x33h
26.1	0x23h	133	0x34h
28.7	0x24h	147	0x35h
31.6	0x25h	162	0x36h
34.8	0x26h	178	0x37h
38.3	0x27h		

Output Voltage and VOUT_MAX Selection (VSET0,1)

The output voltage can be set to any voltage between 0.54V and 5.5V if the input voltage is higher than the desired output voltage by at least 1.1V. Using the pin-strap method, V_{OUT} can be set to any of the voltages shown in Table 4. V_{OUT} can also be set using a PMBus command. VOUT_MAX is also determined by this pin-strap setting, and is 10% greater than the VSET0 and VSET1 voltage settings.

TABLE 4. OUTPUT VOLTAGE SETTINGS

RVSET (kΩ)	VOUT (V)	RVSET (kΩ)	VOUT (V)
LOW	1.00	38.3	1.30
OPEN	1.20	42.2	1.40
HIGH	2.50	46.4	1.50
10	0.60	51.1	1.60
11	0.65	56.2	1.70
12.1	0.70	61.9	1.80
13.3	0.75	68.1	1.90
14.7	0.80	75	2.00
16.2	0.85	82.5	2.10
17.8	0.90	90.9	2.20
19.6	0.95	100	2.30
21.5	1.00	110	2.50
23.7	1.05	121	2.80
26.1	1.10	133	3.00
28.7	1.15	147	3.30
31.6	1.20	162	4.00
34.8	1.25	178	5.00

Switching Frequency Setting (SYNC)

The device's switching frequency can be set from 200kHz to 1333kHz using the pin-strap method shown in Table 5, or by using a PMBus command. The ZL8800 generates the device switching frequency by dividing an internal precision 16MHz clock by integers from 11 to 80.500kHz (n = 32) and 1000kHz (n = 16) are not recommended operating frequencies; use 533kHz and 1067kHz for best performance.

TABLE 5. DEVICE SWITCHING FREQUENCY SETTINGS

RSYNC (kΩ)	FREQ (kHz)	RSYNC kΩ	FREQ (kHz)
SGND	200	23.7	471
OPEN	400	26.1	533
HIGH	1067	28.7	571
10	200	31.6	615
11	222	34.8	727
12.1	242	38.3	800
13.3	267	42.2	842

TABLE 5. (Continued) DEVICE SWITCHING FREQUENCY SETTINGS

RSYNC (kΩ)	FREQ (kHz)	RSYNC kΩ	FREQ (kHz)
14.7	296	46.4	889
16.2	320	51.1	1067
17.8	364	56.2	1143
19.6	400	61.9	1231
21.5	421	68.1	1333

The ZL8800 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Intersil devices.

By default, the SYNC pin is configured as an input. The device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL8800's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200kHz to 1.33MHz and must be stable when the enable pin (EN0, EN1) is asserted. When using an external clock, the frequencies are not limited to discrete values as when using the internal clock. The external clock signal must not vary more than 10% from its initial value, and should have a minimum pulse width of 150ns. In the event of a loss of the external clock signal, the output voltage may show transient overshoot or undershoot.

If synchronization loss occurs, the ZL8800 will automatically switch to its internal oscillator and switch at its programmed frequency.

The SYNC pin can also be configured as an output. The device will run from its internal oscillator and will drive the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

The switching frequency can be set to any value between 200kHz and 1.33MHz using a PMBus command. The available frequencies below 1.33MHz are defined by f_{SW} = 16MHz/N, where 11 ≤ N ≤ 80.

If a value other than f_{SW} = 16MHz/N is entered using a PMBus command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 20).

Input Voltage Undervoltage Lockout Setting (UVLO)

The input Undervoltage Lockout (UVLO) prevents the ZL8800 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage undervoltage lockout threshold can be set between 2.85V and 16V using the pin-strap method shown in Table 6. UVLO can also be set or changed using the VIN_UV_FAULT_LIMIT command.

TABLE 6. INPUT VOLTAGE UNDERVOLTAGE LOCKOUT THRESHOLD SETTINGS

RUVLO (kΩ)	UVLO (V)	RUVLO (kΩ)	UVLO (V)
LOW	Not used	46.4	7.42
OPEN	4.5	51.1	8.18
HIGH	10.8	56.2	8.99
26.1	4.18	61.9	9.90
28.7	4.59	68.1	10.90
31.6	5.06	75	12.00
34.8	5.57	82.5	13.20
38.3	6.13	90.9	14.54
42.2	6.75	100	16.00

When an input undervoltage fault condition occurs, the user can determine the desired response to the fault condition. The following input undervoltage protection response options are available:

- Shut down and stay off until the fault has cleared and the device has been disabled and reenabled
- Shut down and attempt to restart when the fault is no longer present
- Shut down and restart continuously after a delay

The default response from an undervoltage fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (option 1).

Refer to "PMBus Command Detail" on page 29 for details on how to select specific overvoltage fault response options using the VIN_UV_FAULT_RESPONSE command.

When controlling the ZL8800 exclusively through the PMBus, a high voltage setting for UVLO can be used to prevent the ZL8800 from being enabled until a lower voltage for UVLO is set using the VIN_UV_FAULT_LIMIT command.

Internal Bias Regulators and Input Supply Connections

The ZL8800 uses internal Low Dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The following lists describes the internal bias regulators:

VR6: The VR6 LDO provides a regulated 6.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X5R or X7R filter capacitor to SGND is required at the VR6 pin. 10µF is recommended.

VR5: The VR5 LDO provides a regulated 5.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X5R or X7R filter capacitor to SGND is required at the VR5 pin. 10µF is recommended. This supply can be used to provide a pull-up supply as long as the load current does not exceed 5mA.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 4.7µF ceramic X5R or X7R filter capacitor to SGND is required at the V25 pin.

VDRV: The VDRV LDO provides a regulated, 5.25V bias supply for external MOSFET driver ICs or DrMOS integrated drivers/FETs. A 4.7µF ceramic X5R or X7R filter capacitor to PGND is required (10µF is recommended). However, additional capacitance will be needed as specified by the MOSFET driver or DrMOS device selected. The maximum rated output current is 80mA, but device thermal limits must be considered. The power dissipated by the VDRV supply will be (VIN - 5.25V) x IDRV, where IDRV is the current supplied by the VDRV bias supply. VDRV is enabled by leaving the VDRVEN unconnected (floating) or connecting it to VR5, and is disabled by connecting VDRVEN to ground.

NOTE: The internal bias regulators, VR6, VR5, and V25, are not designed to be outputs for powering other circuitry. The multimode pins can be connected to the V25 pin for logic HIGH settings, and the VR5 supply can be used to provide up to 5mA of pull-up current for the SDA, SCL, SALRT, DDC, and PG pins.

Start-Up Procedure

The ZL8800 follows a specific internal start-up procedure after power is applied to the VDD pin, as shown in Figure 6.

The device requires approximately 70ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded.

After this process is completed, the device is ready to accept commands through the serial interface and is ready to be enabled. If the device is synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. When enabled, the device requires approximately 2ms before the output voltage starts its ramp-up process.

After the TON_DELAY period has expired, the output will begin to ramp towards its target voltage according to the preconfigured TON_RISE time.

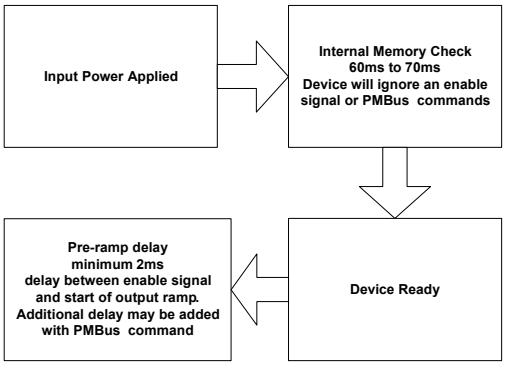


FIGURE 6. ZL8800 INTERNAL START-UP PROCEDURE

TON_DELAY and Rise Times

In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL8800 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The TON_DELAY time begins when the EN pin is asserted. The TON_DELAY time is set using the PMBus command TON_DELAY.

The TON_RISE time enables a precisely controlled ramp to the nominal V_{OUT} value that begins when the TON_DELAY time has expired. The ramp-up is monotonic and its slope can be precisely set using the PMBus command TON_RISE.

The TON_DELAY and TON_RAMP times can be set using PMBus commands TON_DELAY and TON_RISE over the serial bus interface. When the TON_DELAY time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized.

The TON_DELAY and TON_RAMP times can be set using PMBus commands TON_DELAY and TON_RISE over the serial bus interface. When the TON_DELAY time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized, which takes approximately 2ms to complete. The TON_RISE time can be set to values less than 2ms, however the TON_RISE time should be set to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush currents. A lower TON_RISE time limit can be estimated using the formula:

$$TON_RISE = C_{OUT} * V_{OUT} / I_{LIMIT}$$

where C_{OUT} is the total output capacitance, V_{OUT} is the output voltage, and I_{LIMIT} is the current limit setting for the ZL8800.

Enable Pin Operation and Timing

The enable pins (EN0 and EN1) are used to enable and disable each channel of the ZL8800. When operated as a 2-phase converter, use EN0 and ground EN1. The enable pins should be held low whenever a configuration file or script is used to configure the ZL8800, or when a PMBus command is sent that could potentially damage the application circuit. When the ZL8800 is used in a self-enabled mode, for example, when EN0 or EN1 is tied to VR5, or to a resistor divider to VIN, the user must consider the ZL8800's default factory settings. When a configuration file is used to configure the ZL8800, the factory default settings are restored to both the user and default stores to set the ZL8800 to an initialized state. Because the default state of the ZL8800 is to be enabled when the enable pin is high, it is possible for the ZL8800 to be enabled while the PMBus commands are sent to the ZL8800 during the configuration process.

When operating the IC in 2 channel mode, avoid transitioning EN0 or EN1 high within 1ms of the beginning of the opposite channel's start-up ramp. For example, if the Page 0 output (VSEN0, PWM) begins to ramp-up at the end of a TON_DELAY of 5ms, EN1 should not transition high between 4ms and 6ms.

Power-Good

The ZL8800 provides a Power-good (PG0, PG1) signal for each channel that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the

target voltage. These limits and the polarity of the pin can be changed using PMBus commands. The VOUT_UV_FAULT_LIMIT must always be set to a value lower than POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the ZL8800 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL8800 PG delay is set equal to 1ms. The PG delay can be set using a PMBus command as described in the "PMBus Command Summary" on page 25.

Power Management Functional Description

Output Overvoltage Protection

The ZL8800 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a programmable threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will deassert and the device can then respond in a number of ways as follows:

- Shut down and stay off until the fault has cleared and the device has been disabled and reenabled
- Shut down and, when the fault is no longer present, attempt to restart
- Shut down and restart continuously after a delay

The default response from an overvoltage fault is to immediately shut down with no retries (option 1).

Refer to "PMBus Command Detail" on page 29 for details about how to select specific overvoltage fault response options using the VOUT_OV_FAULT_RESPONSE command.

Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ZL8800 provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the desired output voltage is present after the TON_DELAY time, the ZL8800 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-up from the prebias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command.

The resulting output voltage rise time will vary depending on the prebias voltage, but the total time elapsed from the end of the TON_DELAY time to when the TON_RISE time is complete and the output is at the desired value will match the preconfigured ramp time (see Figure 7).

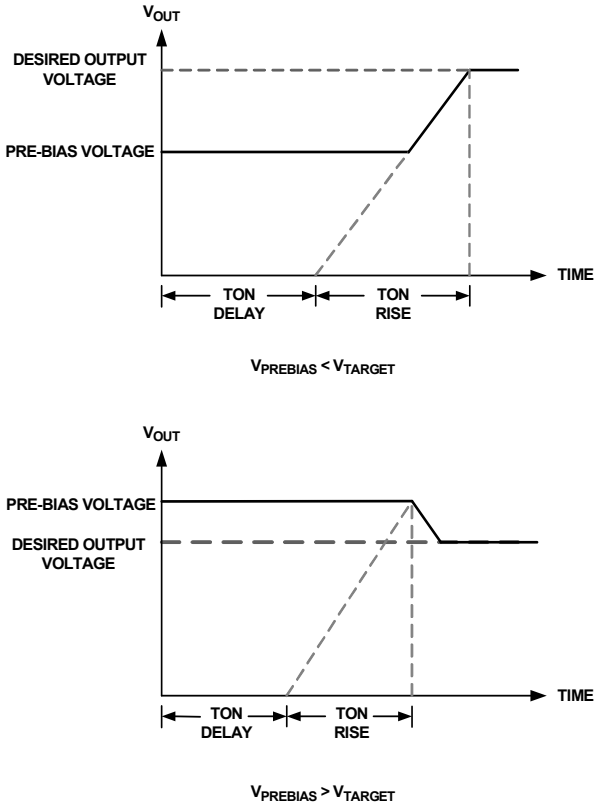


FIGURE 7. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage higher than the target voltage exists after the preconfigured TON_DELAY time and TON_RISE time have completed, the ZL8800 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-down from the prebias voltage is monotonic. The output voltage is then ramped down to the desired output voltage.

If a prebias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will stay off with an output OV fault recorded.

Output Overcurrent Protection

The ZL8800 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. After the current limit threshold has been selected (see "Current Limit Configuration" on page 17), the user can determine the desired response to the fault condition. The following overcurrent protection response options are available:

- Shut down and stay off until the fault has cleared and the device has been disabled and reenabled
- Shut down and, when the fault is no longer present, attempt to restart
- Shut down and restart continuously after a delay

The default response from an overcurrent voltage fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (option 1).

Refer to the "PMBus Command Detail" section for details on how to select specific overvoltage fault response options using the IOUT_OC_FAULT_RESPONSE command.

CURRENT-SENSING COMPONENTS

The ZL8800 uses the inductor DCR current-sensing technique. Current sensing is achieved by selecting an R/C network as shown in Figure 8.

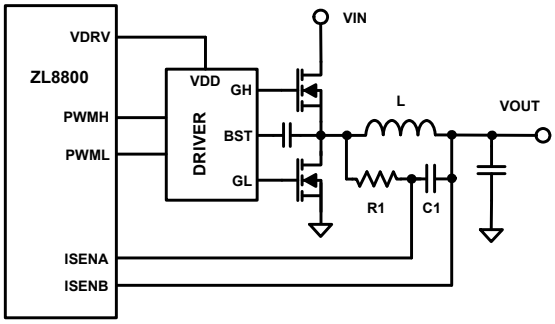


FIGURE 8. DCR CURRENT SENSING

For the voltage across C_1 to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR}$$
$$R1 \cdot C1 = \frac{L}{DCR} \quad \text{(EQ. 1)}$$

For *L*, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC bias, and switching frequency on the inductance when determining the minimum value of *L*. Use the typical room temperature value for *DCR*.

The value of R_1 should be as small as feasible and no greater than 5kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. When calculating the minimum value of R_1, the average voltage across C_1 (which is the average $I_{OUT} \cdot$ DCR product) is small and can be neglected. Therefore, the minimum value of R_1 can be approximated by the following equation:

$$R1_{min} = \frac{D(V_{IN} - V_{OUT})^2 + (1-D) \cdot V_{OUT}^2}{P_{R1}} \quad \text{(EQ. 2)}$$

where P_{R1} is the maximum power dissipation specification for the resistor. After $R1_{min}$ has been calculated, solve for the maximum value of C_1 from:

$$C1_{max} = \frac{L}{R1_{min} \cdot DCR} \quad \text{(EQ. 3)}$$

and choose the next-lowest readily available value (for example, for $C1_{max}$ = 1.86µF, C_1 = 1.5µF is a good choice), then substitute the chosen value into the same equation and recalculate the value of R_1. Choose the 1% resistor standard value closest to this recalculated value of R_1.

Current Limit Configuration

The ZL8800 gives the power supply designer several choices for the fault response during over or undercurrent condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected. These parameters are configured using the ISENSE_CONFIG command.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (less accurate due to potential ringing). It is a configurable parameter from 0 to 832ns.

The ZL8800 provides an adjustable, maximum full scale sensing range. Three ranges are available: ±25mV, ±35mV, and ±50mV maximum input voltage.

By default, current-sensing is enabled during the inductor current down slope period of the switching period (D'). In applications where the steady state duty cycle is >0.5, for example, a 5V to 3.3V converter, the ZL8800 can be configured to sense current during the inductor up slope period of the switching cycle (D).

The user has the option of selecting how many consecutive overcurrent readings must occur before an overcurrent fault and subsequent shutdown are initiated. Either 1, 3, 5, 7, 9, 11, or 13 consecutive faults can be selected.

After the ISENSE_CONFIG parameters have been selected, the user must select the desired current limit thresholds and the resistance of the sensing element.

The current limit thresholds are set with four commands:

- IOUT_OC_FAULT_LIMIT – this sets the overcurrent threshold that must be exceeded by the number of consecutive times chosen in ISENSE_CONFIG.
- IOUT_UC_FAULT_LIMIT – this is the same as IOUT_OC_FAULT_LIMIT, but represents the negative current that flows lower FET during the D' interval. Large negative currents can flow during faults such as a higher voltage rail being shorted to a lower voltage rail.
- IOUT_AVG_OC_FAULT_LIMIT – this limit is similar to IOUT_OC_FAULT_LIMIT, but the limit represents an average reading over several switching cycles. Because it is an average, the response time is slower, but the limit can be set closer to the maximum average expected output current.
- IOUT_AVG_UC_FAULT_LIMIT – this limit is similar to IOUT_AVG_OC_FAULT_LIMIT, but represents the negative current that flows lower FET during the D' interval.

Input Current Monitor

The input current can be monitored through the IINN and IINP pins. When no input current is being measured through the IINN and IINP pins, the input current can be estimated using the measured duty cycle and measured average output current. Fault detection is not allowed using the estimated input current. This estimation is enabled by setting IIN_SCALE to zero.

The input current monitor input should be connected across a current-sensing resistor in series with the input supply. The IINP pin is connected to the input supply side of the current-sense resistor, and the IINN pin is connected to the ZL8800 VDD side of the current-sense resistor. Using the IIN_SCALE command, set the current-sense resistor value. Select the current-sense resistor value such that the maximum expected input current times the current-sense resistor value does not exceed the maximum current-sensing input voltage of 20mV.

If this feature is not used, IINN and IINP should be tied to VDD.

Thermal Overload Protection

The ZL8800 includes an on-chip thermal sensor that continuously measures the internal temperature of the die. This thermal sensor is used to provide both over-temperature and under-temperature protection. If the over-temperature limit is exceeded, or the temperature falls below the under-temperature limit, the ZL8800 is shut down. The over-temperature and under-temperature limits are set by the OT_FAULT_LIMIT and UT_FAULT_LIMIT, respectively. The ZL8800 will not attempt to restart until the temperature falls below the OT_WARN_LIMIT for over-temperature faults or rises above the UT_WARN_LIMIT for under-temperature faults. The default temperature limits are +125°C and -45°C, but the user can set the limits to different values if desired. Note that setting a higher over-temperature or under-temperature limit may result in permanent damage to the device. When the device has been disabled due to an internal temperature fault, the user can select one of several fault response options as follows:

- Shut down and stay off until the fault has cleared and the device has been disabled and reenabled
- Shut down and, when the fault is no longer present, attempt to restart
- Shut down and restart continuously after a delay

The default response from an over-temperature or under-temperature fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (option 1).

Refer to "PMBus Command Summary" on page 25 for details about how to select specific overvoltage fault response options using the OT_FAULT_RESPONSE and UT_FAULT_RESPONSE commands.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore, the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ZL8800 integrates a tracking scheme that allows one of its outputs (Channel 0 or Channel 1, or the single output in a dual phase application) to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when the tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation.

Figure 9 illustrates the typical connection and the two tracking modes:

- **Coincident**. This mode configures the ZL8800 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.
- **Ratio-metric**. This mode configures the ZL8800 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string can be used to configure a different tracking ratio. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.

The master ZL8800 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. The maximum tracking rise time is 1V/ms. The slave device must be enabled before the master.

Any device that is configured for tracking mode will ignore its TON_DELAY and TON_RISE settings and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin.

Tracking mode can be configured by using the TRACK_CONFIG command.

Note that current sharing groups that are also configured to track another voltage do not offer prebias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside source.

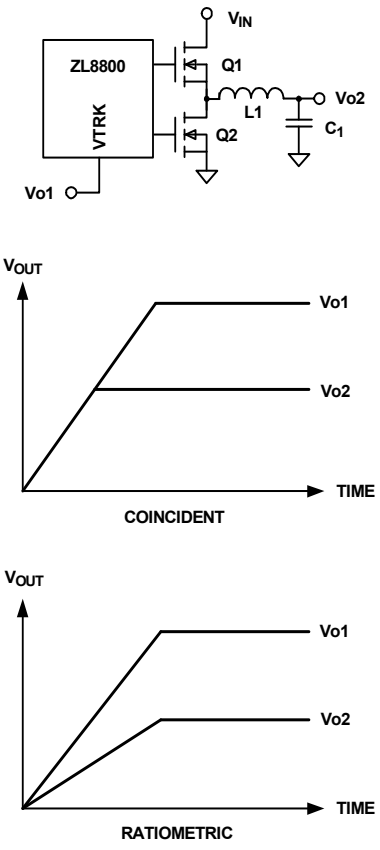


FIGURE 9. TRACKING MODES

Voltage Margining

The ZL8800 offers a simple method to vary its output higher or lower than its nominal voltage setting to determine whether the load device is capable of operating over its specified supply voltage range. Margining is controlled through the OPERATION command.

Default margin limits of V_{OUT} ±5% are preloaded in the factory, but the margin limits can be modified through PMBus commands to be as high as V_{OUT} + 10% or as low as 0V, where V_{OUT} is the nominal output voltage set point determined by the VSET pin or the VOUT_COMMAND command.

A safety feature prevents the user from configuring the output voltage to exceed V_{OUT} + 10% under any condition.

Additionally, the transition rate between the nominal output voltage and either margin limit can be configured using the VOUT_TRANSITION_RATE command.

External Voltage Monitoring

The voltage monitoring (VMON) pin can monitor the voltage supply for the external driver IC. The VMON input must be scaled by a 16:1 ratio in order to read-back the VMON voltage correctly. A 100kΩ and 6.65kΩ resistor divider is recommended. Overvoltage and undervoltage fault thresholds can be set using the MFR_VMON_OV_FAULT_LIMIT and MFR_VMON_UV_FAULT_LIMIT commands. The response to these limits are set using the VMON_OV_FAULT_RESPONSE and VMON_ UV_FAULT_RESPONSE commands.

When the device has been disabled due to a VMON fault, the user can select one of the following fault response options:

- Shut down and stay off until the fault has cleared and the device has been disabled and reenabled
- Shut down and, when the fault is no longer present, attempt to restart
- Shut down and restart continuously after a delay

The default response from an overvoltage or undervoltage VMON fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (option 1).

SMBus Communications

The ZL8800 provides a SMBus digital interface. The ZL8800 can be used with any standard 2-wire SMBus host device. In addition, the device is compatible with SMBus version 2.0 and includes a SALRT line to help reduce bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor can be tied to VR5 or to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the ZL8800 (nominally 4mA). A pull-up resistor of 10kΩ is a good value for most applications.

SMBus data and clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V, respectively, will cause command transmissions to be interrupted and result in slow bus operation or missed commands. A 10kΩ resistor provides good performance on an SMBus with fewer than 10 devices.

The ZL8800 accepts most standard PMBus commands. When enabling the device with the ON_OFF_CONFIG command, it is recommended that the enable pin is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the SMBus are compliant to the PMBus command standards. Any device that can malfunction in a way that permanently shorts SMBus lines will disable PMBus communications. Incomplete PMBus commands can also cause the ZL8800 to halt PMBus communications. This can be corrected by disabling, then reenabling the device.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil Digital-DC devices and within the ZL8800 itself. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. **The DDC pin must be pulled up to VR5 (or configured as a push-pull output using the GLOBAL_USER_CONFIG command) even if the ZL8800 is operating in standalone.** In addition, the DDC pin must be pulled up or configured as a push-pull output **before** the Enable pin is set high. Push-pull mode can be used only when the ZL8800 is operating in standalone mode. The DDC pins on all Digital-DC devices that use sequencing, fault spreading, or current sharing must be connected together. The DDC pins on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus to guarantee the rise time as follows:

Rise time = $R_{PU} * C_{LOAD} \leq 1\ \mu s$

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor must be tied to VR5. Generally, each device connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) and the pull-down current capability of the ZL8800 (nominally 4mA). As with SMBus data and clock lines, the DDC data line should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the DDC signal can cause the voltage on this line to cross the high and low logic thresholds of 2V and 0.8V, respectively, and will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 devices on the DDC bus, a 10kΩ resistor provides good performance.

Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device so that not all devices have coincident rising edges. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to I_{RMS}^2 are reduced.

To enable phase spreading, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in "Configurable Pins" on page 13. Selecting the phase offset for the device is accomplished by selecting a device address according to the following calculation:

Phase offset = device address x 45°

This behavior is illustrated in Table 7:

TABLE 7. PHASE OFFSET

ADDRESS LSB	PHASE OFFSET (°)	ADDRESS LSB	PHASE OFFSET (°)
0	0	8	0
1	45	9	45
2	90	A	90
3	135	B	135
4	180	C	180
5	225	D	225
6	270	E	270
7	315	F	315

The phase offset of each device can also be set to any value between 0° and 360° in 22.5° increments using the INTERLEAVE PMBus command.

Output Sequencing

A group of Intersil devices can be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage to avoid latch-up from occurring. Multidevice sequencing can be achieved by configuring each device using the SEQUENCE PMBus command.

Multiple device sequencing is achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain.

The enable (EN) pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Sequencing can also be accomplished by connecting the enable pin of a sequel device to the Power-good pin of a prequel device. Sequencing is also achieved by using the TON_DELAY and TON_RISE commands and choosing appropriate delay and rise durations such that sequel devices start after their associated prequel devices. The drawback to this method is that if a prequel device fails to start properly, its sequel device will still start and ramp on according to its delay and rise time settings.

Fault Spreading

Digital DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to restart in their prescribed order if configured to do so.

Active Current Sharing

The two channels of the ZL8800 can be used in parallel to create a dual phase power rail. The device outputs will share the current equally within a few percent.

Figure 10 shows a typical connection for a dual phase application. When used in this configuration, the ZL8800 can current share between phases without using output voltage droop.

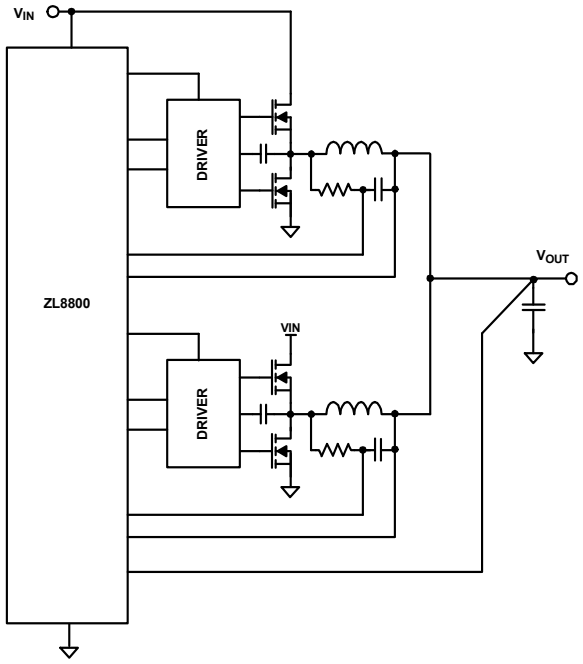


FIGURE 10. DUAL PHASE EXAMPLE

Temperature Monitoring Using XTEMP Pin

Each channel of the ZL8800 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA, or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 11 on page 21 illustrates the typical connections required. A noise filtering capacitor, not exceeding 100pF, should be connected across the external temperature sensing device. The external temperature sensors can be used to provide the temperature reading for over-temperature and under-temperature faults. The external sensors can also be used to provide more accurate temperature compensation for inductor DCR current sensing by being placed

close to the inductor. These options for the external temperature sensors are selected using the USER_CONFIG PMBus command.

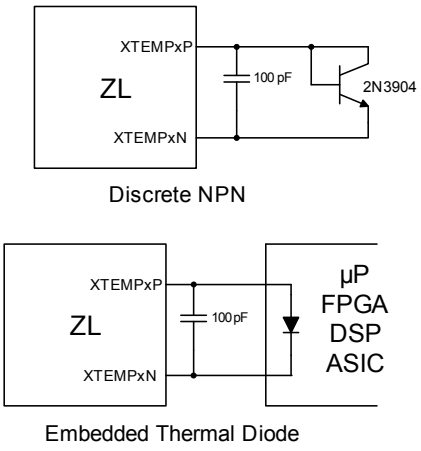


FIGURE 11. EXTERNAL TEMPERATURE MONITORING

Nonvolatile Memory and Security Features

The ZL8800 has internal nonvolatile memory that stores user configurations. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. During the initialization process, the ZL8800 checks for stored values contained in its internal non-volatile memory. The ZL8800 offers two internal memory storage units that are accessible by the user as follows:

- **Default Store**: A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory settings.
- **User Store**: The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

The User Store takes priority over the Default Store. If there are no values set in the User or Default Store, the device will use the pin-strap setting value.

DC/DC Converter Design

The ZL8800 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external driver, MOSFETs, capacitors, and an inductor to perform power conversion.

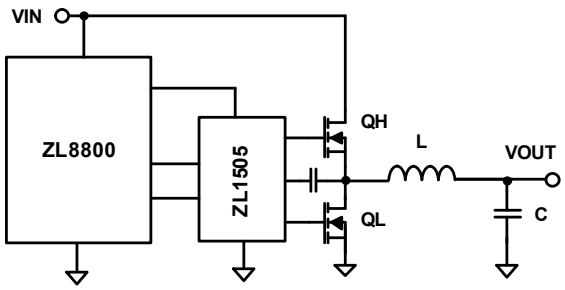


FIGURE 12. SYNCHRONOUS BUCK CONVERTER

Figure 12 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

DUAL OUTPUT PWM PER CHANNEL

The ZL8800 has been designed to provide independent upper and lower FET drive signals to a two-input MOSFET driver such as the ZL1505.

The ZL8800 uses adaptive dead time control to improve the power conversion efficiency. The ZL8800 monitors the power converter's operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side driver input signals to optimize the overall efficiency of the power supply.

The ZL8800 can also be used with single-ended DrMOS integrated driver and MOSFET devices. Power supplies using DrMOS devices can be made smaller than discrete solutions using separate drivers and MOSFETs, but at a slightly lower efficiency. The option to use DrMOS or drivers and discrete MOSFETs is set using the USER_CONFIG command.

Power Train Component Selection

The ZL8800 is a dual output or dual phase synchronous buck converter that uses external drivers, MOSFETs, inductors, and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 8 must be known.

TABLE 8. POWER SUPPLY REQUIREMENTS

PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	12V
Output Voltage (V_{OUT})	1.2V
Output Current (I_{OUT})	30A
Output Voltage Ripple (V_{orip})	1% of V_{OUT}
Output Load Step (I_{ostep})	50% of I_o
Output Load Step Rate	10A/µs
Output Deviation Due to Load Step	±2%
Maximum PCB Temperature	85°C
Desired Efficiency	90%
Other Considerations	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors, however, these components are physically large.

To start the design, select a switching frequency based on Table 9. This frequency is a starting point and can be adjusted as the design progresses.

TABLE 9. CIRCUIT DESIGN CONSIDERATIONS

FREQUENCY RANGE	EFFICIENCY	CIRCUIT SIZE
200 to 400kHz	Highest	Larger
400 to 800kHz	Moderate	Smaller
800kHz to 1.33MHz	Lower	Smallest

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (ΔI_L), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to 30 to 50% of the maximum output current (I_{OUT}).

$\Delta I_L = 0.5 * I_{OUT}$

Now the output inductance can be calculated using the following equation, where V_{IN} is the input voltage:

$$L = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{sw} \times \Delta I_L} \quad \text{(EQ. 4)}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I}{2} \quad \text{(EQ. 5)}$$

Select an inductor rated for the average DC current and with saturation current rating above the peak current calculated above.

After an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{\ 2} \quad \text{(EQ. 6)}$$

I_{Lrms} is given by:

$$I_{Lrms} = \sqrt{I_{OUT}^{\ 2} + \frac{(\Delta I_L)^2}{12}} \quad \text{(EQ. 7)}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation (V_{step}) during transient load steps and low output voltage ripple (ΔV). However, capacitors with low ESR, such as X5R and X7R dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in the following equations:

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \frac{\Delta V}{2}} \quad \text{(EQ. 8)}$$

$$ESR = \frac{\Delta V}{2 \times \Delta I_L} \quad \text{(EQ. 9)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$\Delta V = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times f_{sw} \times C_{OUT}} \quad \text{(EQ. 10)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the ΔV should be less than the desired maximum output ripple.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{inRMS}) can be determined from the following equation:

$$I_{inRMS} = I_{OUT} \times \sqrt{D} \quad \text{(EQ. 11)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated above the ripple current calculated above and the maximum expected input voltage.

QL SELECTION

The bottom or lower MOSFET should be selected with the lowest possible $r_{DS(ON)}$ while maintaining the desired circuit size and cost.

Calculate the RMS current in QL as follows:

$$I_{QLRMS} = I_{OUT} \times \sqrt{1-D} \quad \text{(EQ. 12)}$$

Calculate the power dissipated due to $r_{DS(ON)}$ as follows:

$$P_{QL} = R_{DSON}\left(I_{botrms}\right)^2 \quad \text{(EQ. 13)}$$

Note that the $r_{DS(ON)}$ given in the manufacturer's datasheet is measured at +25°C. The actual $r_{DS(ON)}$ in the end-use application will be much higher. Select a candidate MOSFET and calculate the required gate drive current as follows:

$$I_g = f_{SW} \times Q_g \quad \text{(EQ. 14)}$$

MOSFETs with lower $r_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off.

QH SELECTION

In addition to the $r_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. Select QH with a lower gate charge, keeping in mind that QH's $r_{DS(ON)}$ will be higher as a result. As was done with QL, calculate the RMS current as follows:

$$I_{QHRMS} = I_{OUT} \times \sqrt{D} \quad \text{(EQ. 15)}$$

$$P_{QH} = R_{DSON}\left(I_{QHRMS}\right)^2 \quad \text{(EQ. 16)}$$

Next, calculate the switching time using:

$$t_{SW} = \frac{Q_g}{I_{DR}} \quad \text{(EQ. 17)}$$

where Q_g is the gate charge of the selected QH and I_{DR} is the peak gate drive current available from the gate drive IC.

To calculate the switching time, use the ZL1505s minimum guaranteed drive current of 3 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad \text{(EQ. 18)}$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad \text{(EQ. 19)}$$

MOSFET THERMAL CHECK

After the power dissipations for QH and QL have been calculated, the MOSFET's junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum Printed Circuit Board (PCB) temperature, calculate the junction temperature as follows:

$$T_{j\max} = T_{pcb} + \left(P_Q \times R_{th}\right) \quad \text{(EQ. 20)}$$

To calculate power losses and junction temperature rise in DrMOS devices, consult the datasheet and application notes for the DrMOS device selected.

EFFICIENCY OPTIMIZED DRIVER DEAD TIME CONTROL

The ZL8800 uses a closed loop algorithm to optimize the dead time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

Minimize this dead time to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by the equation:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 21)}$$

However, the real duty cycle sometimes extends beyond the ideal. Dead time can be manipulated to improve efficiency. The ZL8800 has an internal algorithm that constantly adjusts dead time nonoverlap to minimize duty cycle, thus maximizing efficiency. This circuit will null out dead time differences due to component variation, temperature, and loading effects. This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times, and circuit layout. In addition, it does not require drive or MOSFET voltage or current waveform measurements. Adaptive dead time is enabled using the DEADTIME_CONFIG PMBus command. Adaptive dead time is only effective when a discrete driver (such as the ZL1505) and MOSFETs are used. When DrMOS devices are selected using USER_CONFIG, adaptive dead time is automatically disabled. Dead time minimum and maximum limits can be set using the DEADTIME PMBus command.

Monitoring Through SMBus

A system controller can monitor a wide variety of different ZL8800 parameters through the SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of preconfigured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Input current
- Output current
- Internal junction temperature
- Temperature of an external device
- Switching frequency
- Duty cycle
- Fault status information

The PMBus host should respond to SALRT as follows:

1. The ZL device pulls SALRT Low.
2. The PMBus host detects that SALRT is now low and performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. The PMBus host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Refer to the "PMBus Command Summary" on page 25 for details on how to monitor specific parameters through the SMBus interface.

PMBus Command Summary

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
00h	PAGE	Selects Controller 0, 1, or both	R/W	BIT	00h	Both controllers addressed
01h	OPERATION	Enable/disable, margin settings	R/W	BIT	00h	Immediate off, nominal margin
02h	ON_OFF_CONFIG	On/off configuration settings	R/W	BIT	17h	ENABLE pin control, active high
03h	CLEAR_FAULTS	Clears faults	Write	N/A	N/A	N/A
11h	STORE_DEFAULT_ALL	Stores values to default store	Write	N/A	N/A	N/A
12h	RESTORE_DEFAULT_ALL	Restores values from default store	Write	N/A	N/A	N/A
15h	STORE_USER_ALL	Stores values to user store	Write	N/A	N/A	N/A
16h	RESTORE_USER_ALL	Restores values from user store	Write	N/A	N/A	N/A
20h	VOUT_MODE	Reports V_{OUT} mode and exponent	Read	BIT	13h	Linear mode, exponent = -13
21h	VOUT_COMMAND	Sets nominal V_{OUT} set-point	R/W	L16u		Pin-strap setting
23h	VOUT_CAL_OFFSET	Applies offset voltage to V_{OUT} set-point	R/W	L16s	0000h	0V
24h	VOUT_MAX	Sets maximum V_{OUT} set-point	R/W	L16u		1.1 X VOUT_COMMAND pin-strap setting
25h	VOUT_MARGIN_HIGH	Sets V_{OUT} set-point during margin high	R/W	L16u		1.05 x VOUT_COMMAND pin-strap setting
26h	VOUT_MARGIN_LOW	Sets V_{OUT} set-point during margin low	R/W	L16u		0.95 x VOUT_COMMAND pin-strap setting
27h	VOUT_TRANSITION_RATE	Sets V_{OUT} transition rate during margin commands	R/W	L11	BA00h	1V/ms
28h	VOUT_DROOP	Sets V/I slope	R/W	L11	0000h	0mV/A
33h	FREQUENCY_SWITCH	Sets switching frequency	R/W	L11		Pin-strap setting
37h	INTERLEAVE	Configures phase offset during group operation	R/W	BIT		Set by pin-strapped PMBus address
38h	IOUT_CAL_GAIN	Sets impedance of current sense circuit	R/W	L11	AA66h	0.3mΩ
39h	IOUT_CAL_OFFSET	Sets an offset to I_{OUT} sense circuit	R/W	L11	0000h	0A
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold	R/W	L16u		1.15 x VOUT_COMMAND pin-strap setting
41h	VOUT_OV_FAULT_RESPONSE	Sets the V_{OUT} overvoltage fault response	R/W	BIT	80h	Disable, no retry
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold. Must be set lower than POWER_GOOD_ON	R/W	L16u		0.85 x VOUT_COMMAND pin-strap setting
45h	VOUT_UV_FAULT_RESPONSE	Sets the V_{OUT} undervoltage fault response	R/W	BIT	80h	Disable, no retry
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold	R/W	L11	DA80h	20A
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold	R/W	L11	DD80h	-20A
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault limit	R/W	L11	EBE8h	+125˚C
50h	OT_FAULT_RESPONSE	Sets the over-temperature fault response	R/W	BIT	80h	Disable, no retry
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit	R/W	L11	EB70h	+110°C
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit	R/W	L11	DC40h	-30°C
53h	UT_FAULT_LIMIT	Sets the under-temperature fault limit	R/W	L11	E530h	-45°C
54h	UT_FAULT_RESPONSE	Sets the under-temperature fault response	R/W	BIT	80h	Disable, no retry
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold	R/W	L11	D380h	14V

PMBus Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
56h	VIN_OV_FAULT_RESPONSE	Sets the V_{IN} overvoltage fault response	R/W	BIT	80h	Disable, no retry
57h	VIN_OV_WARN_LIMIT	Sets the V_{IN} overvoltage warning threshold	R/W	L11	D360h	13.5V
58h	VIN_UV_WARN_LIMIT	Sets the V_{IN} undervoltage warning threshold	R/W	L11	N/A	1.03 x VIN_UV_FAULT_LIMIT pin-strap setting
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold	R/W	L11	N/A	Pin-strap setting
5Ah	VIN_UV_FAULT_RESPONSE	Sets the V_{IN} undervoltage fault response	R/W	BIT	80h	Disable, no retry
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-good indication. Must be set higher than VOUT_UV_FAULT_LIMIT	R/W	L16u	N/A	0.9 x VOUT_COMMAND pin-strap setting
60h	TON_DELAY	Sets the delay time from enable to V_{OUT} rise	R/W	L11	CA80h	5ms
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY	R/W	L11	CA80h	5ms
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall	R/W	L11	0000h	0ms (immediate off)
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY	R/W	L11	CA80h	5ms
78h	STATUS_BYTE	Summary of most critical faults	Read	BIT	00h	No faults
79h	STATUS_WORD	Summary of critical faults	Read	BIT	0000h	No faults
7Ah	STATUS_VOUT	Reports V_{OUT} warnings/faults	Read	BIT	00h	No faults
7Bh	STATUS_IOUT	Reports I_{OUT} warnings/faults	Read	BIT	00h	No faults
7Ch	STATUS_INPUT	Reports input warnings/faults	Read	BIT	00h	No faults
7Dh	STATUS_TEMP	Reports temperature warnings/faults	Read	BIT	00h	No faults
7Eh	STATUS_CML	Reports communication, memory, and logic errors	Read	BIT	00h	No errors
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock synchronization faults	Read	BIT	00h	No faults
88h	READ_VIN	Reports input voltage measurement	Read	L11	N/A	N/A
89h	READ_IIN	Reports input current measurement	Read	L11	N/A	N/A
8Bh	READ_VOUT	Reports output voltage measurement	Read	L16u	N/A	N/A
8Ch	READ_IOUT	Reports output current measurement	Read	L11	N/A	N/A
8Dh	READ_TEMPERATURE_1	Reports internal temperature measurement	Read	L11	N/A	N/A
8Eh	READ_TEMPERATURE_2	Reports external temperature measurement	Read	L11	N/A	N/A
94h	READ_DUTY_CYCLE	Reports actual duty cycle	Read	L11	N/A	N/A
95h	READ_FREQUENCY	Reports actual switching frequency	Read	L11	N/A	N/A
99h	MFR_ID	Sets a user defined identification	R/W	ASC	N/A	<null>
9Ah	MFR_MODEL	Sets a user defined model	R/W	ASC	N/A	<null>
9Bh	MFR_REVISION	Sets a user defined revision	R/W	ASC	N/A	<null>
9Ch	MFR_LOCATION	Sets a user defined location identifier	R/W	ASC	N/A	<null>
9Dh	MFR_DATE	Sets a user defined date	R/W	ASC	N/A	<null>
9Eh	MFR_SERIAL	Sets a user defined serialized identifier	R/W	ASC	N/A	<null>

PMBus Command Summary (Continued)

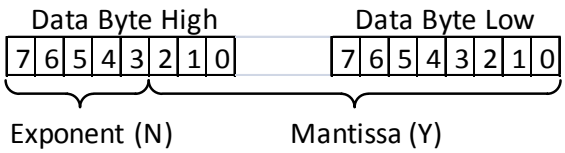
CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
ADh	IC_DEVICE_ID	Reports device identification information	Read	CUS	49A02400h	Intersil, ZL8800
AEh	IC_DEVICE_REV	Reports device revision information	Read	CUS	00000000h	Initial Release
B0h	USER_DATA_00	Sets a user defined data	R/W	ASC	N/A	<null>
BFh	DEADTIME_MAX	Sets the max dead time value for the adaptive dead time	R/W	BIT	3838h	56ns, 56ns
D0h	ISENSE_CONFIG	Configures current sensing circuitry	R/W	BIT	4204h	Downslope, 5 fault count, 256ns blanking, low range
D1h	USER_CONFIG	Configures several user-level features	R/W	BIT	0402h	Enable XTEMP0, 1, PG open-drain, DRMOS enabled
D2h	IIN_CAL_GAIN	Sets the resistance of the input current sensing resistor	R/W	L11	C200h	2mΩ
D3h	DDC_CONFIG	Configures the DDC addressing and current sharing	R/W	BIT	N/A	Set by pin-strapped PMBus address
D4h	POWER_GOOD_DELAY	Sets the delay between PG threshold and PG assertion	R/W	L11	BA00h	1ms
D6h	INDUCTOR	Sets the inductor value	R/W	L11	B23D	0.56µH
D7h	VOUT_MARGIN_RATIO	% MARGIN_HIGH, LOW above/below VOUT_COMMAND	R/W	L11	CA80h	5%
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection	R/W	BIT	00h	Low-side FET off on fault, 1 violation triggers fault
D9h	XTEMP_SCALE	Calibrates external temperature sensor	R/W	L11	BA00h	1/°C
DAh	XTEMP_OFFSET	Offset calibration for external temperature sensor	R/W	L11	0000h	No offset
DCh	TEMPCO_CONFIG	Sets tempco settings	R/W	BIT	27h	3900ppm/°C
DDh	DEADTIME	Sets default dead time settings	R/W	L8s	1010h	16ns/16ns
DEh	DEADTIME_CONFIG	Configures the adaptive dead time optimization mode	R/W	BIT	0808h	Adaptive dead time enabled, 8ns/8ns
DFh	ASCR_CONFIG	Configures the ASCR settings	R/W	BIT	015A0100h	Gain = 256, Residual = 90
E0h	SEQUENCE	DDC rail sequencing configuration	R/W	BIT	00h	Prequel and sequel disabled
E1h	TRACK_CONFIG	Configures voltage tracking modes	R/W	BIT	00h	Tracking disabled
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION and V_{OUT}	R/W	BIT	000000h	Ignore broadcast, sequenced shutdown
E4h	DEVICE_ID	Returns the device identifier string	Read	ASC	N/A	ZL8800, current revisions
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response	R/W	BIT	80h	Disable, no retry
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response	R/W	BIT	80h	Disable, no retry
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold	R/W	L11	DA00h	16A
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold	R/W	L11	DE00h	-16A
E9h	USER_GLOBAL_CONFIG	Sets options pertaining to advanced features	R/W	BIT	0000h	Numerous device settings
EAh	SNAPSHOT	32-byte read back of parametric and status values	Read	BIT	N/A	<null>

PMBus Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
EBh	BLANK_PARAMS	Indicates recently saved parameter values	Read	BIT	FFF...FFFh	<null>
F0h	LEGACY_FAULT_GROUP	Configures fault group compatibility with older Intersil digital power devices	R/W	BIT	00000000h	<null>
F3h	SNAPSHOT_CONTROL	Snapshot feature control command	R/W	BIT	N/A	N/A
F4h	RESTORE_FACTORY	Restores device to the hard-coded default values	Write	N/A	N/A	N/A
F5h	MFR_VMON_OV_FAULT_LIMIT	Sets the VMON overvoltage fault threshold	R/W	L11	D300h	12V
F6h	MFR_VMON_UV_FAULT_LIMIT	Sets the VMON undervoltage fault threshold	R/W	L11	CA40h	4.5V
F7h	MFR_READ_VMON	Reads the VMON voltage	Read	L11	N/A	N/A
F8h	VMON_OV_FAULT_RESPONSE	Configures the VMON overvoltage fault response	R/W	BIT	80h	Disable, no retry
F9h	VMON_UV_FAULT_RESPONSE	Configures the VMON undervoltage fault response	R/W	BIT	80h	Disable, no retry
FAh	SECURITY_LEVEL	Reports the security level	Read	Hex	01h	Public security level
FBh	PRIVATE_PASSWORD	Sets the private password string	R/W	ASC	00...00h	<null>
FCh	PUBLIC_PASSWORD	Sets the public password string	R/W	ASC	00...00h	<null>
FDh	UNPROTECT	Identifies which commands are protected	R/W	Custom	FF...FFh	N/A

PMBus Data Formats

Linear-11 (L11)
The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent a real world decimal value (X).



The relation between a real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent a real world decimal value (X). The relation between a real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent a real world decimal value (X).
The relation between a real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)
An explanation of the Bit Field format is provided in "PMBus Command Detail" on page 29.

Custom (CUS)
An explanation of the Custom data format is provided in "PMBus Command Detail" on page 29. A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)
A variable length string of text characters in the ASCII data format.

PMBus Command Detail

PAGE (00h)

Definition: Selects Controller 0, Controller 1, or both Controller 0 and Controller 1 to receive commands. All commands following this command will be received and acted on by the selected controller or controllers.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: No

Default Value: 00h (Page 0)

Units: N/A

COMMAND	PAGE (00h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:4	BITS 3:0	PAGE
0000	0000	0
0000	0001	1
1111	1111	Both

OPERATION (01h)

Definition: Sets Enable, Disable, and V_{OUT} Margin settings. Data values of OPERATION that force margin high or low only take effect when the MGN pin is left open (that is, in the NOMINAL margin state). This command can also be monitored to read the operating state of the device on bits 7:6.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (immediate off)

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:6	BITS 5:4	BITS 3:0 (NOT USED)	UNIT ON OR OFF	MARGIN STATE
00	00	0000	Immediate off (No sequencing)	N/A
01	00	0000	Soft off (With sequencing)	N/A
10	00	0000	On	Nominal
10	01	0000	On	Margin Low
10	10	0000	On	Margin High

NOTE: Bit combinations not listed above may cause command errors.

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 17h (ENABLE pin control, active high, turn off output immediately – no ramp down)

Units: N/A

COMMAND	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
7:5	Not Used	000	Not used.
4:2	Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin, OPERATION command, or when both the Enable pin and OPERATION command are valid.	000	Device starts any time power is present regardless of ENABLE pin or OPERATION command states.
		101	Device starts from the ENABLE pin only.
		110	Device starts from the OPERATION command only.
		111	Device starts when the ENABLE pin is active and OPERATION “on” command has been sent.
1	Polarity of the ENABLE pin	0	Active low (Pull pin low to start the device)
		1	Active high (Pull pin high to start the device)
0	ENABLE pin action when commanding the unit to turn off	0	Use the programmed ramp down settings
		1	Turn off the output immediately

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Paged or Global: Global

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores all current PMBus values from the operating memory into the nonvolatile DEFAULT Store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation. The device will be unresponsive for 20ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus settings from the nonvolatile DEFAULT Store memory into the operating memory. These settings are loaded at power-up if not superseded by settings in USER store. Security level is changed to level 1 following this command. This command should not be used during device operation. The device will be unresponsive for 20ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation. The device will be unresponsive for 20ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command should not be used during device operation. The device will be unresponsive for 20ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 13h (Linear Mode, Exponent = -13)

Units: N/A

COMMAND	VOUT_MODE (20h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1

MODE	BITS 7:5	BITS 4:0 (PARAMETER)
Linear	000	Five-bit, two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set to be higher than the lowest setting of either VOUT_MAX or 110% of the pin-strap V_{OUT} setting.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: Pin-strap setting

Units: Volts

Equation: V_{OUT} = VOUT_COMMAND × 2^{-13}

Range: 0 to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27,034

Target voltage equals 27034 × 2^{-13} = 3.3V

COMMAND	VOUT_COMMAND (21h)															
Format	Linear, Unsigned Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	Pin-strap Setting															

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: Volts

Equation: V_{OUT} cal offset = VOUT_CAL_OFFSET× 2^{-13}

Range: ±3.99V

COMMAND	VOUT_CAL_OFFSET (23h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. This command provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. If a VOUT_COMMAND is sent with a value higher than VOUT_MAX, the device will set the output voltage to VOUT_MAX.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.10 x VOUT_COMMAND pin-strap setting

Units: Volts

Equation: V_{OUT} max = VOUT_MAX × 2^{-13}

Range: 0V to 5.5V

COMMAND	VOUT_MAX (24h)															
Format	Linear, Unsigned Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.10 x VOUT_COMMAND Pin-strap Setting															

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W word

Protectable: Yes

Default Value: 1.05 x VOUT_COMMAND setting

Units: V

Equation: V_{OUT} margin high = VOUT_MARGIN_HIGH x 2^{-13}

Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VOUT_COMMAND															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.95 x VOUT_COMMAND pin-strap setting

Units: V

Equation: V_{OUT} margin low = VOUT_MARGIN_LOW

Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_LOW (26h)															
Format	Linear, Two’s Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VOUT_COMMAND															

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible. This commanded rate does not apply when the device is commanded to turn on or to turn off.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0V/ms)

Units: V/ms

Equation: VOUT_TRANSITION_RATE = $Y \times 2^N$

Range: 0.1 to 4V/ms

COMMAND	VOUT_TRANSITION_RATE (27h)															
Format	Linear Data Format															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

VOUT_DROOP (28h)

Definition: Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases with increasing output current. For devices that are set to sink output current (negative output current), the output voltage continues to increase as the output current is negative. VOUT_DROOP is not needed for 2-phase operation with a single ZL8800.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0mV/A)

Units: mV/A

Equation: VOUT_DROOP = $Y \times 2^N$

Range: 0 to 40mV/A

COMMAND	VOUT_DROOP (28h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is used, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation f_{SW} = 16MHz/n where 11 ≤ n ≤ 80

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Pin-strap setting

Units: kHz

Equation: FREQUENCY_SWITCH = $Y \times 2^N$

Range: 200kHz to 1.33MHz

COMMAND	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Pin-strapped Value															

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. An INTERLEAVE group number and desired phase position are specified. Interleave is used for setting the phase offset in noncurrent sharing devices. For current sharing rails, INTERLEAVE is ignored and DDC_CONFIG is used to configure the phase relationship between current sharing phases.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by pin-strapped PMBus address, page 1 is automatically offset from page 0

Units: N/A

COMMAND	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	Four LSBs of SMBus Address				Four LSBs of SMBus Address			

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	Not Used	0	Not used.
7:4	Group Number	0 to 15	Sets the group number. A value of 0 is interpreted as 16.
3:0	Position of Device	0 to 15	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 will have a 22.5° offset.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current-sense circuit to calculate output current at +25°C.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: AA66h (0.3mΩ)

Units: mΩ

Equation: IOUT_CAL_GAIN = $Y \times 2^N$

COMMAND	IOUT_CAL_GAIN (38h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0

IOUT_CAL_OFFSET (39h)

Definition: Nulls out any offsets in the output current-sensing circuit, and compensates for delayed measurements of current ramp due to Isense blanking time.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0A)

Units: A

Equation: IOUT_CAL_OFFSET = $Y \times 2^N$

COMMAND	IOUT_CAL_OFFSET (39h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VOUT_COMMAND pin-strap setting

Units: V

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT$\times 2^{-13}$

Range: 0V to 7.99V

COMMAND	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VOUT_COMMAND															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Shut down immediately, no retries)

Units: Retry time = 70ms

COMMAND	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the device is restarted.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp, before Power-good is asserted, or when the device is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below POWER_GOOD_ON.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.85 x VOUT_COMMAND pin-strap setting

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT$\times 2^{-13}$

Range: 0V to 7.99V

COMMAND	VOUT_UV_FAULT_LIMIT (44h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.85 x VOUT_COMMAND															

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response. Note that VOUT UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances, this will cause the output to stay fixed below the Power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Shut down immediately, no retries)

Units: Retry time unit = 70ms

COMMAND	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Not used.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded for the number of consecutive samples as defined in ISENSE_CONFIG. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_AVG_OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DA80h (20A)

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_OC_FAULT_LIMIT (46h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded for the number of consecutive sample as defined in ISENSE_CONFIG. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_AVG_UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -20A (DD80h)

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_UC_FAULT_LIMIT (4Bh)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-1 x IOUT_OC_FAULT_LIMIT															

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_WARN_LIMIT to clear this fault.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EBE8h (+125°C)

Units: Celsius

Equation: OT_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to +175

COMMAND	OT_FAULT_LIMIT (4Fh)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device what action to take in response to an over-temperature fault. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Shut down immediately, no retries)

Units: Retry time unit = 210ms

COMMAND	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110°C)

Units: Celsius

Equation: OT_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 175

COMMAND	OT_WARN_LIMIT (51h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature Warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30°C)

Units: Celsius

Equation: UT_WARN_LIMIT = $Y \times 2^N$

Range: -55 to +25

COMMAND	UT_WARN_LIMIT (52h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit at which it should indicate an under-temperature fault. Note that the temperature must rise above UT_WARN_LIMIT to clear this fault.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: E530h (-45°C)

Units: Celsius

Equation: UT_FAULT_LIMIT = $Y \times 2^N$

Range: -55 to +25

COMMAND	UT_FAULT_LIMIT (53h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the table below. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Shut down immediately, no retries)

Units: Retry time unit = 210ms

COMMAND	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the device is restarted.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: D380h (14V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the table below. The retry time is the time between restart attempts.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retry)

Units: Retry time unit = 70ms

COMMAND	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold as defined by the table below. In response to the OV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, Sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D360h (13.5V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_OV_WARN_LIMIT (57h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 1.03 x VIN_UV_FAULT_LIMIT pin-strap setting

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_UV_WARN_LIMIT (58h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1.03 x VIN_UV_FAULT_LIMIT															

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Pin-strap setting

Units: V

Equation: VIN_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Pin-Strapped Value															

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the table below. The retry time is the time between restart attempts.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retries)

Units: Retry time unit = 70ms

COMMAND	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used.
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and de-asserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. POWER_GOOD_ON must be set to a value above VOUT_UV_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned.

Type: R/W

Protectable: Yes

Default Value: 0.9 x VOUT_COMMAND pin-strap setting

Units: V

COMMAND	POWER_GOOD_ON (5Eh)															
Format	Linear, Unsigned Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VOUT_COMMAND															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h, 5ms

Units: ms

Equation: TON_DELAY = $Y \times 2^N$

Range: 0 to 5 seconds. The minimum delay time is 3ms. Values below 3ms will result in a delay time of 3ms.

COMMAND	TON_DELAY (60h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TON_RISE (61h)

Definition: Sets the rise time of VOUT after ENABLE and TON_DELAY.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: CA80h, 5ms

Units: ms

Equation: TON_RISE = $Y \times 2^N$

Range: 1 to 100ms. The minimum rise time is 1ms. Values below 1ms will default to 1ms. Short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

COMMAND	TON_RISE (61h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of VOUT fall.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h, 0ms

Units: ms

Equation: TON_DELAY = $Y \times 2^N$

Range: 0 to 5 seconds. Values less than 0.5ms will set the device to immediate off (no TOFF_FALL ramp down).

COMMAND	TOFF_DELAY (64h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 5ms (CA80h)

Units: ms

Equation: TOFF_FALL = $Y \times 2^N$

Range: 0 to 100ms. Although values can be set below 0.50ms, fall time accuracy cannot be guaranteed. In addition, short fall times may cause excessive negative output current to flow, thus triggering undercurrent faults at shut-down.

COMMAND	TOFF_FALL (65h)															
Format	Linear, Two's Complement Binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1 x TON_RISE															

STATUS_BYTE (78h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read only

Protectable: No

Default Value: 00h

Units: N/A

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read only

Protectable: No

Default Value: 0000h

Units: N/A

COMMAND	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal is negated if present (Note 17).
10	NOT USED	Not used.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

NOTE:

17. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	Not Used	Not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output under current fault has occurred.
3:0	Not Used	Not used.

STATUS_INPUT (7Ch)

Definition: Returns input voltage and input current status information.
Paged or Global: Global
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	Not Used	Not used.

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_TEMP (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	Not Used	Not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any Communications, Logic, and/or Memory errors.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	A packet error was detected in the PMBus command.
4:2	Not used.
1	A PMBus command tried to write to a read only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used.

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults. Note: The VMON OV/UV warnings are set at ±10% of the VMON_XX_FAULT commands.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	MEANING
7:6	Not Used	Not used.
5	VMON UV Warning	The VMON voltage has dropped below the VMON UV warning limit which is automatically set to 10% above MFR_VMON_UV_FAULT_LIMIT (1.1 * MFR_VMON_UV_FAULT_LIMIT).
4	VMON OV Warning	The VMON voltage has risen above the VMON OV warning limit which is automatically set to 10% below MFR_VMON_OV_FAULT_LIMIT (0.9 * MFR_VMON_UV_FAULT_LIMIT).
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Not Used	Not used.
1	VMON UV Fault	The VMON voltage has dropped below MFR_VMON_UV_FAULT_LIMIT.
0	VMON OV Fault	The VMON voltage has risen above MFR_VMON_OV_FAULT_LIMIT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: No

Default Value: N/A

Units: V

Equation: READ_VIN = $Y \times 2^N$

Range: N/A

COMMAND	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IIN (89h)

Definition: Returns the input current reading.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IIN = $Y \times 2^N$
Range: N/A

COMMAND	READ_IIN (89h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: Read only
Protectable: No
Default Value: N/A
Equation: READ_VOUT = READ_VOUT × 2^{-13}
Units: V

COMMAND	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IOUT (8Ch)

Definition: Returns the output current reading.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IOUT = $Y \times 2^N$
Range: N/A

COMMAND	READ_IOUT (8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading internal to the device.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read only
Protectable: No
Default Value: N/A
Units: ˚C
Equation: READ_TEMPERATURE_1 = $Y \times 2^N$
Range: N/A

COMMAND	READ_INTERNAL_TEMP (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_2 (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read only
Protectable: No
Default Value: N/A
Units: ˚C
Equation: READ_TEMPERATURE_2 = $Y \times 2^N$
Range: N/A

COMMAND	READ_EXTERNAL_TEMP (8Eh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: No

Default Value: N/A

Units: %

Equation: READ_DUTY_CYCLE = $Y \times 2^N$

Range: 0 to100%

COMMAND	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Default Value: N/A

Units: kHz

Equation: READ_FREQUENCY = $Y \times 2^N$

Range: N/A

COMMAND	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

MFR_ID (99h)

Definition: Sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Paged or Global: Global

Data Length in Bytes: 4

Data Format: CUS

Type: Block Read

Protectable: No

Default Value: 49A02400h

Units: N/A

COMMAND	IC_DEVICE_ID (ADh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	MFR code	ID High Byte	ID Low Byte	Reserved
Default Value	49h	A0h	24h	00h

IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Paged or Global: Global

Data Length in Bytes: 4

Data Format: CUS

Type: Block Read

Protectable: No

Default Value: 00000000h

Units: N/A

COMMAND	IC_DEVICE_REV (AEh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	Firmware Major	Firmware Minor	Factory Configuration	Reserved
Default Value	00h	00h	00h	00h

USER_DATA_00 (B0h)

Definition: Sets a user defined data string not to exceed 32bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

DEADTIME_MAX (BFh)

Definition: Sets the maximum dead time value for the PWMH and PWML outputs. This limit applies during frozen or adaptive dead time algorithm modes (see DEADTIME_CONFIG).

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 3838h (56ns/56ns)

Units: ns

Range: 0 to 60ns

Reference: N/A

COMMAND	DEADTIME_MAX (BFh)															
Format	Bit Field/Linear-7 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15	Not Used	0	Not used.
14:8	Sets the maximum HIGH to LOW dead time	H	Limits the maximum allowed HIGH to LOW dead time when using the adaptive dead time algorithm. dead time = Hns (signed)
7	Not Used	0	Not used.
6:0	Sets the maximum LOW to HIGH dead time	L	Limits the maximum allowed LOW to HIGH dead time when using the adaptive dead time algorithm. dead time = Lns (signed)

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Bit Field
Type: R/W word
Protectable: Yes
Default Value: 4204h (256ns, 5 counts, downslope, low range)
Units: N/A
Range: N/A

COMMAND	ISENSE_CONFIG (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Current-Sense Blanking Time	00000	0	Sets the blanking time current-sense blanking time in increments of 32ns
		00001	32	
		00010	64	
		00011	96	
		00100	128	
		00101	160	
		00110	192	
		00111	224	
		01000	256	
		01001	288	
		01010	320	
		01011	352	
		01100	384	
		01101	416	
		01110	448	
		01111	480	
		10000	512	
		10001	544	
		10010	576	
		10011	608	
		10100	640	
		10101	672	
		10110	704	
		10111	736	
		11000	768	
		11001	800	
		11010	832	

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
10:8	Current-Sense Fault Count	000	1	Sets the number of consecutive overcurrent (OC) or undercurrent (UC) events required for a fault. An event can occur once during each switching cycle. For example, if 5 is selected, an OC or UC event must occur for 5 consecutive switching cycles, resulting in a delay of at least 5 switching periods.
		001	3	
		010	5	
		011	7	
		100	9	
		101	11	
		110	13	
		111	15	
7:4	Not Used	0000	Not Used	Not used
3:2	Current-Sense Control	00	Not Used	Selection of current-sensing method (DCR based: VOUT referenced)
		01	DCR (Down Slope)	
		10	DCR (Up Slope)	
		11	Not Used	
1:0	Current-Sense Range	00	Low Range	Low Range ±25mV, Medium Range ±35mV, High Range ±50mV
		01	Medium Range	
		10	High Range	
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command should be saved immediately after being written to the desired user or default store. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0402h

Units: N/A

COMMAND	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Minimum Duty Cycle	00000	0-31d	Sets the minimum duty-cycle to 2 x (VALUE + 1)/512. Must be enabled with Bit 7
10	Enable DR MOS	0	Disable	0 = PWML and PWMH are direct drive to MOSFET driver
		1	Enable	1 = PWML is DRMOS Enable, PWMH is DRMOS PWM input
9:8	Not Used	0	Not Used	Not used.
7	Minimum Duty Cycle Control	0	Disable	Control for minimum duty cycle
		1	Enable	
6	Not Used	0	Not Used	Not used.
5	VSET Select	0	VSET0	0 = Uses only VSET0 to set Pin-strapped output voltage
		1	VSET1	1 = Uses only VSET1 to set Pin-strapped output voltage
4	Margin Ratio Enable	0	Disable	Use VOUT_MARGIN_RATIO to program margin values when enabled
		1	Enable	
3	PWML disabled state	0	Low when disabled	PWML is low (off) when device is disabled (Bit 3 set to 0), or high (on) when device is disabled (Bit 3 set to 1)
		1	High when disabled	
2	Power-good Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-pull	1 = PG is push-pull output
1	XTEMP Enable	0	Disable	Enables external temperature sensor
		1	Enable	
0	XTEMP Fault Select	0	Disable	Selects external temperature sensor to determine temperature faults
		1	Enable	

IIN_CAL_GAIN (D2h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating input current at +25°C.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: C200h (2mΩ)

Units: mΩ

Equation: IIN_CAL_GAIN = $Y \times 2^N$

COMMAND	IIN_CAL_GAIN (D2h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing. To operate as a 2-phase controller, set both phases to the same Rail ID, set Phases in Rail to 2, then set each phase ID **sequentially** as 0 and 1. The ZL8800 will automatically equally offset the phases in the rail. Phase spreading is done automatically as part of the DDC_CONFIG command, the INTERLEAVE command only applies to non-current sharing rails. The ZL8800 can operate as a 2-phase controller, current sharing between its two internal phases, but does not support current sharing with other ZL8800 devices or phases.

NOTE: The output MUST be connected to VSEN0P and VSEN0N when operating as a 2-phase controller.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: PMBus address pin-strap dependent.

Units: N/A

COMMAND	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (shared output)
7:3	Not Used	00	00	Not used.
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h, 1ms

Units: ms

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0 to 5 seconds

COMMAND	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

INDUCTOR (D6h)

Definition: Informs the device of the circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: B23Dh (0.56µH)

Units: µH

Equation: INDUCTOR = $Y \times 2^N$

Range: 0 to 100µH

COMMAND	INDUCTOR (D6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	1	0	0	0	1	1	1	1	0	1

VOUT_MARGIN RATIO (D7h)

Definition: Percentage to set MARGIN_HIGH and MARGIN_LOW above and below VOUT_COMMAND when the feature is enabled by USER_CONFIG.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 5 (CA80h)

Units: %

Equation: VOUT_MARGIN_RATIO = $Y \times 2^N$

Range: 0 to 50%

COMMAND	VOUT_MARGIN_RATIO (D7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection feature

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	OVUV_CONFIG (D8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
7	Controls how an OV fault response shutdown sets the output driver state	0	An OV fault does not enable low-side power device
		1	An OV fault enables the low-side power device
6:4	Not Used	0	Not used.
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response

XTEMP_SCALE (D9h)

Definition: Sets a scalar value that is used for calibrating the external temperature. The constant is applied in the equation below to produce the read value of XTEMP through the PMBus command READ_EXTERNAL_TEMP.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0)

Units: 1/°C

Equation: $$READ_TEMPERATURE_2 = \left(ExternalTemperature \cdot \frac{1}{XTEMP_SCALE} \right) + XTEMP_OFFSET$$

Range: 0.1 to 10

COMMAND	XTEMP_SCALE (D9h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

XTEMP_OFFSET (DAh)

Definition: Sets an offset value that is used for calibrating the external temperature. The constant is applied in the equation below to produce the read value of XTEMP through the PMBus command READ_EXTERNAL_TEMP.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: 0000h (0)

Units: °C

Equation: $$READ_TEMPERATURE_2 = \left(ExternalTemperature \cdot \frac{1}{XTEMP_SCALE} \right) + XTEMP_OFFSET$$

Range: -100 to 100

COMMAND	XTEMP_OFFSET (DAh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values are applied as negative correction to a positive temperature coefficient.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 27h (3900ppm/°C)

Equation: To determine the hex value of the Tempco Correction factor (TC) for current scale of a power stage current sensing, first determine the temperature coefficient of resistance for the sensing element, α. This is calculated with the equation:

$$\alpha = \frac{R_{REF} - R}{R_{REF}(T_{REF} - T)}$$

where:

R = Sensing element resistance at temperature "T"

R_{REF} = Sensing element resistance at reference temperature T_{REF}

α = Temperature coefficient of resistance for the sensing element material

T = Temperature measured by temperature sensor, in degrees Celsius

T_{REF} = Reference temperature that α is specified at for the sensing element material

After α is determined, convert the value in units of 100ppm/°C. This value is then converted to a hex value with the following equation:

$$TC = \frac{\alpha \times 10^6}{100}$$

Typical Values: Copper = 3900ppm/°C (27h), silicon = 4800ppm/°C (30h)

Range: 0 to 6300ppm/°C

COMMAND	TEMPCO_CONFIG (DCh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	1	0	0	1	1	1

BITS	PURPOSE	VALUE	DESCRIPTION
7	Selects the temp sensor source for tempco correction	0	Selects the internal temperature sensor
		1	Selects the XTEMP pin for temperature measurements (2N3904 Junction). Note that XTEMP must be enabled in USER_CONFIG, bit 1.
6:0	Sets the tempco correction in units of 100ppm/°C for IOUT_CAL_GAIN	TC	RSEN (DCR) = IOUT_CAL_GAIN x (1 + TC x (T-25)) where RSEN = resistance of sense element

DEADTIME (DDh)

Definition: Sets the nonoverlap between PWM transitions using a 2-byte data field. The most significant byte controls the high-side to low-side dead time value as a single two's-complement signed value in units of ns. The least-significant byte controls the low-side to high-side dead time value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. The device will operate at the dead time values written to this command when adaptive dead time is disabled, between the minimum dead time specified in DEADTIME_CONFIG and the maximum dead time specified in DEADTIME_MAX. When switching from adaptive dead time mode to frozen mode (by writing to Bit 15 of DEADTIME_CONFIG) the frozen dead time will be whatever the last dead time was before the device switches to frozen dead time mode.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Two 2's complement bytes

Type: R/W

Protectable: Yes

Default Value: 1010h (16ns/16ns)

Units: ns

Range: -15ns to 60ns

COMMAND	DEADTIME (DDh)															
Format	Linear-8 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	High to low-side dead time 8-bit two's complement signed								Low to high-side dead time 8-bit two's complement signed							
Default Value	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

DEADTIME_CONFIG (DEh)

Definition: Configures the adaptive dead time optimization mode. Also sets the minimum dead time value for the adaptive dead time mode range.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0808h (Adaptive dead time control, 8ns/8ns minimum dead time)

Units: N/A

COMMAND	DEADTIME_CONFIG (DEh)															
Format	Bit Field/Linear-7 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15	Sets the HIGH to LOW transition dead time mode	0	Adaptive HIGH to LOW dead time control
		1	Freezes the HIGH to LOW dead time
14:8	Sets the minimum HIGH to LOW dead time	0-126d	Limits the minimum allowed HIGH to LOW dead time when using the adaptive dead time algorithm (2ns resolution)
7	Sets the LOW to HIGH transition dead time mode	0	Adaptive LOW to HIGH dead time control
		1	Freezes the LOW to HIGH dead time
6:0	Sets the minimum LOW to HIGH dead time	0-126d	Limits the minimum allowed LOW to HIGH dead time when using the adaptive dead time algorithm (2ns resolution)

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain and residual value are automatically set by the ZL8800 based on input voltage and output voltage. ASCR Gain is analogous to bandwidth, ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR Gain settings range from 100 to 1000, and ASCR Residual settings range from 10 to 90.

Paged or Global: Paged

Data Length in Bytes: 4

Data Format: Bit Field and nonsigned binary

Type: R/W

Protectable: Yes

Default Value: 015A0100h (Gain = 256d, Residual = 90d, ASCR enabled)

Units: N/A

COMMAND	ASCR_CONFIG (DFh)															
Format	Bit Field/Linear-8 Unsigned															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
31:25	Not Used	0000000h	Not used
24	ASCR Enable	1	Enable
		0	Disable
23:16	ASCR Residual Setting	5Ah	ASCR residual
15:0	ASCR Gain Setting	0100h	ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multirail sequencing. The device will enable its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a Power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus.

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (Prequel and sequel disabled)

Units: N/A

COMMAND	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by bits 12:8
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device. Only one channel can be configured to track: Channel 0, Channel 1, or the output of a 2-phase application.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	TRACK_CONFIG (E1h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	Voltage Tracking Control	0	Disable	Tracking is disabled
		1	Enable	Tracking is enabled
6:3	Not Used	0000	Not Used	Not used
2	Tracking Ratio Control	0	100%	Output tracks at 100% ratio of VTRK input
		1	50%	Output tracks at 50% ratio of VTRK input
1	Tracking Upper Limit	0	Target Voltage	Output voltage is limited by target voltage
		1	VTRK Voltage	Output voltage is limited by VTRK voltage
0	Ramp-Up Behavior	0	Track after PG	The output is not allowed to track VTRK down before Power-good
		1	Track always	The output is allowed to track VTRK down before Power-good

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned group numbers in order to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC groups are separate and unique from DDC phases and INTERLEAVE groups. Current sharing rails need to be in the same DDC group in order to respond to broadcast VOUT_COMMAND and OPERATION commands. Power fail event responses (and Phases) are automatically spread in phase 0 and 1 when the ZL8800 is operating in 2-phase current sharing mode when it is configured using DDC_CONFIG, regardless of its setting in DDC_GROUP.

Paged or Global: Paged

Data Length in Bytes: 3

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 000000h (Ignore BROADCAST VOUT_COMMAND and OPERATION, Sequence shutdown on POWER_FAIL event)

Units: N/A

COMMAND	DDC_GROUP (E2h)																							
Format	Bit Field																							
Bit Position	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table																							
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	Lower 5 bits of device address					0	0	0	Lower 5 bits of device address				

BITS	PURPOSE	VALUE	DESCRIPTION
23:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to BROADCAST_VOUT_COMMAND with same Group ID
		0	Ignores BROADCAST_VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast BROADCAST_VOUT_COMMAND events
15:14	Not Used	00	Not used
13	BROADCAST_OPERATION response	1	Responds to BROADCAST_OPERATION with same Group ID
		0	Ignores BROADCAST_OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast BROADCAST_OPERATION events
7:6	Not Used	00	Not used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string. The format is: Part number, Major Revision, (period), Minor Revision, Engineering version letter.

Paged or Global: Global

Data Length in Bytes: 16

Data Format: ASCII. ISO/IEC 8859-1

Type: Block Read

Protectable: No

Default Value: ZL8800, current major revision, (period), current minor revision, current engineering version letter

Units: N/A

COMMAND	DEVICE_ID (E4h)															
Format	Characters (Bytes)															
Characters	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Part Number										Maj. Rev.		.	Min. Rev		Engr.
Default Value	Z	L	8	8	0	0					*	*	*	*	*	*
* current revision at time of manufacture																

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retries)

Units: Retry time = 70ms

COMMAND	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used.
		01	Not used.
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Not used.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Data Length in Bytes: 1

Paged or Global: Paged

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retries)

Units: Retry time unit = 70ms

COMMAND	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used.
		01	Not used.
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For downslope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 16A (DA00h)

Units: Amperes

Equation: IOUT_AVG_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100 to 100A

COMMAND	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0.8 x IOUT_OC_FAULT_LIMIT															

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the IOUT average undercurrent fault threshold. For downslope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -16A (DE00h)

Units: Amperes

Equation: IOUT_AVG_UC_FAULT_LIMIT = $Y \times 2^N$

Range: -100 to 100A

COMMAND	IOUT_AVG_UC_FAULT_LIMIT (E8h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0.8 x IOUT_UC_FAULT_LIMIT															

USER_GLOBAL_CONFIG (E9h)

Definition: Sets options for the output voltage sensing, maximum output voltage override, SMBus time-out, and DDC and SYNC output configurations.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: N/A

COMMAND	USER_GLOBAL_CONFIG (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15:10	Not Used	000000	Not used
9:8	Vsense Select for monitoring and fault detection	00	Output 0 uses VSEN0, Output 1 uses VSEN1
		01	Both outputs use VSEN0
		10	Both outputs use VSEN1
7	Not Used	0	Not used
6	DDC Output Configuration	0	DDC output open-drain
		1	DDC output push-pull
5	Not Used	0	Not used
4	Disable SMBus Time-Outs	0	SMBus time-outs enabled
		1	SMBus time-outs disabled
3	Not Used	0	Not used
2:1	Sync I/O Control	00	Use internal clock (frequency initially set with pin-strap)
		01	Use internal clock and output internal clock (not for use with pin-strap)
		10	Use external clock
		11	Not used
0	Not Used	0	Not used

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Paged or Global: Paged

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: No

Default Value: N/A

Units: N/A

BYTE NUMBER	VALUE	PMBus COMMAND	FORMAT
31:23	Not Used	Not Used	0000h
22	Flash Memory Status Byte	N/A	Bit Field
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	Iout Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	Vout Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
13:12	External Temperature	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
11:10	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
7:6	Highest Measured Output Current	N/A	2 Byte Linear-11
5:4	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
3:2	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
1:0	Input Voltage	READ_VIN (88h)	2 Byte Linear-11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Paged or Global: Paged

Data Length in Bytes: 16

Data Format: Bit Field

Type: Block Read

Protectable: No

Default Value: FF...FFh

Units: N/A

LEGACY_FAULT_GROUP (F0h)

Definition: Allows the ZL8800 to sequence and fault spread with devices other than the ZL8800 family of ICs. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

NOTE: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail (devices other than the ZL8800 family ICs) must shut down for the rail to report a shutdown.

If fault spread mode is enabled in USER_CONFIG, the device will immediately shut down if one of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults.

If fault spread mode is disabled in USER_CONFIG, the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Paged or Global: Paged

Data Length in Bytes: 4

Data Format: Bit field

Type: Block R/W

Protectable: Yes

Default Value: 00000000h

Units: N/A

COMMAND	LEGACY_FAULT_GROUP (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
31:0	Fault Group	NA	00000000h	Identifies the devices in the fault spreading group.

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current SNAPSHOT values from NVRAM to the 32-byte SNAPSHOT command parameter. Writing a 02h will cause the device to write the current SNAPSHOT values to NVRAM, 03h will erase all SNAPSHOT values from NVRAM. Write (02h) and Erase (03h) can be used only when the device is disabled. All other values will be ignored.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W byte

Protectable: Yes

Default Value: N/A

Units: N/A

COMMAND	SNAPSHOT_CONTROL (F3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

VALUE	DESCRIPTION
01	Read SNAPSHOT values from NVRAM
02	Write SNAPSHOT values to NVRAM
03	Erase SNAPSHOT values from NV RAM

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Sets the VMON overvoltage fault threshold. A VMON parameter equals 16 times the voltage applied to the VMON pin. The VMON overvoltage warn limit is automatically set to 90% of this fault value.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D300h (12V)

Units: V

Equation: MFR_VMON_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	MFR_VMON_OV_FAULT_LIMIT (F5h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Sets the VMON undervoltage fault threshold. A VMON parameter equals 16 times the voltage applied to the VMON pin. The VMON undervoltage warn limit is automatically set to 110% of this fault value.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA40h (4.5V)

Units: V

Equation: MFR_VMON_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	MFR_VMON_UV_FAULT_LIMIT (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read only
Protectable: No
Default Value: N/A
Units: V
Equation: MFR_READ_VMON = Y x 2^N
Range: 0 to 19V

COMMAND	MFR_READ_VMON (F7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Configures the VMON overvoltage fault response as defined by the following table. The retry time is the time between restart attempts.
Paged or Global: Global
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate Shutdown, no retries)
Units: Retry time unit = 70ms

COMMAND	VMON_OV_FAULT_RESPONSE (F8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used.
		01	Not used.
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Configures the VMON undervoltage fault response as defined by the following table. Note: The retry time is the time between restart attempts.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retries)

Units: Retry time unit = 70ms

COMMAND	VMON_UV_FAULT_RESPONSE (F9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior—the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used.
		01	Not used.
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	000-111	Not used.

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writeable (commands are always readable). If a command is not writeable, a password must be entered in order to change its parameter (that is, to enable writes to that command). Passwords can be either public or private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as non-writeable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as non-writeable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT Store must be sent in order to change that command. If a command is writeable according to the Default UNPROTECT parameter, it may still be marked as non-writeable in the User Store UNPROTECT parameter. In this case, the User private password can be sent to make the command writeable.

The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed in the following sections. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1.

Figure 13 shows the algorithm used by the device to determine if a particular command write is allowed.

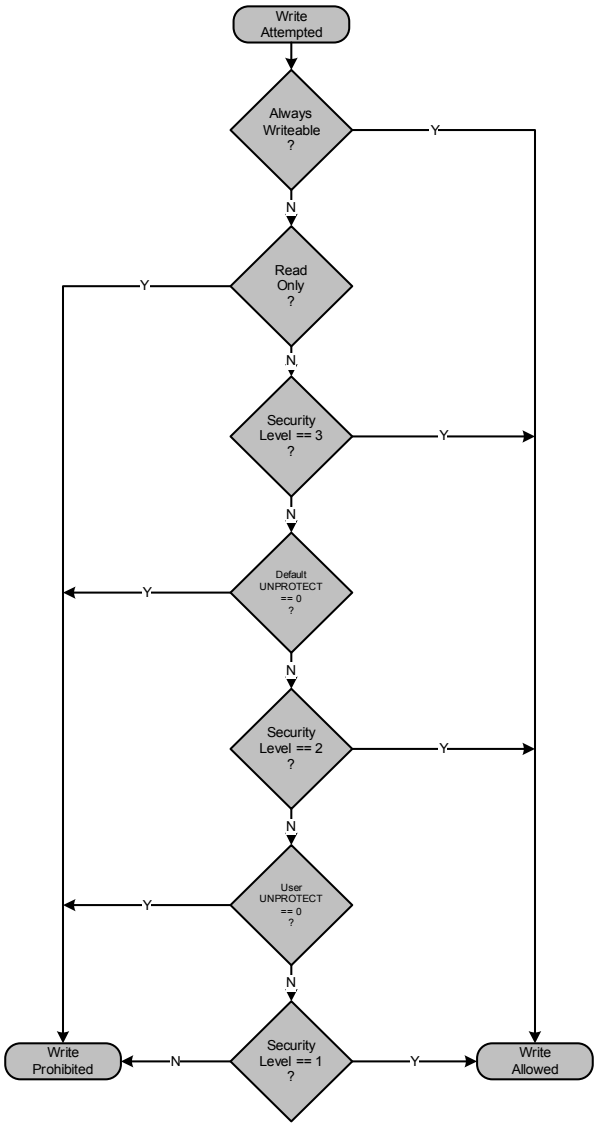


FIGURE 13. ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITEABLE

Security Level 3 – Module Vendor

Level 3 is intended primarily for use by Module vendors to protect device configurations in the Default Store. Clearing an UNPROTECT bit in the Default Store implies that a command is writeable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the Default Store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 – User

Level 2 is intended for use by the end user of the device. Clearing an UNPROTECT bit in the User Store implies that a command is writeable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL, and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 – Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the Default and User Store. Security is raised to Level 1 by writing the public password stored in the User Store using the PUBLIC_PASSWORD command. The public password stored in the Default Store has no effect.

Security Level 0 - Unprotected
Level 0 implies that only commands which are always writeable (such as PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value which does not match the stored public password.

Paged or Global: Global
Data Length in Bytes: 1
Data Format: Hex
Type: Read Byte
Protectable: No
Default Value: 01h
Units: N/A
Reference: AN2031 - "Writing Configuration Files for Intersil Digital Power"

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.
Paged or Global: Global
Data Length in Bytes: 9
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: No
Default Value: 000000000000000000h
Units: N/A
Reference: AN2031 - "Writing Configuration Files for Intersil Digital Power"

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.
Paged or Global: Global
Data Length in Bytes: 4
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: No
Default Value: 00000000h
Units: N/A
Reference: AN2031 - "Writing Configuration Files for Intersil Digital Power"

UNPROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protectable or supported by the device. Clearing a command's UNPROTECT bit indicates that write-access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the DEFAULT store require a security level 3 or greater to be writeable. The UNPROTECT bits in the USER store require a security level of 2 or higher.

Data Length in Bytes: 32
Paged or Global: Global
Data Format: Custom
Type: Block R/W
Protectable: No
Default Value: FF...FFh
Units: N/A
Reference: AN2031 - "Writing Configuration Files for Intersil Digital Power"

Firmware Revision History

FIRMWARE REVISION CODE	CHANGE DESCRIPTION	NOTE
1.06	Fix to start-up routine to improve SA pin read performance at cold temperatures. Improved fault retry performance. Improved DDC compatibility with previous generations of Intersil controllers and modules. Addition of the LEGACY_FAULT_GROUP command to allow for fault spreading over Intersil's DDC bus with previous generation of controllers and modules. Defaults for IOUT_XXX and TOFF_FALL are fixed values; they are no longer dependent on other command values. Some command defaults may differ from 1.04 values by one bit. TOFF_DELAY settings less than 0.5ms will set the device to immediate off shutdown behavior. INTERLEAVE default automatically phase spread in 2 channel mode. DDC_CONFIG default automatically sets group number.	Recommended for new designs
1.04	Initial release	Not recommended for new designs

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov 8, 2017	FN7558.6	Added an explanation of the EN0 and EN1 timing restrictions to "Enable Pin Operation and Timing" on page 15. Updated to the current Renesas format.
Aug 10, 2017	FN7558.5	In the Features section, updated the voltage range to "4.5V to 5.5V or 6.5V to 14V" Updated application diagrams to show use of DRMOS devices. Added a two phase schematic diagram with DrMOS. Pin Description section For the SCL and SDA pins, added "Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source. Pull-up supply must be from an "always on" source or VR5." For the SALRT pin, added "Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source. Leave floating if not used." For the SGND pin, added "All pin-strap resistors should be connected to SGND. SGND must be connected to DGND and PGND using a single point connection." For the SA pin, added "Connect resistor to SGND." For VSET0, added "Default VOUT max is 115% of VOUT setting, but this can be overridden through the PMBus interface with the VOUT_MAX command. Connect resistor to SGND." For VSET1, added "Default VOUT max is 115% of VOUT setting, but this can be overridden through the PMBus interface with the VOUT_MAX command. Connect resistor to SGND. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode." For XTEMP0P, XTEMP0N, VTRKP, and VTRKN, added "If not used connect to SGND." For VDRV, VR6, and VR5, added "10µF recommended." For VSEN1N, added "in 2-channel or 2-phase mode." For VSEN1P, added "in 2-channel or 2-phase mode." In the Ordering Information table, added "Recommended for new designs" column. For 4Bh IOUT_UC_FAULT_LIMIT, changed the default setting to "-20A". For 65h TOFF_FALL, changed the default setting to "5ms". For E7h IOUT_AVG_OC_FAULT_LIMIT, changed the default setting to "16A". For E8h IOUT_AVG_UC_FAULT_LIMIT, changed the default setting to "-16A". For 80h STATUS_MFR_SPECIFIC, reworded VMON_UV_WARNING and VMON_OV_WARNING for clarity. In the Firmware Revision History, added some previously undocumented firmware changes to the 1.06 revision. Added a recommendation for 10uF bypass capacitor on VR5, VR6, and VDRV. Added a recommendation to pull-up DDC to VR5. Corrected several PMBus command descriptions to show correct default value and Global or Paged behavior.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
May 1, 2017	FN7558.4	Updated Related Literature section. Applied new header/footer. Updated Ordering Information table added ZL8800ALAFT7A and ZL8800ALBFT7A Clarified relationship between POWER_GOOD_ON and VOUT_UV_FAULT_LIMIT thresholds in “Power-Good” on page 15, the “PMBus Command Summary” table, and the “VOUT_UV_FAULT_LIMIT (44h)” and “POWER_GOOD_ON (5Eh)” register descriptions.
Sept 14, 2015	FN7558.3	Added Related Literature section on page 1. Added Key Differences table to page 1. Updated Ordering Information table on page 8 by adding ZL8800ALBFT and ZL8800ALBFTK part numbers, added FIRMWARE REVISION column, and added Note 5. Added LEGACY_FAULT_GROUP command to “PMBus Command Summary” on page 28 and in the Command descriptions on page 79. Changed reference to 30ms to 70ms, and 20 to 30ms to 60 to 70ms in “Start-Up Procedure” on page 15. Added detail to TON_DELAY Range description on page 48. Added detail to TON_RISE Range description on page 48. Added detail to TOFF_DELAY Range description on page 49. Added Firmware Revision History section.
Nov 11, 2013	FN7558.2	Added “™” to ChargeMode - page 1 title, third paragraph and trademark statement.
Oct 10, 2013	FN7558.1	The maximum ramp-up time and ramp-down time changed from 200ms to 100ms: pages 10, 47, 48. The maximum soft-start delay, turn-off delay, and Power-good delay changed on pages 47, 48 and 62 to 5 seconds to match the limits in the EC table (page 10). The second table on page 60. The location and size of the bit field for minimum duty cycle changed from 2 bits in location 9:8 to 5 bits in location 15:11.
Sept 18, 2013	FN7558.0	Initial release

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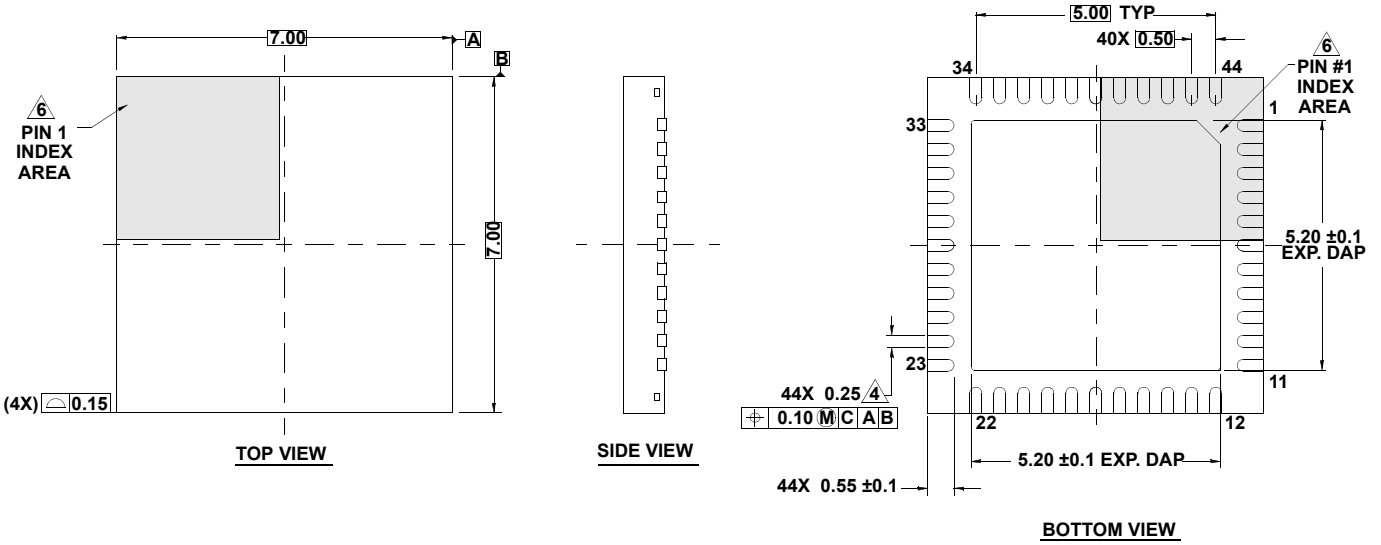
Package Outline Drawing

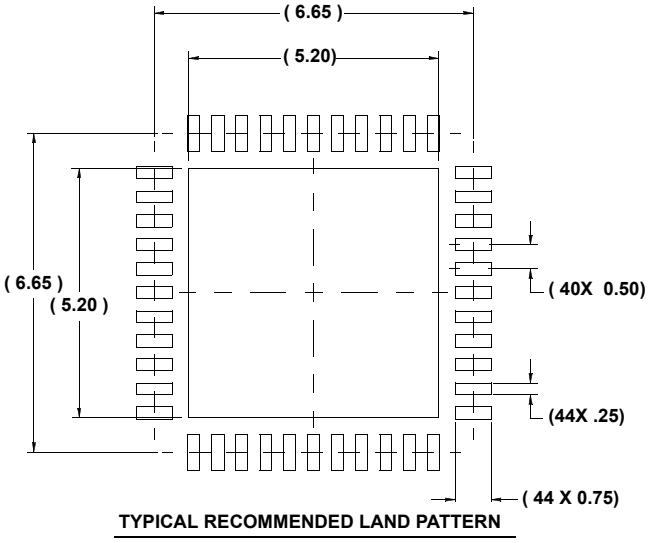
For the most recent package outline drawing, see L44.7x7B.

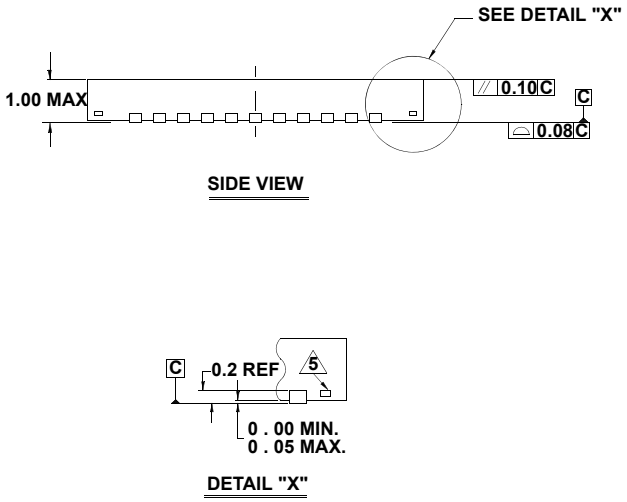
L44.7x7B

44 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 10/09







NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Complies to JEDEC MO220 VKKD-1.