Document Title

256Kx16 Bit High Speed Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Ranges.

Revision History

RevNo. | **History** | **Draft Data** | **Remark**

Rev. 0.0 | Initial release with Preliminary. | Aug. 20. 2001 | Preliminary

Rev. 0.1 | Add Low Ver. | Sep. 19. 2001 | Preliminary

Rev. 0.2 | Package dimensions modify on page 11. | Sep. 28. 2001 | Preliminary

Rev. 0.3 | Change ICC , ISB, ISB1 | Oct. 09. 2001 | Preliminary

Item		Previous	Current
ICC(Commercial)	8ns	110mA	80mA
	10ns	90mA	65mA
	12ns	80mA	55mA
	15ns	70mA	45mA
ICC(Industrial)	8ns	130mA	100mA
	10ns	115mA	85mA
	12ns	100mA	75mA
	15ns	85mA	65mA
ISB		30mA	20mA
ISB1(L-ver.)		0.5mA	1.2mA

Rev. 0.4 | 1. Correct AC parameters : Read & Write Cycle
2. Change Data Retention Current :
from 0.45mA to 1.1mA when Vcc=3.0V
from 0.35mA to 0.9mA when Vcc=2.0V
3. Limit L-Ver. to 48 TBGA Package | Nov.23. 2001 | Preliminary

Rev. 1.0 | 1. Delete 12ns,15ns speed bin.
2. Change Icc for Industrial mode. | Dec.18. 2001 | Final

Item		Previous	Current
ICC(Industrial)	8ns	100mA	90mA
	10ns	85mA	75mA

Rev. 2.0 | 1. Add tBA,tBLZ,tBHZ,tBW AC paremeters. | Feb. 14. 2002 | Final

Rev. 2.1 | 1. Correct the Package dimensions(48-TBGA) | Oct. 23. 2002 | Final

Rev. 2.2 | 1. Add the tPU and tPD into the waveform. | Mar. 10, 2003 | Final

Rev. 2.3 | 1. Change the current parameters (Isb1 L-ver, Idr) | June. 12, 2003 | Final

Rev. 3.0 | 1. Add the Lead Free Package type. | June. 20, 2003 | Final

Rev. 4.0 | 1. Change the Idr parameters | Mar. 15, 2004 | Final

	previous	Current
Idr(2V)	1.2mA	1.4mA
Idr(3V)	1.8mA	2.0mA

4Mb Async. Fast SRAM Ordering Information

Org.	Part Number	VDD(V)	Speed (ns)	PKG	Temp. & Power
1M x4	K6R4004C1D-J(K)C(I) 10	5	10	J : 32-SOJ K : 32-SOJ(LF)	C : Commercial Temperature ,Normal Power Range I : Industrial Temperature ,Normal Power Range L : Commercial Temperature ,Low Power Range P : Industrial Temperature ,Low Power Range
	K6R4004V1D-J(K)C(I) 08/10	3.3	8/10		
512K x8	K6R4008C1D-J(K,T,U)C(I) 10	5	10	J : 36-SOJ K : 36-SOJ(LF) T : 44-TSOP2 U : 44-TSOP2(LF)	
	K6R4008V1D-J(K,T,U)C(I) 08/10	3.3	8/10		
256K x16	K6R4016C1D-J(K,T,U,E)C(I) 10	5	10	J : 44-SOJ K : 44-SOJ(LF) T : 44-TSOP2 U : 44-TSOP2(LF) E : 48-TBGA	
	K6R4016V1D-J(K,T,U,E)C(I,L,P) 08/10	3.3	8/10		

256K x 16 Bit High-Speed CMOS Static RAM

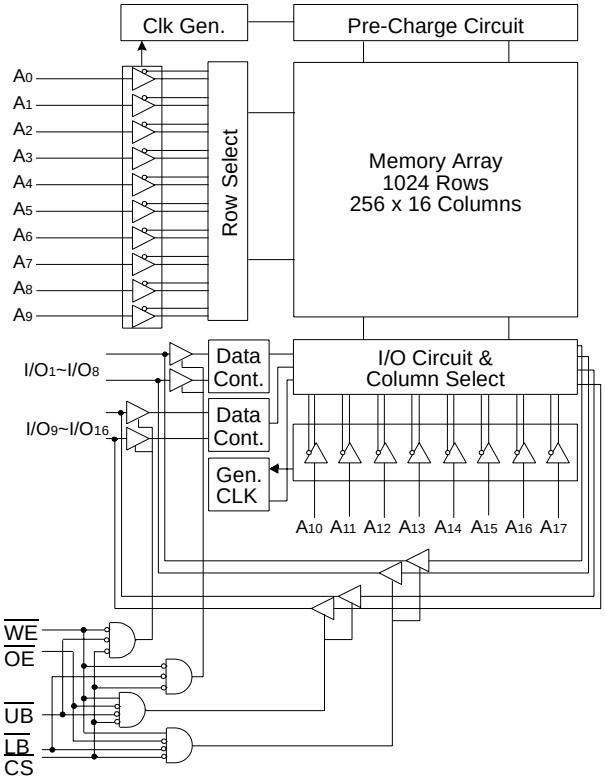
FEATURES

- Fast Access Time 8,10ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 20mA(Max.)
  (CMOS) : 5mA(Max.)
  1.2mA(Max.)L-Ver. only.
  Operating K6R4016V1D-08 : 80mA(Max.)
  K6R4016V1D-10 : 65mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention: L-Ver. only.
- Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- Standard Pin Configuration
  K6R4016V1D-J : 44-SOJ-400
  K6R4016V1D-K : 44-SOJ-400(Lead-Free)
  K6R4016V1D-T : 44-TSOP2-400BF
  K6R4016V1D-U : 44-TSOP2-400BF (Lead-Free)
  K6R4016V1D-E : 48-TBGA with 0.75 Ball pitch
  (7mm X 9mm)
- Operating in Commercial and Industrial Temperature range.

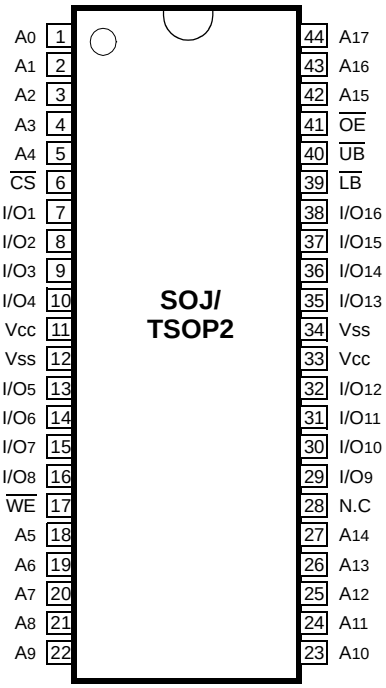
GENERAL DESCRIPTION

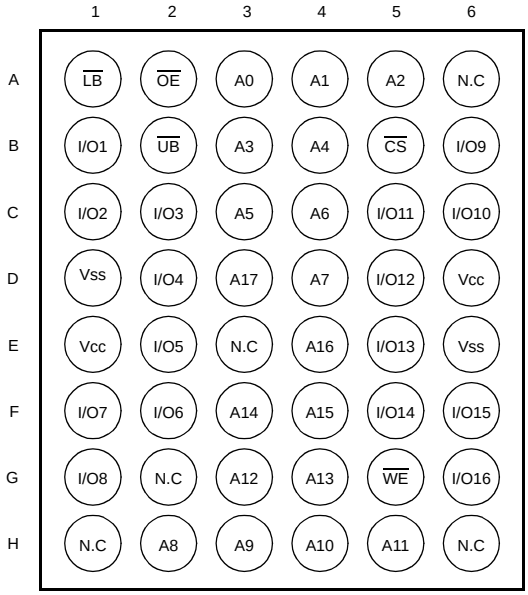
The K6R4016V1D is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The K6R4016V1D uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control(UB, LB). The device is fabricated using SAMSUNG′s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4016V1D is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward or 48 TBGA.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*





48-TBGA

PIN FUNCTION

Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_1~I/O_8)
$\overline{UB}$	Upper-byte Control(I/O_9~I/O_{16})
I/O_1 ~ I/O_{16}	Data Inputs/Outputs
V_{CC}	Power(+3.3V)
V_{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}		V_{CC}	-0.5 to 4.6	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

***** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3***	V
Input Low Voltage	V_{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.
** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.
*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, Vcc=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}			-2	2	µA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	Com.	8ns	-	80	mA
				10ns	-	65	
			Ind.	8ns	-	90	
				10ns	-	75	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}			-	20	mA
	I_{SB1}	f=0MHz, $\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	Normal		-	5	
			L-ver.**		-	2.4	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA			-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA			2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.
** L-var is only supported with TBGA package type.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* Capacitance is sampled and not 100% tested.

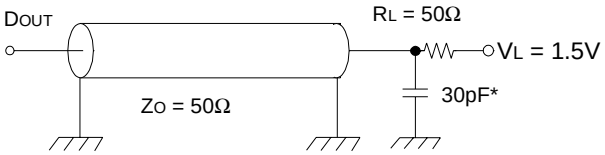
AC CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS*

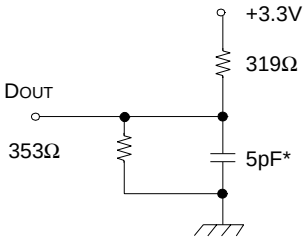
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R4016V1D-08		K6R4016V1D-10		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	ns
Address Access Time	t_{AA}	-	8	-	10	ns
Chip Select to Output	t_{CO}	-	8	-	10	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	ns
$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	4	-	5	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	4	0	5	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	ns
Chip Selection to Power DownTime	t_{PD}	-	8	-	10	ns

* The above parameters are also guaranteed at industrial temperature range.

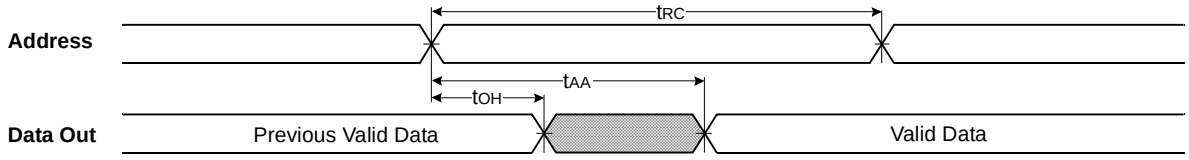
WRITE CYCLE*

Parameter	Symbol	K6R4016V1D-08		K6R4016V1D-10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	8	-	10	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	6	-	7	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	ns

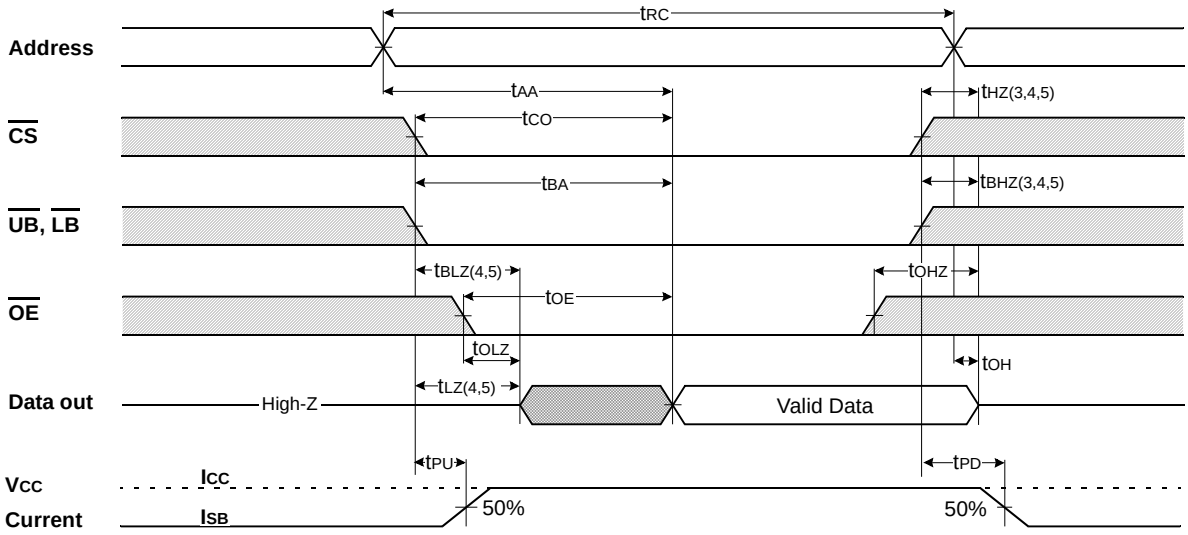
* The above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$, $\overline{LB}$=V_{IL})



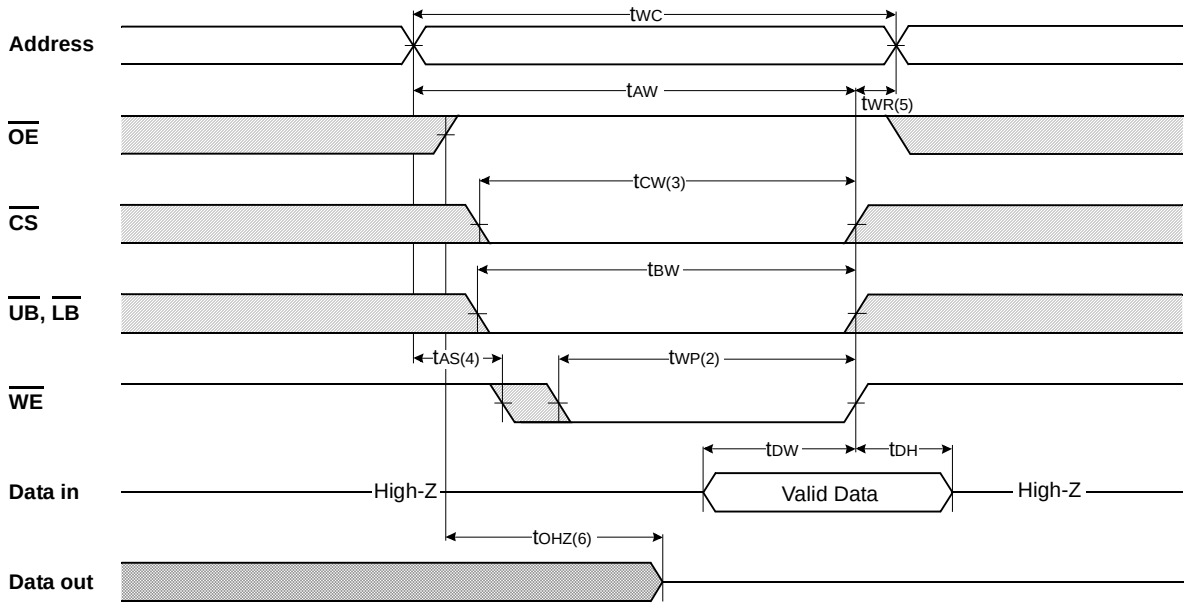
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



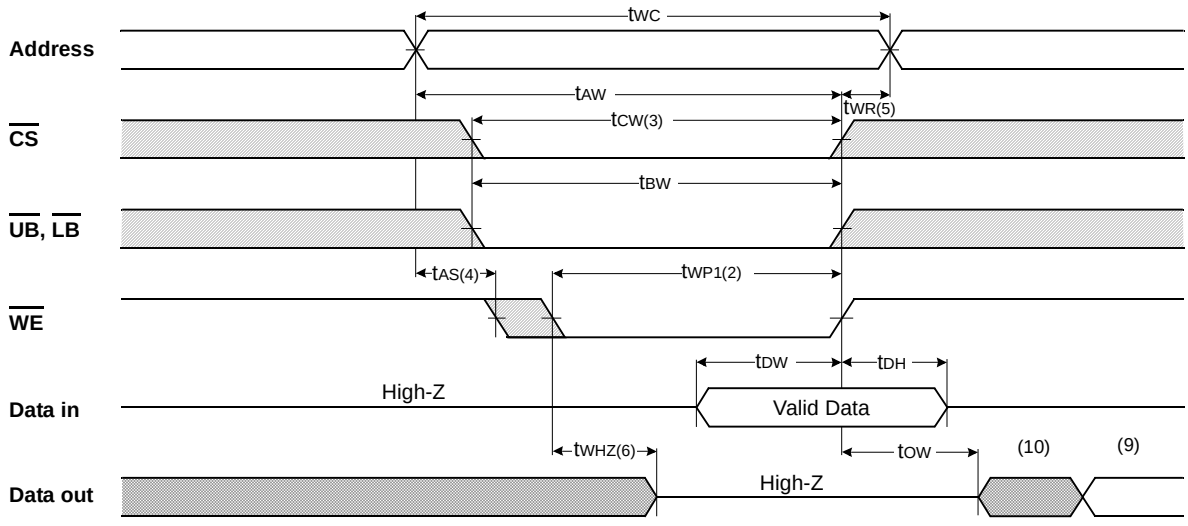
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

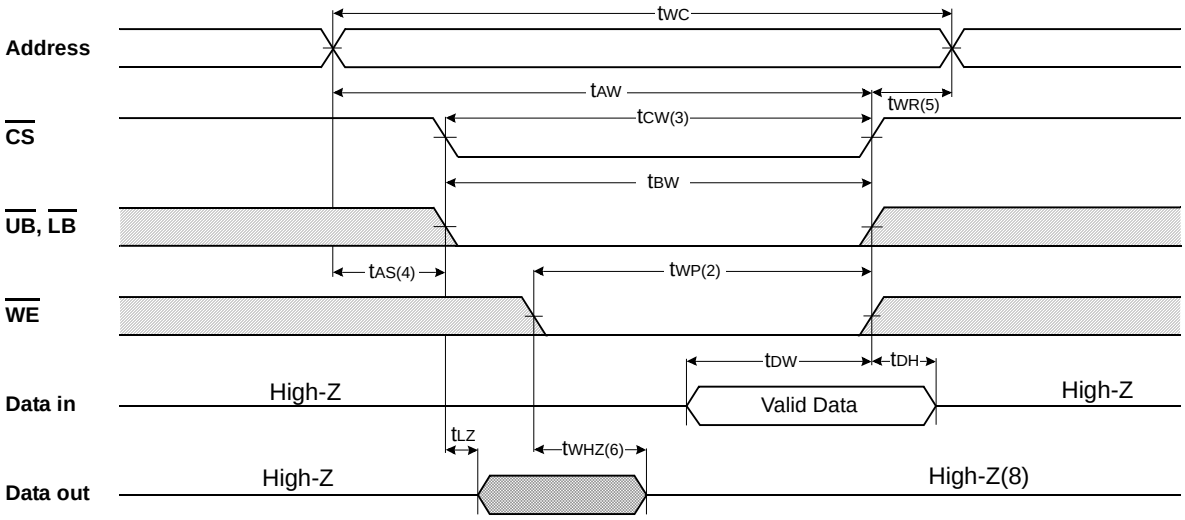
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



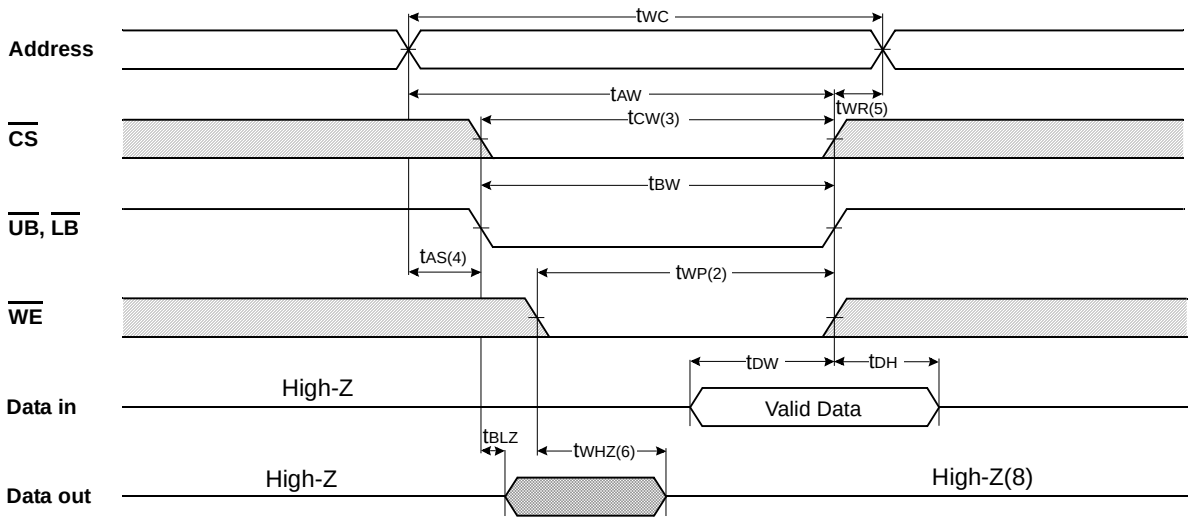
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not . be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* X means Don't Care.

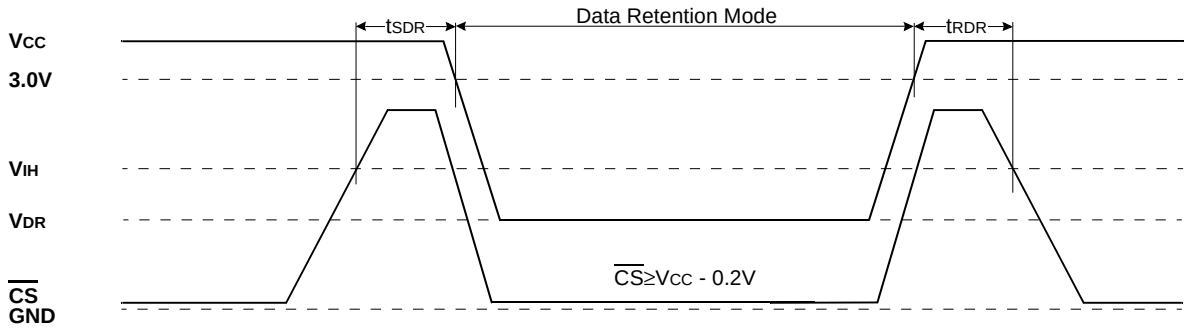
DATA RETENTION CHARACTERISTICS*(T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ ≥V_{CC} - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, $\overline{CS}$≥V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN}≤0.2V	-	-	2.0	mA
		V_{CC}=2.0V, $\overline{CS}$≥V_{CC} - 0.2V V_{IN}≥V_{CC} - 0.2V or V_{IN}≤0.2V	-	-	1.4	
Data Retention Set-Up Time	t_{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t_{RDR}		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

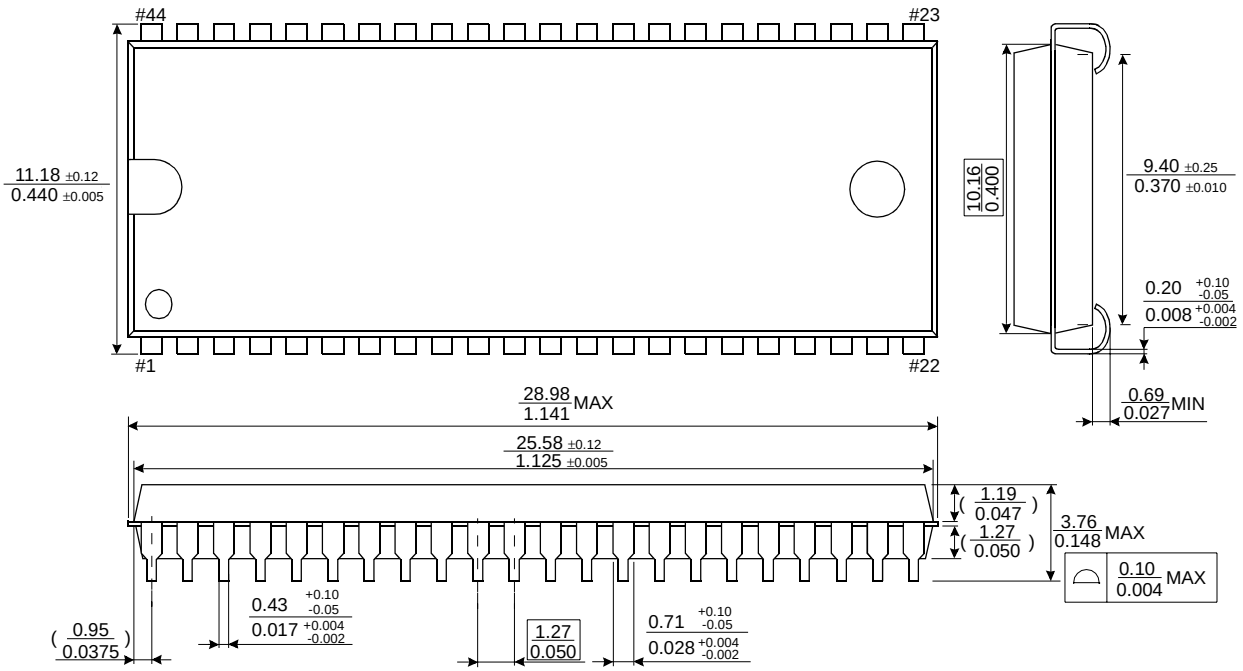
$\overline{CS}$ controlled



PACKAGE DIMENSIONS

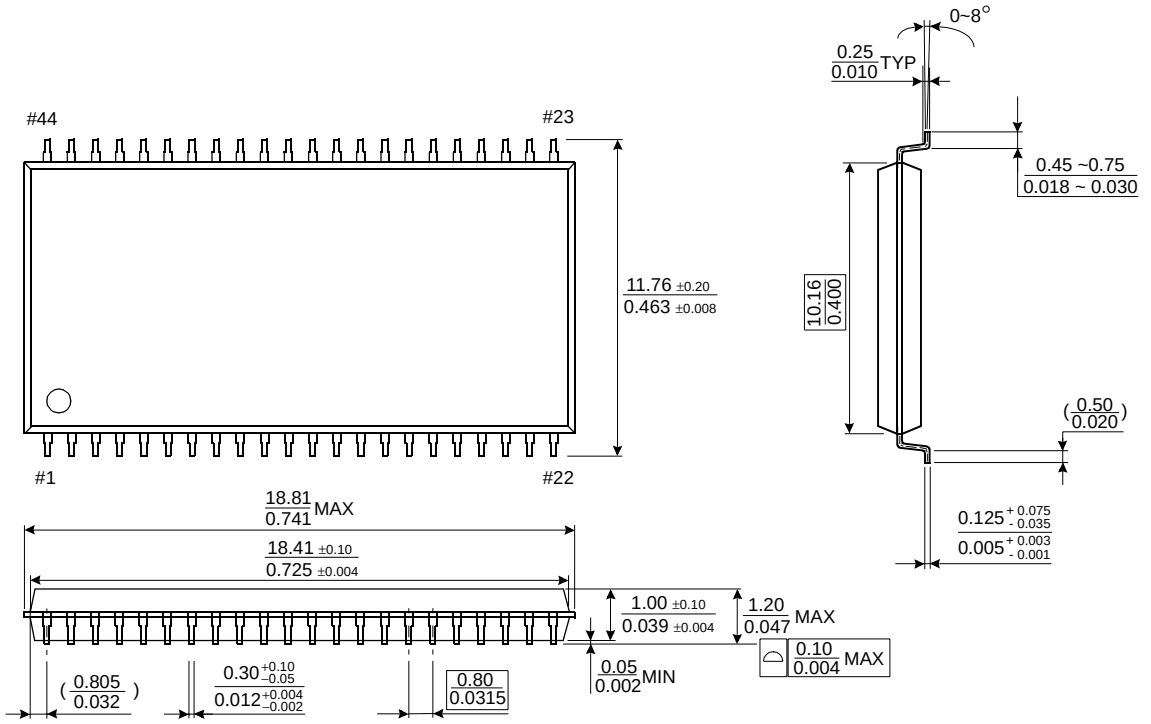
Units:millimeters/Inches

44-SOJ-400



44-TSOP2-400BF

Units:millimeters/Inches

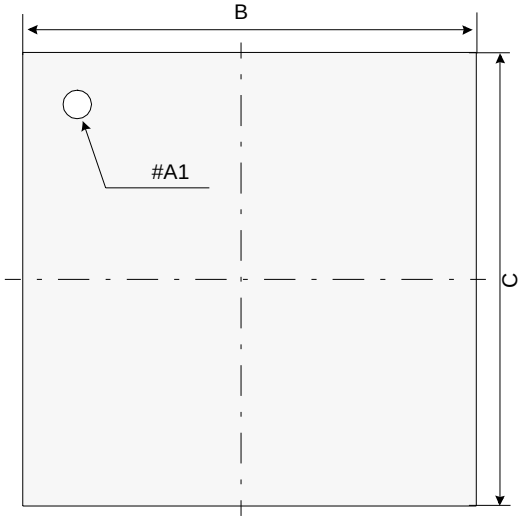


SAMSUNG ELECTRONICS

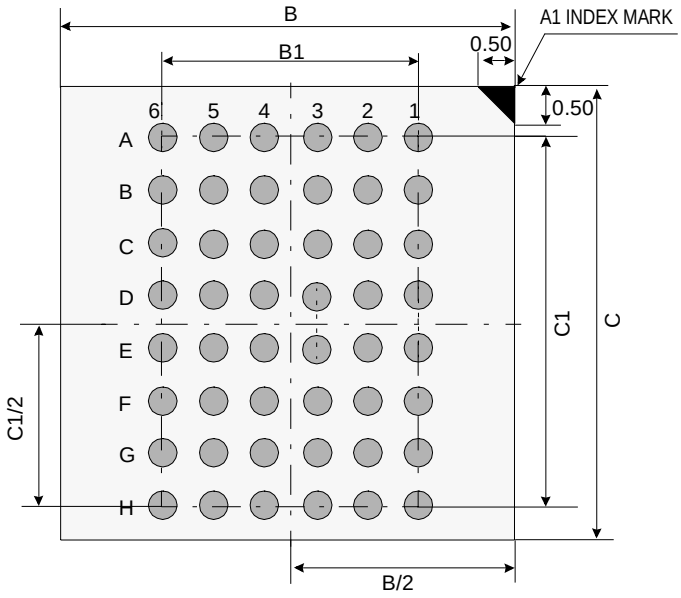
PACKAGE DIMENSIONS

Units : millimeter.

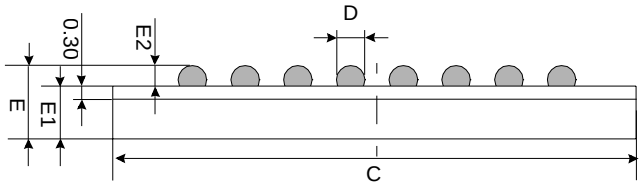
Top View



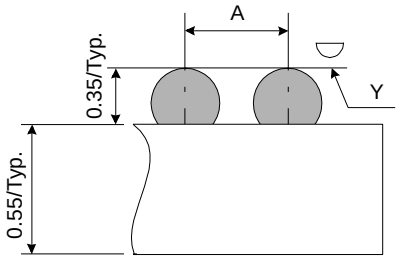
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	6.90	7.00	7.10
B1	-	3.75	-
C	8.90	9.00	9.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)