SC1104A/B
Simple, Synchronous Voltage Mode PWM Controller

Description

The SC1104A/B is a versatile voltage-mode PWM controller designed for use in single ended DC/DC power supply applications. A simple, fixed frequency high efficiency buck regulator can be implemented using the SC1104A/B with a minimum of external components. Internal level shift and drive circuitry eliminates the need for an expensive P-channel, high-side switch. The small device footprint allows for compact circuit design.

SC1104A/B features include temperature compensated voltage reference, triangle wave oscillator, current limit comparator and an externally compensated error amplifier. Current limit is implemented by sensing the voltage drop across the top FET's $R_{DS(ON)}$.

The SC1104A/B operates at fixed frequencies of 300kHz or 600kHz providing an optimum compromise between efficiency, external component size, and cost. 600kHz switching frequency is reserved for the SC1104B +5V operation only.

SC1104A/B has a thermal protection circuit, which is activated if the junction temperature exceeds 150°C.

Features

- +5V or +12V 300kHz operation (SC1104A)
- +5V 600kHz operation (SC1104B)
- High efficiency (>90%)
- 1% Reference voltage accuracy
- Hiccup mode over current protection
- Robust output drive
- $R_{DS(ON)}$ Current sensing
- Industrial temperature range
- SO-8 package

Applications

- Termination supplies
- Low cost microprocessor supplies
- Peripheral card supplies
- Industrial power supplies
- High density DC/DC conversion

Typical Application Circuit

Typical Distributed Power Supply

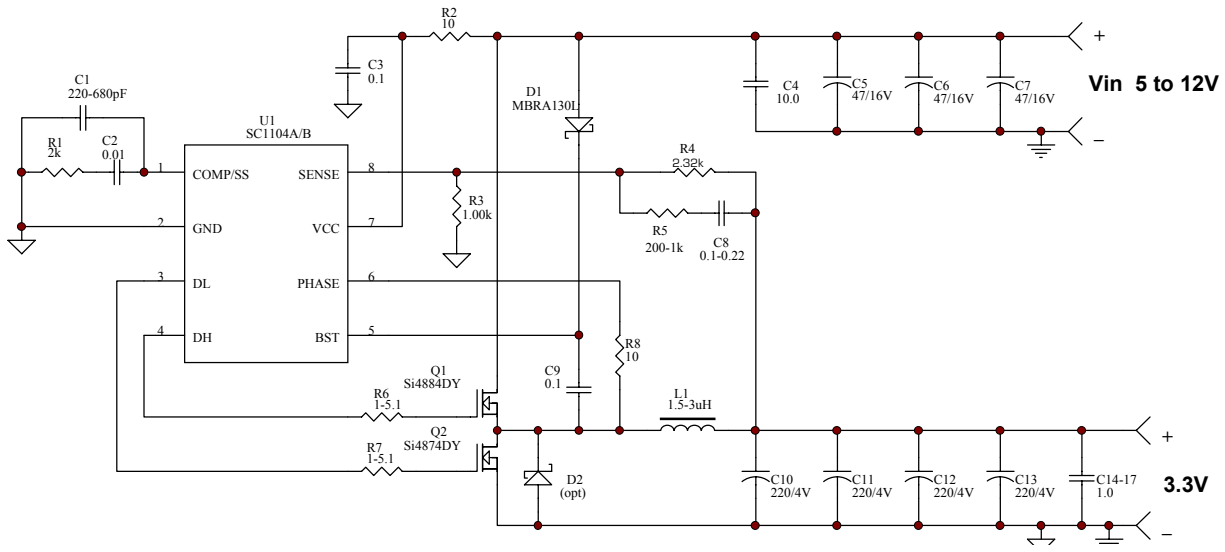


Figure 1

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
V_{CC} to GND		15	V
BST to PHASE		15	V
PHASE to GND		-1 to 15	V
DH to PHASE		15	V
DL to GND		15	V
COMP/SS to GND		7	V
SENSE to GND		7	V
Thermal Resistance Junction to Case	θ_{JC}	40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	160	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{Lead}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, T_A = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}	F_{SW} = 300kHz (nom.), SC1104A	4.2		12.6	V
	V_{CC}	F_{SW} = 600kHz (nom.), SC1104B	4.2		7	
Supply Current	I_{CC}	$V_{COMP} \leq 0.4V$		11	14	mA
Error Amplifier						
E/A Transconductance	g_m			12		mS
Open Loop DC Gain	A_O			42		dB
Bandwidth - 3dB	F_{BW}			400		kHz
Input Bias Current	I_{FB}			1	3	µA
Output Sink Current	I_{SIK}	$V_{SENSE} \geq 1.1V$; V_{COMP} = 1.5V		0.7		mA
Source Current	I_{SC}	$V_{SENSE} \geq 0.9V$; V_{COMP} = 1.5V		1.1		
Oscillator						
Switching Frequency	F_{OSC}	V_{CC} = 12V ± 0.6V	270	300	330	kHz
		V_{CC} = 5V ± 0.25V	540	600	660	

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, T_A = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Ramp Peak Voltage	V_{P-K}	4.75V ≤ V_{CC} ≤ 12.6V		2.0		V
Ramp Valley Voltage	V_V	4.75V ≤ V_{CC} ≤ 12.6V		1.0		V
Maximum Duty Cycle	dc_{MAX}	V_{CC} = 12V (300kHz, SC1104A)		95		%
		V_{CC} = 5V (600kHz, SC1104B)		90		
MOSFET Drivers						
DH Sink/Source Current SC1104A	I_{DH}	d.c. < 2%, t_{PW} < 100µs V_{GS} = 4.5V (src)	0.6			A
DL Sink/Source Current SC1104A	I_{DL}	V_{GS} = 2.5V (snk)	0.6			
DH Sink/Source Current SC1104B	I_{DH}	d.c. < 2%, t_{PW} < 100µs V_{GS} = 4.5V (src)	0.45			A
DL Sink/Source Current SC1104B	I_{DL}	V_{GS} = 2.5V (snk)	0.45			
DH Rise/Fall Time	tr, tf	C_L = 3000pF, See Fig. 2		50		ns
DL Rise/Fall Time	tr, tf	C_L = 4000pF, See Fig. 2		50		
Dead Time	t_{dt}	See Fig. 2		80		ns
DH Minimum Off Time	t_{OFF}	4.75V ≤ Vcc ≤ 12.6V		160		
Reference Section						
Reference Voltage	V_{REF}	4.75V ≤ Vcc ≤ 12.6V	0.990	1.000	1.010	V
Reference Accuracy			-1		1	%
		-40 < T_A < +85°C	-1.5		1.5	
Long Term Stability		T_J = 125°C, 1000 hrs.			5	mV
Current Limit						
Trip Voltage	V_{trp}	4.75V < Vcc < 12.6V V_{trp} = Vcc - V_{PHASE}	180	200	220	mV
Soft-Start/Enable						
SS Source Current	I_{SRC}	V_{COMP} < 2.5V		1.5		µA
SS Sink Current	I_{SNK}	V_{COMP} > 0.5V		1.5		
Enable Input Threshold				1		V
Enable Input Current		V_{COMP} = 0.8V			2	mA
Under Voltage Lockout						
UVLO Threshold	V_{th}	-40< T_A < 85°C	3.9	4.15	4.5	V

POWER MANAGEMENT

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, T_A = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			150		°C

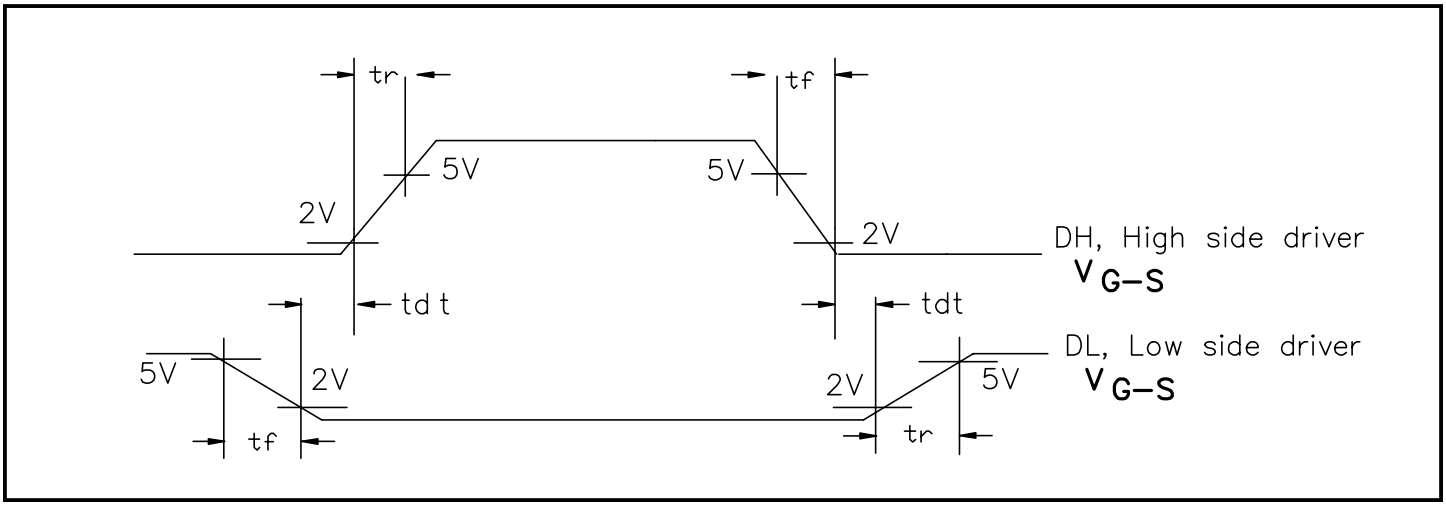


Figure 2

Block Diagram

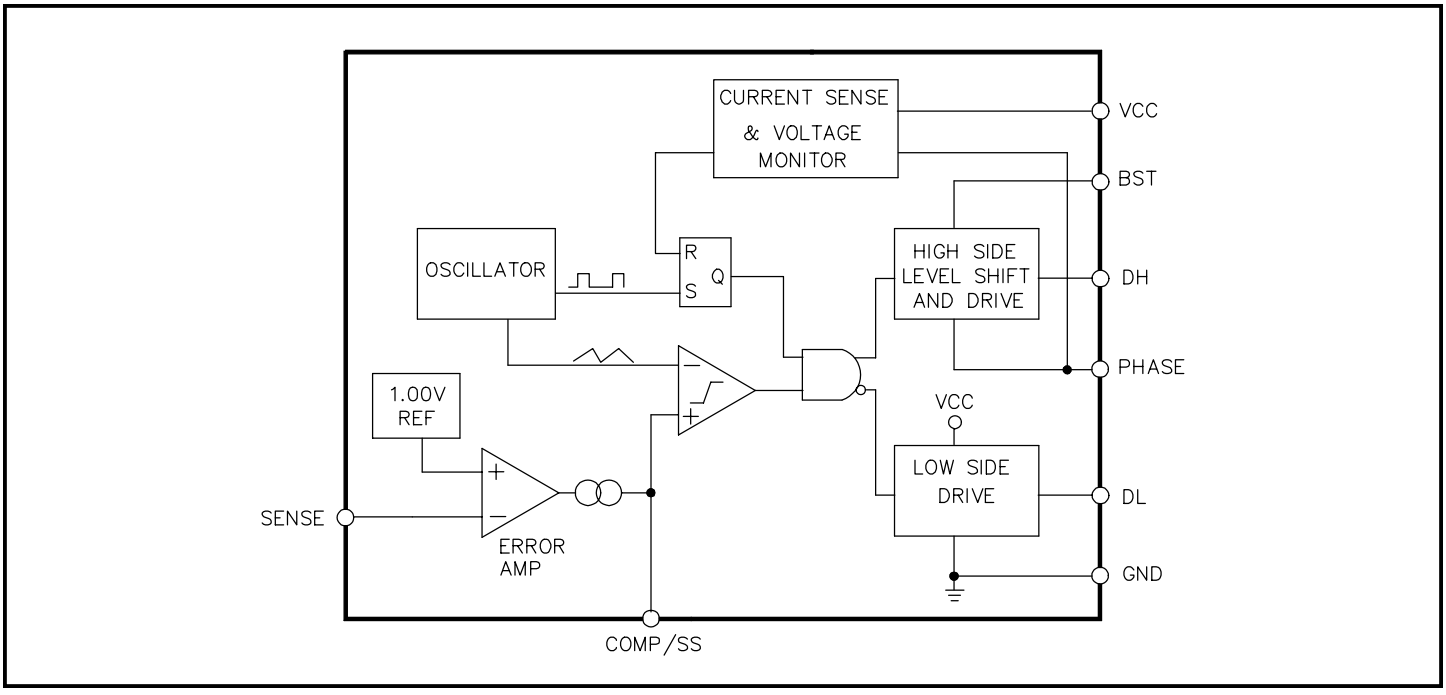
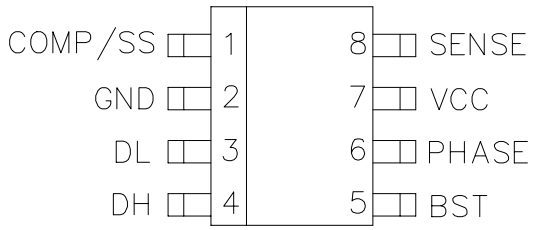


Figure 3

Pin Configuration

Top View



(8-Pin SOIC)

Ordering Information

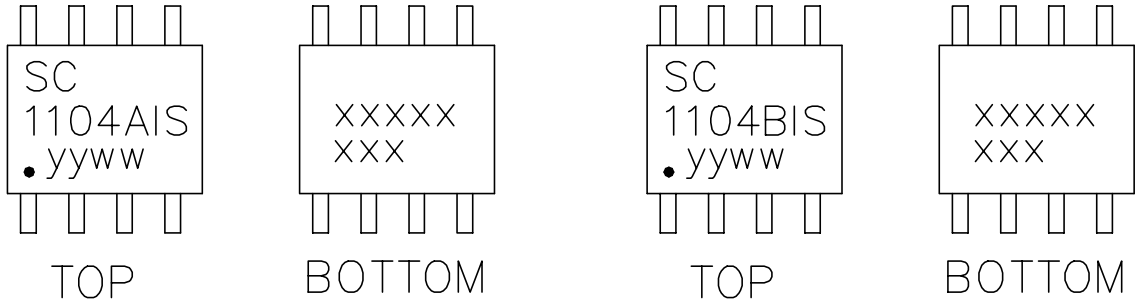
Device (2)	Package	Temp Range (T_J)
SC1104XISTR (1)	SOIC-8	-40° to 125°C

Note:
(1) In place of "X": A = 300kHz, V_{CC} = 5V to 12V.
B = 600kHz, V_{CC} = 5V.
(2) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	COMP/SS	Error amplifier output. Compensation, soft start/enable.
2	GND	Ground.
3	DL	Low side driver output
4	DH	High side driver output
5	BST	Bootstrap, high side driver.
6	PHASE	Input from the phase node between the MOSFETs.
7	VCC	Chip bias supply voltage.
8	SENSE	Output voltage sense input.

Marking Information



yyww = Date Code (Example: 0012)
xxxxxxx = Semtech Lot No. (Example: E90101-1)

Theory of Operation

Synchronous Buck Converter

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The inverting input of the error amplifier receives its voltage from the SENSE pin. The non-inverting input of the error amplifier is connected to an internal 1V reference.

The error amplifier output is connected to the COMPensation pin. The error amplifier generates a current proportional to (Vsense – 1V), which is the COMP pin output current (Transconductance ~ 10mS). The voltage on the COMP pin is the integral of the error amplifier current. The COMP voltage is the non-inverting input to the PWM comparator and controls the duty cycle of the MOSFET drivers. The size of capacitor Ccomp controls the stability and transient response of the regulator. The larger the capacitor, the slower the COMP voltage changes, and the slower the duty cycle changes.

The inverting input voltage of the PWM comparator is the triangular output of the oscillator.

When the oscillator output voltage drops below the COMP voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET. After a short delay ("dead time"), DH is pulled high, turning on the high-side FET. When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and after a dead time delay, DL is pulled high, turning on the low-side FET. The dead time delay is determined by a monostable on the chip.

The triangle wave minimum is about 1V, and the maximum is about 2V. Thus, if Vcomp = 0.9V, high side duty cycle is the minimum (~0%) , but if Vcomp is 2.0V, duty cycle is at maximum (~90%).The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 300kHz (SC1104A) or 600kHz (SC1104B).

Figure 1 shows a 3.3V output converter. If the Vout <3.3V, then the SENSE voltage < 1V. In this case the error amplifier will be sourcing current into the COMP pin so that COMP voltage and duty cycle will gradually increase. If Vout > 3.3V, the error amplifier will sink current and reduce the COMP voltage, so that duty cycle will decrease. The circuit will be in steady state when Vout =3.3V , Vsense = 1V, Icomp = 0 . The COMP voltage and duty cycle depend on Vin.

Under Voltage Lockout

The under voltage lockout circuit of the SC1104A/B assures that both high-side and low-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.2V typ.

$R_{DS(ON)}$ Current Limiting

In case of a short circuit or overload, the high-side (HS) FET will conduct large currents. To prevent damage, in this situation, large currents will generate a fault condition and begin a soft start cycle.

While the HS driver is on, the phase voltage is compared to the Vcc pin voltage. If the phase voltage is 200mV lower than Vcc, a fault is latched and the soft start cycle begins.

The voltages are compared during the middle of the HS pulse, to prevent transients from affecting the accuracy.

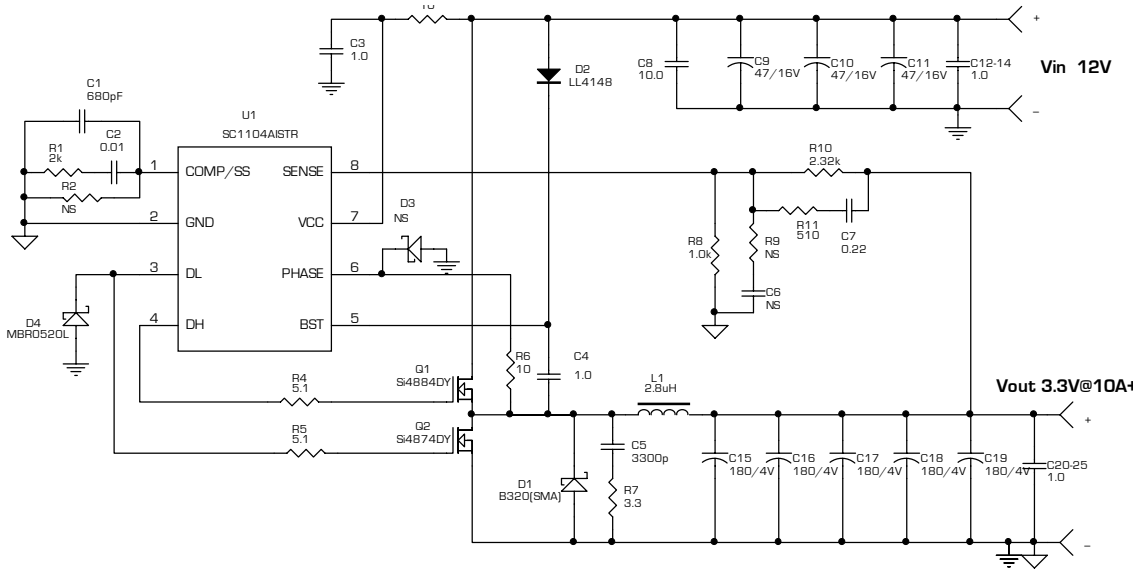
Soft Start

The soft start (or hiccup) circuitry is activated when a fault occurs. Faults occur for three reasons:

1) Under voltage (V_{CC} < 4.2V)
2) Over temperature (die temperature > 150°C)
3) Over current in high side FET.

All faults are handled the same way. Both DH and DL are forced low. The error amplifier is turned off, but a 2µA current flows into the comp pin (soft start current). The sink current reduces the Comp voltage down to 0.6V over a period of a few milliseconds. When Vcomp ~ 0.6V, the fault is cleared and the DL goes high. Also, the soft start current changes polarity and begins to increase the voltage on the Comp capacitor. The DH remains low, because Vcomp is less than the lowest excursion of the oscillator ramp (1.0V). After a few ms, the Vcomp increases to about 1.0V and the DH will start to switch. The duty cycle will gradually increase, and Vsns will increase. When Vsns ~ 1.00V, the error amplifier turns on again. The circuit has now reached its operating point. If a fault occurs during the soft start, the cycle will begin again (drivers low, Vcomp decreasing down to 0.6V).

Evaluation Board Schematic - 300kHz



C9,10,11: Sanyo, 16TPB47M

C15,16,17,18,19: Sanyo, 4TPB220M or Panasonic, EEFUE0G181R

L1: Sumida, CEP125-2R8MC-H

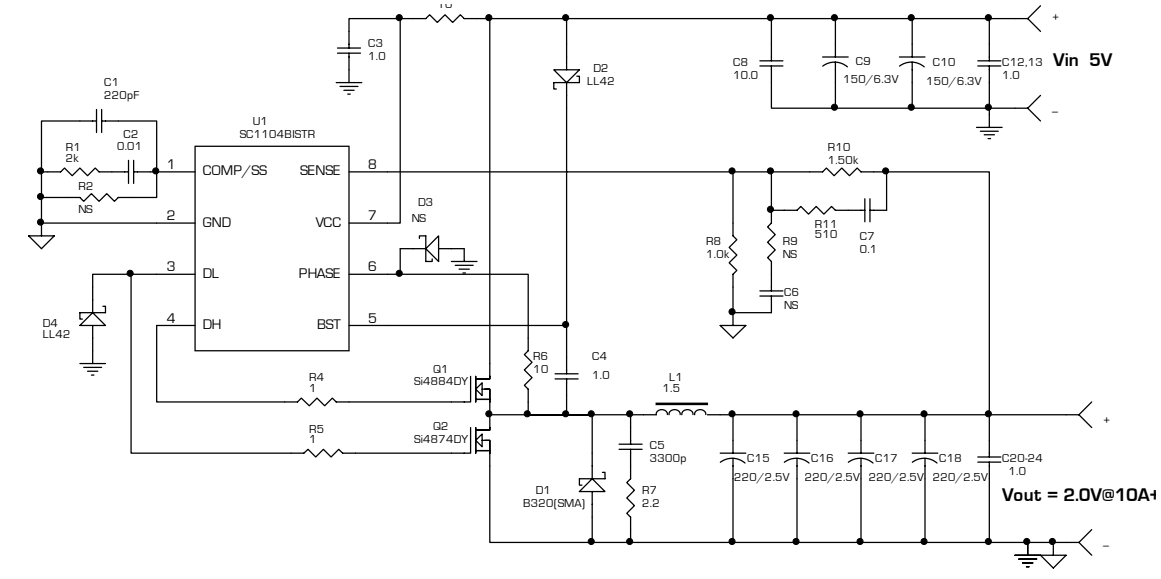
Q,Q2: Siliconix-Vishay

D1-4: Vishay

U1: SEMTECH, SC1104AISTR

1104A - 300kHz

Evaluation Board Schematic - 600kHz



C9,10: Sanyo, 6TPB150M or Panasonic, EEFUE0J151R

C15,16,17,18: Sanyo, 4TPB220M or Panasonic, EEFUE0E221R

L1: Sumida, CEP125-1R5MC

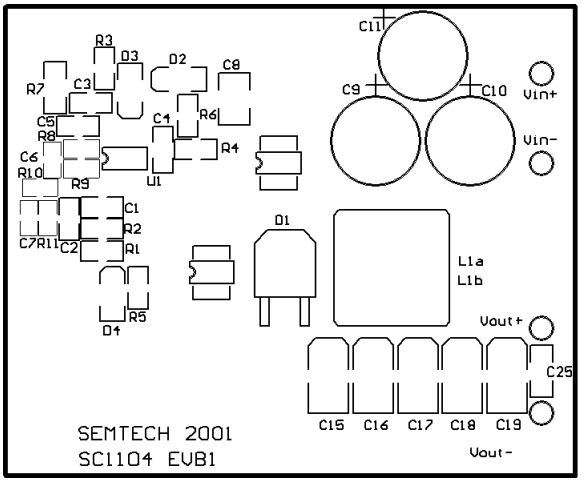
Q,Q2: Siliconix-Vishay

D1-4: Vishay

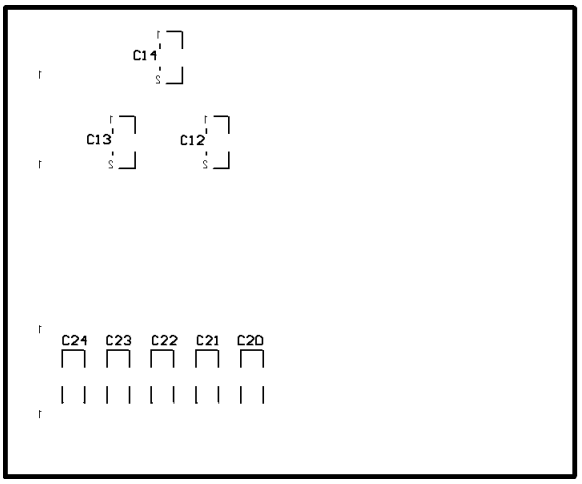
U1: SEMTECH, SC1104BISTR

1104B - 600kHz

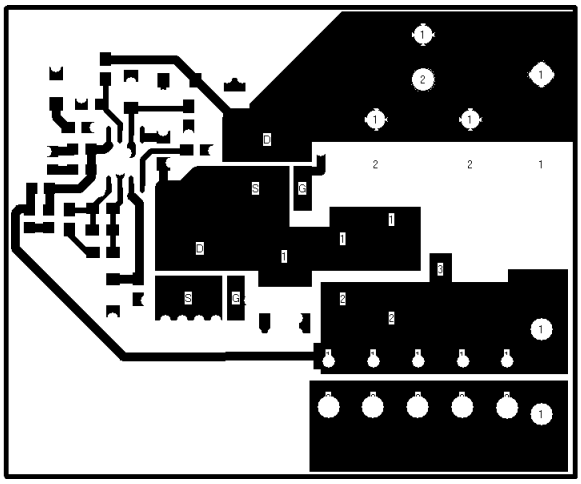
Evaluation PC Board



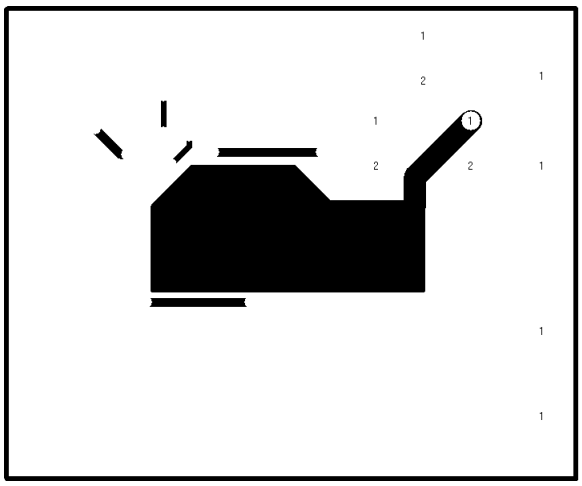
Top View



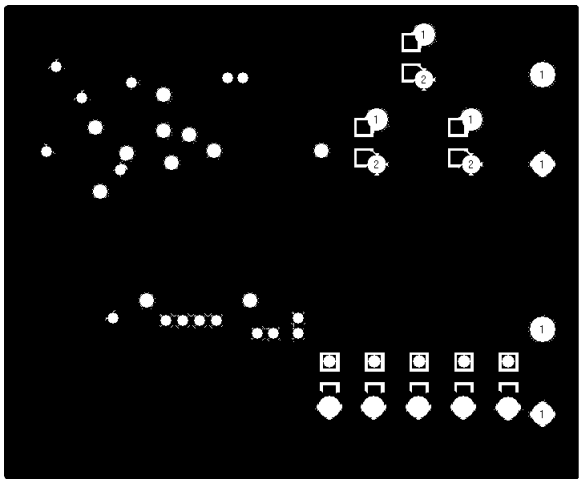
Bottom View



Top Layer

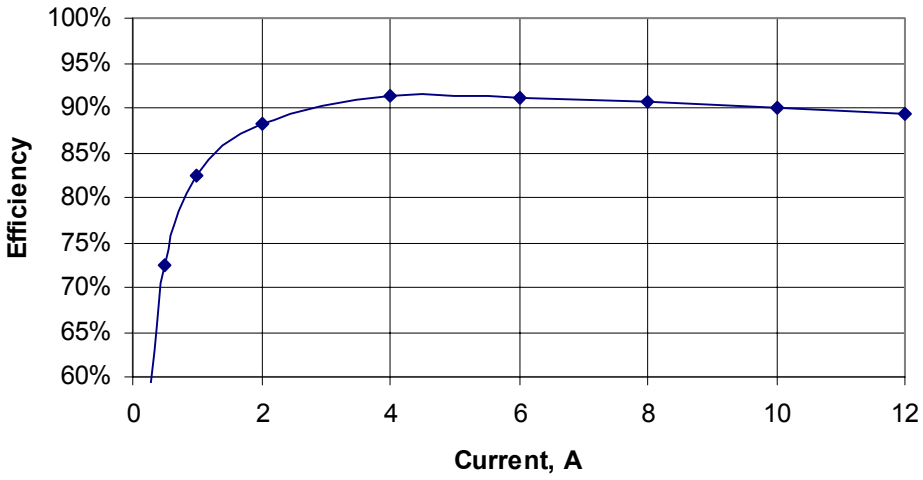


Mid Layer

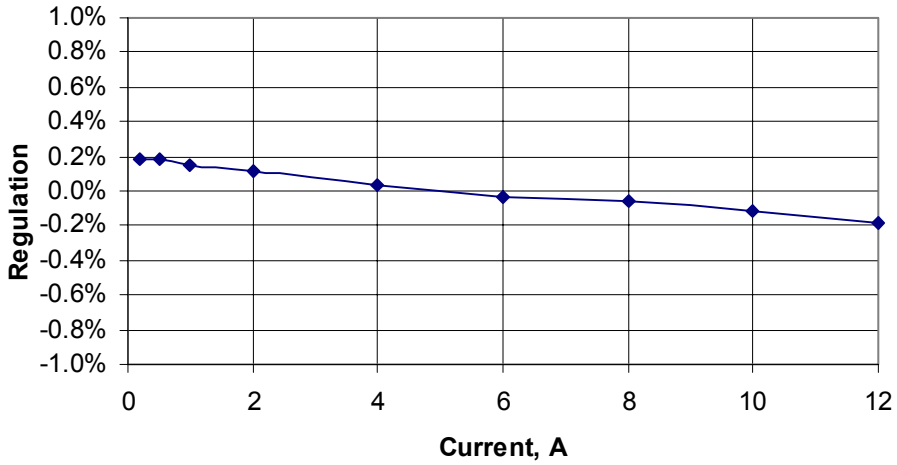


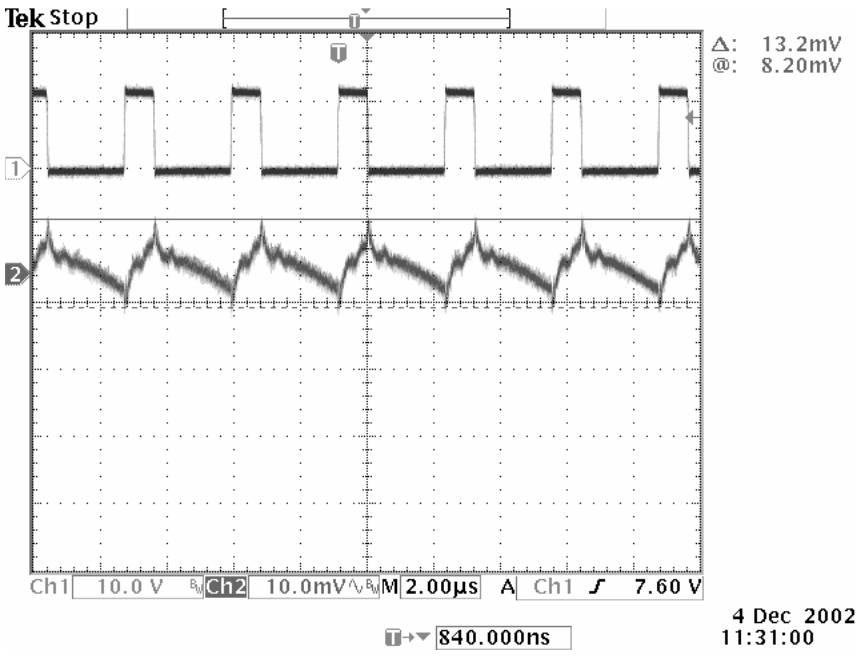
Bottom Layer

Typical Characteristics

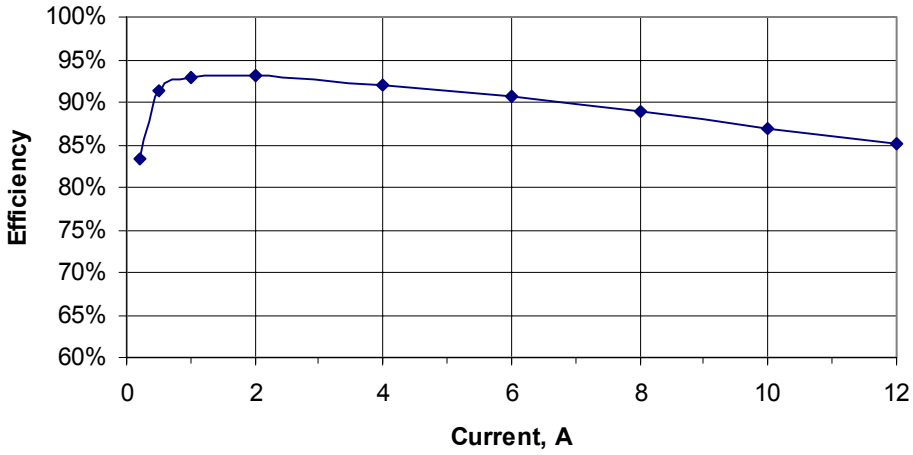


12V = Vin
3.3V = Vout
12A = Iout

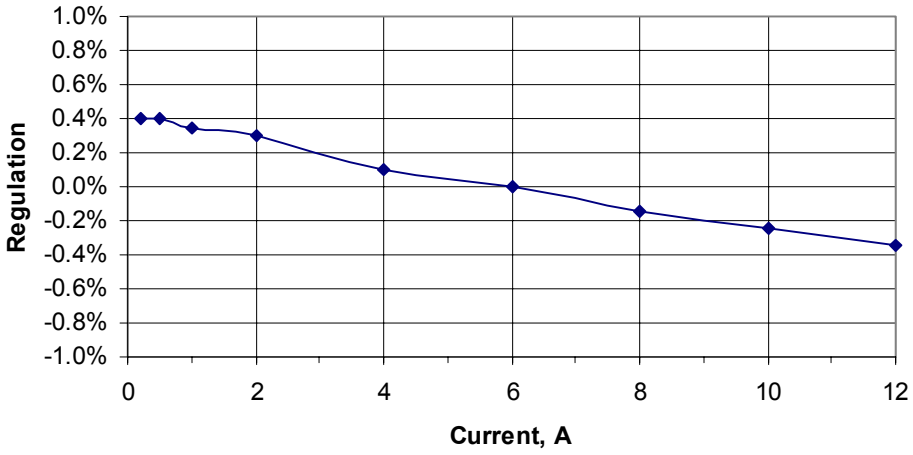


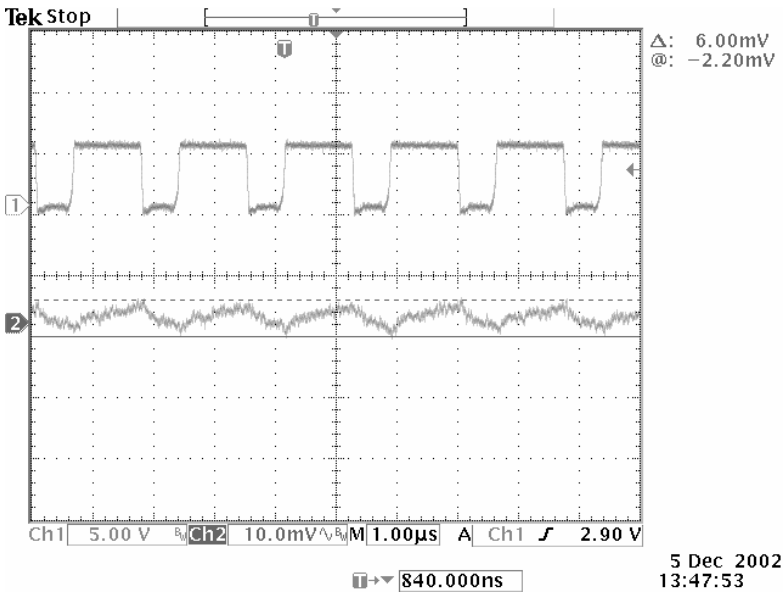


Typical Characteristics (Cont.)

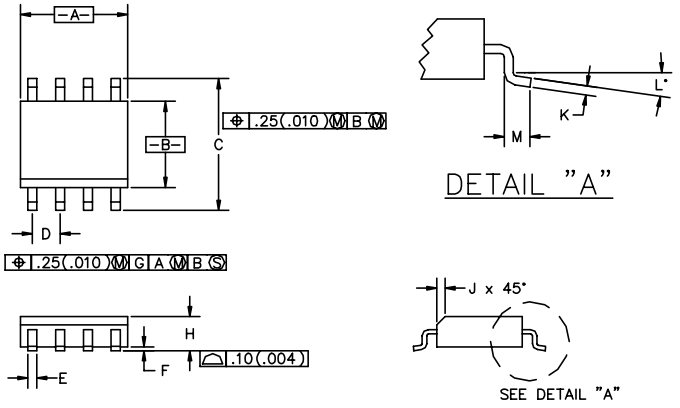


5V = Vin
2V = Vout
12A = Iout



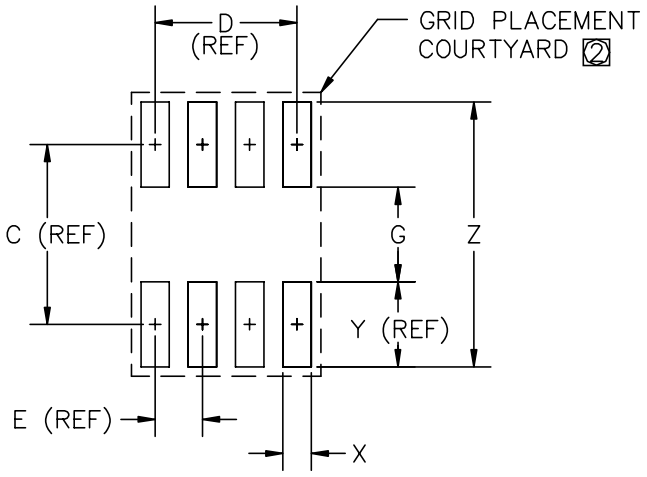


Outline Drawing - SO-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

Contact Information

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Power Management Products Division
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Phone: (805)498-2111 FAX (805)498-3804