

POWER MANAGEMENT

Description

The SC2602 and SC2602A are low-cost, full featured, synchronous voltage-mode controllers designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC2602s are ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive N-channel power switches.

SC2602s features include temperature compensated voltage reference, triangle wave oscillator and current sense comparator circuitry. Power good signaling, shut-down, and over voltage protection are also provided.

The SC2602 operates at a fixed 200kHz and the SC2602A at 500kHz, providing a choice for optimum compromise between efficiency, external component size, and cost.

Two SC2602s can be used together to sequence power up of telecom systems. The power good of the first SC2602 connected to the enable of the second SC2602 makes this possible.

Features

- ◆ Synchronous operation for high efficiency (95%)
- ◆ $R_{DS(ON)}$ current sensing
- ◆ On-chip power good and OVP functions
- ◆ Small size with minimum external components
- ◆ Soft Start
- ◆ Enable function

Applications

- ◆ Microprocessor core supply
- ◆ Low cost synchronous applications
- ◆ Voltage Regulator Modules (VRM)
- ◆ DDR termination supplies
- ◆ Networking power supplies
- ◆ Sequenced power supplies

Typical Application Circuit

Typical Distributed Power Supply

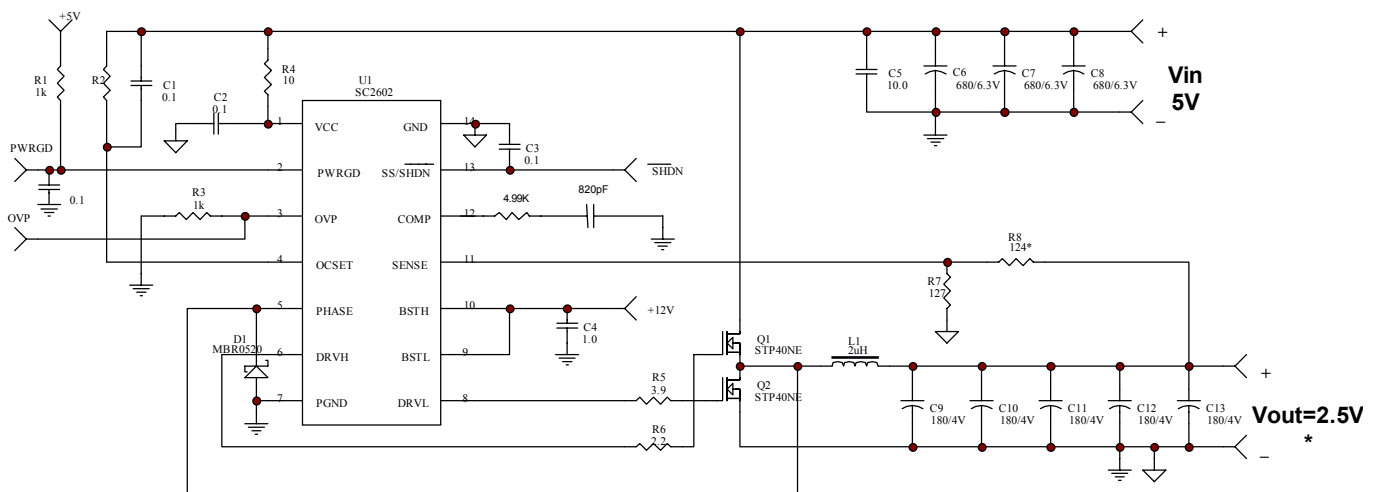


Figure 1.

NOTE:
*) $V_{out} = 1.265 \times (1 + R8/R7)$

POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
VCC, BSTL to GND	V_{IN}	-1.0 to 16 (20V Surge)	V
PGND to GND		± 0.5	V
PHASE to GND ⁽¹⁾		-0.5 to 18 (20V Surge)	V
BSTH to PHASE		16 (20V Surge)	V
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	115	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Note: (1) -1.5V to 20V for 25ns repetitive every cycle.

Electrical Characteristics

Unless specified: $V_{CC} = 4.75V$ to $12.6V$; $GND = PGND = 0V$; $FB = V_O$; $V_{BSTL} = 12V$; $V_{BSTH-PHASE} = 12V$; $T_J = 25^\circ C$

Parameter	Conditions	Min	Typ	Max	Units
Power Supply					
Supply Voltage	VCC	4.2		12.6	V
Supply Current	EN = VCC		6	10	mA
Line Regulation	VO = 2.5V		0.5		%
Error Amplifier					
Gain (AOL)			50		dB
Input Bias			5	8	μA
Oscillator					
Oscillator Frequency	SC2602	180	200	220	kHz
	SC2602A	450	500	550	
Oscillator Max Duty Cycle		90	95		%
MOSFET Drivers					
DH Source/Sink	BSTH - DH = 4.5V, DH - PHASE = 2V	1			A
DL Source/Sink	BSTL - DL = 4.5V. DL - PGND. = 2V	1			A

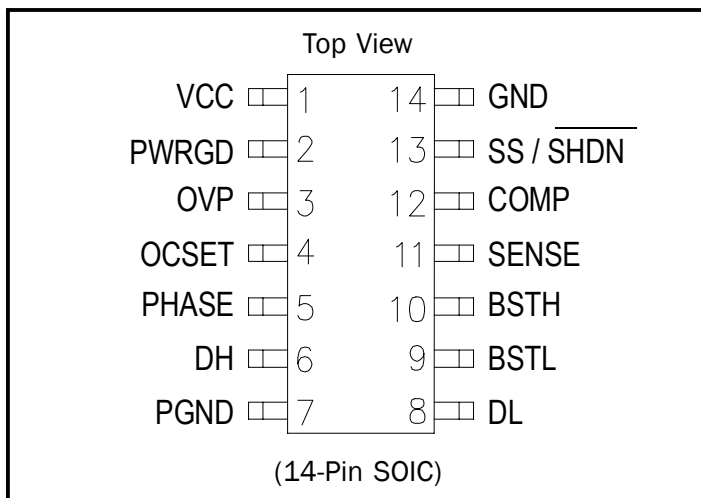
POWER MANAGEMENT
Electrical Characteristics (Cont.)

Unless specified: $V_{CC} = 4.75V$ to $12.6V$; $GND = PGND = 0V$; $FB = V_O$; $V_{BSTL} = 12V$; $V_{BSTH-PHASE} = 12V$; $T_J = 25^\circ C$

Parameter	Conditions	Min	Typ	Max	Units
PROTECTION					
OVP Threshold Voltage			20		%
OVP Source Current	$V_{OVP} = 3V$	10			mA
Power Good Threshold		88		112	%
Dead Time		45		100	ns
Over current Set Isink	$2.0V \leq V_{OCSET} \leq 12V$	180	200	220	μA
Reference					
Reference Voltage	$0^\circ C$ to $70^\circ C$	1.252	1.265	1.278	V
Accuracy		-1		+1	%
Soft Start					
Charge Current	$V_{SS} = 1.5V$	8.0	10	12	μA
Discharge Current	$V_{SS} = 1.5V$		1.5		μA

Note:

(1) Specification refers to application circuit (Figure 1).

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Pin Configuration

Ordering Information

Device ⁽¹⁾	Frequency	Package
SC2602STR	200kHz	SO-14
SC2602ASTR	500kHz	
SC2602EVB	Evaluation Board	

Note:

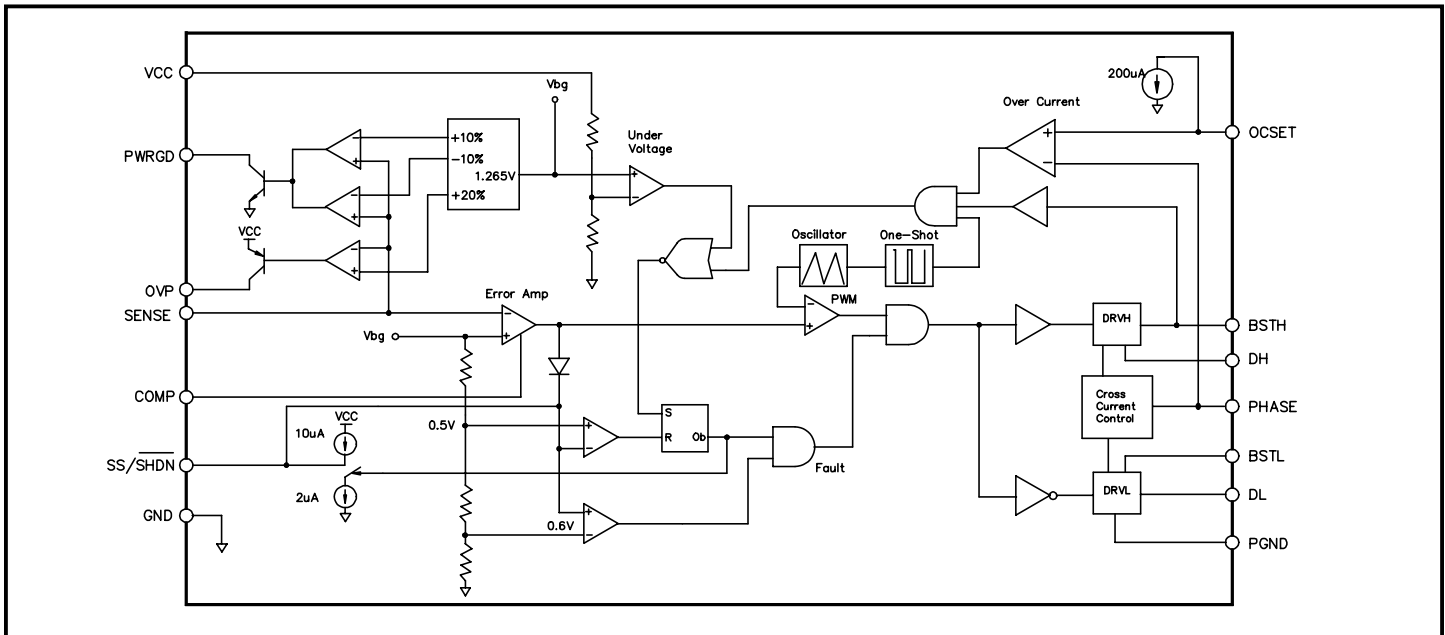
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Chip supply voltage.
2	PWRGD	Logic high indicates correct output voltage.
3	OVP	Over voltage protection.
4	OCSET	Sets the converter overcurrent trip point.
5	PHASE	Input from the phase node between the MOSFETs.
6	DH	High side driver output.
7	PGND	Power ground.
8	DL	Low side driver output.
9	BSTL	Bootstrap, low side driver.
10	BSTH	Bootstrap, high side driver.
11	SENSE	Voltage sense input.
12	COMP	Compensation pin.
13	SS/SHDN	Soft start. A capacitor to ground sets the slow start time.
14	GND	Signal ground.

Note:

(1) All logic level inputs and outputs are open collector TTL compatible.

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Block Diagram

Theory of Operation
Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including “Power Good” flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference (See Fig. 1). The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200kHz/500kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. The non-inverting input of the comparator receives its input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the SC2602 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP’s collector.

Power Good

The power good function is to confirm that the regulator outputs are within +/-10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

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Applications Information (Cont.)

Soft Start

Initially, $\overline{\text{SS/SHDN}}$ sources $10\mu\text{A}$ of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on $\overline{\text{SS/SHDN}}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

$R_{\text{DS(ON)}}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the $200\mu\text{A}$ internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switch turns off and $\overline{\text{SS/SHDN}}$ starts to sink $2\mu\text{A}$. When $\overline{\text{SS/SHDN}}$ reaches 0.8V , it then starts to source $10\mu\text{A}$ and a new cycle begins.

Hiccup Mode

During power up, the $\overline{\text{SS/SHDN}}$ pin is internally pulled low until VCC reaches the undervoltage lockout level of 4.2V . Once V_{CC} has reached 4.2V , the $\overline{\text{SS/SHDN}}$ pin is released and begins to source $10\mu\text{A}$ of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of $200\text{kHz}/500\text{kHz}$, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V .

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the valley of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the $\overline{\text{SS/SHDN}}$ pin begins to sink $2\mu\text{A}$. The soft-start voltage will begin to decrease as the $2\mu\text{A}$ of current discharges the external capacitor. When the soft-start voltage reaches 0.8V , the $\overline{\text{SS/SHDN}}$ pin will begin to source $10\mu\text{A}$ and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the $\overline{\text{SS/SHDN}}$ pin will again begin to sink $2\mu\text{A}$. This cycle will continue indefinitely until the over-current condition is removed.

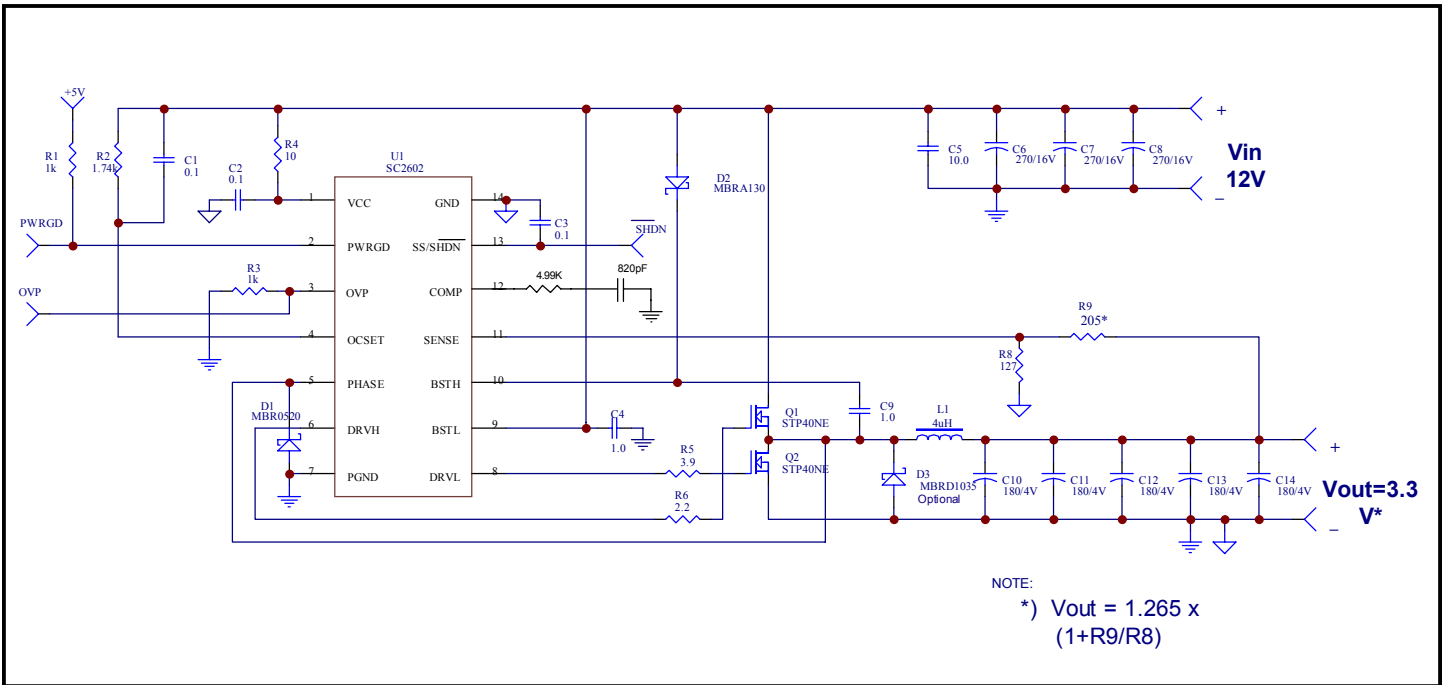
In conclusion, below is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of 12V is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

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Application Circuit

Typical 12V Application Circuit with Bootstrapped BSTH



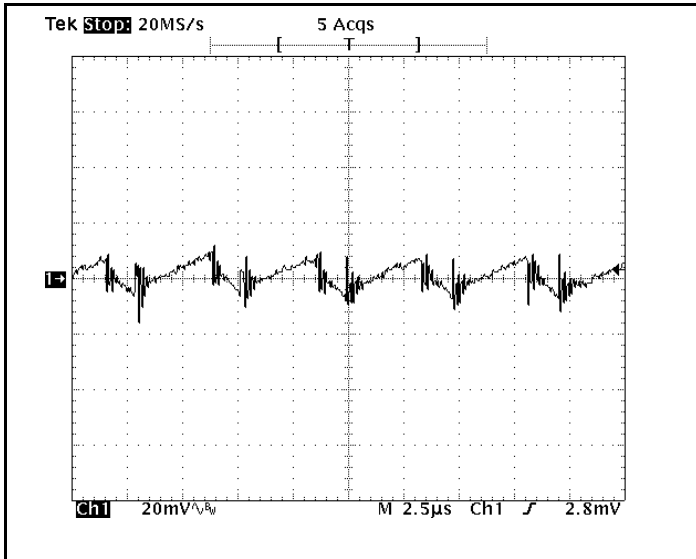
POWER MANAGEMENT

Typical Characteristics

Output Ripple Voltage

Ch1: Vo_rpl

1. $V_{IN} = 5V$; $V_O = 3.3V$; $I_{OUT} = 12A$

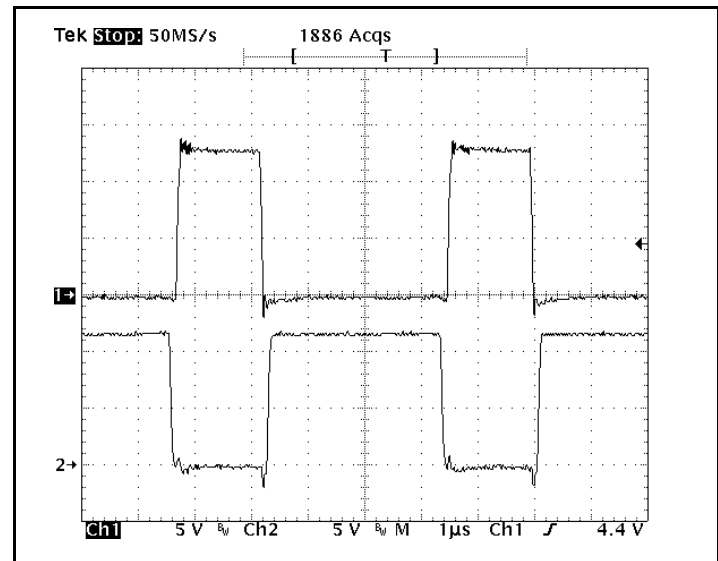
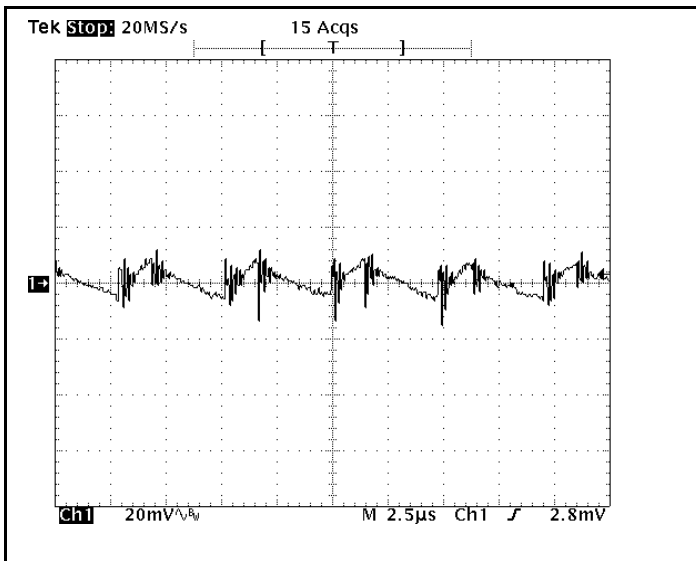
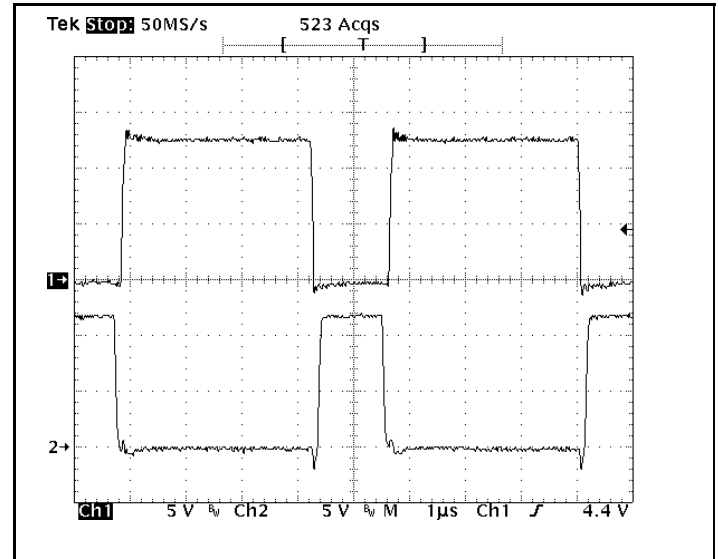


Wave forms are shown for SC2602 and are similar for SC2602A but at higher frequency.

Gate Drive Waveforms

Ch1: Top FET

Ch2: Bottom FET



Ch1: Vo_rpl

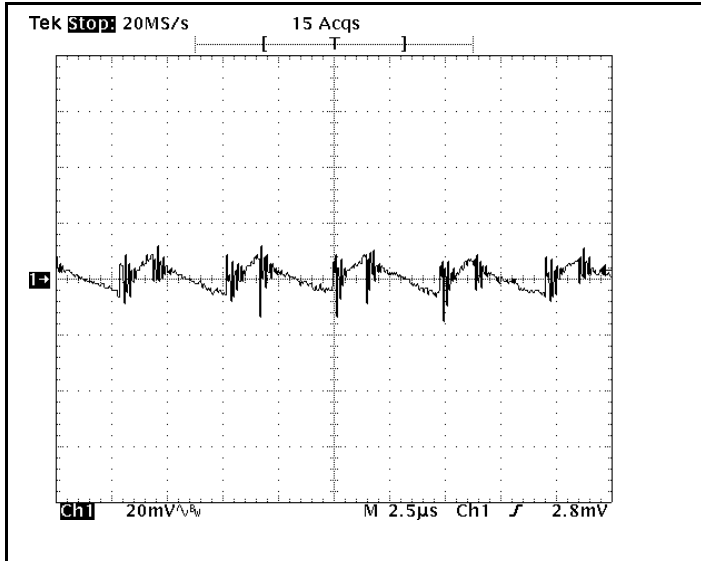
2. $V_{IN} = 5V$; $V_{OUT} = 1.3V$; $I_{OUT} = 12A$

Ch1: Top FET

Ch2: Bottom FET

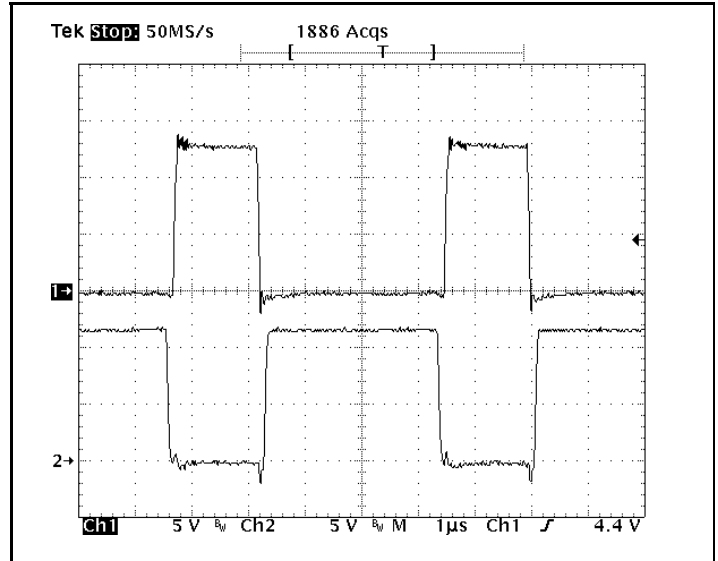
POWER MANAGEMENT
Typical Characteristics (Cont.)

Ch1: Vo_rpl

 2. $V_{IN} = 5V$; $V_{OUT} = 1.3V$; $I_{OUT} = 12A$


Ch1: Top FET

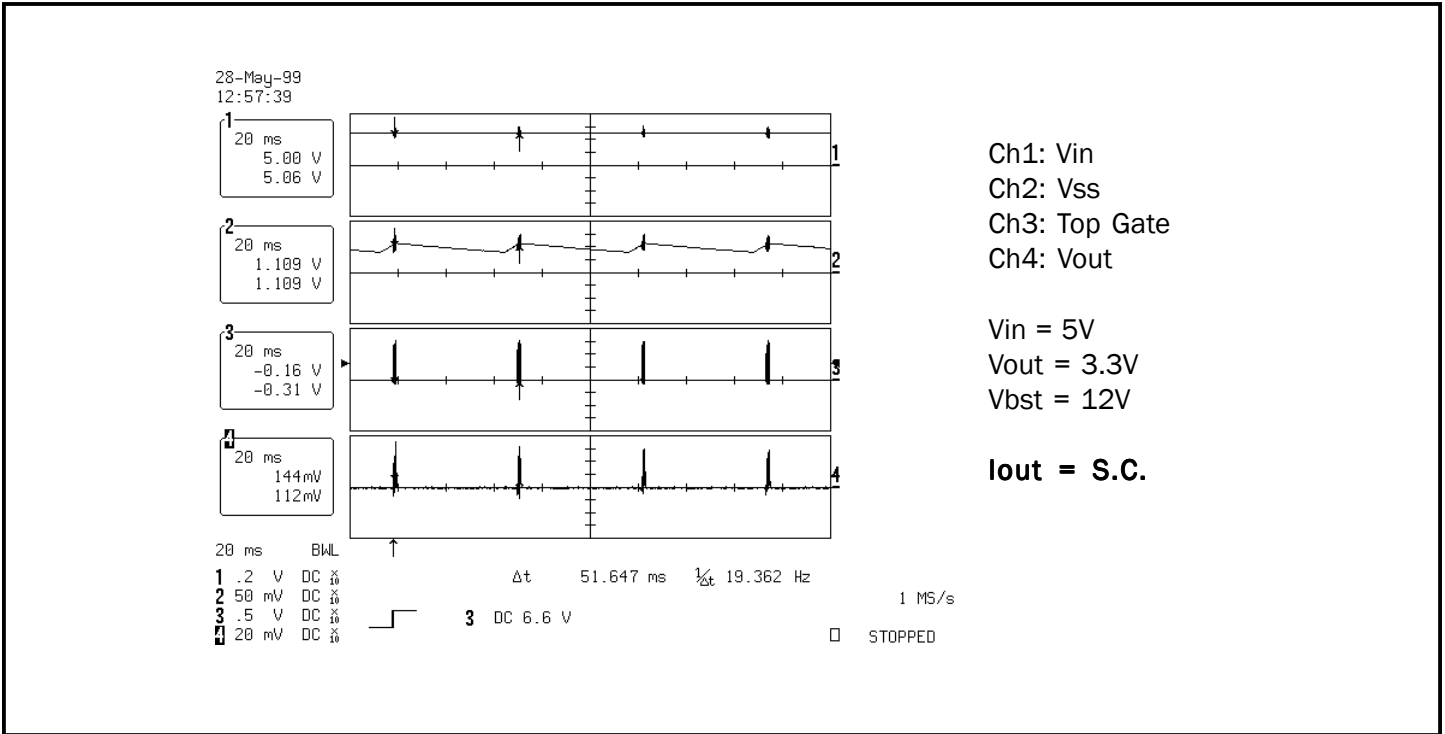
Ch2: Bottom FET



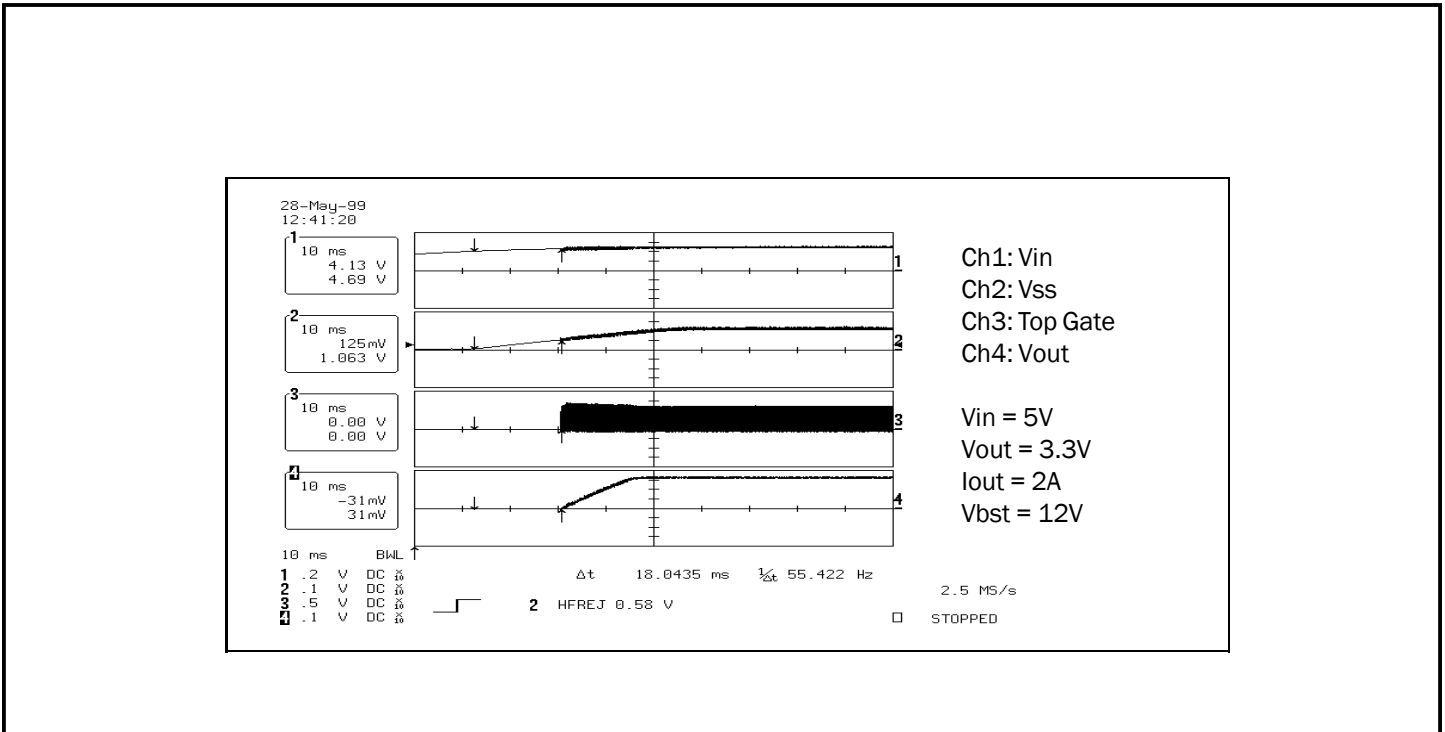
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Typical Characteristics (Cont.)

Hiccup Mode



Start Up Mode



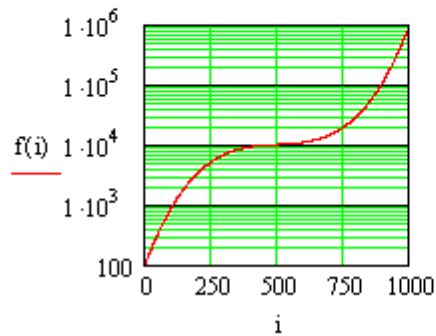
Math Cad Close Loop Stability Analysis

General Equations | Sample Frequencies Calculations

$$i := 1, 2 \dots 10^3$$

$$Fc := 10 \cdot 10^3$$

$$f(i) := Fc \cdot 1.0005^{i-500} + 10^{-4.16} \cdot (i-500)^3$$

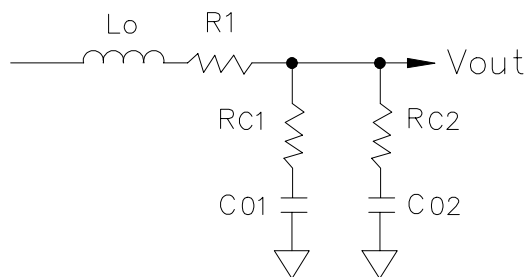


$$g(i) := \text{if} \left(i - 900 \geq 0, \frac{i - 900}{100}, 0 \right)$$

$$j := (-1)^{.5}$$

$$W(i) := 2 \cdot \pi \cdot j \cdot f(i)$$

Output Filter Schematic:



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Typical Characteristics (Cont.)

Output filter calculation

$$L_o := 4.3 \cdot 10^{-6} \quad R_l := 5 \cdot 10^{-3} \quad C_{o1} := 1500 \cdot 10^{-6} \quad R_{c1} := 20 \cdot 10^{-3} \quad C_{o2} := 100 \cdot 10^{-6} \quad R_{c2} := 1 \cdot 10^{-3}$$

$$Z_{c1}(i) := R_{c1} + \frac{1}{C_{o1} \cdot W(i)} \quad Z_{c2}(i) := R_{c2} + \frac{1}{C_{o2} \cdot W(i)} \quad Z_c(i) := \frac{Z_{c1}(i) \cdot Z_{c2}(i)}{Z_{c1}(i) + Z_{c2}(i)}$$

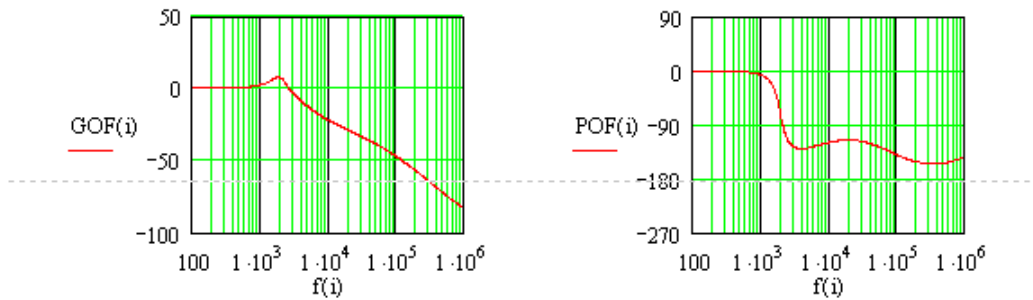
$$OF(i) := \frac{Z_c(i)}{R_l + L_o \cdot W(i) + Z_c(i)} \quad Gof(i) := \left(\text{Re}(OF(i))^2 + \text{Im}(OF(i))^2 \right)^{.5}$$

$$GOF(i) := 20 \cdot \log(Gof(i))$$

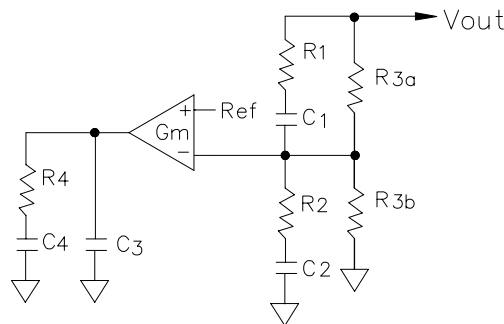
$$C(i) := \frac{\text{Re}(OF(i) \cdot j^{g(i)})}{Gof(i)} \quad S(i) := \frac{\text{Im}(OF(i) \cdot j^{g(i)})}{Gof(i)}$$

$$POF(i) := \frac{360}{2 \cdot \pi} \cdot \text{acos}(C(i)) \cdot \text{if}(S(i) \geq 0, 1, -1) + 180 \cdot \text{if}(S(i) \geq 0, -2, 0) - 90 \cdot g(i)$$

Output Filter Plots



Error Amplifier Schematic



Error Amplifier calculation

$$\begin{aligned}
 R3a &:= 10 \cdot 10^{-3} & R1 &:= .1 \cdot 10^{-3} & R2 &:= .1 \cdot 10^{-3} & R4 &:= 15 \cdot 10^{-3} & C3 &:= .01 \cdot 10^{-9} \\
 R3b &:= 10 \cdot 10^{-3} & C1 &:= 30 \cdot 10^{-9} & C2 &:= 1000 \cdot 10^{-9} & C4 &:= 100 \cdot 10^{-9} & Gm &:= 1.5 \cdot 10^{-3}
 \end{aligned}$$

$$\begin{aligned}
 Z1(i) &:= \frac{R3a \cdot \left(R1 + \frac{1}{C1 \cdot W(i)} \right)}{R3a + R1 + \frac{1}{C1 \cdot W(i)}} & Z2(i) &:= \frac{R3b \cdot \left(R2 + \frac{1}{C2 \cdot W(i)} \right)}{R3b + R2 + \frac{1}{C2 \cdot W(i)}} & Z3(i) &:= \frac{\left(R4 + \frac{1}{C4 \cdot W(i)} \right) \cdot \frac{1}{C3 \cdot W(i)}}{R4 + \frac{1}{C4 \cdot W(i)} + \frac{1}{C3 \cdot W(i)}}
 \end{aligned}$$

$$EA(i) := -\frac{Z2(i)}{Z1(i) + Z2(i)} \cdot Z3(i) \cdot Gm$$

$$G_{ea}(i) := \left(\text{Re}(EA(i))^2 + \text{Im}(EA(i))^2 \right)^{.5}$$

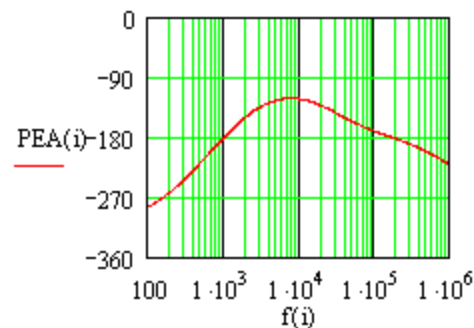
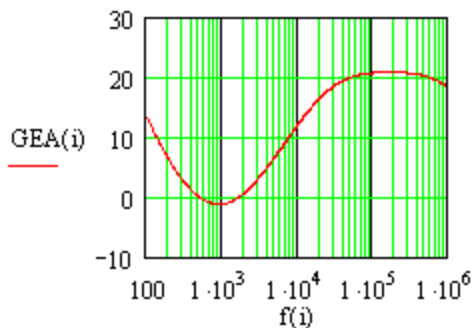
$$GEA(i) := 20 \cdot \log(G_{ea}(i))$$

$$C(i) := \frac{\text{Re}(EA(i) \cdot j^{g(i)})}{G_{ea}(i)}$$

$$S(i) := \frac{\text{Im}(EA(i) \cdot j^{g(i)})}{G_{ea}(i)}$$

$$PEA(i) := \frac{360}{2 \cdot \pi} \cdot \text{acos}(C(i)) \cdot \text{if}(S(i) \geq 0, 1, -1) + 180 \cdot \text{if}(S(i) \geq 0, -2, 0) - 90 \cdot g(i)$$

Error Amplifier plots



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Typical Characteristics (Cont.)

Close Loop Calculation

$$V_{in} := 3.3$$

$$V_{pp} := \frac{1}{1.7}$$

$$CL(i) := OF(i) \cdot EA(i) \cdot \frac{v_{in}}{V_{pp}}$$

$$G_{cl}(i) := \left(\text{Re}(CL(i))^2 + \text{Im}(CL(i))^2 \right)^{0.5}$$

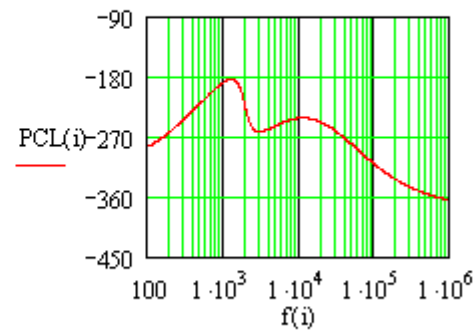
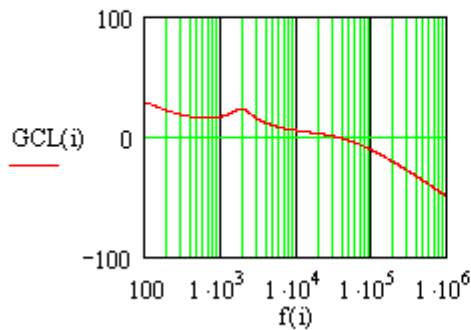
$$GCL(i) := 20 \cdot \log(G_{cl}(i))$$

$$C(i) := \frac{\text{Re}(CL(i) \cdot j^{g(i)})}{G_{cl}(i)}$$

$$S(i) := \frac{\text{Im}(CL(i) \cdot j^{g(i)})}{G_{cl}(i)}$$

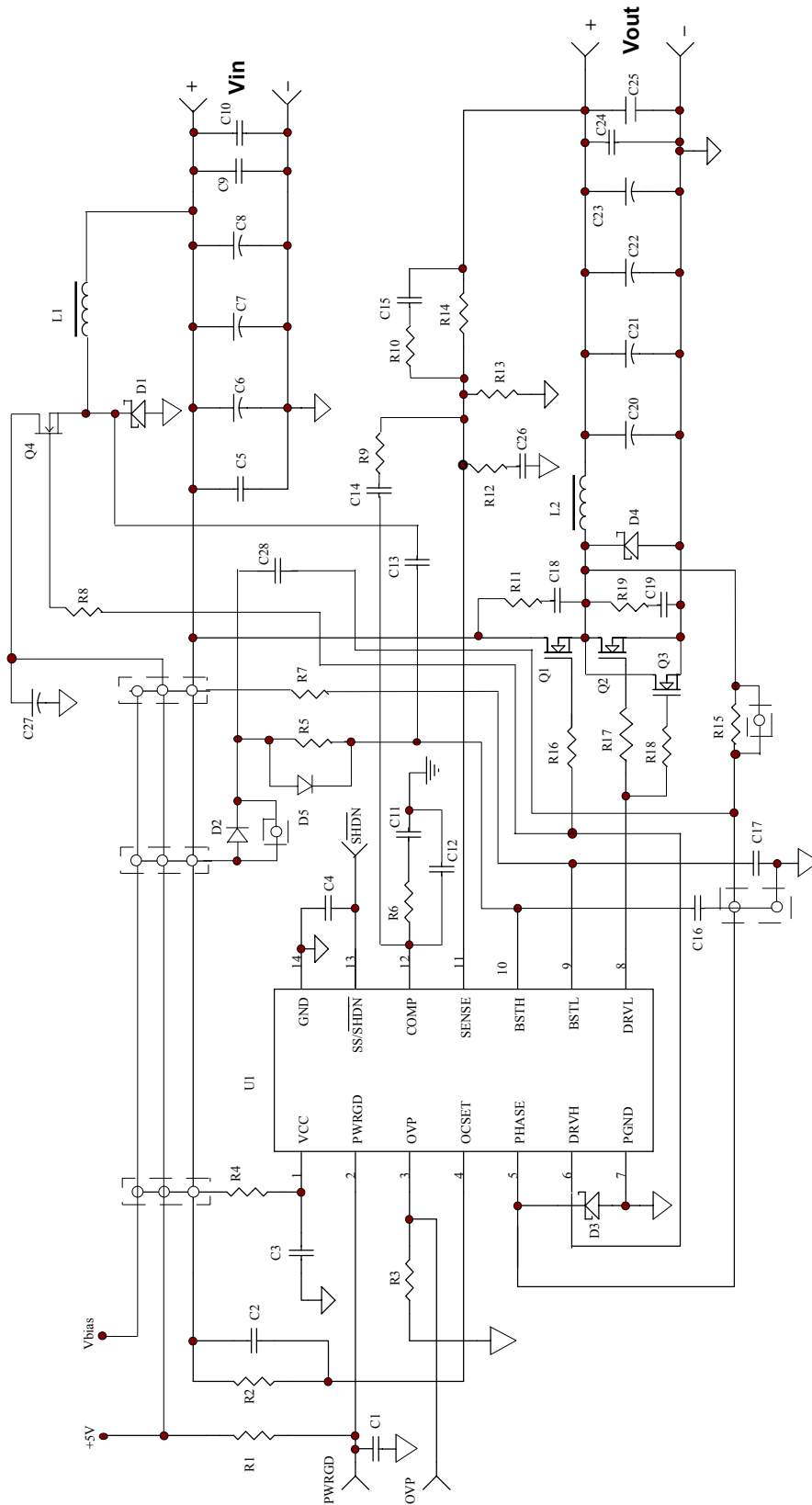
$$PCL(i) := \frac{360}{2 \cdot \pi} \cdot \text{acos}(C(i)) \cdot \text{if}(S(i) \geq 0, 1, -1) + 180 \cdot \text{if}(S(i) \geq 0, -2, 0) - 90 \cdot g(i)$$

Close Loop plots



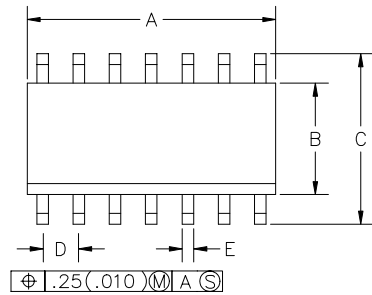
POWER MANAGEMENT

Evaluation Board Schematic

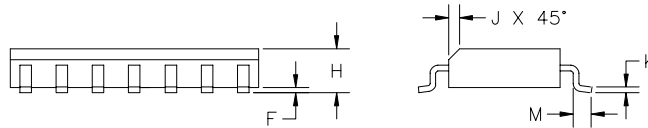


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Outline Drawing - S0-14

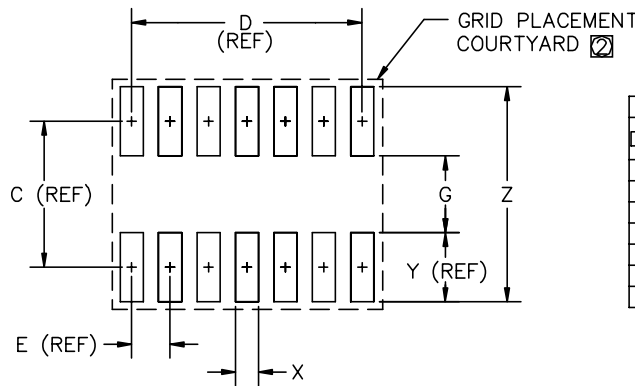


DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.337	.344	8.55	8.75	2
B	.150	.158	3.80	4.00	3
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.010	.020	0.25	0.50	
K	.007	.010	.19	.25	
M	.016	.050	0.40	1.27	



- ③ DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.
- ④ DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.
- ⑤ CONTROLLING DIMENSION : MILLIMETER

Land Pattern - S0-14



DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	-	.19	-	5.00	-
D	-	.30	-	7.62	-
E	-	.05	-	1.27	-
G	.10	.11	2.60	2.80	-
X	.02	.03	.60	.80	-
Y	-	.09	-	2.40	-
Z	-	.29	7.20	7.40	-

- ⑥ GRID PLACEMENT COURTYARD IS 20x16 ELEMENTS (10mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.
- ⑦ CONTROLLING DIMENSION: MILLIMETERS

Contact Information

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