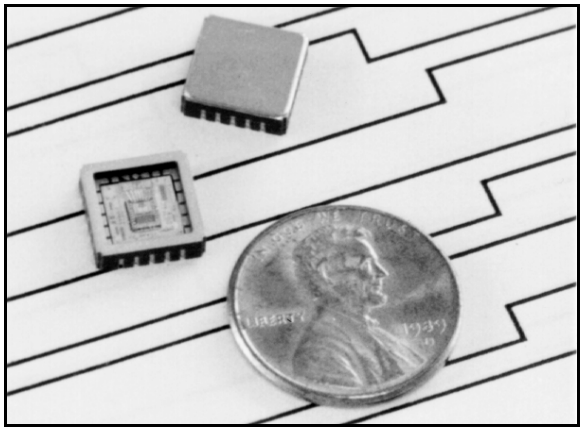
# SILICON DESIGNS, INC

**Model 1010**
**DIGITAL ACCELEROMETER**

## CAPACITIVE
## DIGITAL OUTPUT
## WIDE TEMPERATURE RANGE
## SURFACE MOUNT PACKAGE



### *FEATURES*

- **Digital Pulse Density Output**
- **Low Power Consumption**
- **-55 to +125 °C Operation**
- **Built-in Nitrogen Damping**
- **TTL/CMOS Compatible**
- **+5 V DC Power**
- **No External Reference Voltage**
- **Easy Interface to Microprocessors**
- **Good EMI Resistance**
- **Responds to DC & AC Acceleration**
- **Non Standard G Ranges Available**
- **Hermetic LCC or J-Lead Surface Mount Package**

### *ORDERING INFORMATION*

| Full Scale Acceleration | Hermetic Packages | |
|---|---|---|
| | 20 pin LCC | 20 pin JLCC |
| ±5 G | 1010L-005 | 1010J-005 |
| ±10 G | 1010L-010 | 1010J-010 |
| ±25 G | 1010L-025 | 1010J-025 |
| ±50 G | 1010L-050 | 1010J-050 |
| ±100 G | 1010L-100 | 1010J-100 |
| ±200 G | 1010L-200 | 1010J-200 |

### *DESCRIPTION*

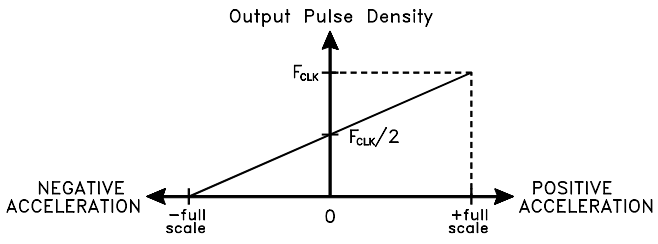
The Model 1010 accelerometer is a low-cost, integrated accelerometer for use in zero to medium frequency instrumentation applications. It combines in a single, miniature, hermetically sealed package a micromachined capacitive sense element and a custom integrated circuit that includes a sense amplifier and a sigma-delta A/D converter. It is relatively insensitive to temperature changes and gradients.

### *OPERATION*

The Model 1010 accelerometer produces a digital pulse train in which the density of pulses (number of pulses per second) is proportional to applied acceleration. It operates with a single +5 volt power supply and requires a clock of 100kHz-1MHz. The output is ratiometric to the clock frequency and independent of the power supply voltage. Two forms of digital signals are provided for direct interfacing to a microprocessor or counter. The sensitive axis is perpendicular to the bottom of the package, with positive acceleration defined as a force pushing on the bottom of the package. External digital line drivers can be used to drive long cables or when used in an electrically noisy environment.

### *APPLICATIONS*

| COMMERCIAL | INDUSTRIAL |
|---|---|
| ● Automotive | ● Vibration Monitoring |
| Air Bags | ● Vibration Analysis |
| Active Suspension | ● Machine Control |
| Adaptive Brakes | ● Modal Analysis |
| Alarm Systems | ● Robotics |
| ● Shipping Recorders | ● Crash Testing |
| ● Appliances | ● Instrumentation |

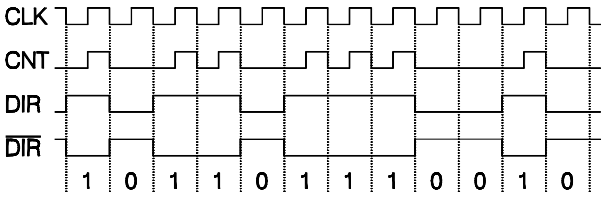


## *SIGNAL DESCRIPTIONS*

**VDD & GND (Power):** Pin 14 (VDD) & pin 19 (GND). Additionally tie pins 3 & 11 to VDD & pins 2, 5, 6 & 18 to GND.

**CLK (Input):** Pin 8. Reference clock input. This hysteresis threshold input must be driven by a 50% duty cycle square wave signal. All 1010 series accelerometers are calibrated at 250 kHz which is the recommended clock frequency for best results. Operation at frequencies as low as 100 kHz or as high as 1 MHz are possible, however a slight bias calibration shift may result.

**CNT (Output)**: Pin 10. Count output. A return-to-zero type digital pulse stream whose pulse width is equal to the input CLK logic high time. The CNT pulse rate increases with positive acceleration. The device experiences positive (+1g) acceleration with its lid facing up in the earth's gravitational field. This signal is meant to drive an up-counter directly.




**DIR and $\overline{DIR}$ (Output):** Pins 12 and 16 respectively. Direction output. This output is updated at the fall of each clock cycle. It is high during clock cycles when a high going CNT pulse is present and low during cycles when no CNT pulse is present. A non-return-to-zero signal meant to control the count direction (i.e. up or down) of a counter. DIR can be low pass filtered to produce an analog measure of the acceleration. $\overline{DIR}$ is the complement of DIR and is provided for use in driving differential transmission lines.

**DV (Input):** Pin 4. Deflection Voltage. Normally left open. A test input that applies an electrostatic force to the sense element, simulating a positive acceleration without the application of an accelerative force.

**VR (Input):** Pin 3. Voltage Reference. Tie to same voltage as VDD or to a filtered version of +5V for better noise immunity. A 0.1uF bypass capacitor is recommended at this pin.

**CLK/2 (Output):** Pin 15. Clock divided by 2. A buffered clock output whose frequency equals CLK divided by 2.

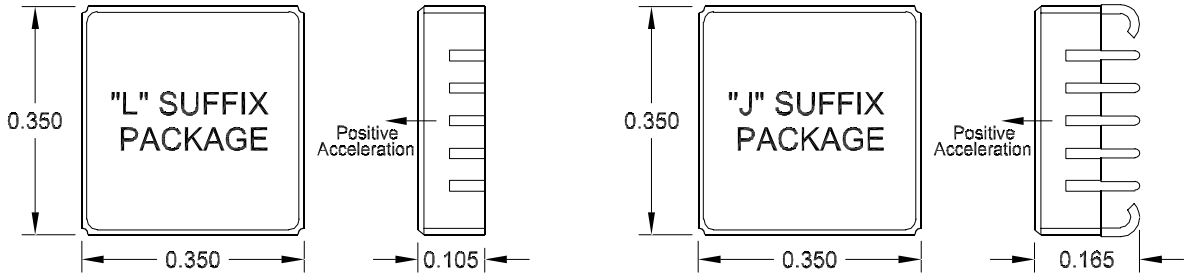
***PERFORMANCE by Model:*** $V_{DD}$=5.0VDC, $T_C$=25°C.

| Model Number | 1010x-005 | 1010x-010 | 1010x-025 | 1010x-050 | 1010x-100 | 1010x-200 | Units |
|---|---|---|---|---|---|---|---|
| Input Range | ±5 | ±10 | ±25 | ±50 | ±100 | ±200 | G |
| Frequency Response (Nominal, 3 dB) | 0 - 600 | 0 - 1000 | 0 - 1600 | 0 - 2000 | 0 - 2500 | 0 - 2500 | Hz |
| Sensitivity ($F_{CLK}$=1MHz) | 0.01 | 0.02 | 0.05 | 0.10 | 0.20 | 0.40 | mG/pulse/sec |
| Max. Mechanical Shock (0.1 ms) | 2000 | | | | | | G |

***PERFORMANCE - All Models:*** Unless otherwise specified, $V_{DD}$=5.0VDC, $F_{CLK}$=250kHz, $T_C$=25°C.

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Cross Axis Sensitivity | | 2 | 3 | % |
| Bias Calibration Error [1] | | 1 | 2 | % of $F_{CLK}$ (span) |
| Bias Temperature Shift ($T_C$=-55 to +125°C) [1] | | 100 | 300 | (ppm of $F_{CLK}$)/°C |
| Scale Factor Calibration Error [1, 2] | | 1 | 2 | % |
| Scale Factor Temp. Shift ($T_C$=-55 to +125°C) [1] | | +300 | | ppm/°C |
| Non-Linearity (-90% to +90% of Full Scale) [1, 2] | | 0.5 | 1.0 | % of span |
| Power Supply Rejection Ratio (VDD tied to VR) | 40 | | | dB |
| Operating Voltage | 4.5 | 5.0 | 5.5 | V |
| Operating Current ($I_{DD}$ + $I_{VR}$) [1] | | 2.0 | 3.0 | mA |
| Clock Input Voltage Range (with respect to GND) | -0.5 | | $V_{DD}$+0.5 | V |
| Mass: 'L' package (add 0.06 grams for 'J' package) | | 0.62 | | grams |

Notes: 1. Tighter tolerances available on special order.
2. 100g versions and above are tested from -65 to +65g.



### ABSOLUTE MAXIMUM RATINGS *

Case Operating Temperature . . . . . -55 to +125°C
Storage Temperature . . . . . -55 to +125°C
Acceleration Over-range . . . . . 2000 G for 0.1 ms
Voltage on $V_{DD}$ to GND . . . . . -0.5V to 6.5V
Voltage on Any Pin (except DV) to GND [1] . . . . . -0.5V to $V_{DD}$+0.5V
Voltage on DV to GND . . . . . ±15V
Power Dissipation . . . . . 50 mW

NOTE 1: Voltages on pins other than DV, GND or $V_{DD}$ may exceed 0.5 volt above or below the supply voltages provided the current into or out of the pin is limited to 1 mA.

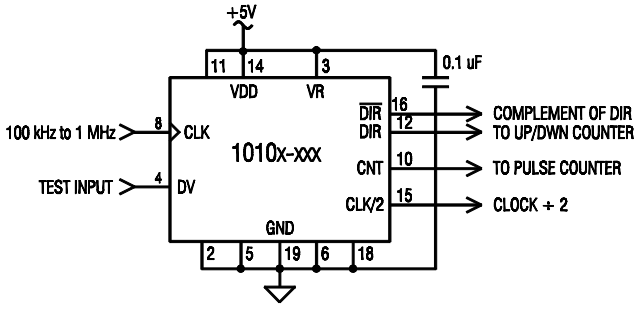
***NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at or above these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### DC CHARACTERISTICS: $V_{DD}$=5V±5%; $T_C$=-55 to +125°C unless otherwise specified.

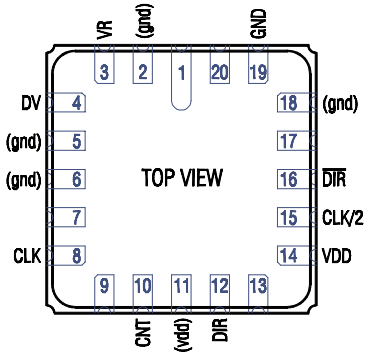
| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{T-}$ | Negative Going Threshold Voltage (CLK) | 0.9 | 1.7 | | V | |
| $V_{T+}$ | Positive Going Threshold Voltage (CLK) | | 3.0 | 3.7 | V | |
| $V_H$ | Hysteresis Voltage (CLK) | 0.5 | 1.3 | | V | |
| $V_{OL}$ | Output Low Voltage (CNT, DIR, CLK/2) | | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ | Output High Voltage (CNT, DIR, CLK/2) | $V_{DD}$-0.4 | | | V | $I_{OH}$ = 2.0 mA |
| $I_I$ | Input Leakage Current (CLK) | | | 10 | µA | $V_I$ = 0 to $V_{DD}$ |
| $C_{IO}$ | Pin Capacitance | | | 10 | pF | 1 MHz, $T_A$ = 25°C |
| $I_{DD}+I_{VR}$ | Operating Current | | 2 | 3 | mA | $F_{CLK}$ = 250kHz |

### A.C. CHARACTERISTICS: $T_C$=-55 to +125°C; $V_{DD}$=5V±5%; Load Capacitance=50pF

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| CLK input frequency | 100 | 250 | 1000 | kHz |
| CLK input rise/fall time | | | 50 | ns |
| CLK duty cycle | 45 | 50 | 55 | % |
| CLK fall to DIR fall | 40 | 85 | 195 | ns |
| CLK fall to DIR rise | 40 | 90 | 205 | ns |
| CLK rise to valid CNT out | 40 | 90 | 230 | ns |
| CLK fall to CNT fall | 40 | 85 | 205 | ns |
| CLK fall to CLK/2 rise/fall | 40 | 90 | 210 | ns |




**RECOMMENDED CONNECTIONS**




**PINOUT (LCC & JLCC PACKAGES)**

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

***USE of the* CNT *output :*** Pulses from the CNT output are meant to be accumulated in a hardware counter. Each pulse accumulation or sample, reflects the average acceleration (change in velocity) over that interval. The sample period or "gate time" over which these pulses are accumulated determines both the bandwidth and quantization of the measurement.

$$\text{Quantization (G's)} = \frac{G_{SPAN} \bullet f_{SR}}{f_{CLK}}$$

$$f_{CNT} = f_{CLK}\left(\frac{1}{2} + \frac{G_{FORCE}}{G_{SPAN}}\right)$$

$$G_{FORCE} = G_{SPAN}\left(\frac{f_{CNT}}{f_{CLK}} - \frac{1}{2}\right)$$

Where:

$G_{SPAN}$ = 2 * (full scale acceleration in G's)

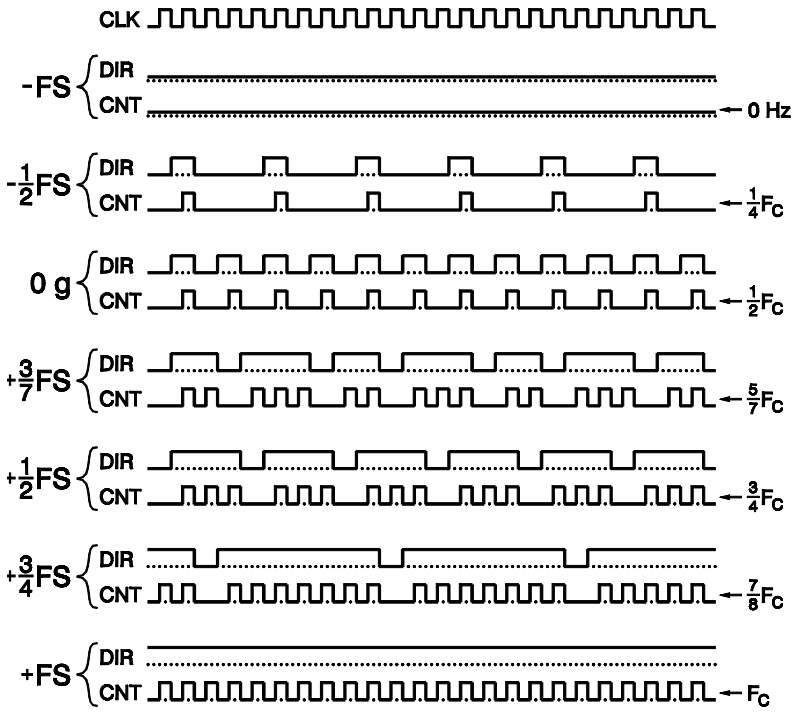
$f_{SR}$ = CNT sample rate in Hertz

$f_{CLK}$ = accelerometer clock rate in Hertz

$f_{CNT}$ = CNT pulse rate in pulses / sec

$G_{FORCE}$ = acceleration in gravity units

1 $G$ = 9.807 m / $s^2$ or 32.175ft / $s^2$



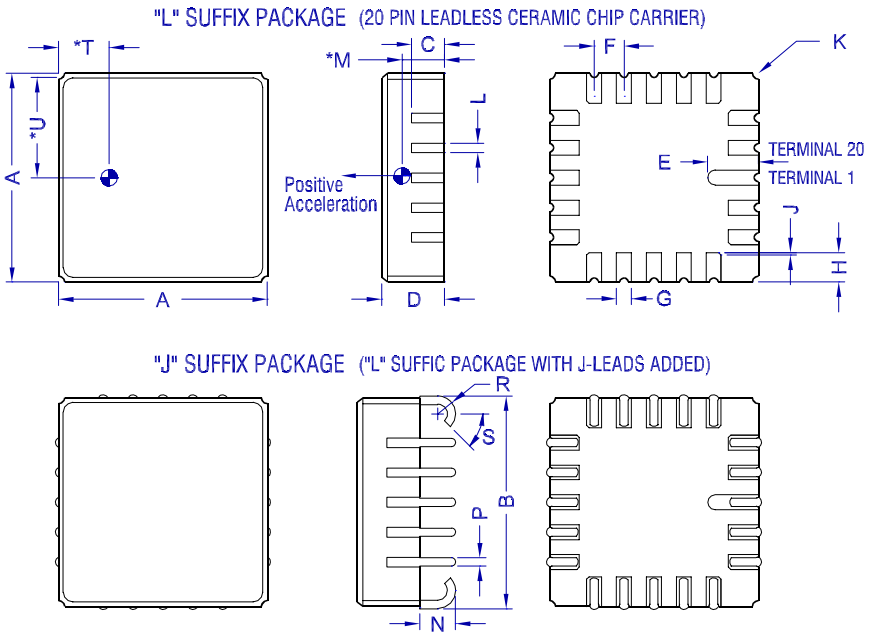

The first equation above shows that as the sample rate is reduced (i.e. a longer sample period), the quantization becomes finer but bandwidth is reduced. Conversely, as the sample rate is increased, quantization becomes coarser but the bandwidth of the measurement is increased. The second and third equations show how the CNT pulse frequency equates to the applied G-force. When using a frequency counter to monitor the CNT output pulse rate, a counter with a DC coupled input must be used. The CNT output is a return-to-zero signal whose duty cycle varies from zero to fifty percent, from minus full scale to positive full scale acceleration. A frequency counter with an AC coupled input will provide an erroneous reading as the duty cycle varies appreciably from fifty percent. The figure to the left illustrates how the CNT and DIR outputs vary as the accelerometer is subjected to accelerations from minus full scale (-FS) to plus full scale (+FS).

***USE of the* (DV) *test input:*** Left unconnected, the DV input has a nominal voltage of 1/3rd $V_{DD}$. For best accuracy during normal operation, this input should be left unconnected or connected to a voltage source equal to 1/3rd of the $V_{DD}$ supply voltage. The change in output pulse rate ($\Delta f$) is proportional to the square of the difference between the voltage applied to the DV input ($V_{DV}$) and 1/3rd $V_{DD}$. Note that only positive shifts in the output pulse rate may be generated by applying voltage to the DV input. The proportionality constant ($k$) varies for each device and is not characterized.

$$\Delta f \approx k\left(V_{DV} - \frac{1}{3}V_{DD}\right)^2$$

***ESD and LATCHUP CONSIDERATIONS:*** The model 1010 accelerometer is a CMOS device subject to damage by large electrostatic charges. Diode protection is provided on the inputs and outputs but care should be exercised during handling to assure that CMOS devices are placed on grounded conductive surfaces only. Individuals and tools should be grounded before coming in contact with CMOS devices. Do not insert or remove CMOS devices in sockets with power applied.

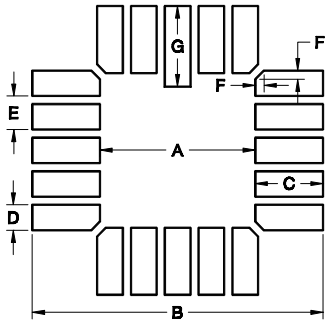
***PACKAGE DIMENSIONS***




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.342 | 0.358 | 8.69 | 9.09 |
| B | 0.354 | 0.370 | 8.99 | 9.40 |
| C | 0.050 | 0.060 | 1.27 | 1.52 |
| D | 0.095 | 0.115 | 2.41 | 2.92 |
| E | 0.075 | 0.095 | 1.91 | 2.41 |
| F | 0.050 BSC | | 1.27 BSC | |
| G | 0.022 | 0.028 | 0.56 | 0.71 |
| H | 0.050 TYP | | 1.27 TYP | |
| J | 0.004 x 45° | | 0.10 x 45° | |
| K | 0.010 R TYP | | 0.25 R TYP | |
| L | 0.016 TYP | | 0.41 TYP | |
| * M | 0.048 TYP | | 1.23 TYP | |
| N | .055 | .065 | 1.40 | 1.65 |
| P | 0.014 TYP | | 0.36 TYP | |
| R | 0.03 R TYP | | 0.76 R TYP | |
| S | 45° MINIMUM | | | |
| * T | 0.085 TYP | | 2.16 TYP | |
| * U | 0.175 TYP | | 4.45 TYP | |

NOTES:
1. * DIM 'M', 'T' & 'U' LOCATE ACCELERATION SENSING ELEMENT'S CENTER OF MASS .
2. LID IS ELECTRICALLY TIED TO TERMINAL 19 (GND).
3. CONTROLLING DIMENSION: INCH.
4. TERMINALS PLATED 60 MICROINCHES MIN GOLD OVER 80 MICROINCHES MIN NICKEL.
5. PACKAGE: 90% MINIMUM ALUMINA (BLACK), LID: SOLDER SEALED KOVAR.

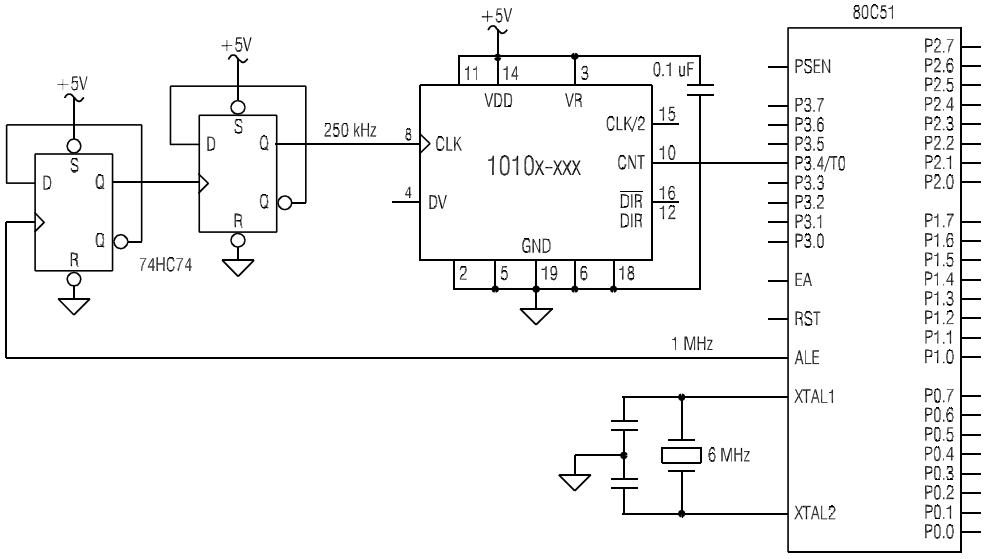
***SOLDERING RECOMMENDATIONS*:** Manual soldering of the 1010 series accelerometers is recommended. Allow a brief cooling period between the soldering of each terminal so that the average case temperature remains at or below 150°C. Maximum allowed case temperature is 175°C for 60 seconds. The recommended solder pad size and shape for both the LCC and J-LCC packages is shown in the diagram and table below. These dimensions are recommendations only and may or may not be optimum for your particular soldering process.




| DIM | inch | mm |
|---|---|---|
| A | .230 | 5.84 |
| B | .430 | 10.92 |
| C | .100 | 2.54 |
| D | .038 | 0.97 |
| E | .050 | 1.27 |
| F | .013 | 0.33 |
| G | .120 | 3.05 |

### *ACCELERATION MEASUREMENT WITH A MICROCONTROLLER:*

The pulse density modulation output (CNT) of the 1010 series accelerometer was designed to drive the type of hardware pulse counter that is sometimes present in microcontrollers. The schematic (below) shows a 1010 series accelerometer driving the 'T0' counter of an Intel 80C51 microcontroller. The accelerometer's clock is provided by the Address Latch Enable (ALE) output of the 80C51 after being divided by a factor of four by the two 74HC74 "D-Type" flip/flops. The divide by 4 flip/flops are needed because the maximum count rate of the 80C51's 'T0' counter is 1/24th of the 8051's clock oscillator frequency ($F_{OSC}$) and the frequency of ALE is 1/6th of $F_{OSC}$. Divisors of greater than four should be used if $F_{OSC}$ is greater than 12 MHz to keep the accelerometer's clock frequency at or below the recommended 1 MHz maximum. Use of ALE for the accelerometer clock is only recommended for applications where no external memory is connected to the 80C51. ALE is missing an output pulse for each MOVX instruction which is used to access external memory. Alternatively, any available clock source asynchronous with the 8051's clock may be used to drive the accelerometer so long as its frequency is between 100 kHz and 1 MHz and is no greater than 1/48th of $F_{OSC}$.




**MODEL 1010 CONNECTION TO A MICROCONTROLLER**

To obtain each interval's average acceleration, the software needs to poll the counter's value at fixed intervals then subtract each new counter value from its previous value to obtain a delta (difference) count for each interval. Of course the software must also account for wraparound of the counter which requires that the counter contain enough bits to prevent more than one counter overflow during each sample period. The delta count relates to the average applied acceleration according to the following equation.

$$\Delta C = \frac{f_{CLK}\left(\frac{1}{2} + \frac{A_G}{G_{SPAN}}\right)}{f_{SR}}$$

Where:

$\Delta C$ = the change in the counter's value over each sample interval
$f_{CLK}$ = the accelerometer's input clock frequency
$A_G$ = the average acceleration force in g's during the sample interval
$G_{SPAN}$ = 2 * (full scale acceleration rating of accelerometer)
$f_{SR}$ = the software sample rate of the counter in samples/sec

At minus full-scale acceleration, the difference count ($\Delta C$) is zero. Zero acceleration results in a difference count of ½ of the maximum difference count value and plus full scale acceleration results in the maximum value where the maximum difference count value possible is ($f_{CLK}/f_{SR}$). The actual difference value achieved at zero acceleration [which will be near ½($f_{CLK}/f_{SR}$)], may be subtracted from each interval's difference count to obtain the acceleration count in sign-magnitude format.



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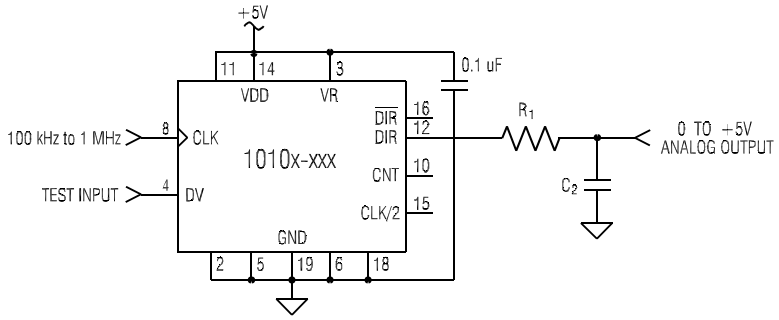
### *CONVERSION TO AN ANALOG VOLTAGE:*

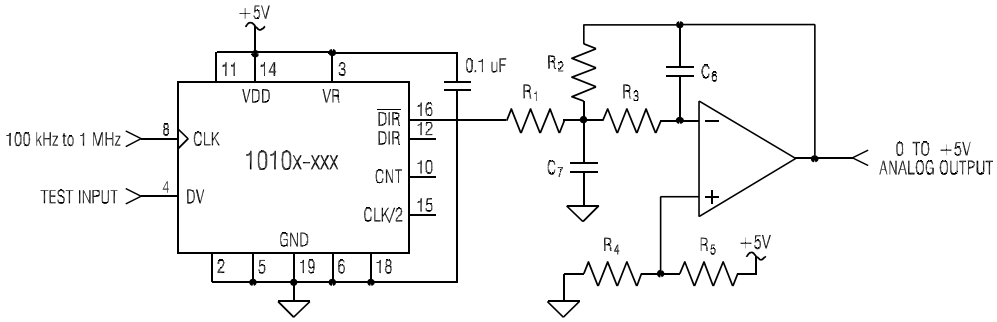
It is best to use a model 1210 for analog applications but if a proportional analog voltage is desired from a model 1010, one can be easily generated by the connection of a low-pass filter to the DIR output as shown in the schematic (below). The table (at right) lists values for $R_1$ and $C_2$ for various cutoff frequencies (-3 dB frequency). $R_1$ is chosen to be at least 100 times the maximum output impedance of DIR which is 200Ω. The circuit or instrument that the 0 to +5V analog output is connected to, must have an input impedance at least 100 times the value of $R_1$. This simple passive RC filter can be used as long as it provides sufficient rejection of the switching noise present on the DIR output for the specific application.

| Cutoff Frequency (Hz) | $R_1$ (kΩ) | $C_2$ (µF) |
|---|---|---|
| 200 | 36.0 | .022 |
| 800 | 35.7 | .0056 |
| 1000 | 34.0 | .0047 |
| 1600 | 30.1 | .0033 |
| 2000 | 36.0 | .0022 |




**SINGLE POLE RC FILTER**

If greater rejection of switching noise is needed, a two pole active filter can be used as shown in the schematic (below). This circuit has the added advantage of providing a very low output impedance compared with the single pole circuit. Its disadvantages include greater complexity and the need for 1 or 2 additional supply voltages for the op-amp. For both filter types, tight tolerance, temperature stable resistors and capacitors should be used. To reject common mode noise over long signal transmission line lengths, DIR and its complement can be used to drive a pair of wires with a differential filter placed at the far end of the wires.




**TWO POLE ACTIVE FILTER**

| Cutoff Frequency (Hz) | $R_1$ & $R_2$ (kΩ) | $R_3$ (kΩ) | $R_4$ & $R_5$ (kΩ) | $C_6$ (µF) | $C_7$ (µF) |
|---|---|---|---|---|---|
| 200 | 21.5 | 36.0 | 93.1 | .012 | .068 |
| 800 | 19.1 | 43.0 | 105 | .0027 | .018 |
| 1000 | 18.2 | 42.2 | 102 | .0022 | .015 |
| 1600 | 17.4 | 38.3 | 93.1 | .0015 | .010 |
| 2000 | 21.5 | 36.0 | 93.1 | .0012 | .0068 |



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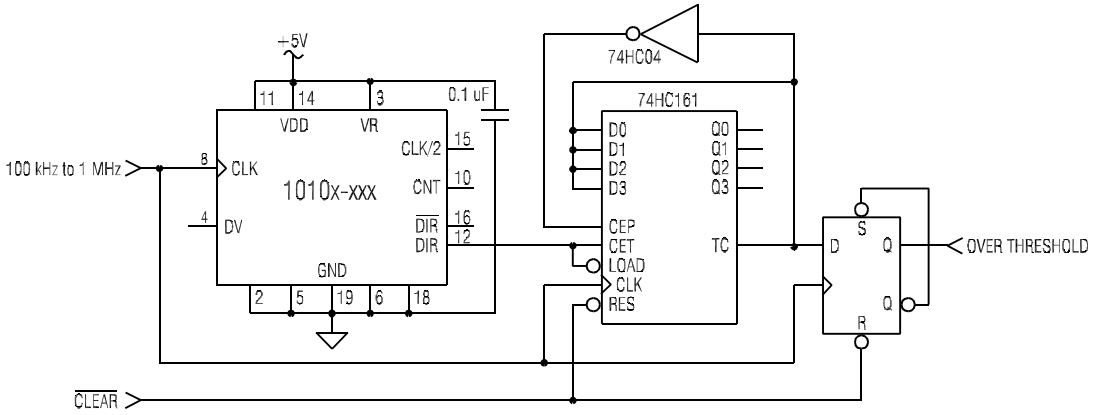
### *ACCELERATION THRESHOLD DETECTION:*

For applications where it is desired to know when acceleration has exceeded a threshold value, the simple circuit shown in the schematic (below) can be used. This circuit uses a 74HC161 synchronous binary counter to detect when the DIR logic output goes high for a minimum of 16 clock cycles in a row. The 74HC74 D-type flip/flop is connected in a "ones-catch" configuration so that once the threshold is exceeded, the flip/flop stores the event. The clear input sets the counter value to zero and clears the flip/flop, making the circuit ready to detect the next 16 ones in a row sequence. When driven by the positive acceleration pulses form the model 1010 accelerometer, this circuit provides a threshold of approximately 7/8ths of full scale (+43.75g for a ±50g device). Negative acceleration pulses can be detected by connecting the counter to $\overline{\text{DIR}}$ instead of DIR.




**THRESHOLD DETECTION CIRCUIT**



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