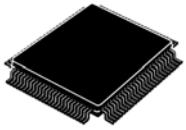
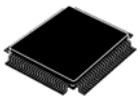
SPC56EL70L3, SPC56EL70L5, SPC564L70L3, SPC564L70L5

32-bit Power Architecture®microcontroller for automotive SIL3/ASILD chassis and safety applications

Datasheet - production data



LQFP144 (20 x 20 x 1.4 mm)



LQFP100 (14 x 14x 1.4 mm)

Features

- High-performance e200z4d dual core
  - 32-bit Power Architecture® technology CPU
  - Core frequency as high as 120 MHz
  - Dual issue five-stage pipeline core
  - Variable Length Encoding (VLE)
  - Memory Management Unit (MMU)
  - 4 KB instruction cache with error detection code
  - Signal Processing Engine (SPE)
- Memory available
  - 2 MB flash memory with ECC
  - 192 KB on-chip SRAM with ECC
  - Built-in RWW capabilities for EEPROM emulation
- SIL3/ASILD innovative safety concept: Lock step mode and Fail-safe protection
  - Sphere of Replication (SoR) for key components (such as CPU core, eDMA, crossbar switch)
  - Fault Collection and Control Unit (FCCU)
  - Redundancy Control and Checker Unit (RCCU) on outputs of the SoR connected to FCCU
  - Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
  - Boot-time Built-In Self-Test for ADC and flash memory triggered by software
  - Replicated safety enhanced watchdog
  - Replicated junction temperature sensor
  - Non Maskable Interrupt (NMI)
  - 16-region Memory Protection Unit (MPU)
  - Clock Monitoring Units (CMU)
  - Power Management Unit (PMU)
  - Cyclic Redundancy Check (CRC) unit
- Decoupled Parallel mode for high performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority controller
  - Replicated 16-channel eDMA controller
- GPIOs individually programmable as input, output or special function
- Three 6-channel general-purpose eTimer units
- 2 FlexPWM units: Four 16-bit channels per module
- Communications interfaces
  - 2 LINFlexD channels
  - 3 DSPI channels with automatic chip select generation
  - 3 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1 Rev. A) with 2 channels, 64 message buffers and data rates up to 10 Mbit/s
- Two 12-bit Analog-to-digital Converters (ADC)
  - 16 input channels
  - Programmable Cross Triggering Unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART/FlexRay Bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56EL70x/SPC564L70x series of microcontroller units (MCUs). For functional characteristics, see the SPC56XL70 Microcontroller Reference Manual. For use of the SPC56XL70 in a fail-safe system according to safety standard ISO26262, see the Safety Application Guide for SPCEL70.

1.2 Description

The SPC56EL70x/SPC564L70x series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The SPC56EL70x/SPC564L70x family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the SPC56XL70 automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.3 Device comparison

Table 1. SPC56XL70/SPC56X64 device summary

Feature		SPC56EL64	SPC56EL70	SPC564L64	SPC564L70
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)	2 × e200z4 (in lock-step or decoupled operation)	1 × e200z4	1 × e200z4
	Architecture	Harvard			
	Execution speed	0–120 MHz (+2% FM)			
	DMIPS intrinsic performance	>240 MIPS			
	SIMD (DSP + FPU)	Yes			
	MMU	16 entry			
	Instruction set PPC	Yes			
	Instruction set VLE	Yes			
	Instruction cache	4 KB, EDC			
	MPU-16 regions	Yes, replicated module			
	Semaphore unit (SEMA4)	Yes			
Buses	Core bus	AHB, 32-bit address, 64-bit data			
	Internal periphery bus	32-bit address, 32-bit data			
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3		4 x 3	
Memory	Code/data flash	1.5 MB, ECC, RWW	2 MB, ECC, RWW	1.5 MB, ECC, RWW	2 MB, ECC, RWW
	Static RAM (SRAM)	160 KB, ECC	192 KB, ECC	160 KB, ECC	192 KB, ECC

Table 1. SPC56XL70/SPC56X64 device summary (continued)

Feature		SPC56EL64	SPC56EL70	SPC564L64	SPC564L70
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module			
	Periodic Interrupt Timer (PIT)	1 × 4 channels			
	System Timer Module (STM)	1 × 4 channels, replicated module			
	Software Watchdog Timer (SWT)	Yes, replicated module			
	eDMA	16 channels, replicated module			
	FlexRay	1 × 64 message buffers, dual channel			
	FlexCAN	3 × 32 message buffers			
	LINFlexD (UART and LIN with DMA support)	2			
	Clock out	Yes			
	Fault Collection and Control Unit (FCCU)	Yes			
	Cross Triggering Unit (CTU)	Yes			
	eTimer	3 × 6 channels(1)			
	FlexPWM	2 Module 4 × (2 + 1) channels(2)			
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)			
	Sine Wave Generator (SWG)	32 point			

Table 1. SPC56XL70/SPC56X64 device summary (continued)

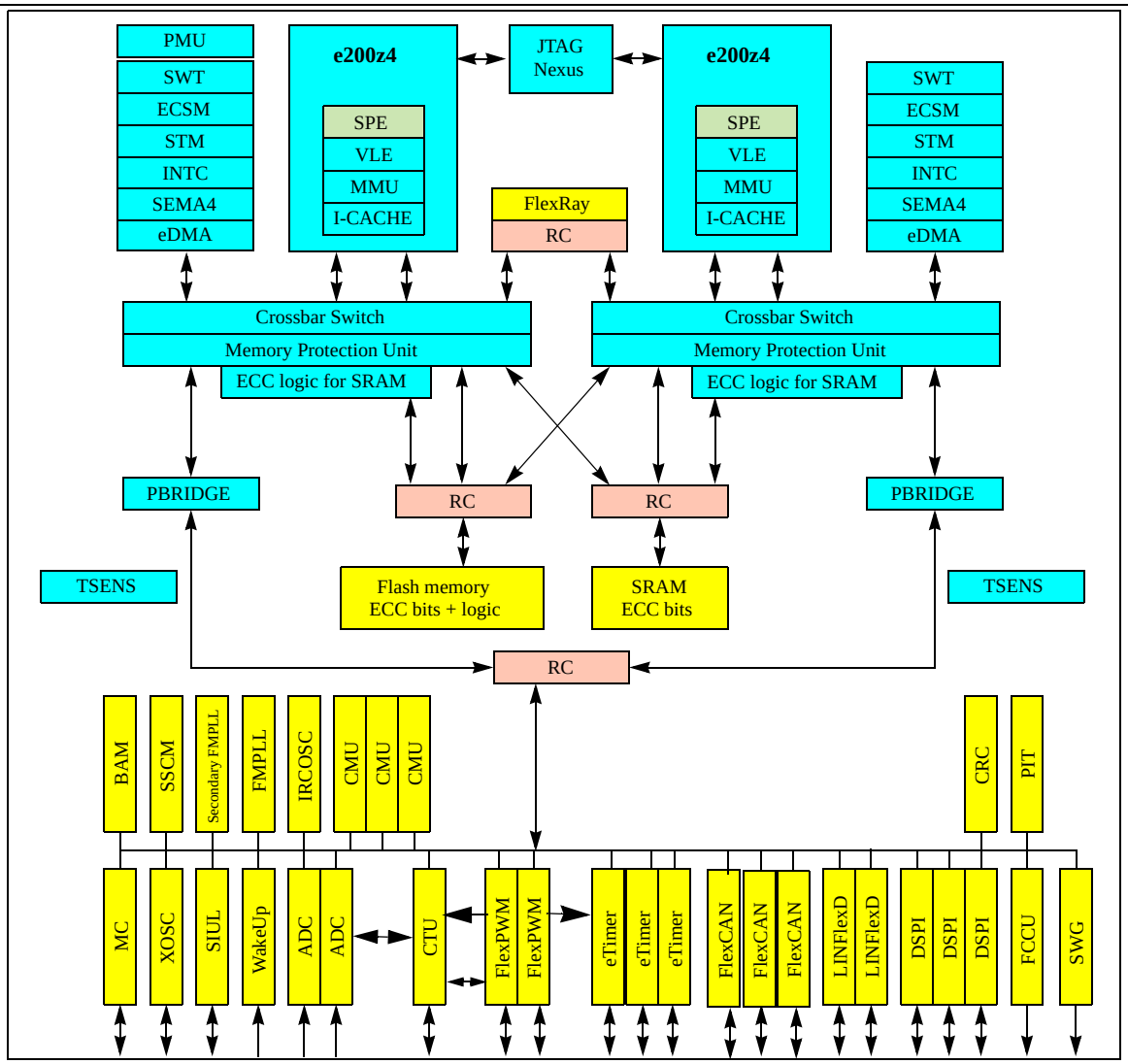
Feature		SPC56EL64	SPC56EL70	SPC564L64	SPC564L70
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects			
	Cyclic Redundancy Checker (CRC) unit	Yes			
	Junction temperature sensor (TSENS)	Yes, replicated module			
	Digital I/Os	≥ 16			
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die			
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V			
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4 – 40 MHz			
Debug	Nexus	Level 3+			
Packages	LQFP	100 pins 144 pins			
Temperature	Temperature range (junction)	–40 to 150 °C			
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C			

1. The third eTimer is not connected to any pins on the package. Its usage is confined internally to the device.
2. The second FlexPWM is not connected to any pins on the package. Its usage is confined internally to the device.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56EL70x/SPC564L70x device.

Figure 1. SPC56EL70 block diagram



ADC – Analog-to-Digital Converter
BAM – Boot Assist Module
CMU – Clock Monitoring Unit
CRC – Cyclic Redundancy Check unit
CTU – Cross Triggering Unit
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access controller
FCCU – Fault Collection and Control Unit
FlexCAN – Controller Area Network controller
FMPLL – Frequency Modulated Phase Locked Loop
INTC – Interrupt Controller
IRCOSC – Internal RC Oscillator
JTAG – Joint Test Action Group interface
LINFlexD – LIN controller with DMA support
MC – Mode Entry, Clock, Reset, & Power
PBRIDGE – Peripheral bridge
PIT – Periodic Interrupt Timer
PMU – Power Management Unit
RC – Redundancy Checker
RTC – Real Time Clock
SEMA4 – Semaphore Unit
SIUL – System Integration Unit Lite
SSCM – System Status and Configuration Module
STM – System Timer Module
SWG – Sine Wave Generator
SWT – Software Watchdog Timer
TSENS – Temperature Sensor
XOSC – Crystal Oscillator

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

- Extensive system development and tracing support via Nexus debug port

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory protection unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features:

- 2 MB of flash memory in unique multi-partitioned hard macro
- Sectorization:
  - Partition 1 (low address): 16 KB + 16 KB + 16 KB + 16 KB
  - Partition 2 (low address): 16 KB + 16 KB + 16 KB + 16 KB
  - Partition 3 (low address): 64 KB + 64 KB
  - Partition 4 (mid address): 128 KB + 128 KB
  - Partition 5 (high address): 256 KB + 256 KB
  - Partition 6 (high address): 256 KB + 256 KB
  - Partition 7 (high address): 256 KB + 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow sector for test, censorship device and user option bits
- Wait states:
  - Access time less or equal to 3 WS at 120 MHz + 4% FM (4-1-2-1 access)
  - Access time less or equal to 2 WS at 80 MHz + 4% FM
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56XL70 SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 192 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state at 120 MHz
  - 0 wait states at 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Data flash (bank1) interface includes a 128-bit register to temporarily hold a single flash page. This logic supports single-cycle read responses (0 AHB data-phase wait states) for accesses that hit in the holding register.
  - No prefetch support is provided for this bank.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.5.8 Platform static RAM controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

1.5.9 Memory subsystem access time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform memory access time summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error correction status module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access right per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

1.5.13 System clocks and clock generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (FlexPWM, eTimer, CTU, ADC, and SWG)

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 KHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control

  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal reference clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

1.5.17 Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - HALT and STOP mode as reduced activity low power mode
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.5.18 Periodic interrupt timer module (PIT)

The PIT module implements the following features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

1.5.19 System timer module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[(a)] requirement

The STM is replicated for each processor.

1.5.20 Software watchdog timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

The SWT module is replicated for each processor.

1.5.21 Fault collection and control unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

a. Automotive Open System Architecture

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-maskable interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot assist module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System status and configuration module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (Parity, Noise and Framing errors)
  - Interrupt driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- Support for DMA enabled transfers

1.5.29 Deserial serial peripheral interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the SPC56XL70 and external devices.

A DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.30 FlexPWM

The pulse width modulator module (FlexPWM) contains four PWM channels, each of which is configured to control a single half-bridge power stage. One module is present in LQFP144 package. Additionally, four fault input channels are provided per FlexPWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.31 eTimer module

The SPC56XL70 provides two eTimer modules on the LQFP144 package. Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

1.5.32 Sine wave generator (SWG)

A digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

- Frequency range from 1 KHz to 50 KHz
- Sine wave amplitude from 0.47 V to 2.26 V

1.5.33 Analog-to-Digital converter module (ADC)

The ADC module features include:

Analog part:

- 2 on-chip ADCs
  - 12-bit resolution SAR architecture
  - Same digital interface as in the SPC560P family
  - A/D Channels: 9 external, 3 internal and 4 shared with other A/D (total 16 channels)
  - One channel dedicated to each T-sensor to enable temperature reading during application
  - Separated reference for each ADC
  - Shared analog supply voltage for both ADCs
  - One sample and hold unit per ADC
  - Adjustable sampling and conversion time

Digital part:

- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: CPU Mode or CTU Mode
- CPU mode features
  - Register based interface with the CPU: one result register per channel
  - ADC state machine managing three request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- CTU mode features
  - Triggered mode only
  - 4 independent result queues (1×16 entries, 2×8 entries, 1×4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit parts
  - DMA compatible interfaces
- Built-in self-test features triggered by software

1.5.34 Cross triggering unit (CTU)

The ADC cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.5.35 Cyclic redundancy checker (CRC) unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to its input register.

The CRC unit has the following features:

- 3 sets of registers to allow 3 concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register.
  The following standard CRC polynomials are implemented:
  - $x^8 + x^4 + x^3 + x^2 + 1$ [8-bit CRC]
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

1.5.36 Redundancy control and checker unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

1.5.37 Junction temperature sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.5.38 Nexus port controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2008 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2008 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[b]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint messaging (WPM) via the auxiliary port

b. 4 MDO pins on LQFP144 package

  - Watchpoint trigger enable of program and/or data trace messaging
  - Data tracing of instruction fetches via private opcodes

1.5.39 IEEE 1149.1 JTAG controller (JTAGC)

The JTAGC block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 5 pins:
  - TDI
  - TMS
  - TCK
  - TDO
  - JCOMP
- Selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.40 Voltage regulator / power management unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V both for packaged and Known Good Die option
  - Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
  - Known Good Die option uses embedded ballast transistor as dissipation capacity is increased to reduce system cost
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

1.5.41 Built-In self-test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the SPC56XL70 in the LQFP100 package.

Figure 2. SPC56XL70 LQFP100 package

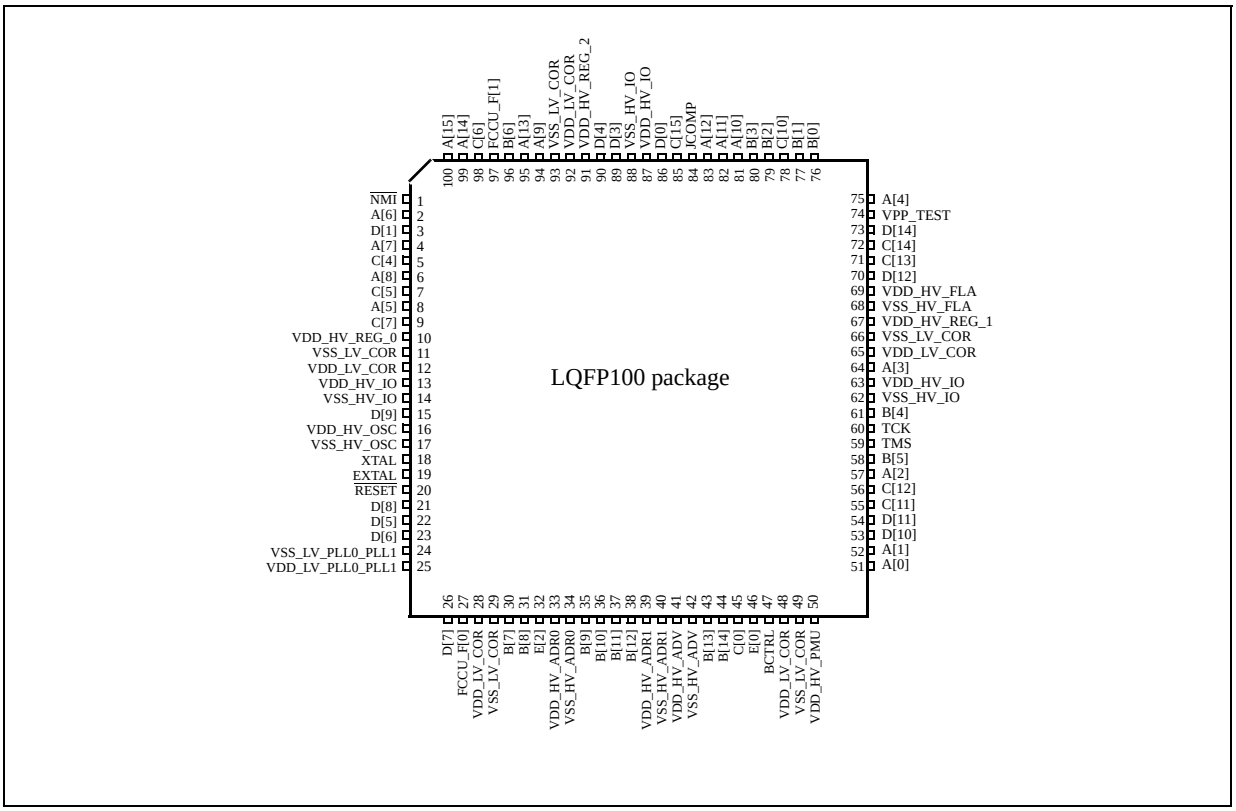


Figure 3 shows the SPC56XL70 in the LQFP144 package.

Figure 3. SPC56XL70 LQFP144 pinout (top view)

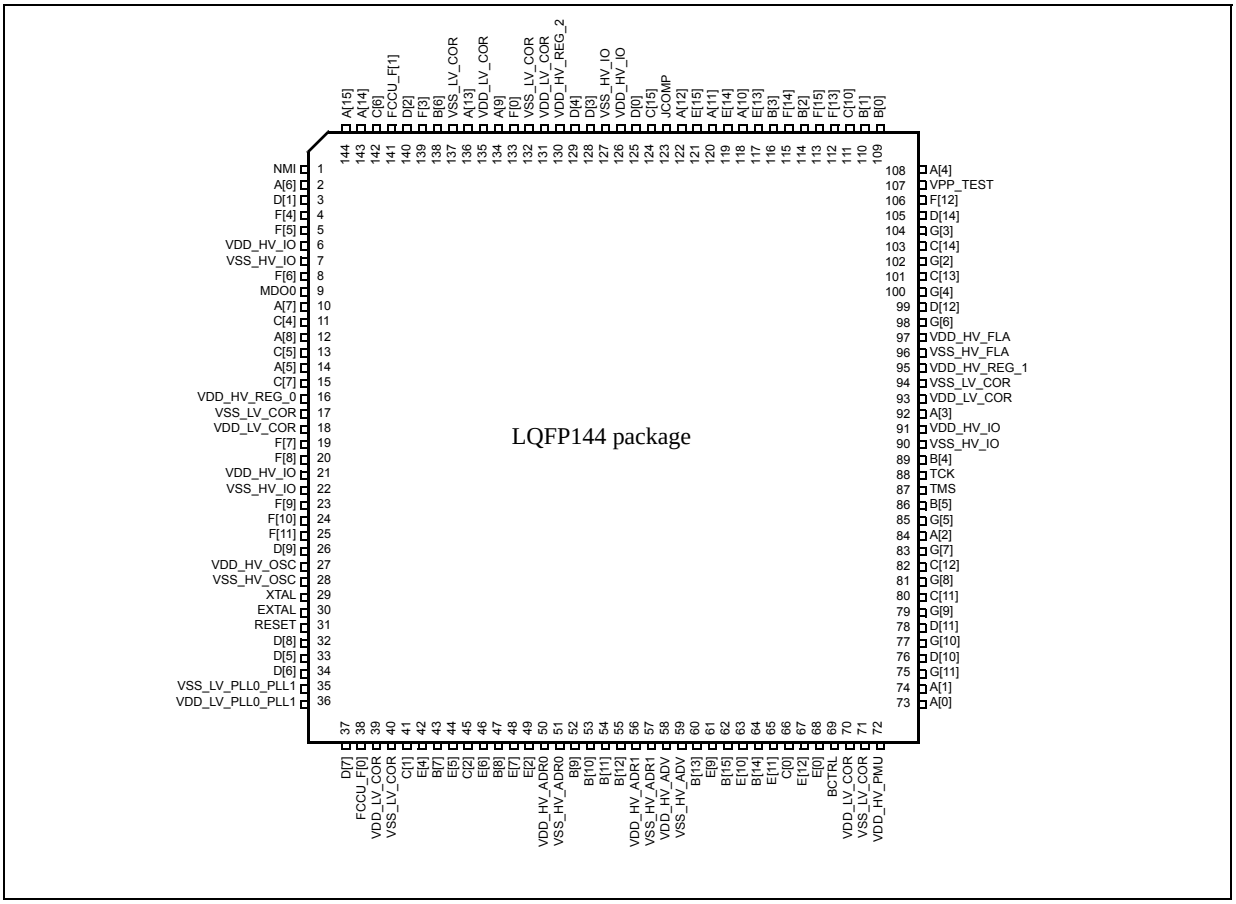


Table 3 and *Table 4* provides the pin function summaries for the 100-pin and 144-pin packages respectively, listing all the signals multiplexed to each pin

Table 3. LQFP100 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
1	NMI	—		
2	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
4	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
		FlexCan_2	—	RXD
5	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
6	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
		FlexCan_2	TXD	—
7	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
8	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
9	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
10	$V_{DD_HV_REG_0}$	—		
11	$V_{SS_LV_COR}$	—		
12	$V_{DD_LV_COR}$	—		
13	$V_{DD_HV_IO}$	—		
14	$V_{SS_HV_IO}$	—		
15	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
16	$V_{DD_HV_OSC}$	—		
17	$V_{SS_HV_OSC}$	—		
18	XTALIN	—		
19	XTALOUT	—		
20	RESET	—		
21	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
22	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
23	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
24	$V_{SS_LV_PLL0_PLL1}$	—		
25	$V_{DD_LV_PLL0_PLL1}$	—		
26	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	Analog output	—
27	FCCU_F[0]	FCCU	F[0]	F[0]
28	$V_{DD_LV_COR}$	—		
29	$V_{SS_LV_COR}$	—		
30	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
31	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
32	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
33	$V_{DD_HV_ADR0}$	—		

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
34	$V_{SS_HV_ADR0}$	—		
35	B[9]	SIUL	—	GPIO[25]
		ADC_0	—	AN[11]
		ADC_1		
36	B[10]	SIUL	—	GPIO[26]
		ADC_0	—	AN[12]
		ADC_1		
37	B[11]	SIUL	—	GPIO[27]
		ADC_0	—	AN[13]
		ADC_1		
38	B[12]	SIUL	—	GPIO[28]
		ADC_0	—	AN[14]
		ADC_1		
39	$V_{DD_HV_ADR1}$	—		
40	$V_{SS_HV_ADR1}$	—		
41	$V_{DD_HV_ADV}$	—		
42	$V_{SS_HV_ADV}$	—		
43	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
44	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
45	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
46	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
47	BCTRL	—		
48	$V_{DD_LV_COR}$	—		
49	$V_{SS_LV_COR}$	—		
50	$V_{DD_HV_PMU}$	—		

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
51	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
52	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
53	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
54	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
55	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
56	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
57	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
58	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
59	TMS	—		
60	TCK	—		
61	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
62	$V_{SS_HV_IO}$	—		
63	$V_{DD_HV_IO}$	—		

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
65	$V_{DD_LV_COR}$	—		
66	$V_{SS_LV_COR}$	—		
67	$V_{DD_HV_REG_1}$	—		
68	$V_{SS_HV_FLA}$	—		
69	$V_{DD_HV_FLA}$	—		
70	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
71	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
72	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
73	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
74	V_{PP_TEST}(1)	—		
75	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
76	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
77	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
78	C[10]	SIUL	GPIO[42]	GPIO[42]
		DSPI_2	CS2	—
		FlexPWM_0	A[3]	A[3]
		FlexPWM_0	—	FAULT[1]
79	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	DEBUG[2]
		SIUL	—	EIRQ[17]
80	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	DEBUG[3]
		LINFlexD_0	—	RXD
81	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
82	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD_HV_IO}$	—		
88	$V_{SS_HV_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD_HV_REG_2}$	—		
92	$V_{DD_LV_COR}$	—		
93	$V_{SS_LV_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
95	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
96	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
97	FCCU_F[1]	FCCU	F[1]	F[1]
98	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
99	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
100	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. LQFP144 pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
1	NMI	—		
2	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
4	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
5	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
6	$V_{DD_HV_IO}$	—		
7	$V_{SS_HV_IO}$	—		
8	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
9	MDO0	—		
10	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
		FlexCAN_2	—	RXD
11	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
12	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
		FlexCAN_2	TXD	—
13	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD_HV_REG_0}$	—		
17	$V_{SS_LV_COR}$	—		
18	$V_{DD_LV_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	MSEO[1]	—
21	$V_{DD_HV_IO}$	—		
22	$V_{SS_HV_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	MSEO[0]	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	EVTI	—
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD_HV_OSC}$	—		
28	$V_{SS_HV_OSC}$	—		
29	XTALIN	—		
30	XTALOUT	—		
31	RESET	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS_LV_PLL0_PLL1}$	—		
36	$V_{DD_LV_PLL0_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD_LV_COR}$	—		
40	$V_{SS_LV_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
47	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
48	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
49	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
50	$V_{DD_HV_ADR0}$	—		
51	$V_{SS_HV_ADR0}$	—		
52	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
53	B[10]	SIUL	—	GPIO[26]
		ADC_0 ADC_1	—	AN[12]
54	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
55	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
56	$V_{DD_HV_ADR1}$	—		
57	$V_{SS_HV_ADR1}$	—		
58	$V_{DD_HV_ADV}$	—		
59	$V_{SS_HV_ADV}$	—		
60	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
61	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
62	B[15]	SIUL	—	GPIO[31]
		SIUL	—	EIRQ[20]
		ADC_1	—	AN[2]
63	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD_LV_COR}$	—		
71	$V_{SS_LV_COR}$	—		
72	$V_{DD_HV_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
78	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
79	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
80	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
81	G[8]	SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
		DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]
82	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
83	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
84	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
85	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
86	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
87	TMS	—		
88	TCK	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS_HV_IO}$	—		
91	$V_{DD_HV_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD_LV_COR}$	—		
94	$V_{SS_LV_COR}$	—		
95	$V_{DD_HV_REG_1}$	—		
96	$V_{SS_HV_FLA}$	—		
97	$V_{DD_HV_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
104	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
105	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
106	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
107	V_{PP_TEST}(1)	—		
108	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
109	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
110	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
111	C[10]	SIUL	GPIO[42]	GPIO[42]
		DSPI_2	CS2	—
		FlexPWM_0	A[3]	A[3]
		FlexPWM_0	—	FAULT[1]
112	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
113	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
		FlexCAN_2	TXD	—
114	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]
115	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
		FlexCAN_2	—	RXD
116	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
117	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
118	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
119	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
120	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
121	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
122	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
123	JCOMP	—	—	JCOMP
124	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD_HV_IO}$	—		
127	$V_{SS_HV_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD_HV_REG_2}$	—		
131	$V_{DD_LV_COR}$	—		
132	$V_{SS_LV_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD_LV_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS_LV_COR}$	—		
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1. V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

2.2 Supply pins

Table 5. Supply pins

Supply		Pin #	
Symbol	Description	100 Pkg	144 Pkg
VREG control and power supply pins			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
$V_{DD_LV_COR}$	Core logic supply	48	70
$V_{SS_LV_COR}$	Core regulator ground	49	71
$V_{DD_HV_PMU}$	Voltage regulator supply	50	72
ADC_0/ADC_1 reference voltage and ADC supply			
$V_{DD_HV_ADR0}$	ADC_0 high reference voltage	33	50
$V_{SS_HV_ADR0}$	ADC_0 low reference voltage	34	51
$V_{DD_HV_ADR1}$	ADC_1 high reference voltage	39	56
$V_{SS_HV_ADR1}$	ADC_1 low reference voltage	40	57
$V_{DD_HV_ADV}$	ADC voltage supply for ADC_0 and ADC_1	41	58
$V_{SS_HV_ADV}$	ADC ground for ADC_0 and ADC_1	42	59
Power supply pins (3.3 V)			
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage	—	6
$V_{SS_HV_IO}$	3.3 V Input/Output ground	—	7
$V_{DD_HV_REG_0}$	VDD_HV_REG_0	10	16
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage	13	21
$V_{SS_HV_IO}$	3.3 V Input/Output ground	14	22
$V_{DD_HV_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS_HV_OSC}$	Crystal oscillator amplifier ground	17	28
$V_{SS_HV_IO}$	3.3 V Input/Output ground	62	90
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage	63	91

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
$V_{DD_HV_REG_1}$	VDD_HV_REG_1	67	95
$V_{SS_HV_FLA}$	VSS_HV_FLA	68	96
$V_{DD_HV_FLA}$	VDD_HV_FLA	69	97
$V_{DD_HV_IO}$	VDD_HV_IO	87	126
$V_{SS_HV_IO}$	VSS_HV_IO	88	127
$V_{DD_HV_REG_2}$	VDD_HV_REG_2	91	130
Power supply pins (1.2 V)			
$V_{SS_LV_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	11	17
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	12	18
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD_LV_PLL}$.	24	35
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS_LV_PLL}$.	25	36
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	28	39
$V_{SS_LV_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	29	40
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS_LV_REGCOR}$.	—	70
$V_{SS_LV_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD_LV_REGCOR}$.	—	71
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	65	93
$V_{SS_LV_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	66	94
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	92	131

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	93	132
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	—	135
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	—	137

2.3 System pins

Table 6. System pins

Symbol	Description	Direction	Pin #	
			100 pkg	**144 pkg**
Dedicated pins				
MDO0(1)	Nexus Message Data Output — line	Output only	—	9
NMI(2)	Non Maskable Interrupt	Input only	1	1
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29
EXTAL(3)	Oscillator amplifier output	Input/Output(4)	19	30
TMS(2)	JTAG state machine control	Input only	59	87
TCK(2)	JTAG clock	Input only	60	88
JCOMP(5)	JTAG compliance select	Input only	84	123
Reset pin				
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31
Test pin				
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107

1. This pad is configured for Fast (F) pad speed.
2. This pad contains a weak pull-up.
3. EXTAL is an "Output" in "crystal" mode, and is an "Input" in "ext clock" mode.
4. In XOSC Bypass Mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock can be applied at EXTAL as an input. In XOSC Normal Mode, EXTAL is an output
5. This pad contains a weak pull-down.

6. RESET output shall be considered valid only after the 3.3V supply reaches its stable value.

None of system pins (except RESET) provides an open drain output.

2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each entry of *Table 7* shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

Note: Pins labeled "NC" are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled "Reserved" are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 7. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port A											
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	Pull down	M	S	51	73
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0					
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0					
		SIUL	—	—	EIRQ[0]	—					
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	Pull down	M	S	52	74
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0					
		DSPI_2	SOUT	ALT2	—	—					
		SIUL	—	—	EIRQ[1]	—					
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0					
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0					
		MC_RGM	—	—	ABS[0]	—					
		SIUL	—	—	EIRQ[2]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S	64	92
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0					
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0					
		MC_RGM	—	—	ABS[2]	—					
		SIUL	—	—	EIRQ[3]	—					
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S	75	108
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0					
		DSPI_2	CS1	ALT2	—	—					
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0					
		MC_RGM	—	—	FAB	—					
		SIUL	—	—	EIRQ[4]	—					
A[5]	PCR[5]	SIUL	GPIO[5]	ALT0	GPIO[5]	—	Pull down	M	S	8	14
		DSPI_1	CS0	ALT1	CS0	—					
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=0					
		DSPI_0	CS7	ALT3	—	—					
		SIUL	—	—	EIRQ[5]	—					
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	Pull down	M	S	2	2
		DSPI_1	SCK	ALT1	SCK	—					
		SIUL	—	—	EIRQ[6]	—					
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	Pull down	M	S	4	10
		DSPI_1	SOUT	ALT1	—	—					
		SIUL	—	—	EIRQ[7]	—					
		FlexCAN_2	RXD	ALT2	—	—					
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	Pull down	M	S	6	12
		DSPI_1	—	—	SIN	—					
		SIUL	—	—	EIRQ[8]	—					
		FlexCAN_2	TXD	ALT2	—	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	Pull down	M	S	94	134
		DSPI_2	CS1	ALT1	—	—					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0					
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	Pull down	M	S	81	118
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1					
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0					
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0					
		SIUL	—	—	EIRQ[9]	—					
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	Pull down	M	S	82	120
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1					
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0					
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0					
		SIUL	—	—	EIRQ[10]	—					
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	Pull down	M	S	83	122
		DSPI_2	SOUT	ALT1	—	—					
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1					
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0					
		SIUL	—	—	EIRQ[11]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	Pull down	M	S	95	136
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1					
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1					
		SIUL	—	—	EIRQ[12]	—					
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	Pull down	M	S	99	143
		FlexCAN_1	TXD	ALT1	—	—					
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0					
		SIUL	—	—	EIRQ[13]	—					
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	Pull down	M	S	100	144
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1					
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0					
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0					
		SIUL	—	—	EIRQ[14]	—					
Port B											
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	Pull down	M	S	76	109
		FlexCAN_0	TXD	ALT1	—	—					
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0					
		SSCM	DEBUG[0]	ALT3	—	—					
		SIUL	—	—	EIRQ[15]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
B[1]	PCR[17]	SIUL	GPIO[17]	ALT0	GPIO[17]	—	Pull down	M	S	77	110
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=0					
		SSCM	DEBUG[1]	ALT3	—	—					
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=1					
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=1					
		SIUL	—	—	EIRQ[16]	—					
B[2]	PCR[18]	SIUL	GPIO[18]	ALT0	GPIO[18]	—	Pull down	M	S	79	114
		LINFlex_0	TXD	ALT1	—	—					
		SSCM	DEBUG[2]	ALT3	—	—					
		SIUL	—	—	EIRQ[17]	—					
B[3]	PCR[19]	SIUL	GPIO[19]	ALT0	GPIO[19]	—	Pull down	M	S	80	116
		SSCM	DEBUG[3]	ALT3	—	—					
		LINFlex_0	—	—	RXD	PSMI[31]; PADSEL=0					
B[4](2)	PCR[20]	SIUL	GPIO[20]	ALT0	GPIO[20]	—	Pull down	F	S	61	89
		JTAGC	TDO	ALT1	—	—					
B[5]	PCR[21]	SIUL	GPIO[21]	ALT0	GPIO[21]	—	Pull up	M	S	58	86
		JTAGC	—	—	TDI	—					
B[6]	PCR[22]	SIUL	GPIO[22]	ALT0	GPIO[22]	—	Pull down	F	S	96	138
		MC_CGM	clk_out	ALT1	—	—					
		DSPI_2	CS2	ALT2	—	—					
		SIUL	—		EIRQ[18]	—					
B[7]	PCR[23]	SIUL	—	ALT0	GPI[23]	—	—	—	—	30	43
		LINFlex_0	—	—	RXD	PSMI[31]; PADSEL=1					
		ADC_0	—	—	AN[0](3)	—					
B[8]	PCR[24]	SIUL	—	ALT0	GPI[24]	—	—	—	—	31	47
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=2					
		ADC_0	—	—	AN[1](3)	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—	35	52
		ADC_0 ADC_1	—	—	AN[11](3)	—					
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—	36	53
		ADC_0 ADC_1	—	—	AN[12](3)	—					
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—	37	54
		ADC_0 ADC_1	—	—	AN[13](3)	—					
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—	38	55
		ADC_0 ADC_1	—	—	AN[14](3)	—					
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60
		LINFlex_1	—	—	RXD	PSMI[32]; PADSEL=0					
		ADC_1	—	—	AN[0](3)	—					
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2					
		SIUL	—	—	EIRQ[19]	—					
		ADC_1	—	—	AN[1](3)	—					
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62
		SIUL	—	—	EIRQ[20]	—					
		ADC_1	—	—	AN[2](3)	—					
Port C											
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66
		ADC_1	—	—	AN[3](3)	—					
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41
		ADC_0	—	—	AN[2](3)	—					
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45
		ADC_0	—	—	AN[3](3)	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
C[4]	PCR[36]	SIUL	GPIO[36]	ALT0	GPIO[36]	—	Pull down	M	S	5	11
		DSPI_0	CS0	ALT1	CS0	—					
		FlexPWM_0	X[1]	ALT2	X[1]	PSMI[28]; PADSEL=0					
		SSCM	DEBUG[4]	ALT3	—	—					
		SIUL	—	—	EIRQ[22]	—					
C[5]	PCR[37]	SIUL	GPIO[37]	ALT0	GPIO[37]	—	Pull down	M	S	7	13
		DSPI_0	SCK	ALT1	SCK	—					
		SSCM	DEBUG[5]	ALT3	—	—					
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=0					
		SIUL	—	—	EIRQ[23]	—					
C[6]	PCR[38]	SIUL	GPIO[38]	ALT0	GPIO[38]	—	Pull down	M	S	98	142
		DSPI_0	SOUT	ALT1	—	—					
		FlexPWM_0	B[1]	ALT2	B[1]	PSMI[25]; PADSEL=0					
		SSCM	DEBUG[6]	ALT3	—	—					
		SIUL	—	—	EIRQ[24]	—					
C[7]	PCR[39]	SIUL	GPIO[39]	ALT0	GPIO[39]	—	Pull down	M	S	9	15
		FlexPWM_0	A[1]	ALT2	A[1]	PSMI[21]; PADSEL=0					
		SSCM	DEBUG[7]	ALT3	—	—					
		DSPI_0	—	—	SIN	—					
C[10]	PCR[42]	SIUL	GPIO[42]	ALT0	GPIO[42]	—	Pull down	M	S	78	111
		DSPI_2	CS2	ALT1	—	—					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=0					
C[11]	PCR[43]	SIUL	GPIO[43]	ALT0	GPIO[43]	—	Pull down	M	S	55	80
		eTimer_0	ETC[4]	ALT1	ETC[4]	PSMI[7]; PADSEL=1					
		DSPI_2	CS2	ALT2	—	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	Pull down	M	S	56	82
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0					
		DSPI_2	CS3	ALT2	—	—					
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	Pull down	M	S	71	101
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0					
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0					
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0					
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	Pull down	M	S	72	103
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1					
		CTU_0	EXT_TGR	ALT2	—	—					
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	Pull down	SYM	S	85	124
		FlexRay	CA_TR_EN	ALT1	—	—					
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1					
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1					
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1					
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1					
Port D											
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	Pull down	SYM	S	86	125
		FlexRay	CA_TX	ALT1	—	—					
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1					
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	Pull down	M	S	3	3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2					
		CTU_0	EXT_TGR	ALT3	—	—					
		FlexRay	—	—	CA_RX	—					
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	Pull down	M	S	—	140
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0					
		FlexRay	—	—	CB_RX	—					
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	Pull down	SYM	S	89	128
		FlexRay	CB_TX	ALT1	—	—					
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2					
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	Pull down	SYM	S	90	129
		FlexRay	CB_TR_EN	ALT1	—	—					
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2					
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	Pull down	M	S	22	33
		DSPI_0	CS3	ALT1	—	—					
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0					
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	Pull down	M	S	23	34
		DSPI_0	CS2	ALT1	—	—					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
D[7]	PCR[55]	SIUL	GPIO[55]	ALT0	GPIO[55]	—	Pull down	M	S	26	37
		DSPI_1	CS3	ALT1	—	—					
		DSPI_0	CS4	ALT3	—	—					
		SWG	analog output	—	—	—					
D[8]	PCR[56]	SIUL	GPIO[56]	ALT0	GPIO[56]	—	Pull down	M	S	21	32
		DSPI_1	CS2	ALT1	—	—					
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=2					
		DSPI_0	CS5	ALT3	—	—					
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=1					
D[9]	PCR[57]	SIUL	GPIO[57]	ALT0	GPIO[57]	—	Pull down	M	S	15	26
		FlexPWM_0	X[0]	ALT1	X[0]	—					
		LINFlexD_1	TXD	ALT2	—	—					
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	Pull down	M	S	53	76
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1					
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1					
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	Pull down	M	S	54	78
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1					
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1					
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		Pull down	M	S	70	99
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1					
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1					
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	Pull down	M	S	73	105
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2					
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port E											
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68
		ADC_1	—	—	AN[5](3)	—					
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49
		ADC_0	—	—	AN[5](3)	—					
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42
		ADC_0	—	—	AN[7](3)	—					
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44
		ADC_0	—	—	AN[8](3)	—					
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46
		ADC_0	—	—	AN[4](3)	—					
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48
		ADC_0	—	—	AN[6](3)	—					
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61
		ADC_1	—	—	AN[7](3)	—					
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63
		ADC_1	—	—	AN[8](3)	—					
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65
		ADC_1	—	—	AN[4](3)	—					
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67
		ADC_1	—	—	AN[6](3)	—					
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	Pull down	M	S	—	117
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1					
		DSPI_2	CS3	ALT2	—	—					
		SIUL	—	—	EIRQ[25]	—					
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	Pull down	M	S	—	119
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3					
		SIUL	—	—	EIRQ[26]	—					
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	Pull down	M	S	—	121
		DSPI_0	CS1	ALT1	—	—					
		SIUL	—	—	EIRQ[27]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port F											
F[0]	PCR[80]	SIUL	GPIO[80]	ALT0	GPIO[80]	—	Pull down	M	S	—	133
		FlexPWM_0	A[1]	ALT1	A[1]	PSMI[21]; PADSEL=2					
		eTimer_0	—	—	ETC[2]	PSMI[37]; PADSEL=1					
		SIUL	—	—	EIRQ[28]	—					
F[3]	PCR[83]	SIUL	GPIO[83]	ALT0	GPIO[83]	—	Pull down	M	S	—	139
		DSPI_0	CS6	ALT1	—	—					
F[4]	PCR[84]	SIUL	GPIO[84]	ALT0	GPIO[84]	—	Pull down	F	S	—	4
		NPC	MDO[3]	ALT2	—	—					
F[5]	PCR[85]	SIUL	GPIO[85]	ALT0	GPIO[85]	—	Pull down	F	S	—	5
		NPC	MDO[2]	ALT2	—	—					
F[6]	PCR[86]	SIUL	GPIO[86]	ALT0	GPIO[86]	—	Pull down	F	S	—	8
		NPC	MDO[1]	ALT2	—	—					
F[7]	PCR[87]	SIUL	GPIO[87]	ALT0	GPIO[87]	—	Pull down	F	S	—	19
		NPC	MCKO	ALT2	—	—					
F[8]	PCR[88]	SIUL	GPIO[88]	ALT0	GPIO[88]	—	Pull down	F	S	—	20
		NPC	MSEO[1]	ALT2	—	—					
F[9]	PCR[89]	SIUL	GPIO[89]	ALT0	GPIO[89]	—	Pull down	F	S	—	23
		NPC	MSEO[0]	ALT2	—	—					
F[10]	PCR[90]	SIUL	GPIO[90]	ALT0	GPIO[90]	—	Pull down	F	S	—	24
		NPC	EVTO	ALT2	—	—					
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	Pull down	M	S	—	25
		NPC	EVTI	ALT2	—	—					
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	Pull down	M	S	—	106
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2					
		SIUL	—	—	EIRQ[30]	—					
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	Pull down	M	S	—	112
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3					
		SIUL	—	—	EIRQ[31]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	Pull down	M	S	—	115
		LINFlexD_1	TXD	ALT1	—	—					
		FlexCAN_2	RXD	ALT2	—	—					
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	Pull down	M	S	—	113
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2					
		FlexCAN_2	TXD	ALT2	—	—					
FCCU											
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S	27	38
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S	97	141
Port G											
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	Pull down	M	S	—	102
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1					
		DSPI_1	CS1	ALT2	—	—					
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	Pull down	M	S	—	104
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2					
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3					
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	Pull down	M	S	—	100
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2					
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3					
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	Pull down	M	S	—	85
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2					
		DSPI_2	CS3	ALT2	—	—					
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	Pull down	M	S	—	98
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		Pull down	M	S	—	83
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3					
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	Pull down	M	S	—	81
		FlexRay	DBG0	ALT1	—	—					
		DSPI_0	CS1	ALT2	—	—					
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2					
		SIUL	—	—	EIRQ[21]	—					
G[9]	PCR[105]	SIUL	GPIO[105]	ALT0	GPIO[105]	—	Pull down	M	S	—	79
		FlexRay	DBG1	ALT1	—	—					
		DSPI_1	CS1	ALT2	—	—					
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=2					
		SIUL	—	—	EIRQ[29]	—					
G[10]	PCR[106]	SIUL	GPIO[106]	ALT0	GPIO[106]	—	Pull down	M	S	—	77
		FlexRay	DBG2	ALT1	—	—					
		DSPI_2	CS3	ALT2	—	—					
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=1					
G[11]	PCR[107]	SIUL	GPIO[107]	ALT0	GPIO[107]	—	Pull down	M	S	—	75
		FlexRay	DBG3	ALT1	—	—					
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=2					
G[12]	PCR[108]	SIUL	GPIO[108]	ALT0	GPIO[108]	—	Pull down	F	S	—	—
		NPC	MDO[11]	ALT2	—	—					
G[13]	PCR[109]	SIUL	GPIO[109]	ALT0	GPIO[109]	—	Pull down	F	S	—	—
		NPC	MDO[10]	ALT2	—	—					
G[14]	PCR[110]	SIUL	GPIO[110]	ALT0	GPIO[110]	—	Pull down	F	S	—	—
		NPC	MDO[9]	ALT2	—	—					
G[15]	PCR[111]	SIUL	GPIO[111]	ALT0	GPIO[111]	—	Pull down	F	S	—	—
		NPC	MDO[8]	ALT2	—	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port H											
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	Pull down	F	S	—	—
		NPC	MDO[7]	ALT2	—	—					
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	Pull down	F	S	—	—
		NPC	MDO[6]	ALT2	—	—					
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	Pull down	F	S	—	—
		NPC	MDO[5]	ALT2	—	—					
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	Pull down	F	S	—	—
		NPC	MDO[4]	ALT2	—	—					
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	Pull down	M	S	—	—
		FlexPWM_1	X[0]	ALT1	X[0]	—					
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0					
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	Pull down	M	S	—	—
		FlexPWM_1	A[0]	ALT1	A[0]	—					
		DSPI_0	CS4	ALT3	—	—					
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	Pull down	M	S	—	—
		FlexPWM_1	B[0]	ALT1	B[0]	—					
		DSPI_0	CS5	ALT3	—	—					
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	Pull down	M	S	—	—
		FlexPWM_1	X[1]	ALT1	X[1]	—					
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0					
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	Pull down	M	S	—	—
		FlexPWM_1	A[1]	ALT1	A[1]	—					
		DSPI_0	CS6	ALT3	—	—					
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	Pull down	M	S	—	—
		FlexPWM_1	B[1]	ALT1	B[1]	—					
		DSPI_0	CS7	ALT3	—	—					
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	Pull down	M	S	—	—
		FlexPWM_1	X[2]	ALT1	X[2]	—					
		eTimer_2	ETC[2]	ALT2	ETC[2]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	Pull down	M	S	—	—
		FlexPWM_1	A[2]	ALT1	A[2]	—					
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	Pull down	M	S	—	—
		FlexPWM_1	B[2]	ALT1	B[2]	—					
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	Pull down	M	S	—	—
		FlexPWM_1	X[3]	ALT1	X[3]	—					
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0					
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	Pull down	M	S	—	—
		FlexPWM_1	A[3]	ALT1	A[3]	—					
		eTimer_2	ETC[4]	ALT2	ETC[4]	—					
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	Pull down	M	S	—	—
		FlexPWM_1	B[3]	ALT1	B[3]	—					
		eTimer_2	ETC[5]	ALT2	ETC[5]	—					
Port I											
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	Pull down	M	S	—	—
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1					
		DSPI_0	CS4	ALT2	—	—					
		FlexPWM_1	—	—	FAULT[0]	—					
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	Pull down	M	S	—	—
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1					
		DSPI_0	CS5	ALT2	—	—					
		FlexPWM_1	—	—	FAULT[1]	—					
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	Pull down	M	S	—	—
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1					
		DSPI_0	CS6	ALT2	—	—					
		FlexPWM_1	—	—	FAULT[2]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	Pull down	M	S	—	—
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1					
		DSPI_0	CS7	ALT2	—	—					
		CTU_0	EXT_TGR	ALT3	—	—					
		FlexPWM_1	—	—	FAULT[3]	—					
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	Pull down	F	S	—	—
		NPC	RDY	ALT2	—	—					

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay).
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.5(2), (3)	V
$V_{DD_HV_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	4.5(2), (3)	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD_HV_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	4.5(2), (3)	V
$V_{SS_HV_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.5(2), (3)	V
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADR0}$(2), (3) $V_{DD_HV_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.4(2)	V

Table 8. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{SS_HV_ADR0}$ $V_{SS_HV_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.5(3), (4)	V
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS_HV_IOx}$)or $V_{ss_HV_ADRx}$	Valid only for ADC pins	–0.3	6.0(4)	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3(4), (5)	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device.
2. Any voltage between operating condition and absolute max rating can be sustained for maximum cumulative time of 10 hours.
3. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
4. Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met (2 mA for all pins) and VDDE is within the operating voltage specifications.
5. V_{DD} has to be considered equal to $V_{DD_HV_ADRx}$ in case of ADC pins, whilst it is $V_{DD_HV_IOx}$ for any other pin.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{SS_HV_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD_HV_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS_HV_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_ADR0}$(2),(3) $V_{DD_HV_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.63	V
$V_{SS_HV_AD0}$ $V_{SS_HV_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD_LV_REGCOR}$(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$(5)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_PLL}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_PLL}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} ≤ 120 MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD_HV_ADR0}$ and $V_{DD_HV_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
3. VDD_HV_ADRx must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail.
4. Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.
5. For the device to function properly, the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Decoupling capacitors

The internal voltage regulator requires an external NPN ballast and some additional decoupling capacitors. These capacitors shall be placed on the board as close as possible to the associated pin.

Table 10. Decoupling capacitors

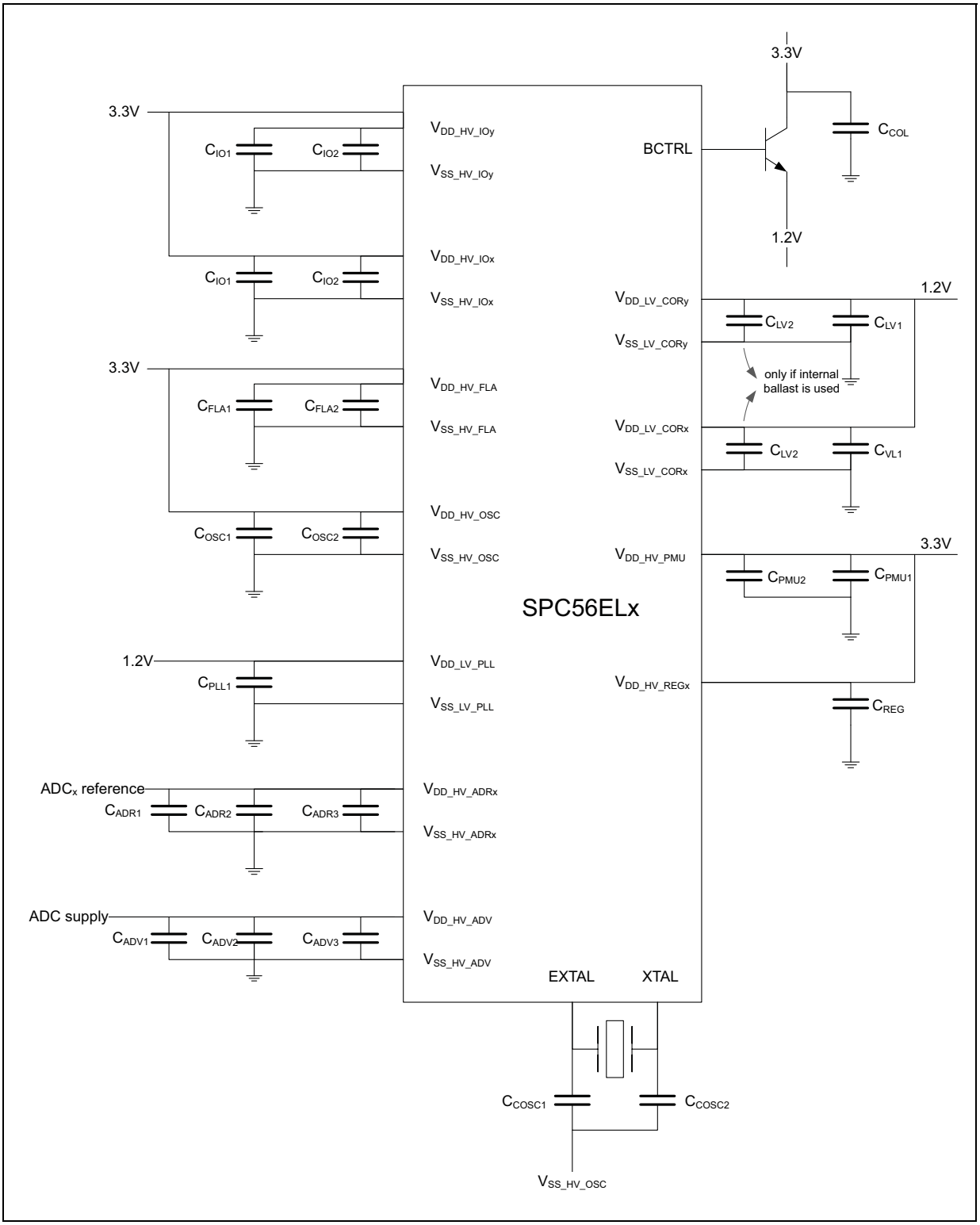
Symbol		Parameter	Conditions(1)	Value			Unit
				Min	Typ	Max	
C_{COL}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Max ESR = 100 mΩ.		20		µF
C_{LV1}	SR	External decoupling / stability capacitor	Sum of C_{LV1} placed close to $V_{DD}/V_{SS_LV_CORy}$ pairs(2).	12µF		40µF	µF
C_{LV2}	SR	External decoupling / stability capacitor	Sum of C_{LV2} placed close to $V_{DD}/V_{SS_LV_CORy}$ pairs shall be between 300 nF and 900 nF.		100(2)		nF
C_{PMU1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		µF

Table 10. Decoupling capacitors (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
C_{PMU2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{REG}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		20		µF
C_{IO1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{IO2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		470		pF
C_{FLA1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{FLA2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{OSC1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{OSC2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{PLL1}	SR	External decoupling / stability capacitor		22		100	nF
C_{ADR1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADR2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADR3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF
C_{ADV1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADV2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADV3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF

1. Capacitors shall be placed as close as possible to the respective pads.
2. Total ESR considering all decoupling capacitor close to the $V_{DD}/V_{SS_LV_CORy}$ pairs shall be between 1 mΩ and 100 mΩ.

Figure 4. Decoupling capacitors



3.5 Thermal characteristics

Table 11. Thermal characteristics for LQFP100 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	36	°C/W
			Four layer board – 2s2p	28	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	19	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 12. Thermal characteristics for LQFP144 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	42	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	35	°C/W
			Four layer board – 2s2p	30	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	24	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T= thermocouple temperature on top of the package (°C)

Ψ_{JT}= thermal characterization parameter (°C/W)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB in JEDEC site.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic Interference (EMI) characteristics

The characteristics in *Table 14* were measured using:

- Device configuration, test conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in *Table 14* is explained in *Table 13*.

Table 13. EMI configuration summary

Configuration name	Description
Configuration A	– High emission = all pads have max slew rate, LVDS pads running at 40 MHz – Oscillator frequency = 40 MHz – System bus frequency = 120 MHz – No PLL frequency modulation – IEC level K (≤ 30 dBµV)
Configuration B	– Reference emission = pads use min, mid and max slew rates, LVDS pads disabled – Oscillator frequency = 40 MHz – System bus frequency = 120 MHz – 2% PLL frequency modulation – IEC level K(≤ 30 dBµV)

Table 14. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	10	—	dBµV
			Configuration A; frequency range 50–150 MHz	—	18	—	
			Configuration A; frequency range 150–500 MHz	—	30	—	
			Configuration A; frequency range 500–1000 MHz	—	18	—	
			Configuration B; frequency range 50–150 MHz	—	10	—	
			Configuration B; frequency range 50–150 MHz	—	18	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	18	—	

EME testing was performed and documented according to these standards: [IEC 61967-2 & -4]

EMS testing was performed and documented according to these standards: [IEC 62132-2 & -4]

3.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (*n* + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 15. ESD ratings(1)(2)

No.	Symbol		Parameter	Conditions	Class	Max value(3)	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.8 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.9 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The SPC56XL70 always powers up using HPREG1 if an external NPN transistor is present. Then the SPC56XL70 makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off. The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- BCX68 from Infineon

Table 17. Recommended operating characteristics

Symbol	Parameter	Value	Unit
$h_{FE}(\beta)$	DC current gain (Beta)	85 - 375	—
P_D	Maximum power dissipation @ T_A=25°C(1)	1.5	W

Table 17. Recommended operating characteristics (continued)

Symbol	Parameter	Value	Unit
I_{CMaxDC}	Maximum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage(Max)	600(2)	mV
V_{BE}	Base-to-emitter voltage (Max)	1.0	V

1. Derating factor 12mW/degC.
2. Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<$VCE_{SAT.}$

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

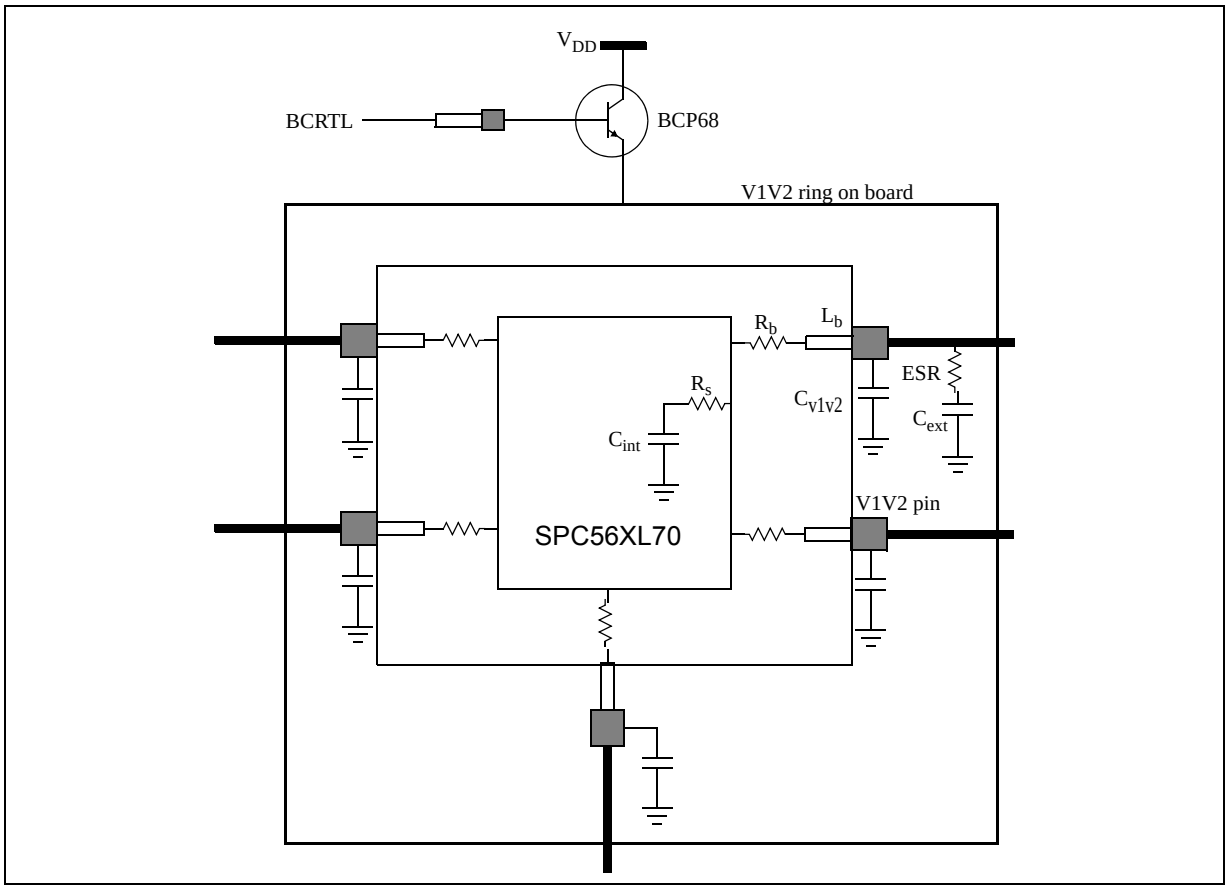
Table 18. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
C_{ext}		External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.93	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V

Table 18. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	1.355	—	1.495	V
			After a destructive reset initialization phase completion	1.39	—	1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.315	—	1.455	V
			After a destructive reset initialization phase completion	1.35	—	1.38	
—	D	Digital supply low voltage detector lower threshold	Before a destructive reset initialization phase completion	1.080	—	1.226	V
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	1.140	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	1.16	—	1.22	V
—	D	Digital supply low voltage detector upper threshold	Before a destructive reset initialization phase completion	1.16	—	1.306	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
—	SR	Supply ramp rate	—	3	—	0.5×10^6	V/s
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

Figure 5. BCP68 board schematic example



Note: The combined ESR of the capacitors used on 1.2 V pins (V1V2 in the picture) shall be in the range of 1 mΩ to 100 mΩ. The minimum value of the ESR is constrained by the resonance caused by the external components, bonding inductance, and internal decoupling. The minimum ESR is required to avoid the resonance and make the regulator stable. DC electrical characteristics

Table 19 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD_HV_IOx}$ < 3.6 V).

Table 19. DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	—	V
V_{IL}	P	Maximum low level input voltage	—	—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	—	V
V_{IH}	D	Maximum high level input voltage	—	—	—	$V_{DD_HV_IOx}$ + 0.1(2),(3)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V

Table 19. DC electrical characteristics(1) (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
I_{INJ}	T	DC injection current per pin (all bi-directional ports)	—	–1	—	1	mA
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	—	µA
			$V_{IN} = V_{IH}$	—	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = –40 to +150 °C	–1	—	1	µA
		Input leakage current (all ADC input-only ports)		–0.25	—	0.25	
		Input leakage current (shared ADC input-only ports)		–0.3	—	0.3	
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1(2)	—	0.35 $V_{DD_HV_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	$V_{DD_HV_IOx}$+0.1(2)	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	

1. These specifications are design targets and subject to change per device characterization.
2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 8*.
3. The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.

3.10 Supply current characteristics

Current consumption data is given in *Table 20*. These specifications are design targets and are subject to change per device characterization.

Table 20. Current consumption characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD_LV_FULL}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	25 [mA]+2.7 [mA/MHz]* f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	115 [mA]+2.28 [mA/MHz]*f_{CPU}[MHz]	
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$[2]	T	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	25 [mA]+2.45 [mA/MHz]*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	115 [mA]+2.02 [mA/MHz]*f_{CPU}[MHz]	
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$[2]	P	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	319	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	358	
$I_{DD_LV_BIST}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	286	mA
			1.2 V supplies during LBIST (full LBIST configuration) T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	326	
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies Tj = 105 °C $V_{DD_LV_COR}$ = 1.2 V	—	—	315	mA
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies Tj = 125 °C $V_{DD_LV_COR}$ = 1.2 V	—	—	339	mA
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies Tj = 105 °C $V_{DD_LV_COR}$ = 1.2 V DPM Mode	—	—	193	mA
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies Tj = 125 °C $V_{DD_LV_COR}$ = 1.2 V DPM Mode	—	—	231	mA
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies Tj = 150 °C $V_{DD_LV_COR}$ = 1.2 V DPM Mode	—	—	277	mA

Table 20. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD_LV_STOP}$	T	Operating current in V_{DD} STOP mode	T_J = 25 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	25	mA
	T		T_J = 55 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	53	
	P		T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	115	
$I_{DD_LV_HALT}$	T	Operating current in V_{DD} HALT mode	T_J = 25 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	30	mA
	T		T_J = 55 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	71	
	P		T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	125	
$I_{DD_HV_ADC}$[3],[4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_ADC}$ = 3.6 V	—	—	11	mA
$I_{DD_HV_AREF}$[4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_REF}$ = 3.6 V	—	—	4	mA
			T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_REF}$ = 5.5 V	—	—	6	
$I_{DD_HV_OSC}$ (oscillator bypass mode)	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	900	µA
$I_{DD_HV_OSC}$ (crystal oscillator mode)	D	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	3.5	mA
$I_{DD_HV_FLASH}$[5]	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	4	mA
$I_{DD_HV_PMU}$	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	10	mA

1. Devices configured for DPM mode, single core only with Core 0 executing typical code at 120 MHz from SRAM and Core 1 in reset. If core execution mode not specified, the device is configured for LSM mode with both cores executing typical code at 120 MHz from SRAM.
2. Enabled Modules in 'Typical mode': FlexPWM0, ETimer0/1/2, CTU, SWG, DMA, FlexCAN0/1, LINFlex, ADC1, DSPI0/1, PIT, CRC, PLL0/1, I/O supply current excluded
3. Internal structures hold the input voltage less than VDDA + 1.0 V on all pads powered by VDDA supplies, if the maximum injection current specification is met and VDDA is within the operating voltage specifications.
4. This value is the total current for both ADCs.
5. VFLASH is only available in the calibration package.

3.11 Temperature sensor electrical characteristics

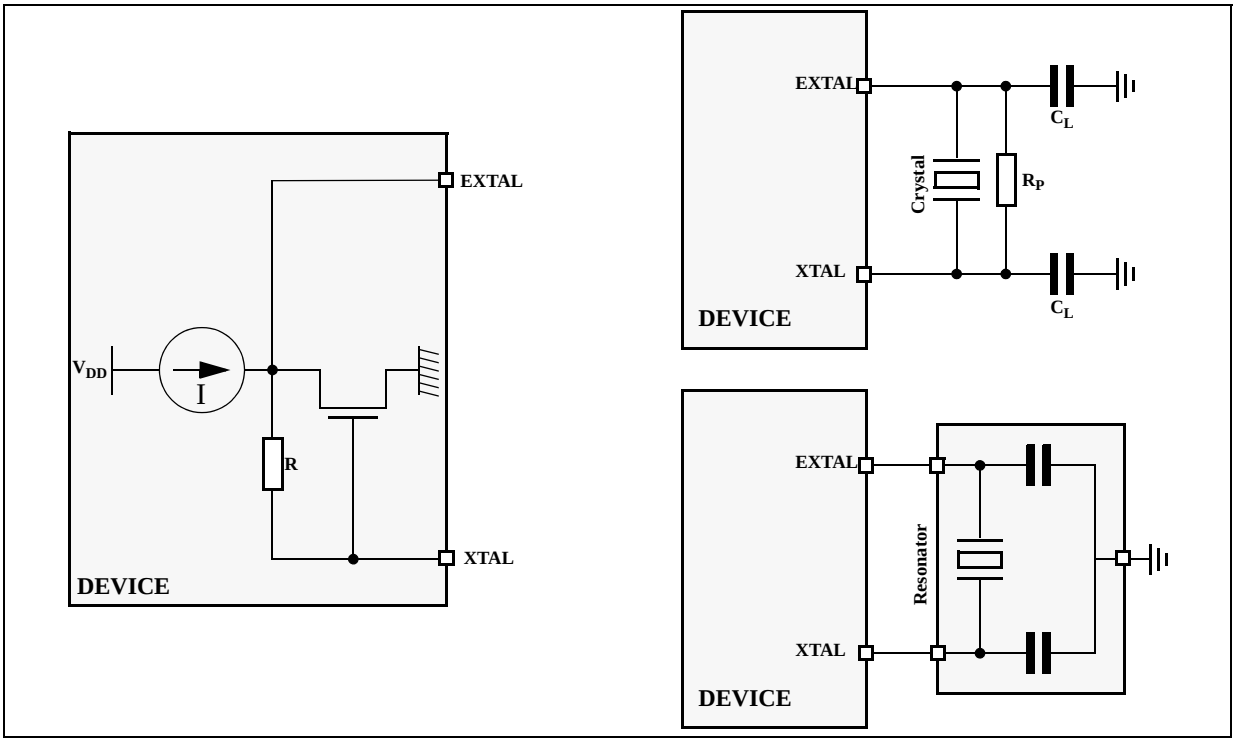
Table 21. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to 150 °C	–10	10	°C
T_S	D	Minimum sampling period	—	4	—	µs

3.12 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver. *Figure 6* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Figure 6. Crystal oscillator and resonator connection scheme



Note: XTAL/EXTAL must not be directly used to drive external circuits.

Figure 7. Main oscillator electrical characteristics

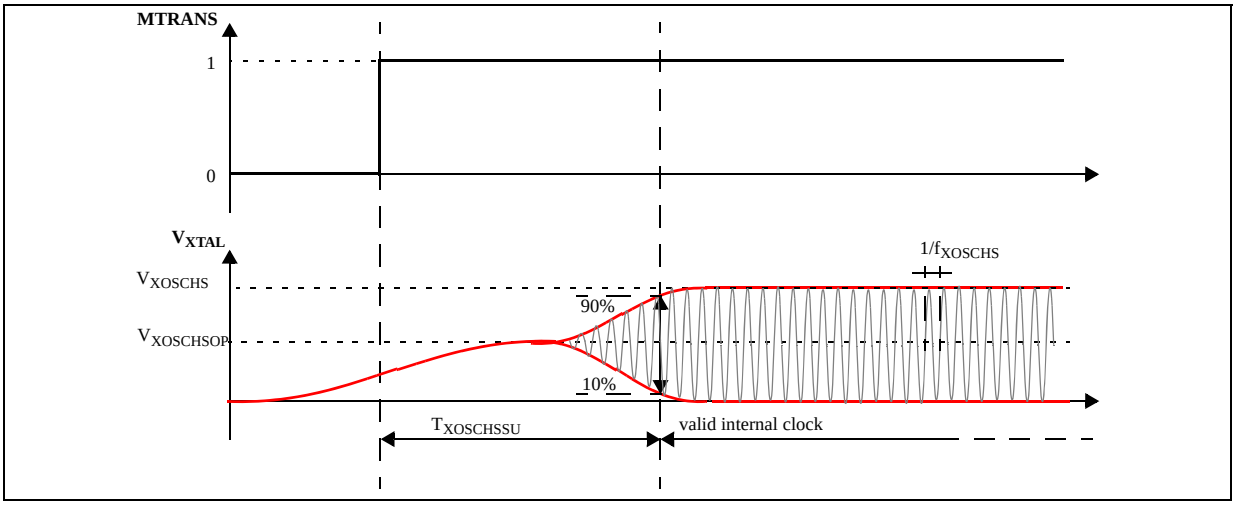


Table 22. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	P	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	13.25	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
I_{XOSCHS}	D	Oscillator consumption	—	—	—	3.5	mA
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]	—	—	6	ms
			f_{OSC} = 16, 40 MHz[2]	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1. V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.
2. The recommended configuration for maximizing the oscillator margin are:
   XOSC_MARGIN = 0 for 4 MHz quartz
   XOSC_MARGIN = 1 for 8/16/40 MHz quartz

3.13 FMPLL electrical characteristics

Table 23. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range(1)	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120(2)	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency(2)	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	—	150	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
t_{lpll}	D	FMPLL lock time (6), (7)	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter(8),(9),(10),(11)	Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% $f_{FMPLLOUT}$
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% $f_{FMPLLOUT}$
f_{CS} f_{DS}	D	Modulation depth	Center spread	±0.25	—	±2.0	% $f_{FMPLLOUT}$
			Down spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency(12)	—	—	—	100	KHz

1. Considering operation with FMPLL not bypassed.
2. With FM; the value does not include a possible +2% modulation
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.

4. Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
   f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
   $f_{SYS} = f_{VCO} \div ODF$
6. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.
7. This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8. This value is determined by the crystal manufacturer and board design.
9. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
10. Proper PC board layout procedures must be followed to achieve specifications.
11. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
12. Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

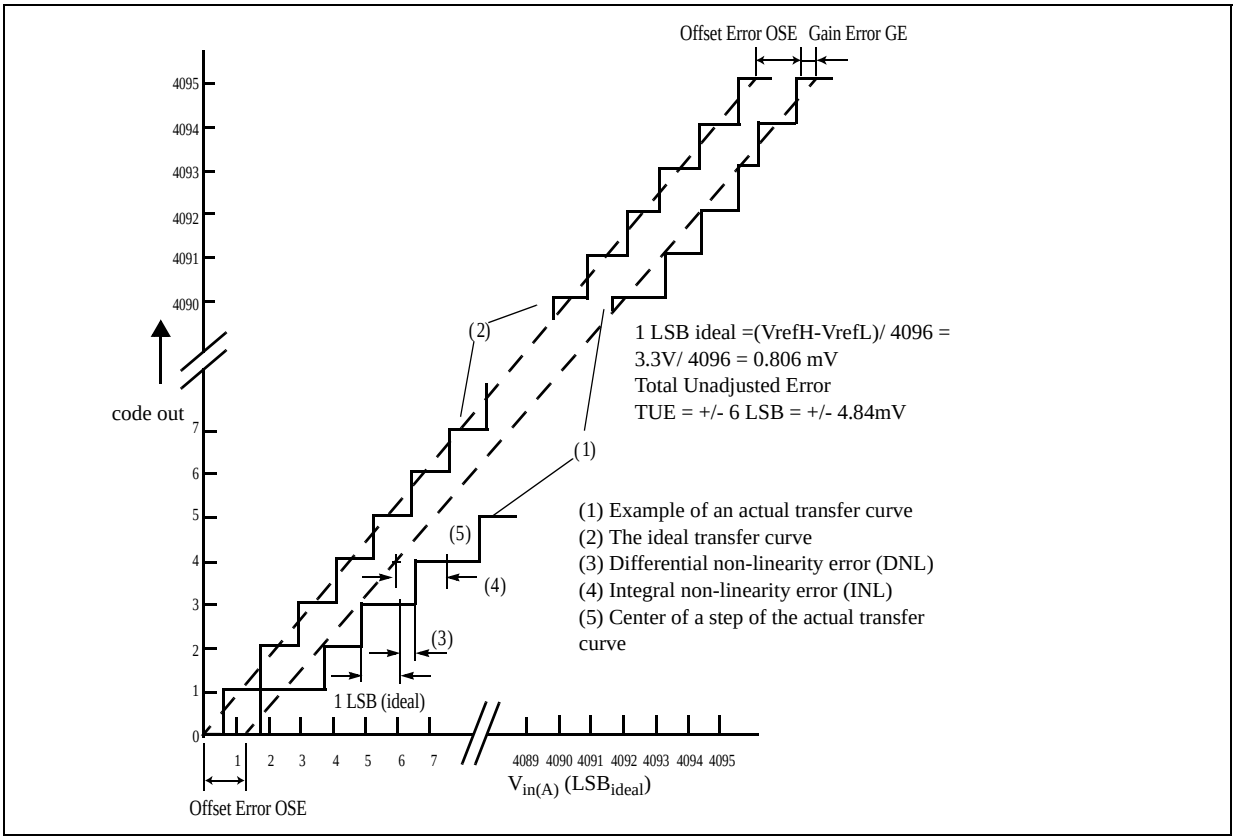
Table 24. RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typical	Max	Unit
f_{RC}	P	RC oscillator frequency	TA = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%

3.15 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Figure 8. ADC characteristics and error definitions



3.15.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

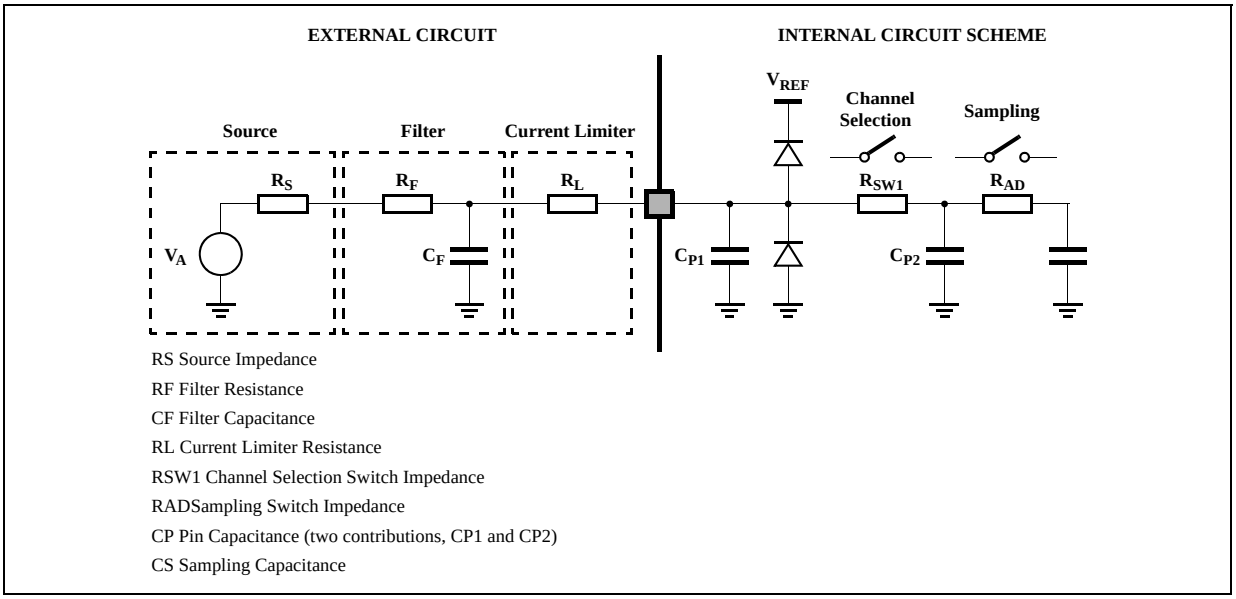
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fS × C_{P2} + C_S), where fs represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of R_S + R_F + R_L + R_{SW} + R_{AD}, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

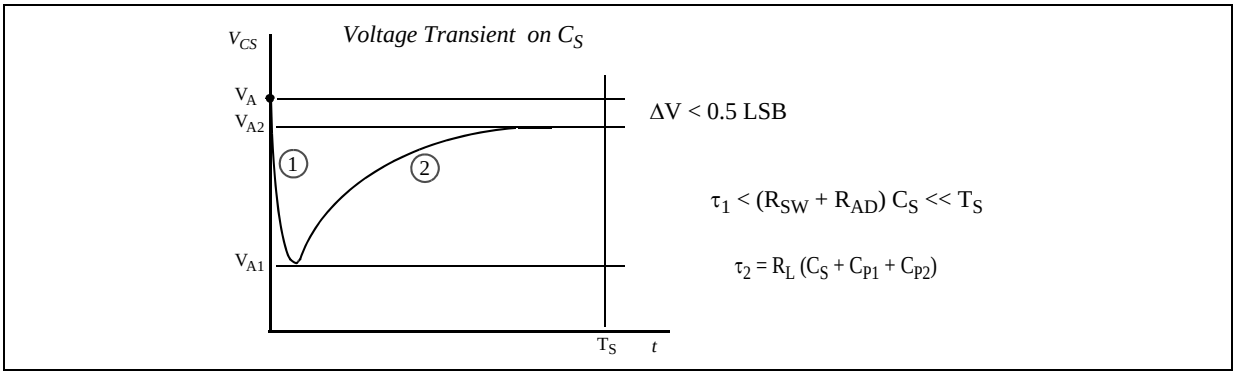
Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 9. Input Equivalent Circuit



A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 9*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 10. Transient Behavior during Sampling Phase



In particular two different transient periods can be distinguished:

A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged):

considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

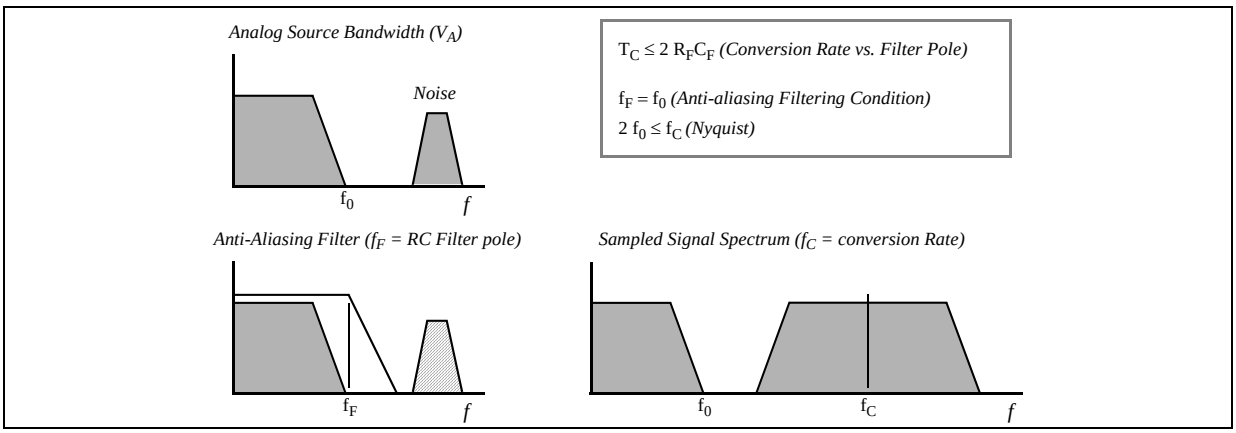
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 11. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 8192 \bullet C_S$$

Table 25. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	983.6[3]	KHz
t_{sample}	D	Sample time[4]	60 MHz	383	—	—	ns
t_{eval}	D	Evaluation time[5]	60 MHz	625	—	—	ns
C_S[6]	D	ADC input sampling capacitance	—	—	—	7.32	pF
C_{P1}[6]	D	ADC input pin capacitance 1	—	—	—	5[7]	pF
C_{P2}[6]	D	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	D	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
			V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[6]	D	Internal resistance of analog source	—	—	—	825	Ω
INL	P	Integral non linearity	—	–3	—	3	LSB
DNL	P	Differential non linearity[8]	—	–1	—	2	LSB
OFS	T	Offset error	—	–6	—	6	LSB
GNE	T	Gain error	—	–6	—	6	LSB
IS1WINJ	—		(single ADC channel)				
	C	Max positive/negative injection		–3	—	3	mA
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1. T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.

4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result.
6. See *Figure 9*.
7. For the 144-pin package.
8. No missing codes.

3.16 Flash memory electrical characteristics

Table 26. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ (1)	Initial Max(2)	Lifetime Max(3)	Unit
1	$t_{DWPROGRAM}$	*(4)	Double word (64 bits) program time(4)	38	—	500	µs
2	$t_{PPROGRAM}$	*(4)	Page(128 bits) program time(4)	45	160	500	µs
3	$t_{16KPPERASE}$	*(4)	16 KB block pre-program and erase time	270	1000	5000	ms
4	$t_{48KPPERASE}$	*(4)	48 KB block pre-program and erase time	625	1500	5000	ms
5	$t_{64KPPERASE}$	*(4)	64 KB block pre-program and erase time	800	1800	5000	ms
6	$t_{128KPPERASE}$	*(4)	128 KB block pre-program and erase time	1500	2600	7500	ms
7	$t_{256KPPERASE}$	*(4)	256 KB block pre-program and erase time	3000	5200	15000	ms

1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. These values are characterized, but not tested.I
2. Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at 25 °C. These values are verified at production test.
3. Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4. Program times are actual hardware programming times and do not include software overhead.

Table 27. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
t_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
t_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
t_{PSRT}	D	Time between program suspend resume and the next program suspend request(1)	100	—	—	µs
t_{ESRT}	D	Time between erase suspend resume and the next erase suspend request(2)	10	—	—	ms

1. Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does not occur is T_{PSRT}.
2. If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

Table 28. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Min	Typ	Max	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range(1)	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range(1)	1000	100000(2)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature(3) Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1. Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C.
2. Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks.
3. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.17 SWG electrical characteristics

Table 29. SPC56XL70 SWG Specifications

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1KHz	—	50 KHz
T	Peak to Peak(1)	0.4 V	—	2.0V
T	Peak to Peak variation(2)	-6%	—	6%
T	Common Mode(3)	—	1.3 V	—
T	Common Mode variation	-6%	—	6%
T	SiNAD(4)	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 µA	—	100 µA
T	ESD Pad Resistance(5)	230 Ω	—	360 Ω

1. Peak to Peak value is measured with no R or I load.
2. Peak to Peak excludes noise, SiNAD must be considered.
3. Common mode value is measured with no R or I load.
4. SiNAD is measured at Max Peak to Peak voltage.
5. Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

3.18 AC specifications

3.18.1 Pad AC specifications

Table 30. Pad AC specifications (3.3 V, IPP_HVE = 0)(1)

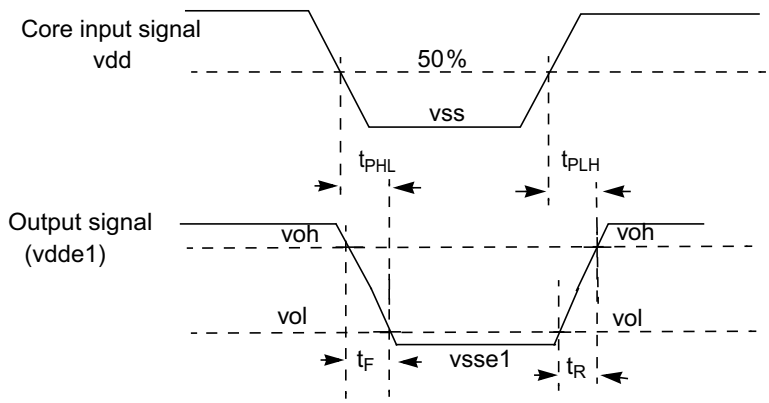
No	Pad		Tswitchon[1] (ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200

Table 30. Pad AC specifications (3.3 V, IPP_HVE = 0)(1) (continued)

No	Pad		Tswitchon[1] (ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25

1. Propagation delay from $V_{DD_HV_IOx}$/2 of internal signal to Pchannel/Nchannel switch-on condition (i.e. t_PHL and t_PLH in *Figure 12: Pad output delay*).
2. Slope at rising/falling edge(i.e. t_F and t_R in *Figure 12: Pad output delay*).
3. Data based on characterization results, not tested in production.

Figure 12. Pad output delay



[1] t_F and t_R are transient times at the FAR END.
[2] t_{PHL} and t_{PLH} are measured at the pad.
[3] Core input slew = 1ns (0 to vdd).

3.19 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.19.1 Reset sequence duration

Table 31 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in *Section 3.19.2: Reset sequence description*.

Table 31. RESET sequences

No.	Symbol		Parameter	Conditions	T_{Reset}			Unit
					Min	Typ	Max(1)	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled		40	47	51	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	—	500	4200	5000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled		41	45	49	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	—	35	150	400	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	—	1	4	10	µs

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.19.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in *Table 31*. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences is specified in *Section 3.19.3: Reset sequence trigger mapping*.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

Note: $\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 31 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

Figure 13. Destructive Reset Sequence, BIST enabled

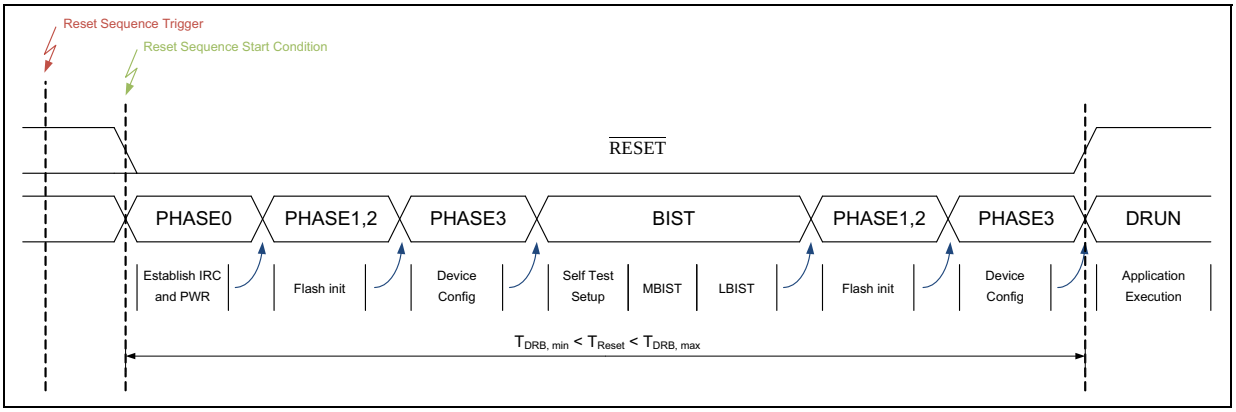


Figure 14. Destructive Reset Sequence, BIST disabled

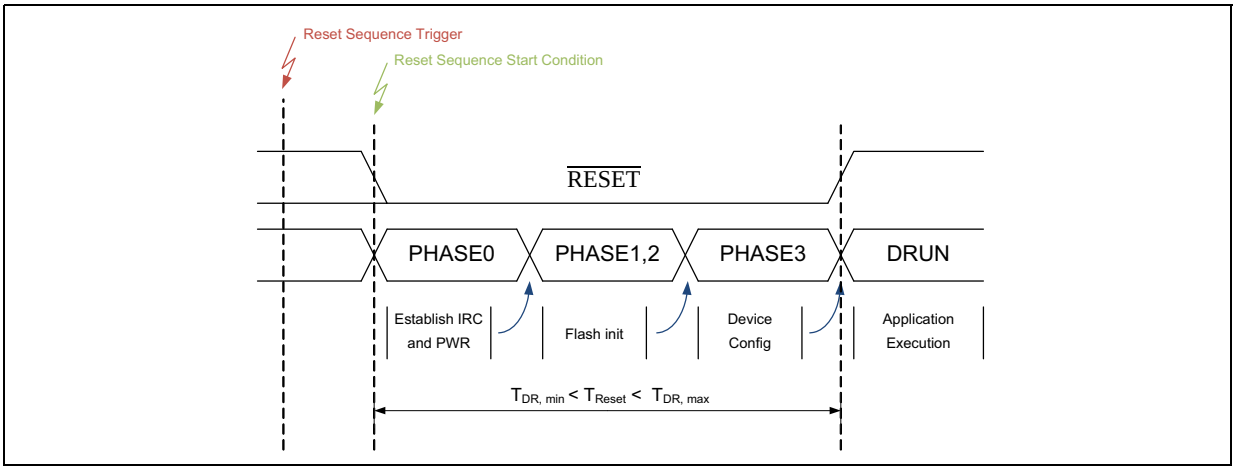


Figure 15. External Reset Sequence Long, BIST enabled

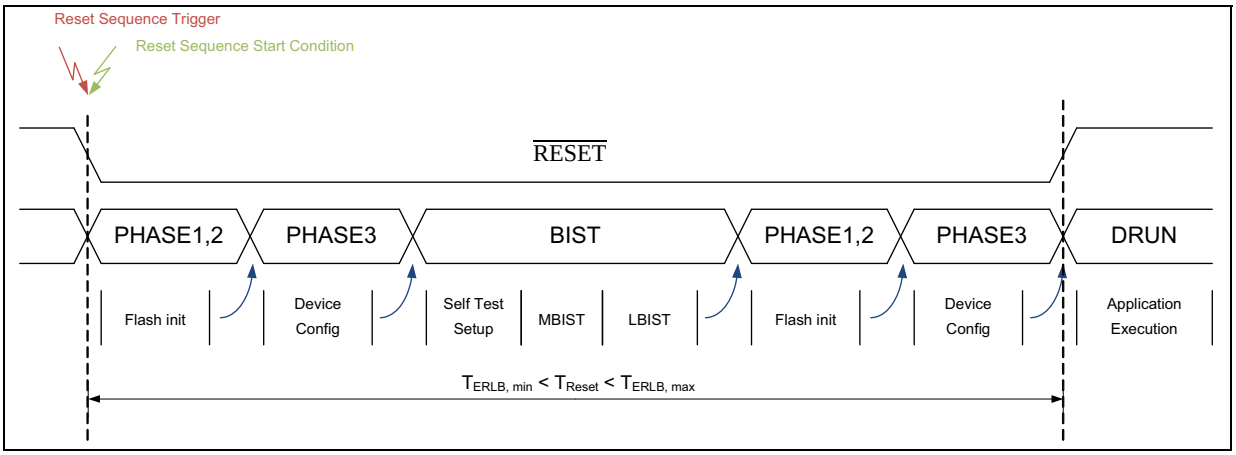


Figure 16. Functional Reset Sequence Long

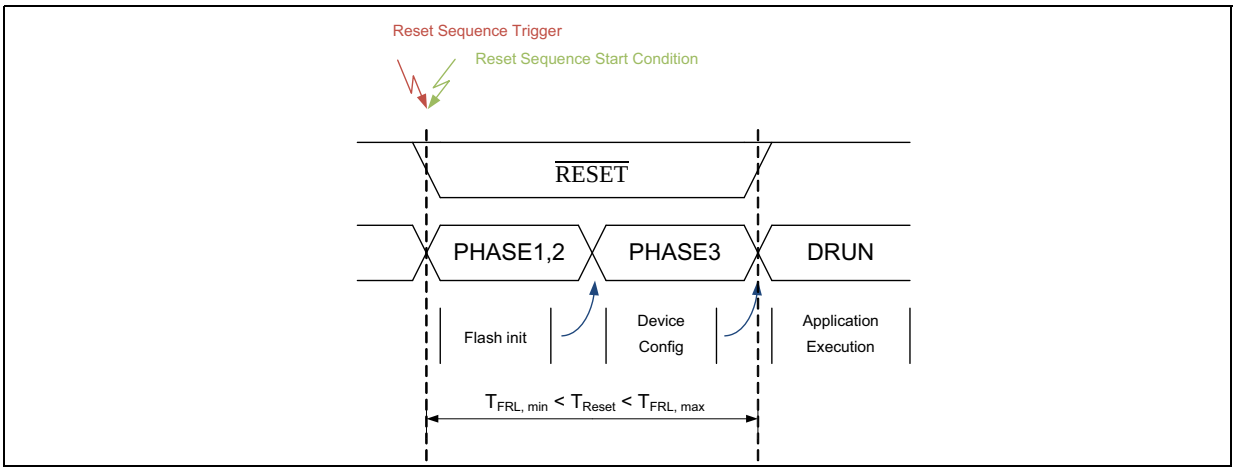
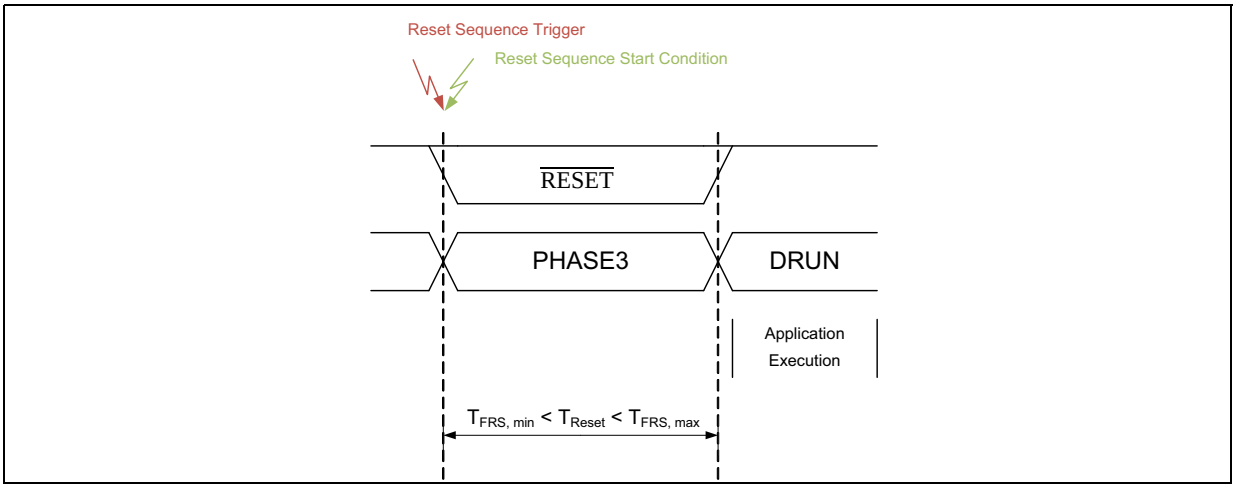


Figure 17. Functional Reset Sequence Short



The reset sequences shown in *Figure 16* and *Figure 17* are triggered by functional reset events. RESET is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET low for the duration of the internal reset sequence(c).

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in *Table 31*.

Table 32. Reset sequence trigger — Reset sequence

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive reset sequence, bist enabled(1)	Destructive reset sequence, bisT disabled(1)	External reset sequence long, bIST enabled	Functional reset sequence long	Functional reset sequence short
All internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	*Section 3.19.4.1: Destructive reset*	Release of RESET(2)	triggers		cannot trigger	cannot trigger	cannot trigger
Assertion of RESET(3)	*Section 3.19.4.2: External reset via RESET*		cannot trigger		triggers(4)	triggers(5)	triggers(6)

c. See RGM_FBRE register for more details.

Table 32. Reset sequence trigger — Reset sequence (continued)

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive reset sequence, bist enabled(1)	Destructive reset sequence, bisT disabled(1)	External reset sequence long, bIST enabled	Functional reset sequence long	Functional reset sequence short
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of RESET(7)	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1. Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.
2. End of the internal reset sequence (as specified in *Table 31*) can only be observed by release of RESET if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till RESET is released externally.
3. The assertion of RESET can only trigger a reset sequence if the device was running (RESET released) before. RESET does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if RESET is held low externally beyond the end of the internal sequence (beyond PHASE3).
4. If RESET is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.
5. If RESET is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.
6. If RESET is configured for short reset.
7. Internal reset sequence can only be observed by state of RESET if bidirectional RESET functionality is enabled for the functional reset source which triggered the reset sequence.

3.19.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.19.4.1 Destructive reset

Figure 18 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

Figure 18. Reset sequence start for destructive resets

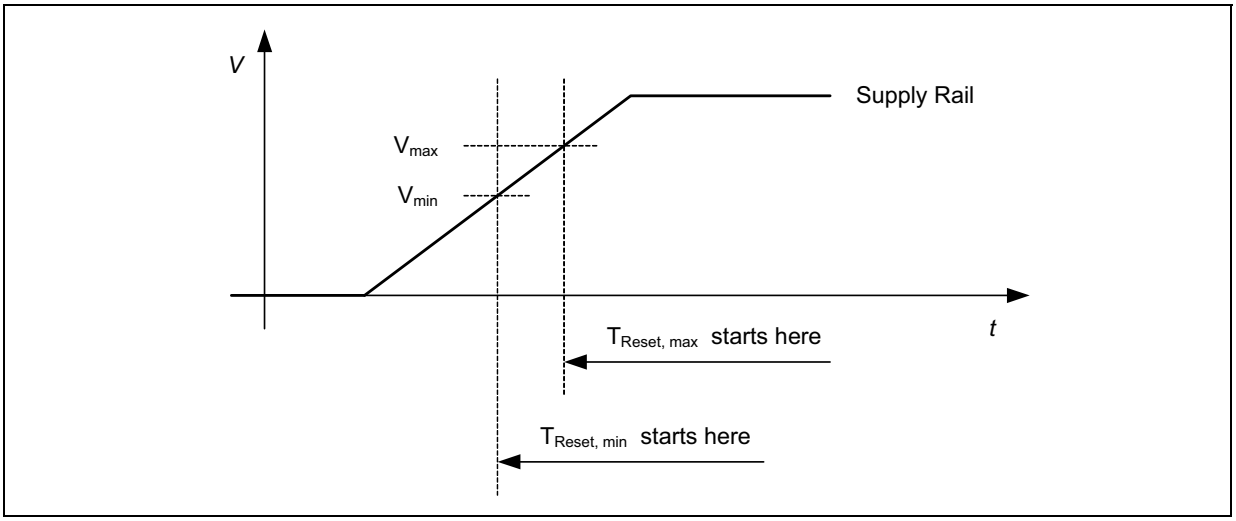


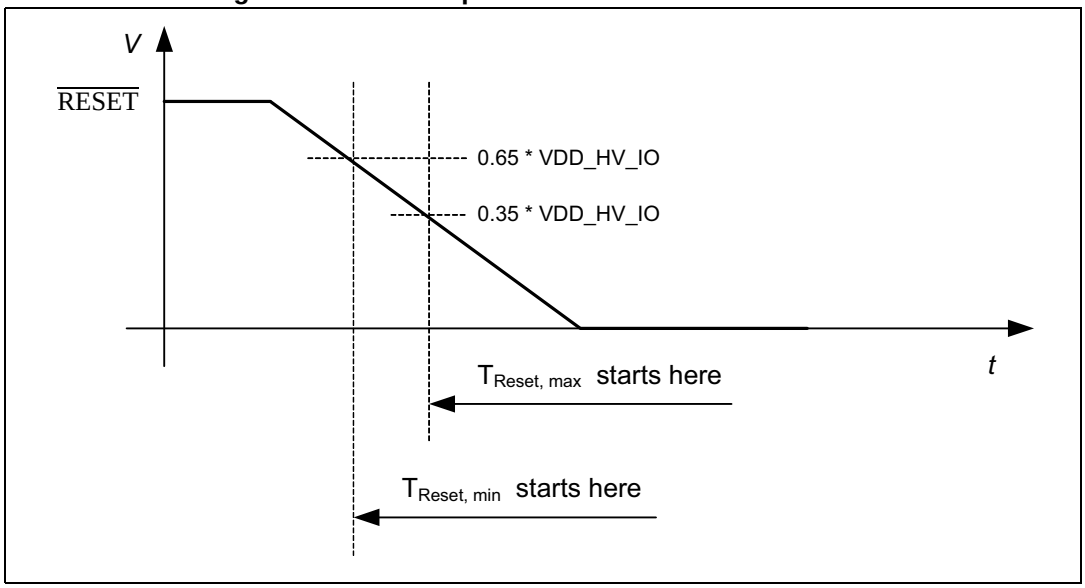
Table 33. Voltage thresholds

Variable name	Value
V_{min}	Refer to *Table 18*
V_{max}	Refer to *Table 18*
Supply Rail	VDD_HV_PMU

3.19.4.2 External reset via $\overline{\text{RESET}}$

Figure 19 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in *Table 32*.

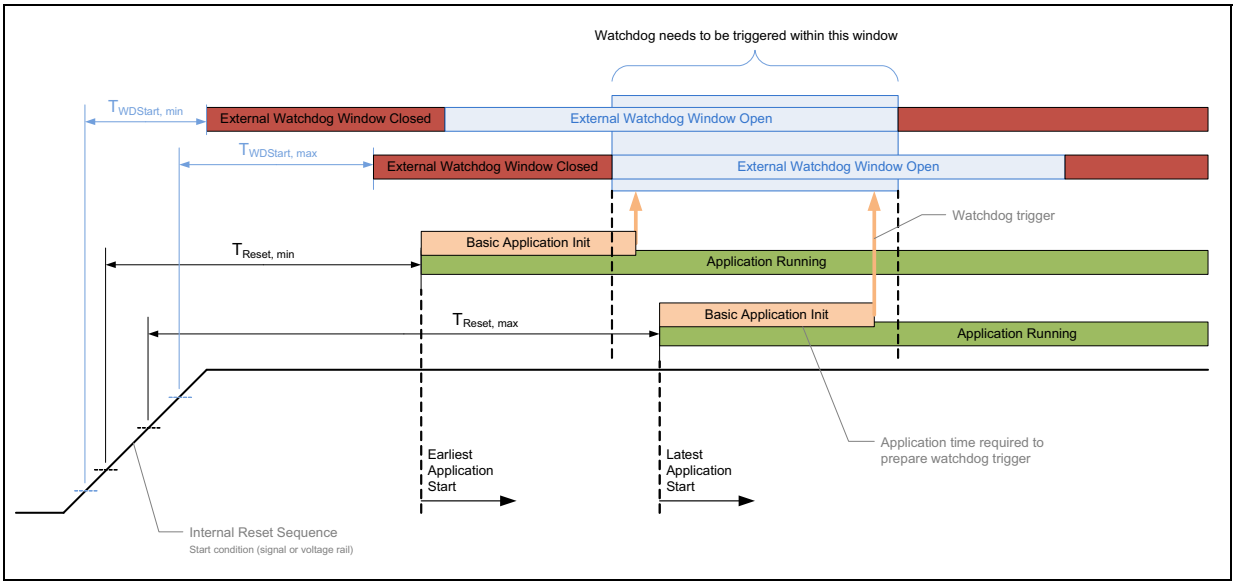
Figure 19. Reset sequence start via $\overline{\text{RESET}}$ assertion



3.19.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in *Section 3.19: Reset sequence* can be used to determine the correct positioning of the trigger window for the external watchdog. *Figure 20* shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

Figure 20. Reset sequence - External watchdog trigger window position



3.20 AC timing characteristics

AC Test Timing Conditions: Unless otherwise noted, all test conditions are as follows:
- TJ = –40°C to 150°C
- Supply voltages as specified in *Table 9*
- Input conditions: All Inputs: tr, tf = 1 ns
- Output Loading: All Outputs: 50 pF

3.20.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56XL70 implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 21. Start-up reset requirements

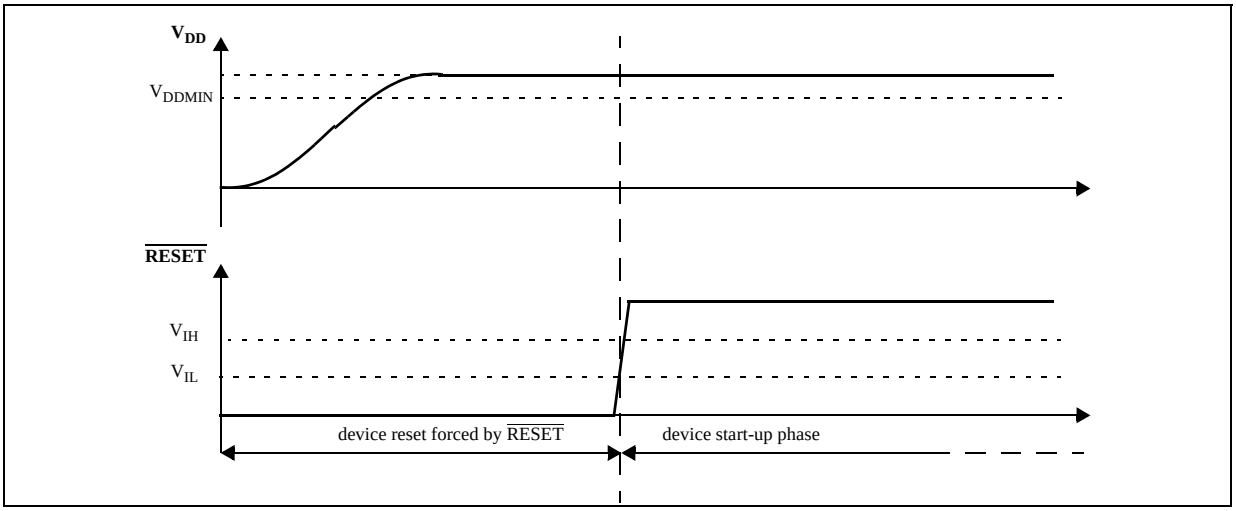


Figure 22. Noise filtering on reset signal

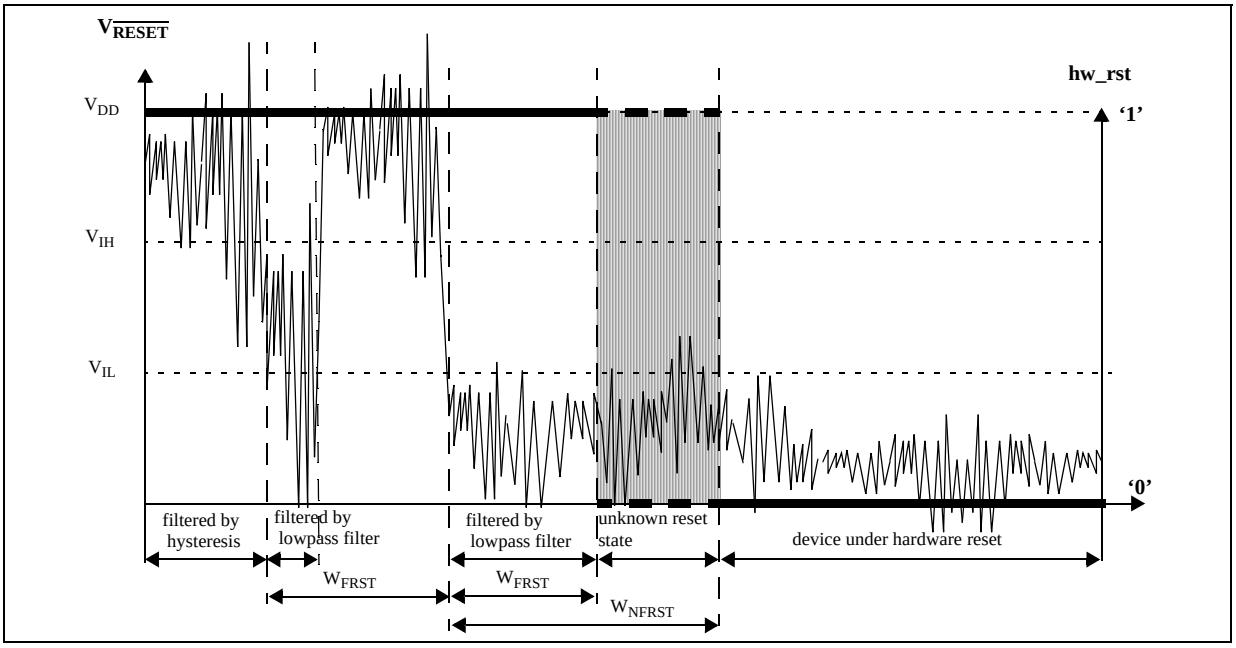


Table 34. $\overline{\text{RESET}}$ electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	$\overline{\text{nRESET}}$ input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	$\overline{\text{nRESET}}$ input not filtered pulse	—	500	—	—	ns

1. V_{DD} = 3.3 V ± 10%, T_J = –40°C to +150 °C, unless otherwise specified.
2. C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.20.2 WKUP/NMI timing

Table 35. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 23. JTAG test clock input timing

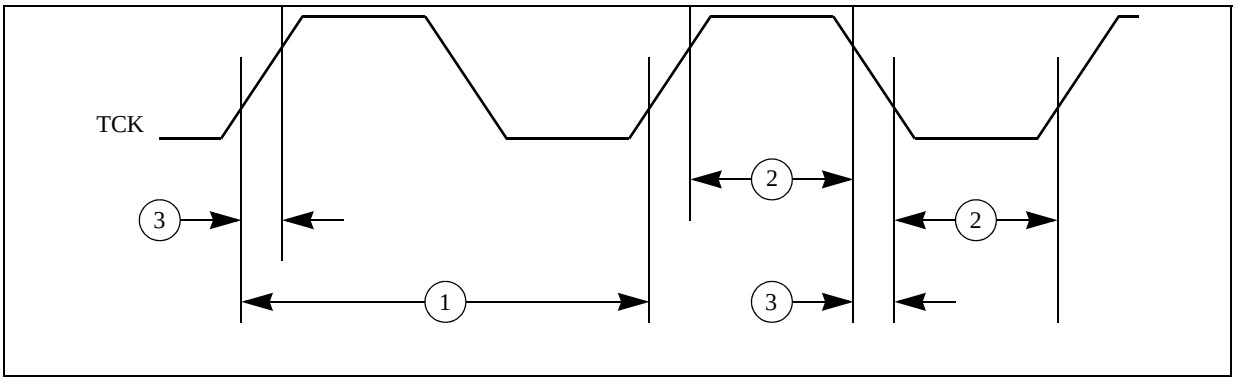


Figure 24. JTAG test access port timing

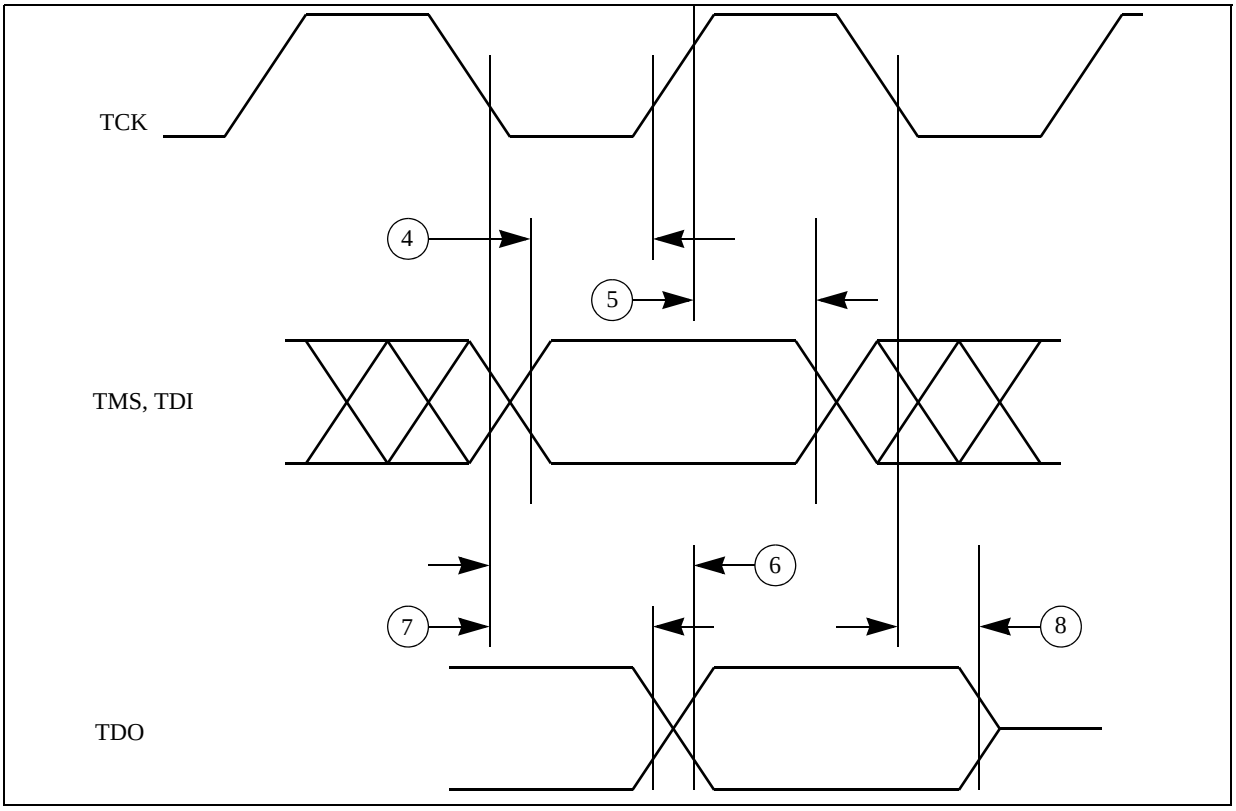
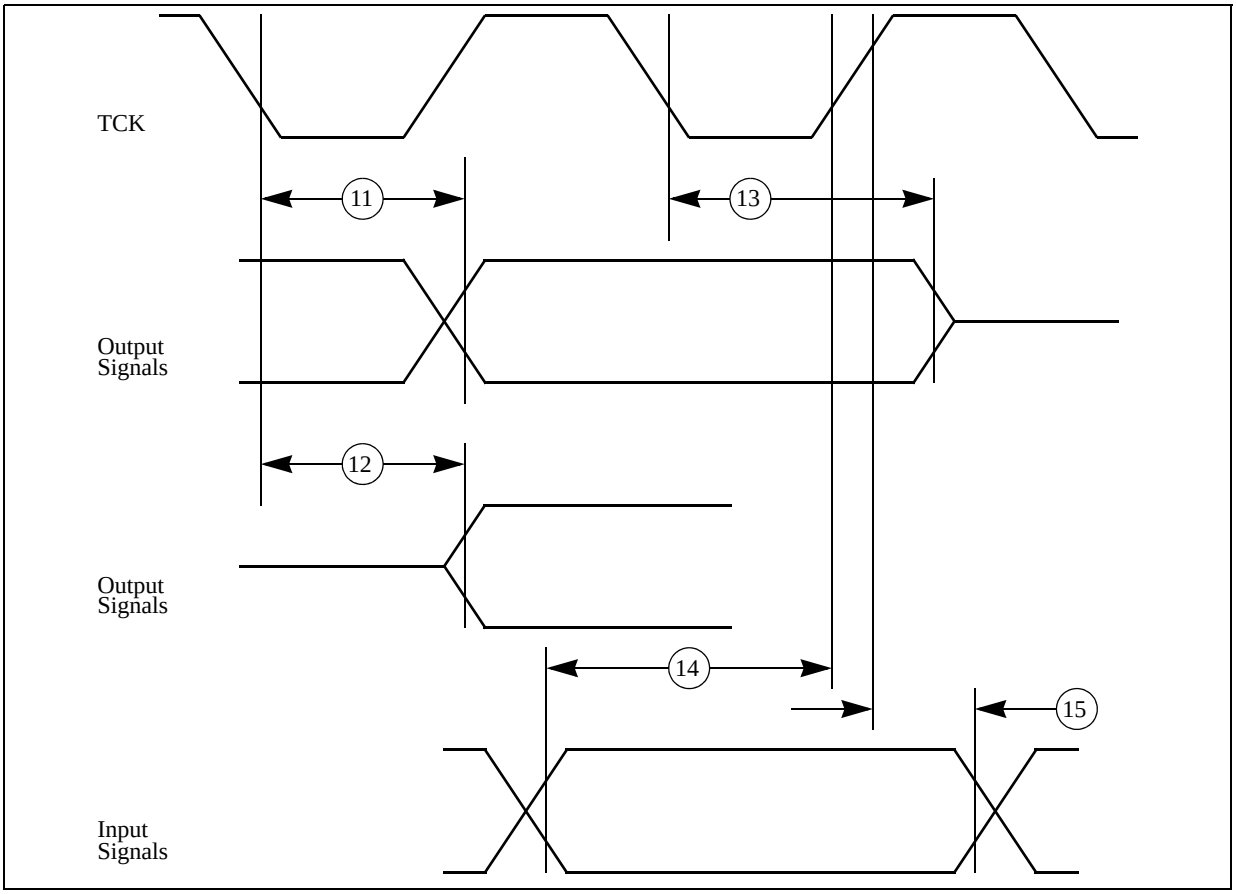


Figure 25. JTAG boundary scan timing



3.20.4 Nexus timing

Table 37. Nexus debug port timing(1)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid(2)	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{\text{EVTI}}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{\text{EVTO}}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time(3)	—	62.5	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	D	TCK Low to TDO Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3. The system clock frequency needs to be four times faster than the TCK frequency.

Figure 26. Nexus output timing

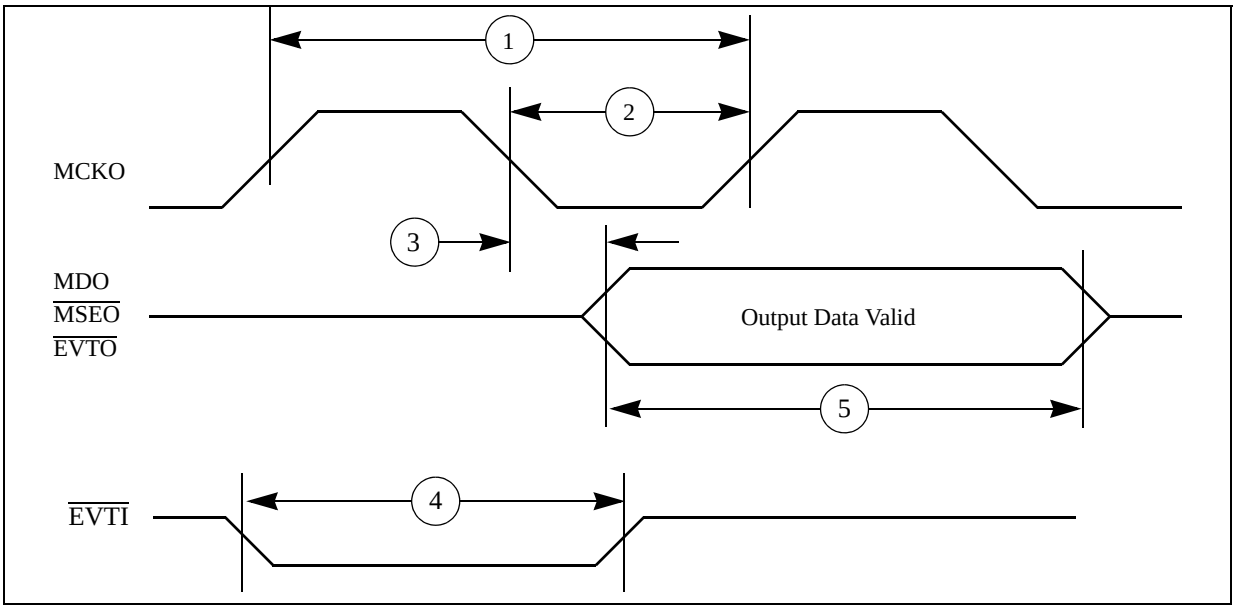


Figure 27. Nexus DDR Mode output timing

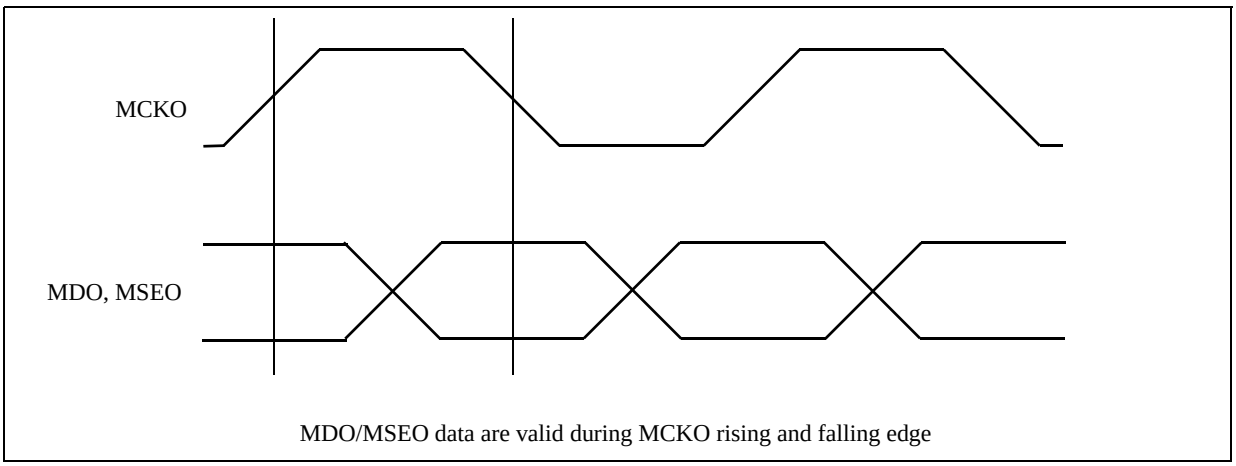
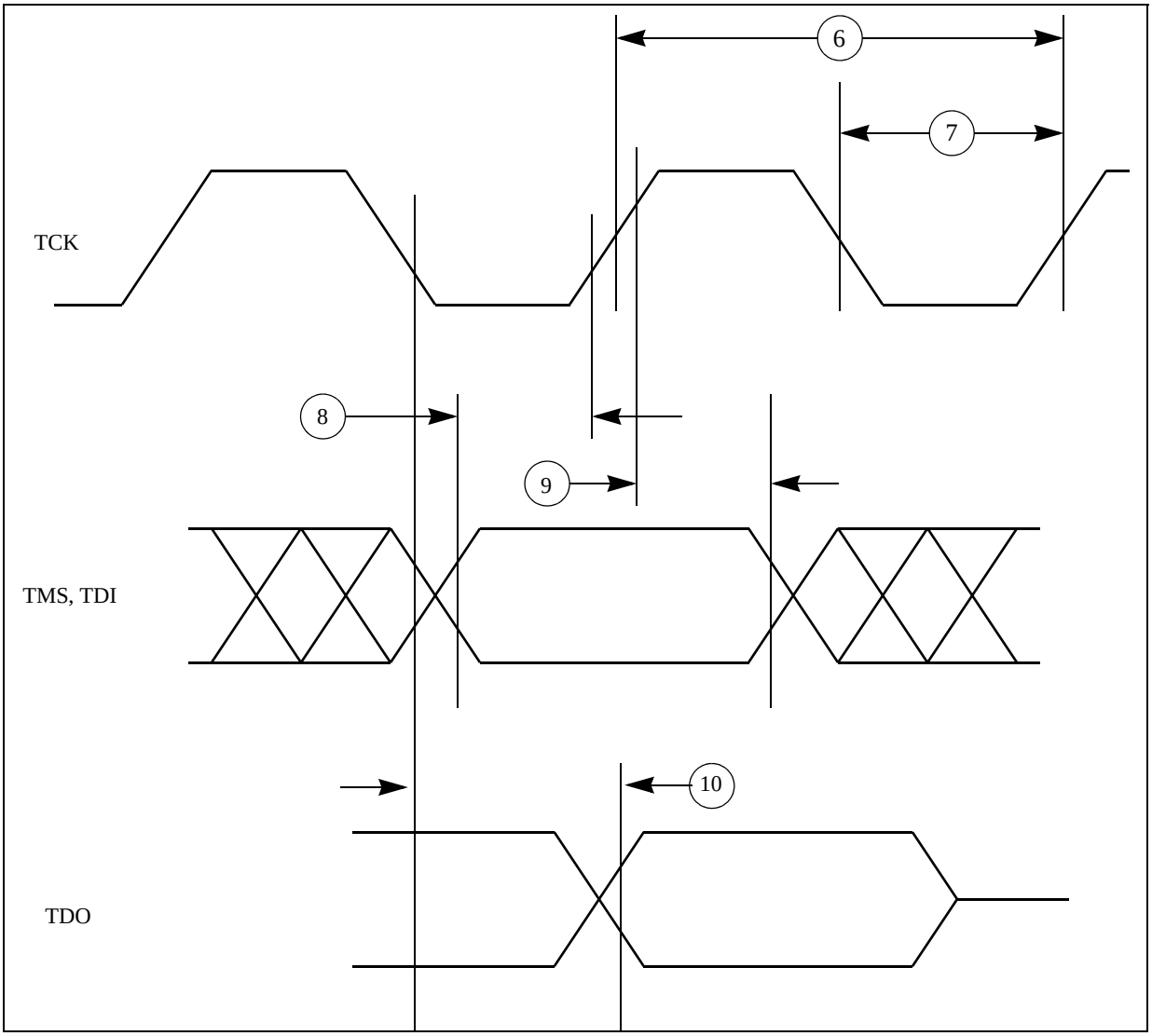


Figure 28. Nexus TDI, TMS, TDO timing



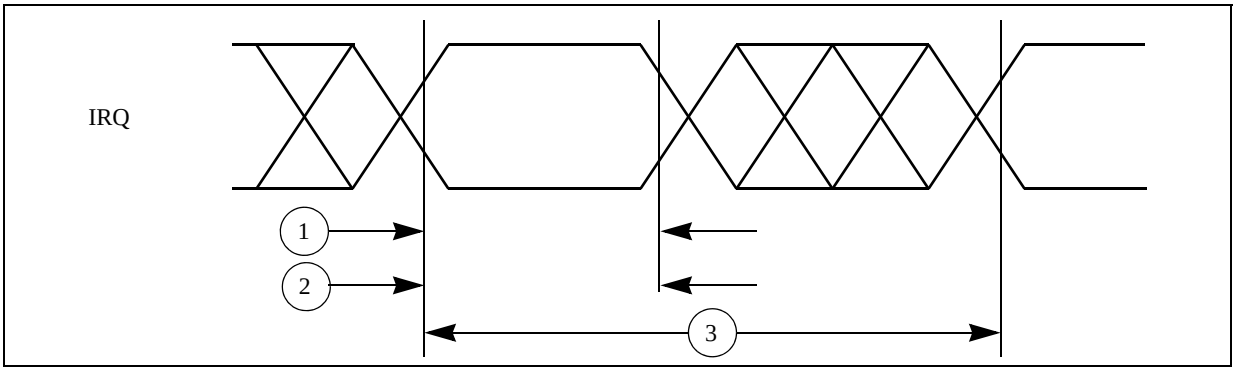
3.20.5 External interrupt timing (IRQ pin)

Table 38. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time(1)	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 29. External interrupt timing



3.20.6 DSPI timing

Table 39. DSPI timing

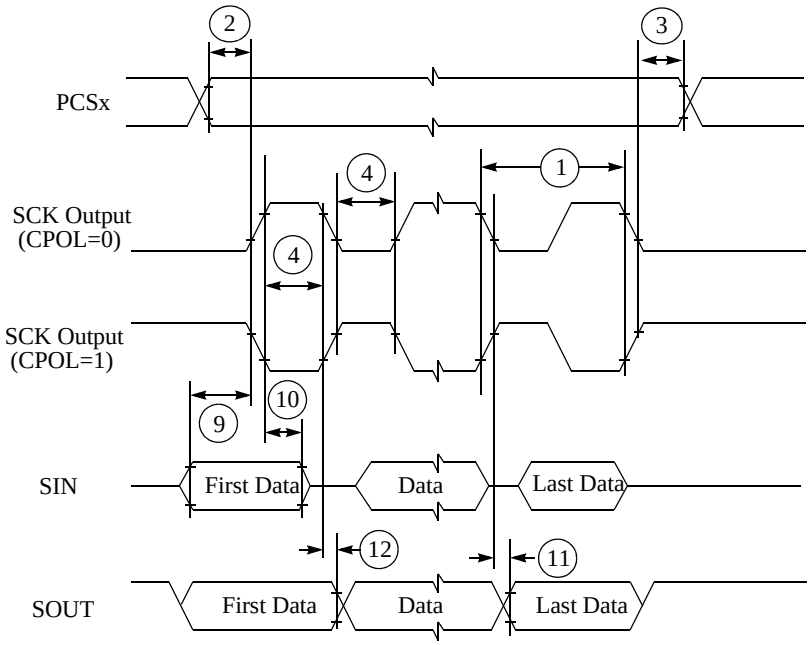
No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode(1)	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	t_{SCK}/2 - 10	t_{SCK}/2 + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	

Table 39. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

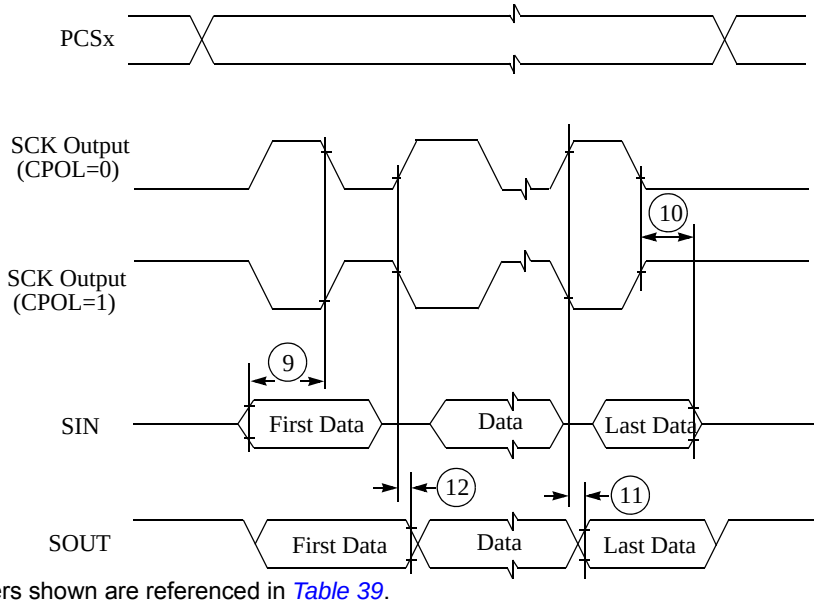
1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

Figure 30. DSPI classic SPI timing — master, CPHA = 0



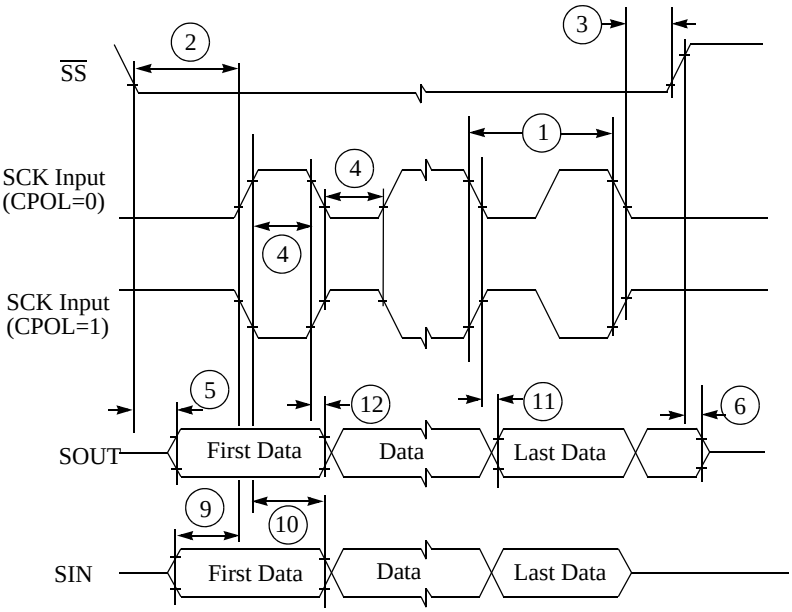
Note: The numbers shown are referenced in *Table 39*.

Figure 31. DSPI classic SPI timing — master, CPHA = 1



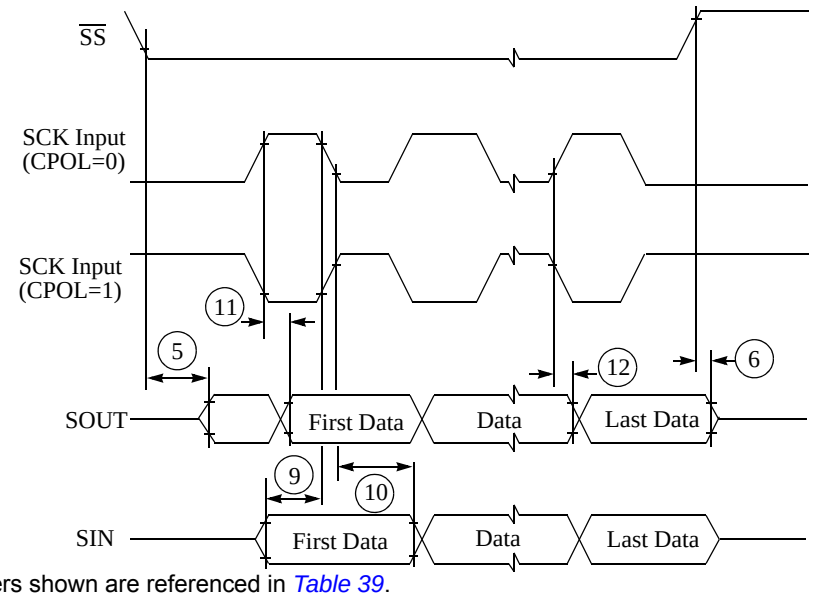
Note: The numbers shown are referenced in *Table 39*.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0



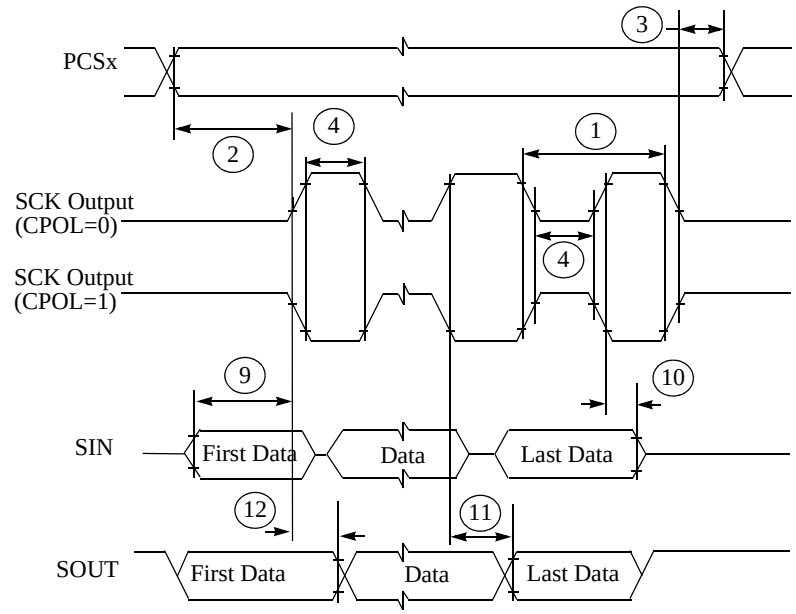
Note: The numbers shown are referenced in *Table 39*.

Figure 33. DSPI classic SPI timing — slave, CPHA = 1



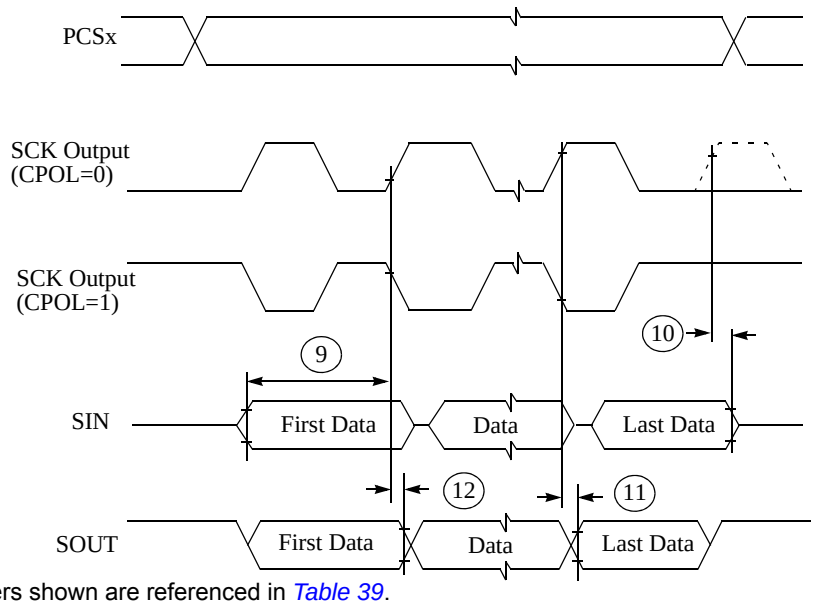
Note: The numbers shown are referenced in *Table 39*.

Figure 34. DSPI modified transfer format timing — master, CPHA = 0



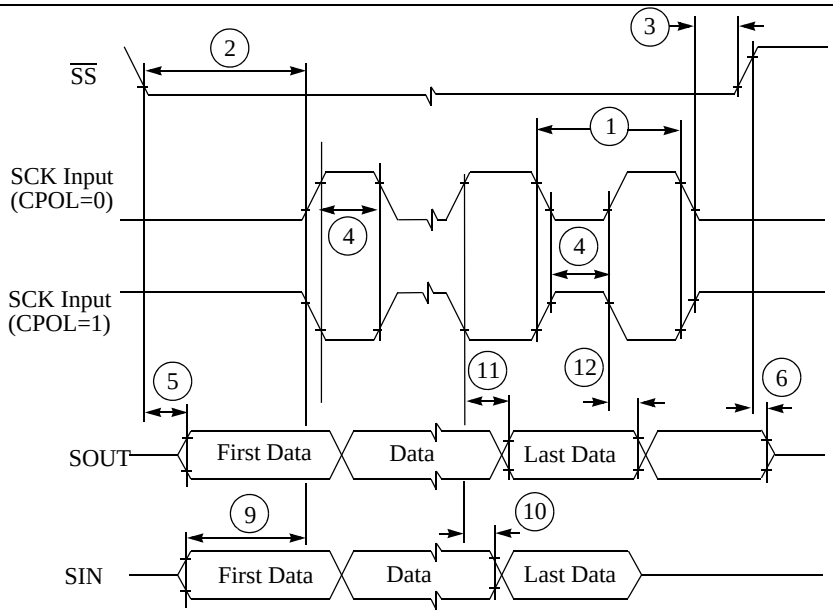
Note: The numbers shown are referenced in *Table 39*.

Figure 35. DSPI modified transfer format timing — master, CPHA = 1



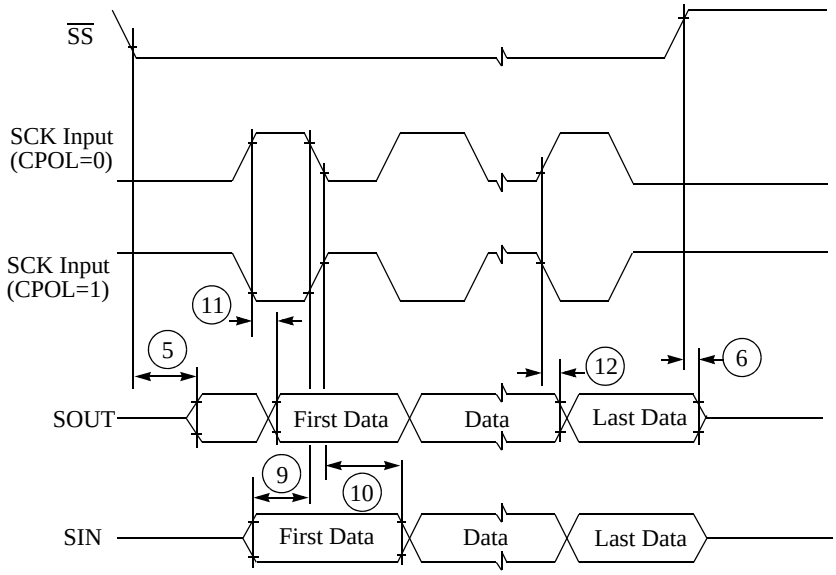
Note: The numbers shown are referenced in *Table 39*.

Figure 36. DSPI modified transfer format timing – slave, CPHA = 0



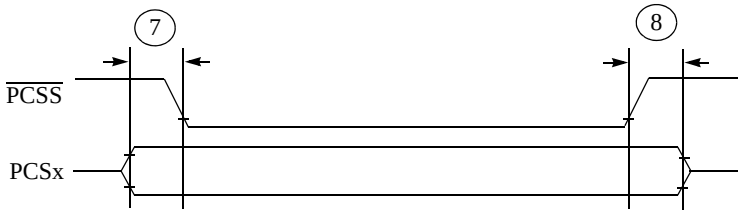
Note: The numbers shown are referenced in *Table 39*.

Figure 37. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 39*.

Figure 38. DSPI PCS strobe (PCSS) timing



Note: The numbers shown are referenced in *Table 39*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

Figure 39. LQFP100 package mechanical drawing

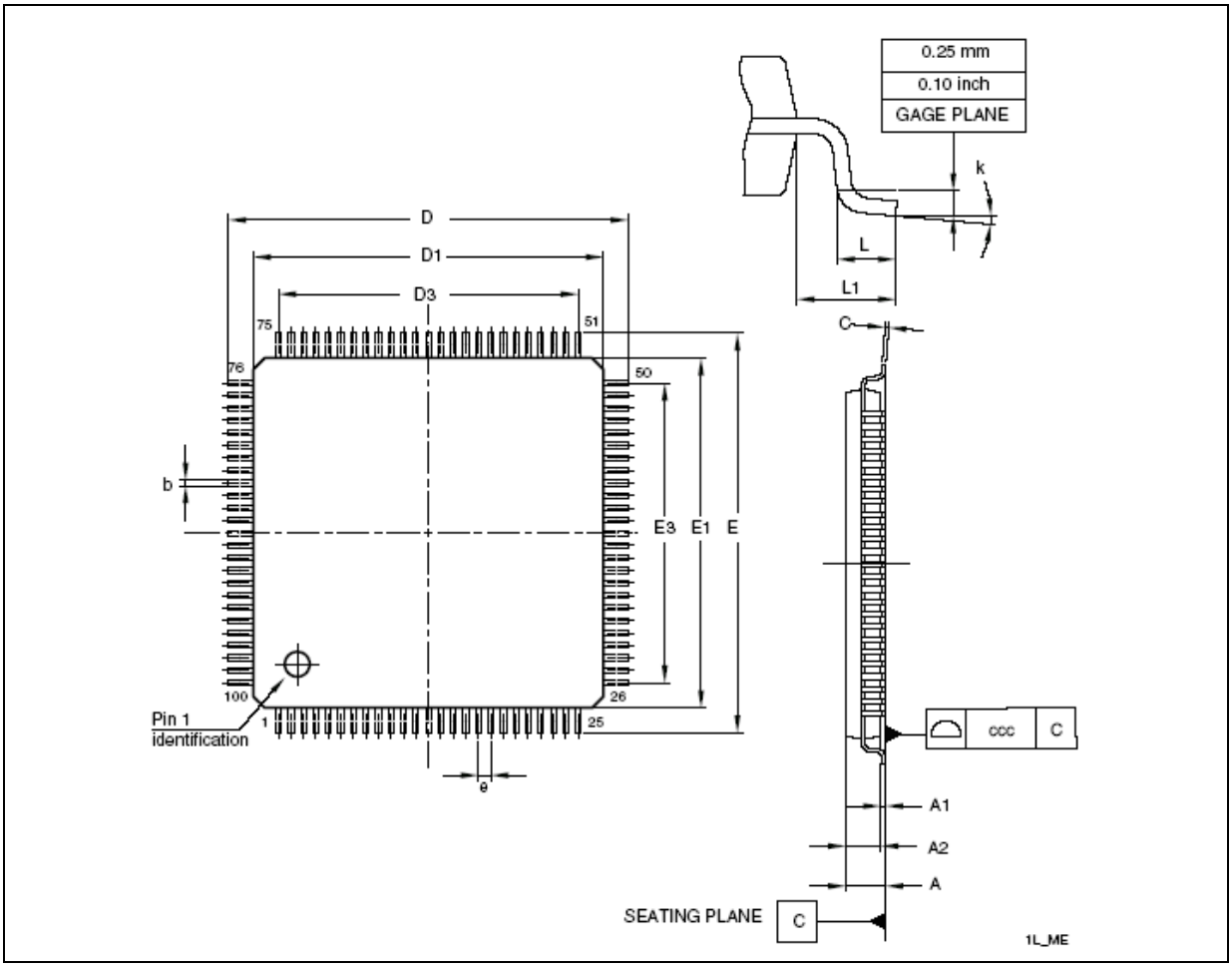


Table 40. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP144 package mechanical drawing

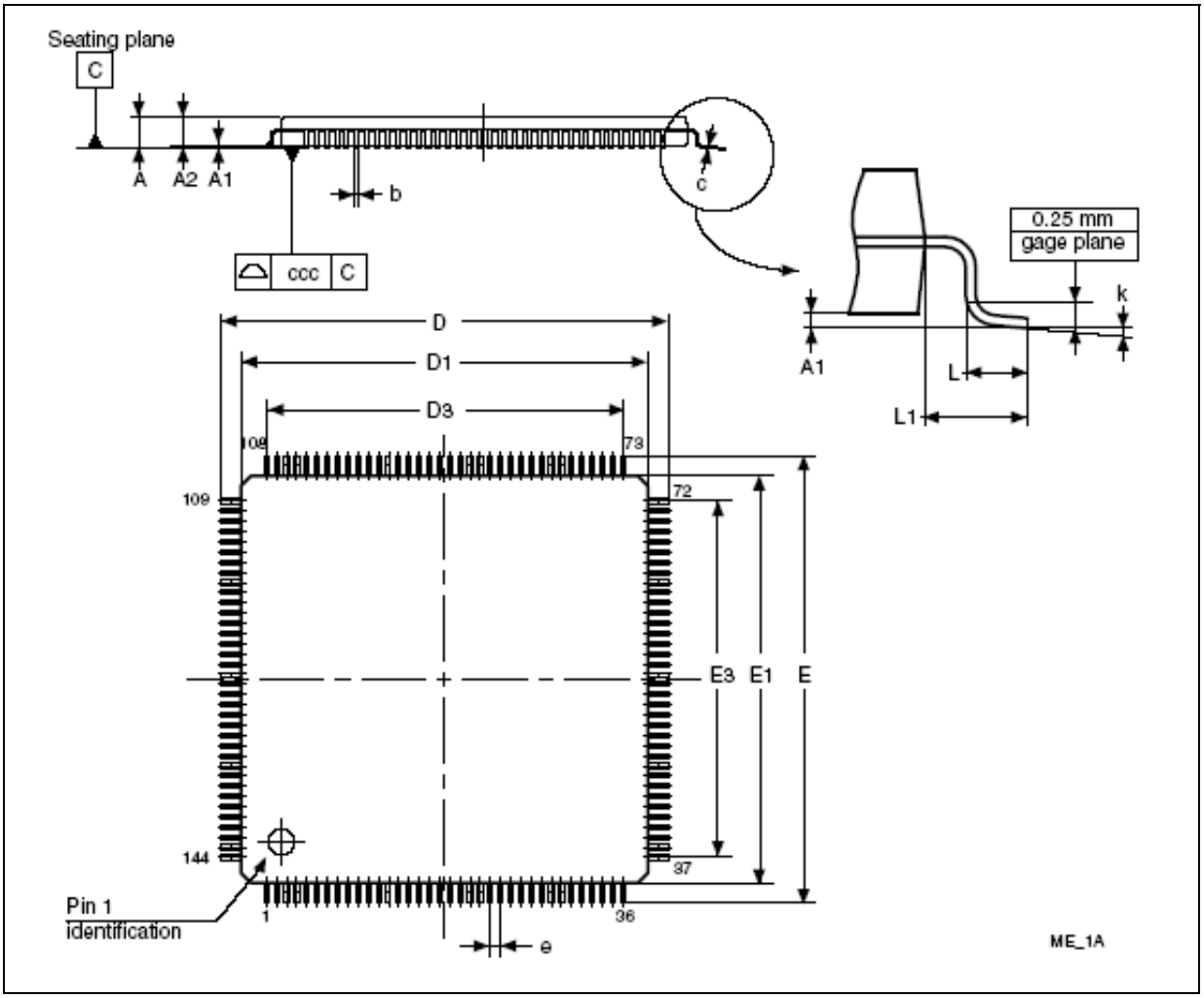


Table 41. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	—	—	1.6	—	—	0.0630
A1	—	0.05	0.15	—	0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c	—	0.09	0.2	—	0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5	—	—	0.6890	—	—
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 41. LQFP144 mechanical data (continued)

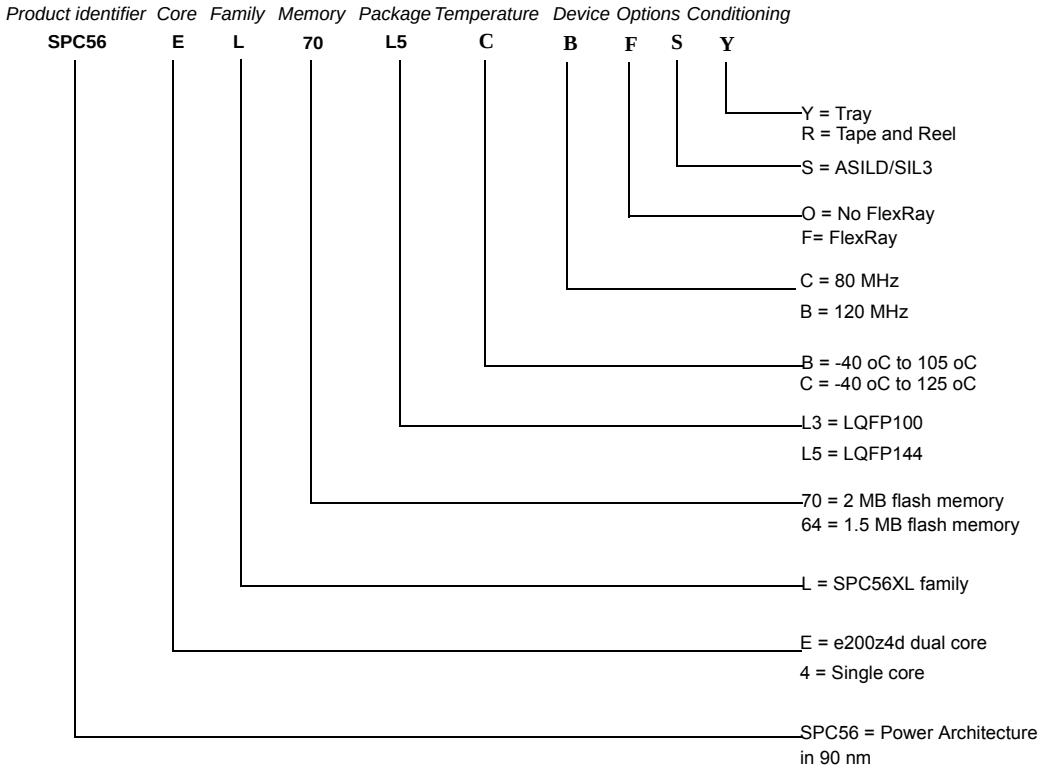
Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
E3	17.5	—	—	0.6890	—	—
e	0.5	—	—	0.0197	—	—
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1	—	—	0.0394	—	—
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
Tolerance	mm			inches		
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to four decimal digits.

5 Ordering information

Figure 41. Commercial product code structure(d)

Example code:



d. Not all configurations are available in the market. Please contact your ST Sales Representative, to get the list of orderable commercial part number.

6 Revision history

Table 42. Revision history

Date	Revision	Changes
23-Nov-2012	1	Initial release.
03-Sep-2013	2	Revision 2 changes: – Replaced IEC with ISO26262 in *Section 1.1: Document overview* – Updated *Section 3.15.1: Input Impedance and ADC Accuracy* - replaced fC by fS – *Table 6: System pins* - added footnote to RESET pin about weak pull down – Updated Equation 11 – Updated *Table 26: Flash memory program and erase electrical specifications* - Removed “Factory Average” column and updated the values in “Initial Max” column from rows 3 to 7 – Updated *Figure 41: Commercial product code structure* and added a note to the figure – Updated the following in *Table 8: Absolute maximum ratings*: Updated the “Max” column values Updated the table footnotes – Updated the following in *Table 9: Recommended operating conditions (3.3 V)*: Added table footnote “VDD_HV_ADRx must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail” Maximum values of $V_{DD_HV_REG}$, $V_{DD_HV_IOx}$, $V_{DD_HV_FLA}$, $V_{DD_HV_OSC}$, $V_{DD_HV_ADV}$ changed from “3.6” to “3.63” Min and max value of $V_{DD_HV_ADR0}$ and $V_{DD_HV_ADR1}$ changed from “4.5 to 5.5 or 3.0 to 3.6” to “4.5 to 5.5 or 3.0 to 3.63” – Updated the following values in *Table 18: Voltage regulator electrical specifications*: For “Combined ESR of external capacitor” min value is updated to “1” and max value is updated to “100” For “Main High Voltage Power - Low Voltage Detection, upper threshold” max value is updated as “2.93” Added row “Digital supply low voltage detector lower threshold” for condition “After a destructive reset initialization phase completion” Added row “Digital supply low voltage detector upper threshold” for condition “Before a destructive reset initialization phase” For row “Digital supply high voltage detector upper threshold”, condition “After a destructive reset initialization phase completion” min value is changed from “1.38” to “1.39”

Table 42. Revision history (continued)

Date	Revision	Changes
03-Sep-2013	2 (continued)	– Updated the following in *Table 19: DC electrical characteristics*: Added table footnote “The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx” Updated V_{OL_F} conditions from “I_{OL} = 1.5 mA” to “I_{OL} = 11 mA” Updated V_{OH_F} conditions from “I_{OH} = – 1.5 mA” to “I_{OH} = –11 mA” Updated I_{INJ} parameter from “DC injection current per pin” to “DC injection current per pin (all bi-directional ports)” For I_{IL} row, parameter “Input leakage current (all ADC input-only ports)” updated min value to “–0.25” and max value to “0.25” – For I_{IL} row, parameter “Input leakage current (shared ADC input-only ports)” updated min value to “–0.3” and max value to “0.3” – Updated the following in *Table 20: Current consumption characteristics*: Specified oscillator bypass mode and crystal oscillator mode Updated STOP and HALT mode values Added IDD_HV_PMU Updated footnote 3 – Updated *Table 24: RC oscillator electrical characteristics* – Updated the following in *Table 25: ADC conversion characteristics*: Changed t_{conv} to t_{eval} and minimum value is changed from “625” to “600” Table footnote 5 updated to “This parameter does not include the sample time T_{sample}, but only the time for determining the digital result”
17-Sep-2013	3	Updated disclaimer.
15-Oct-2013	4	Updated *Table 1*.
09-Jul-2015	5	Editorial and formatting changes throughout document. *Chapter 3: Electrical characteristics*: – In *Table 9: Recommended operating conditions (3.3 V)*, changed Max value from “3.6” to “3.63” for $V_{DD_HV_FLA}$ symbol. – Added *Section 3.4: Decoupling capacitors*. – *Figure 9: Input Equivalent Circuit*: changed “V_{DD}” to “V_{REF}” in Internal circuit scheme – In *Table 30: Pad AC specifications (3.3 V, IPP_HVE = 0)* updated footnote 1 and footnote 2. – Updated *Figure 12: Pad output delay* Updated Disclaimer.

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