# 6+2-Ch. multistandard audio decoder

## Technical Literature

### CUSTOM ATTRIBUTES

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**DOCUMENT HISTORY**

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AUTOMATIC OBSOLETE RPN WORKFLOW STARTED

**DOCUMENT APPROVAL**

| User | Function | Date |
|---|---|---|
| Camilleri Evelina | Document Controller | 12-Jun-2013 |

# STA310

## 6+2-CH. MULTISTANDARD AUDIO DECODER

**PRELYMINARY DATA**

## 1 FEATURES

- *DVD Audio* **decoder:**
    - *Meridian Lossless Packing* (*MLP*), with up to 6 channels,
    - Uncompressed LPCM with 1-8 channels,
    - Precision of up to 24 bits and sample rates of between 44.1 kHz and 192 kHz.
- *Dolby Digital* (*) **decoder:**
    - Decodes 5.1 *Dolby Digital Surround.*
    - Output up to 6 channels. downmix modes: 1, 2, 3 or 4 channels.
- **MPEG** -1 2- channel audio decoder, layers I and II.
- **MPEG-2 6-channel audio decoder, layer II.**
    - 24 bits decoding precision.
- **MP3 (MPEG layer III) decoder.**
- Accepts MPEG-2 PES stream format for: MPEG-2, MPEG-1, Dolby Digital and linear PCM.
- **Karaoke System.**
- **Prologic decoder.**
- **Downmix for Dolby Prologic compatible.**
    - A separate (2-ch) PCM output available for simultaneous playing and recording.
- Bitstream input interface: serial, parallel or SPDIF.
- SPDIF and IEC-61937 input interface.
- SPDIF and IEC-61937 output interface.
- PLL for internal PCM clock generation. frequencies supported: 44.1KHz family (22.05, 88.2, 176.4) and 48KHz family (24, 48, 96, 192).
- PCM: transparent, downsampling 192 to 96 Khz and 96 to 48kHz.
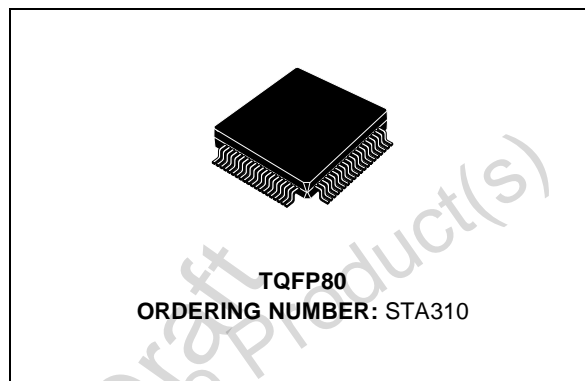- PTS handling control on-chip.
- **No external DRAM required**
- I$^2$C or parallel control bus
- Embedded *Development RAM* for customizable software capability.
- Configurable internal PLLs for system and audio clocks, from an externally provided clock.
- 80-PIN TQFP package



**TQFP80**
**ORDERING NUMBER:** STA310

- 2.5V (for core) and 3V (for I/O) power supply.
    - 3V Capable I/O Pads .
- True-SPDIF input receiver supporting AES/EBU, IEC958, S/PDIF.
    - No external chip required.
    - Differential or single ended inputs can be decoded.

## APPLICATIONS

- High-end audio equipment.
- DVD consumer players.
- Set top box.
- HDTV .
- Multimedia PC.

(*) **"Dolby ", "AC-3"** and **"ProLogic"** are trademarks of **Dolby Laboratories.**

## DESCRIPTION

The STA310 is a fully integrated Audio Decoder capable of decoding all the above listed formats.

Encoded input data can be entered either by a serial (I2S or SPDIF) or a parallel interface. A second input data stream (I2S) is available for micro input.

The control interface can be either **I$^2$C** or a parallel 8-bit interface. No external DRAM is necessary for a total of 35ms surround delays.

June 2003

This is preliminary information on a new product now in development. Details are subject to change without notice.

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## 2   STA310 AUDIO DECODER PIN DESCRIPTION

| Pin Number | Name | Type | Function |
|---|---|---|---|
| **CONTROL INTERFACES** | | | |
| 48 | IRQB | O [1] | Interrupt Signal (level), active low |
| 47 | SELI2C | I [2] | Selects the Control Interface (when high: serial interface; when low: parallel interface) |
| **I $^2$C Control Interface** | | | |
| 43 | SDAI2C | I/O [1] | I $^2$C Serial Data |
| 46 | SCLKI2C | I | I $^2$C Clock |
| 53 | MAINI2CADR | I [2] | Determines the slave address |
| **Parallel Control Interface** | | | |
| 78 - 79 - 80 - 1  2 - 3 - 6 - 7 | D0 - D1 - D2 - D3  D4 - D5 - D6 - D7 | I/O | Host Data |
| 12 - 13 - 14 - 15  16 - 18 - 19 - 20 | A0 - A1 - A2 - A3  A4 - A5 - A6 - A7 | I | Host Address |
| 21 | DCSB | I | Chip Select, active low |
| 22 | R/$\overline{W}$ | I | Read/Write Selection: read access when high, write access when low |
| 35 | WAITB | O [3] | Data Acknowledge, active low |
| **DATA INPUT INTERFACE** | | | |
| **First Serial Data Interface (I$^2$S)** | | | |
| 37 | DSTRB | I | Clock Input Data, active low |
| 41 | SIN | I | Serial Input Data |
| 40 | LRCLKIN | I | Word Clock for the Input |
| 42 | REQ | O | Handshake for the Data Transfer, aconfigurable by the SIN_SETUP register |
| **Second Serial Data Interface (I$^2$S)** | | | |
| 62 | DSTRB2 | I | Clock Input Data, active low |
| 60 | SIN2 | I | Serial Input Data |
| 61 | LRCLKIN2 | I | Word Clock for the Input |
| 63 | REQ2 | O | Handshake for the Data Transfer, active low |
| **DATA OUTPUT INTERFACES** | | | |
| 69 | PCMCLK | I/O | Oversampling Clock input for STA310 when generated externally |
| **DAC Interface** | | | |
| 67 | SCLK | O | Bit Clock for the DAC |

## 2    STA310 AUDIO DECODER PIN DESCRIPTION  (continued)

| Pin Number | Name | Type | Function |
|---|---|---|---|
| 68 | LRCLK | O | Word Clock for the DAC |
| 72 | PCM_OUT0 | O | Data from a Prologic downmix (VCR_L/VCR_R) |
| 73 | PCM_OUT1 | O | Data for the first DAC (Left/Right) |
| 76 | PCM_OUT2 | O | Data for the second DAC (Centre/Sub) |
| 77 | PCM_OUT3 | O | Data for the third DAC (LeftSur/RightSur) |
| **IEC958 Interface (S/PDIF) - One Output Port., One  Input Ports.** | | | |
| 58 | I958OUT | O | S/PDIF Signal |
| 25 | SPDP | I | First  differential input of S/P DIF port |
| 24 | SPDN | I | Second  differential   input of S/P DIF port |
| 26 | SPDF | I | External Filter |
| 28 | VDDA | I | Analog VDD for S/P DIF Input port |
| 29 | GNDA | I | Analog GND for S/P DIF Input port |
| **STATUS INFORMATION** | | | |
| **PCM Related Information** | | | |
| 54 | SFREQ | O | Then high, indicates that the sampling freq. is either 44.1Khz or 22.05Khz.<br>When low, indicates that the sampling frequency is either 32 Khz, 48 Khz, 24 Khz or 16Khz. |
| 57 | DEEMPH | O | Indicates if de-emphasis is performed. |
| **Audio Video Synchronization** | | | |
| 59 | PTSB | O | Indicates that a PTS has been detected, active low. |
| **Other Signals** | | | |
| 31 | CLK | I | Master Clock Input Signal. |
| 36 | RESET | I[2] | Reset signal input, active low. |
| 52 | TESTB | I[2] | Reserved pin: to be connected to VDD |
| 49 | SMODE | I | Reserved pin : to be connected to GND |
| **RS232 Interface** | | | |
| 8 | RS232RX | I | |
| 9 | RS232TX | O | |
| **PLLs INTERFACES** | | | |
| 64 | CLKOUT | O | System clock output with programmable division ratio |
| 27 | PLLAF | I | External Filter For Audio PLL. |

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## 2  STA310 AUDIO DECODER PIN DESCRIPTION  (continued)

| Pin Number | Name | Type | Function |
|---|---|---|---|
| 30 | PLLSF | I | External Filter For System PLL. |
| **Power  and Ground** | | | |
| 5 - 11 - 23 - 33 - 39 - 45 - 50 - 56 - 66 - 71 - 75 | GND | GND | Ground |
| 4 - 17 - 34 - 38 44 - 55 - 65  - 74 | VDD | VDD | 2.5V Power Supply |
| 10 - 32 - 51 - 70 | VDD3 | VDD3 | 3.3V Power Supply |

Notes   (1)  Open Drain
        (2)  Internal Pull-up
        (3)  Tri-State

**PIN CONNECTION** (Top view)



*D00AU1225*
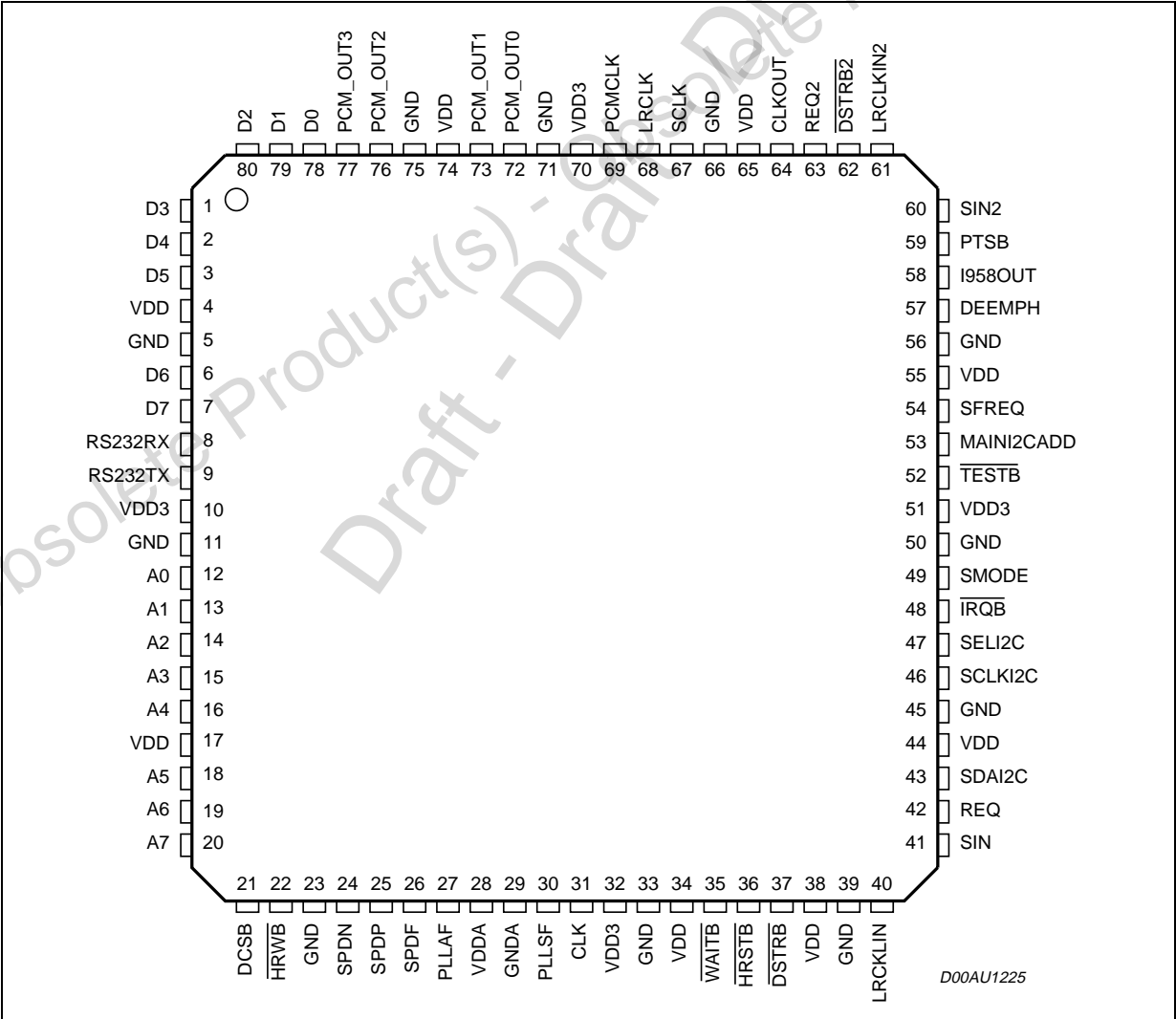
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### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameters | Value | Unit |
|--------|-----------|-------|------|
| Vdd | 2.5V Power Supply Voltage | -0.5 to 3.3 | V |
| | 2.5V Input or Output Voltage | -0.5 to (Vdd+0.5) | V |
| Vdd3 | 3.3V Power Supply Voltage | -0.5 to 4 | V |
| | 3.3V Input or Output Voltage | -0.5 to (Vdd+0.5) | V |

### ELECTRICAL CHARACTERISTICS ($V_{DD}$ = 3.3V +/-0.3V; $T_{amb}$ = 0 to 70°C; Rg = 50 $\Omega$ unless otherwise specified

| DC OPERATING CONDITIONS | | | |
|--------|-----------|-------|------|
| Symbol | Parameters | Value | Unit |
| Vcc | Power Supply Voltage | 2.5 | V |
| Tj | Operating Junction Temperature | -20 to 125 | °C |

### GENERAL INTERFACE

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit | Note |
|--------|-----------|-----------|-----|-----|-----|------|------|
| $I_{il}$ | Low level input current without pull-up device | Vi = 0V | | | 1 | μA | 1 |
| $I_{ih}$ | High level input current without pull-down device | Vi = Vdd | | | 1 | μA | 1 |
| $I_{oz}$ | Tri-state output leakage without pull-up/down device | Vi = 0V or Vdd | | | 1 | μA | 1 |
| $I_{latchup}$ | I/O Latch-up current | V<0V, V>Vdd | 200 | | | mA | 2 |
| Vesd | Electrostatic protection | Leakage <1μA | 2000 | | | V | 3 |

Note:   1.  The leakage currents are generally very small, <1nA. The value given here, 1μA, is a maximum that can occur after an Electrostatic Stress on the pin.
2.  V> Vdd3 for 3.3V buffers.
3.  Human Body Model

### LVTTL & LVCMOS DC Input Specification 2.7V <Vdd3 <3.6V

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit | Note |
|--------|-----------|-----------|-----|-----|-----|------|------|
| $V_{il}$ | Low level input voltage | | | | 0.8 | V | 1 |
| $V_{ih}$ | High level input voltage | | 2.0 | | | V | 1 |
| $V_{ilhyst}$ | Low level threshold input falling | | 0.8 | | 1.35 | V | 1 |
| $V_{ihhyst}$ | High level threshold input rising | | 1.3 | | 2.0 | V | 1 |
| $V_{hyst}$ | Schmitt trigger hysteresis | | 0.3 | | 0.8 | V | 1 |

Note:   1.  Takes into account 200mV voltage drop in both supply lines.
2.  X in the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability

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### ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Ipu | Pull-up current | Vi = 0V | | -66 | 0.8 | µA | 1 |
| Rpu | Equivalent Pull-up resistance | Vi = 0V | | 50 | | KΩ | |

Note: 1. **Min condition**: $V_{DD}$ = 2.7V, 125°C Min precess **Max condition:** $V_{DD}$ = 3.6V, -20°C Max

### POWER DISSIPATION

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| $P_D$ | Power Dissipation @$V_{DD}$ = 2.4V | Sampling frequecy ≤ 24KHz | | t.b.d. | | mW | 1 |
| | | Sampling frequecy ≤ 32KHz | | t.b.d. | | mW | 1 |
| | | Sampling frequecy ≤ 48KHz | | t.b.d. | | mW | 1 |

### INTRODUCTION

The STA310 is a fully integrated multi-format audio decoder. It accepts as input, audio data streams coded with all the formats listed above.
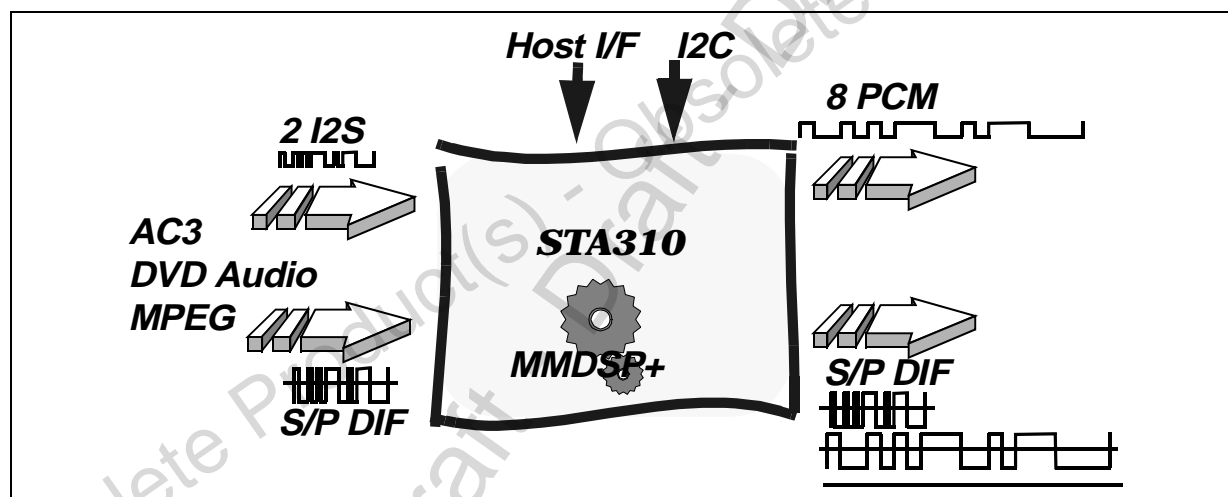


## 2.1 Inputs and Outputs

### 2.1.1 Data Inputs

- Through a parallel interface (shared with the control interface)
- Through a serial interface (for all the **I²S** formats)
- Through a S/P DIF (**SPDIF** or **IEC-61937** standards).

- Trough a second, independent,**I²S** (for application like i..e. Karaoke mixing).
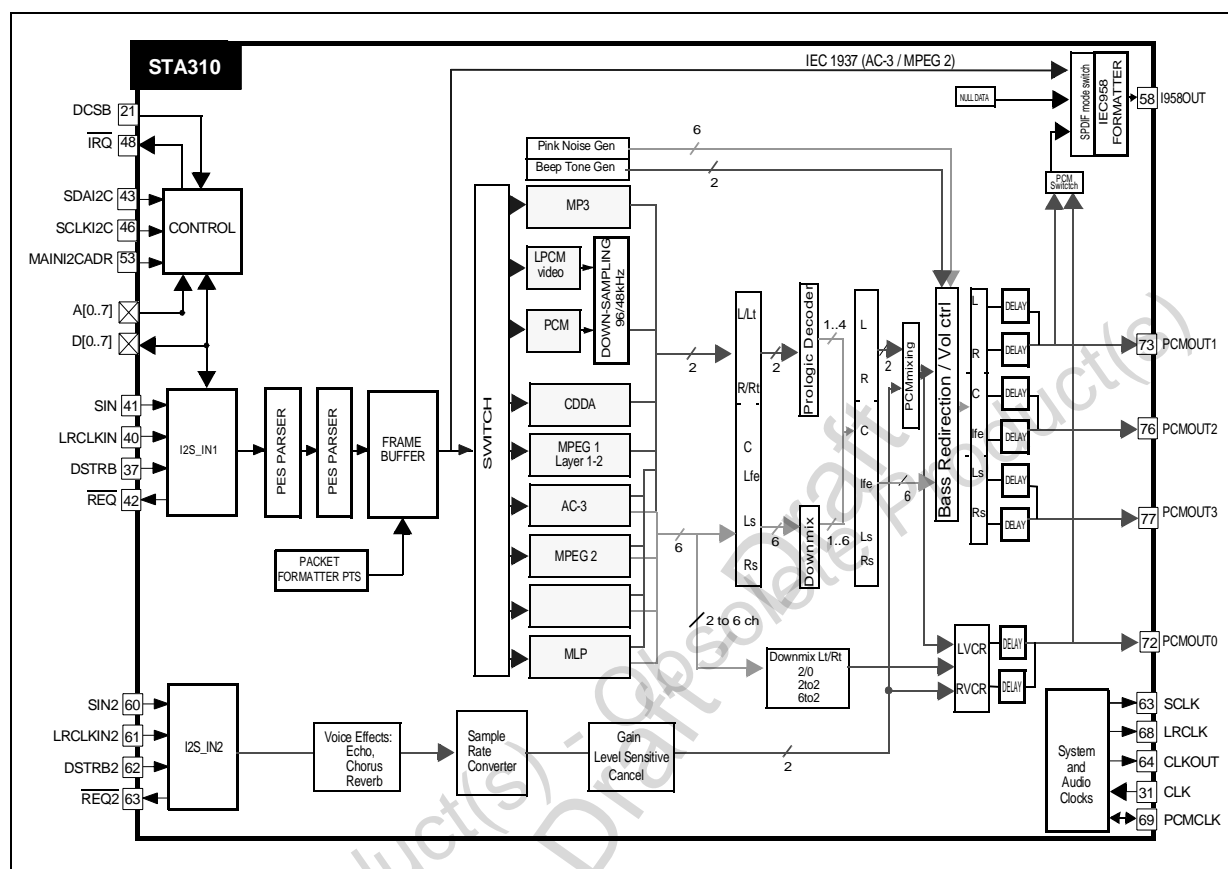
### 2.1.2 Data outputs

- The PCM audio oooutput interface, which provide:
  PCM data on 4 outputs:
  - Left/Right,
  - Centre/Subwoofer
  - Left Surround/Right Surround.

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• Data From a Prologic downmix (encoder)

"Lrclk" "Sclk" "PcmClk"

- S/P DIF Output

### 2.1.3 Control I/F

I2C slave or parallel interface:

The device configuration and the command issuing is done via this interface. To facilitate the contact with the MCU, 2 interrupt lines (IRQB and INTLINE) are available.

## 3    ARCHITECTURE OVERVIEW

### 3.1  Data flow

The STA310 is based on a programmable MMDSP+ core optimized for audio decoding algorithms.

Dedicated hardware has been added to perform specific operations such as bitstream depacking or IEC data formatting.

The arrows in Figure 3 indicate the data flow within the chip.

The compressed bitstream is input via the data input interface.

Data are transferred on a byte basis to the FIFO. This FIFO allows burst input data at up to 33Mbit/s.

The input processor, which is composed of a packet parser and an audio parser, unpacks the bitstream (Packet parser) and verifies the syntax of the incoming stream (audio parser).

The compressed audio frames with their associated information (PTS) are stored into the circular frame buffer.

While a second frame is stored in the circular frame buffer, the first frame is extracted by the audio core decoder which decodes it to produce audio samples.

The PCM unit converts the samples to the PCM format. The PCM unit controls also the channel delay buffer in order to delay each channel independently.

In parallel, the IEC unit transmits non compressed data or compressed data according to the selected mode. In the compressed mode, the data are extracted directly from the circular buffer and formatted according to the IEC-61937 standard. In non compressed mode, the left and right PCM channels formatted by the PCM unit are output by the IEC unit, according to the SPDIF standard

**Figure 1. Architecture and data flows**

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### 3.2  Functional diagram

**Figure 2. Audio decoder top level functional diagram**



### 3.3  Control interface description

The IC can be controlled either by a host using an I²C interface, or by a general purpose host interface.

These interfaces provide the same functions and are described in the following sections. The selection is performed by the means of the pin SELI2C: when high, this pin indicates that the I²C interface is used. When low, the parallel interface is used.

### 3.3.1  Parallel control interface

When the pin SELI2C is low, the control of the chip is performed through the parallel interface. When accessing the device through the parallel interface, the following signals are used:

-   The address bus A[7..0]. It is used to select one of the 256 register locations.
-   The data bus DATA[7..0]. If a read cycle is requested, the data lines D[7:0] will be driven by the IC. For a write cycle, the STA310 will latch the data placed on the data lines when the $\overline{\text{WAIT}}$ signal is driven high.
-   The signal R/$\overline{\text{W}}$. It defines the type of register access: either read (when high), or write (when low). Some registers can be either written or read, some are read only, some are write only.
-   The signal $\overline{\text{DCSB}}$. A cycle is defined by the assertion of the signal $\overline{\text{DCSB}}$.

Note:   1.  The address bus A[7..0], and read/write signal R/$\overline{\text{W}}$ must be setup before the $\overline{\text{DCSB}}$ line is activated.

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- The signal $\overline{\text{WAIT}}$. This signal is always driven low in response to the $\overline{\text{DCSB}}$ assertion.

The timing diagrams for the parallel control interface are given in *Electrical specifications* on page 5.

### 3.4  I²C control interface

When the pin SELI2C is high, the chip is controlled through the I²C interface. The I²C unit works at up to 400kHz in slave mode with 7-bit addressing.

- The Pin MAINI2CADR selects the device address. When MAINI2CADR is high the slave address is 0x5C, when low the device address is equal to the value on the address bus (A0...A6).
- The pin SDAI2C is the serial data line.
- The pin SCLKI2C is the serial clock.

The I²C Bus standard does not specify sub-addressing. There are thus potentially multiple ways to implement it. Any implementation that respects the standard is of course legal but a particular implementation is used by many companies. The following paragraphs describe this implementation.

#### 3.4.1  Protocol description

For write accesses only, the first data which follows the slave address is always the sub-address.

This is the one and only way to declare the sub-address. It should be noticed that the sub-address is implemented as a standard data on the I²C Bus protocol point of view. It is a sub-address because the slave knows that it must load its address pointer with the first data sent by the master.

See in the Appendix X.x for I²C message format examples.

### 3.5  Decoding process

The decoding process in the STA310 is done in several stages:

- Parsing,
- Main decoding,
- Post decoding,
- Bass redirection,
- Volume and Balance control.

Each of the stages can be activated or bypassed according to the configuration registers.

**Parsing**

The bitstream parsing (performed by the input processor) is in charge of discarding all the non audio information in order to transmit to the next stage (the circular frame buffer) only the audio elementary stream (AC3, MPEG1/2, LPCM, PCM, DVD Audio).

The parsing stage operates in two phases: the packet parser unpacks the stream, the audio parser checks the syntax of the bitstream.

**Main Decoding**

The input of this stage is an elementary stream, the outputs are decoded samples. The number of output channels is defined by the downmix register (1 channel up to 6 channels). For details, please refer to the description of the register.

The decoding formats currently supported are AC3, MPEG1 layers I and II, MPEG2 layer II, LPCM. It is necessary to select the appropriate stream format by configuring the registers STREAMSEL and DECODESEL before running the decoder.

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**Post Decoding**

The post decoding includes specific PCM processing: DC filter, de-emphasis filter, downsampling filter. These filters can be independently enabled or disabled through the register DWSMODE.

It provides also a Pro Logic decoder, which is described in detail in a next section.

**Bass Redirection**

This stage redirects the low frequency signals to the subwoofer.

The subwoofer is extracted from the other channels (L, R, C, Ls, Rs, LFe). There are six possible configurations to extract the subwoofer channel, which can be selected thanks to the OCFG register.

**Volume and Balance Control**

The volume is a master volume (no independent control for each channel). It is controlled by the PCMSCALE register, which enables to attenuate the signals by steps of 2dB.

Two balance controls are available: one for Left/Right channels, one for Left Surround/Right Surround channels. They are configurable by means of registers BAL_LR (Left-Right Balance) and BAL_SUR (Left Surround-Right Surround Balance), which provide attenuation of signals by steps of 0.5dB.

## 4   OPERATION

### 4.1   Reset

The STA310 can be reset either by a hardware reset or by a software reset:

- The hardware reset is sent when the pin $\overline{\text{RESET}}$ is activated low during at least 60ns. This is equivalent to a power-on reset.
  This resets all the configuration registers, i.e. PLL registers (PLLSYS, PLLPCM), Interrupt registers (INTE, INT, ERROR), interface registers (SIN_SETUP, CAN_SETUP) and command registers (SOFTRESET, RUN, PLAY, MUTE, SKIP_FRAME, REPEAT_FRAME).

- The software reset is sent when the register SOFTRESET is written to 1 (the register is automatically reset once the software reset is performed). It resets only the interrupt related registers (INTE, INT, ERROR) and the command registers (SOFTRESET, RUN, PLAY, MUTE, SKIP_FRAME, REPEAT_FRAME). All other decoding configurations are not changed by softreset.

Some information concerning the post-processing are anywayt of date after a soft-reset

Note:   1.   The chip must be soft reset before changing any configuration register.

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## 4.2  Clocks

There are two embedded PLLs in the STA310: the system PLL and the PCM PLL.

The following is the block diagram of the system and audio clocks used in the STA310
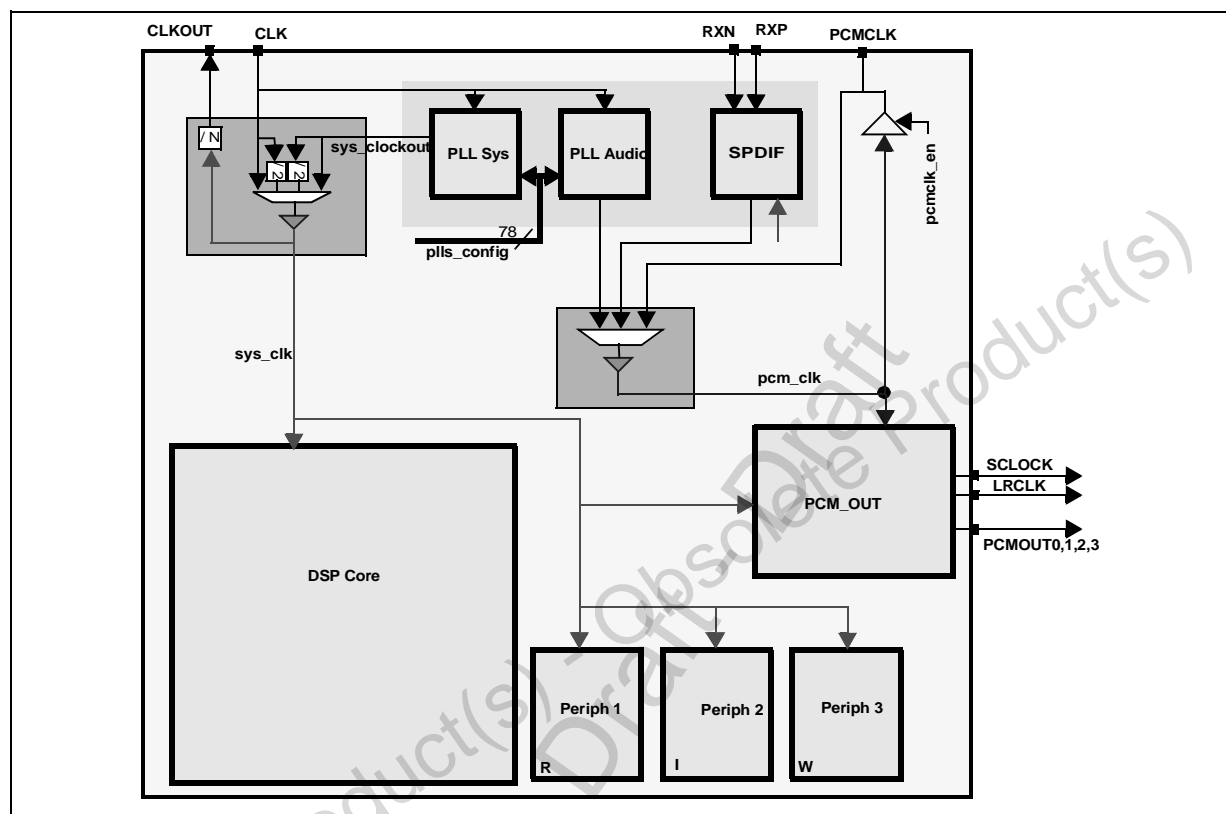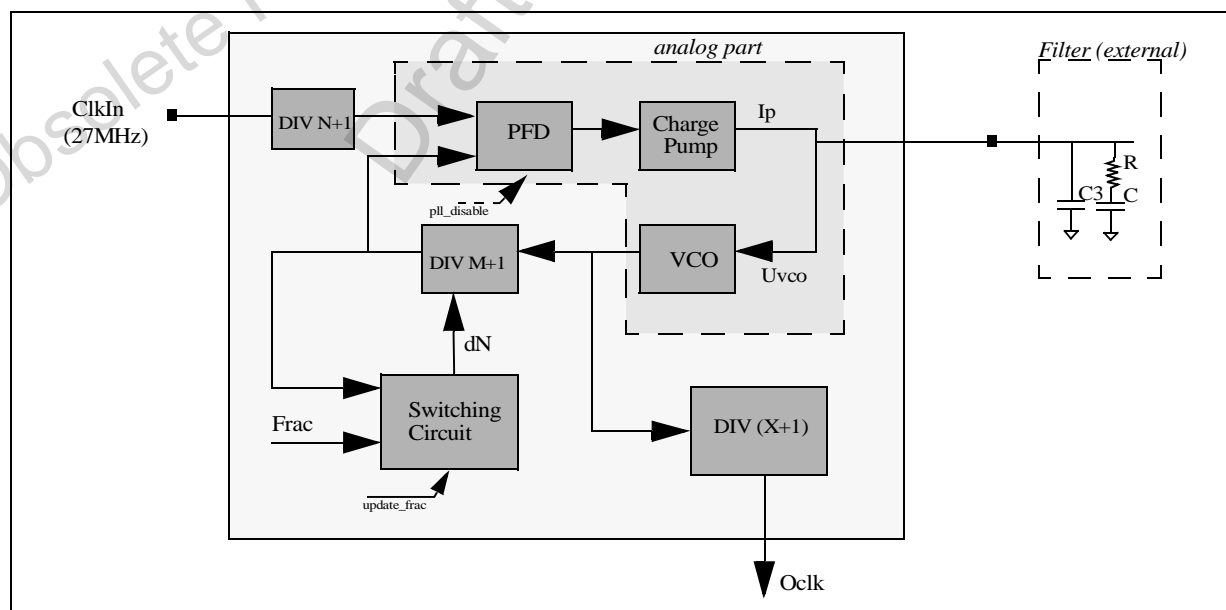
**Figure 3. PLL Block Diagram**



**Figure 4. Block Diagram of Functional PLL**

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### 4.2.1 System clock

The system clock sent to the DSP core and the peripherals can be derived from 4 sources and the selection is performed through an Host Register; external clock, external clock divided by 2, internal system PLL and internal system PLL divided by 2.

The system PLL is used to create the system clock from the input clock. This PLL is software programmable through the Host Registers mechanism. The system PLL is used to set the any frequency up to the maximum allowed device speed. After hard reset the system clock is running at 47.25MHz. An RC network must be connected to the filter Pin PLLSF.

The system clock is output on the pin CLKOUT after a programmable divider ranging from 1 to 16.

### 4.2.2 DAC clocks

#### 4.2.2.1 PCM clock

The PCM clock can be either input to the device or generated by the internal PLL or recovered by the embedded SPDIF receiver. The selection is done via the Host Registers.

After a hardware reset, the internal PLL is disabled and the PCMCLK pad is an input. PCMCLK may be equal to the PCM output bit rate, or it may be an integer multiple of this, allowing the use of oversampling D-A converters.

The internal fractional PLL is able to generate PCMCLK at any "FsX Oversampling Factor" frequencies, where Fs is any multiple or sub-multiple of the two 44.1kHz and 48kHz sampling frequencies. An RC network must be connected to the filter pin PLLAF; refer to External circuitry on page 9 for recommended values.

If the PCMCLK is recovered from the embedded SPDIF receiver, the only supported overampling frquency is 128 Fs.

#### 4.2.2.2 Bit clock SCLK

The PCM serial clock SCLK is the bit clock. It provides clocks for each time slot (16 cycles for each channel in 16-bit mode, 32 cycles for each channel in 18-, 20-, 24-bit modes). The frequency of SCLK is therefore fixed to 2 x Nb time slots x Fs, where Fs is the sample frequency.

The clock is derived from the clock PCMCLK. The register PCMDIVIDER must be configured according to the selected output precision and the frequency of PCMCLK, so that the device can construct SCLK:

Fsclk = Fpcmclk / (2 x (PCMDIVIDER+1)) gives

**Table 1.**

| PCM Divider Value | Mode Description |
|---|---|
| 5 | PCMCLK = 384 Fs, DAC is 16-bit mode |
| 3 | PCMLK = 256 Fs, DAC is 16-bit mode |
| 2 | PCMLK = 384 Fs, DAC is 32-bit mode |
| 1 | PCMLK = 256 Fs, DAC is 32-bit mode |

The value of PCMDIVIDER = 0 is reserved. If this number is loaded, the divider is bypassed and the frequency of SCLK equals the frequency of PCMCLK. The PCMDIVIDER register must be setup before the output of SCLK starts.

This can be done by first disabling PCM outputs, by de-asserting the MUTE and PLAY commands and then writing into the PCMDIVIDER register. Once the register is setup, the MUTE and/or PLAY commands can be asserted. PCMDIVIDER can not be changed "on the fly".

### 4.2.2.3 Word clock LRCLK

The frequency of LRCLK is given by:

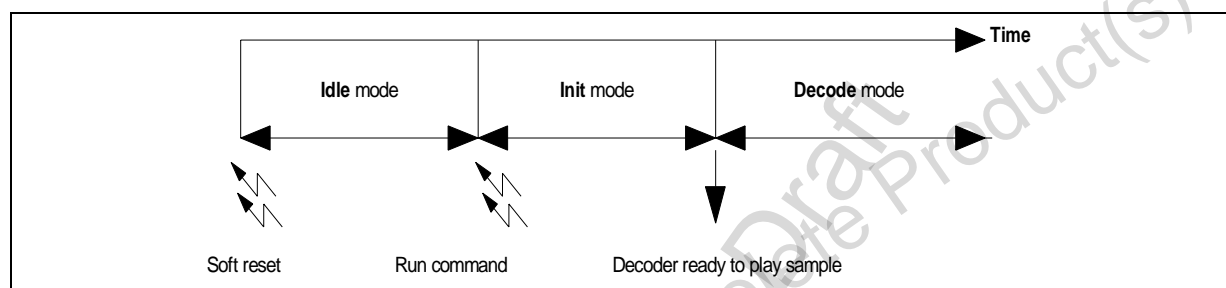- Flrclk = Fsclk/32; for 16 bit PCM output,
- Flrclk = Fsclk/64; for 18, 20 or 24 bits PCM output.

No special configuration is required. The polarity can be changed in the register PCMCONF, by setting up the field INV as needed.

### 4.3  Decoding states

There are two different decoder states: Idle state and decode state (see <Blue HT>Figure 3). To change states, register

**Figure 5. Decoding States**



### Idle Mode

This is the state entered after a hardware or software reset. In this state, the embedded DSP does not decode, i.e. no data are processed. The chip is waiting for the RUN command, and during this state all configuration registers must be initialized. In this state, even if the chip is not processing data, the DACs clocks can be output, which enables to setup the external DACs. Once the PCMCLK, SCLK and LRCLK clocks are configured, it is possible to output them by setting the MUTE register.I

**Table 2. Idle mode. play and mute commands effects**

| Play | Mute | Clock (SCLK, LRCLK) State | PCM Output |
|------|------|---------------------------|------------|
| X | 0 | Not running | 0 |
| X | 1 | Running | 0 |

Note:  1.  The PLAY command has no effect in this state as the decoder is not running. It can however be sent and it will be taken into account as soon as the decoder enters the decode state.

### Decode Mode

This state is entered after the RUN command has been sent (i.e. RUN register = 1). In this mode, the data are processed. The decoder can play sound, or mute the outputs, by using the PLAY and MUTE registers:

- To decode streams, the PLAY register must be set. When decoding, the sound will be sent to outputs if the MUTE register is reset. The outputs are muted if the MUTE register is set.

- To stop decoding, the PLAY register should be reset. Resuming decoding is performed by writing PLAY to 1 again

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**Table 3. Decode Mode. Play and Mute commands effects**

| Play | Mute | Clock State | PCM Output | Decoding |
|------|------|-------------|------------|----------|
| 0 | 0 | Not running | 0 | No |
| 0 | 1 | Running | 0 | No |
| 1 | 0 | Running | Decoded Samples | Yes |
| 1 | 1 | Running | 0 | Yes |

Note:  1.  It is not possible to change configuration registers in this state. It is necessary to soft reset the chip before. Only the following registers can be changed "on-the-fly": PCM_SCALE, BAL_LR, BAL_SUR, OCFG, DOWNMIX registers.

## 4.4 Data input interface description.

**Figure 6. Block Diagram of Data Flow**
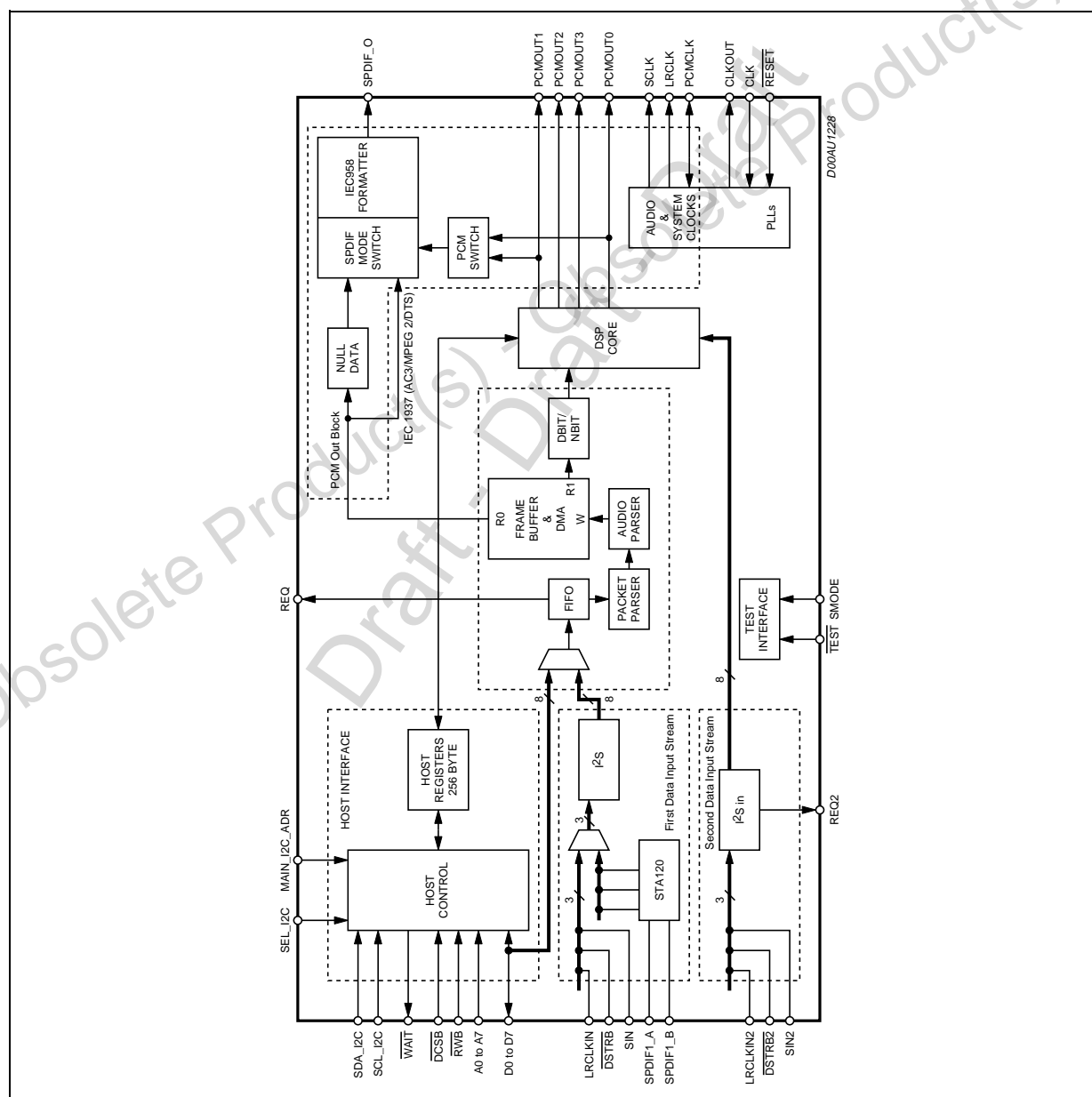
Two independent inputs are available on the STA310.

The main one allows to enter input data stream through through:

- A serial interface (referred to as Data Serial Interface),
- And a parallel interface (referred to as Data Parallel Interface).

The choice is performed by the register SIN_SETUP.

### 4.4.1  Data serial interface

When the serial mode is selected, the bitstreams can be entered into the STA310 through either:

- a four-signal data interface or ,
- trough a SPDIF input (no external circuit is required).

The four-signal data interface (see Figure 5) provides:

- An input data line SIN,
- An input clock $\overline{DSTR}$,
- A word clock input LRCLKIN
- And a hand-shake output signal $\overline{REQ}$.
-

Note:   1.  Only 16-bit PCM streams are supported. For 20-bit or 24-bit PCM, the 4 or 8 least significant bits are ignored

.

The specifications of those signals can be configured by the means of the register CAN_SETUP.

Two modes exist in serial mode, one that uses the LRCLKIN pin and one that does not use the LRCLKIN pin.

### 4.4.1.1  Modes without the LRCLKIN pin

In this mode the signal LRCLKIN is not used by the STA310. The input data SIN is sampled on the rising edge of $\overline{DSTR}$. When the STA310 input buffer is full the $\overline{REQ}$ signal is asserted. The polarity of $\overline{REQ}$ signal is programmable through the register SIN_SETUP. The data must be sent most significant bits first.

When the decoder cannot accept further data the $\overline{REQ}$ is de-asserted and the $\overline{DSTR}$ clock must be stopped as soon as possible to avoid data loss. After the $\overline{REQ}$ is de-asserted, the decoder is still able to accept data for a limited number of clock cycles.

The maximum number of data that can be transmitted with respect to the change of $\overline{REQ}$ is given by the following formula: Nbits = 23 - 6 * $F_{DSTR}$/33MHz, where: $F_{DSTR}$ is the $\overline{DSTR}$ clock frequency, (max is 33 MHz).

### 4.4.1.2  Modes using the LRCLKIN pin

When receiving data from an A/D converter or from an S/PDIF receiver, the signal LRCLKIN is used.

The LRCLKIN signal is used to make the distinction between the left and right channels. Any edge of the LRCLKIN signal indicates a word boundary.

The data transfer between the input interface and the FIFO is done on a byte basis. After the edge (rising or falling) of the LRCLKIN, a new byte is transferred to the first stage of the STA310 every 8 $\overline{DSTR}$ clock cycles.

If the number of time slots is not a multiple of 8, the remaining data is lost. The polarity of LRCLKIN and $\overline{DSTR}$ is programmable.

The LRCLKIN can be delayed by one time slot, in order to support PCM delayed mode. All these configurations are programmable through the CAN_SETUP register.

The register CAN_SETUP has 4 significant bits, and each bit has a specific meaning, see *CAN_SETUP* on page 41.

Only the first byte is transferred to the STA310 because the number of time slots is 12 (8 + 4). SIN and LRCLKIN are sampled on the falling edge of DSTR In this case SIN_SETUP = 3 and CAN_SETUP = LeftFirstChannel + FallingStrobe + AllSlot = 2 + 4 + 8 = 14

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**Table 4.**

|  | **When Set** | **When Clear** | **Name** |
|---|---|---|---|
| Bit 0 | The input data is one slot delayed with respect to LRCLKIN | The input data is not delayed | DelayMode |
| Bit 1 | First channel when LRCLKIN is set | First channel when LRCLKIN is reset | LeftFirstChannel |
| Bit 2 | Data are sampled on falling edge of DSTR | Data are sampled on rising edge of DSTR | FallingStrobe |
| Bit 3 | All the bytes are extracted | Only the first 16 data bits are extracted | AllSlot |

**Figure 7.**
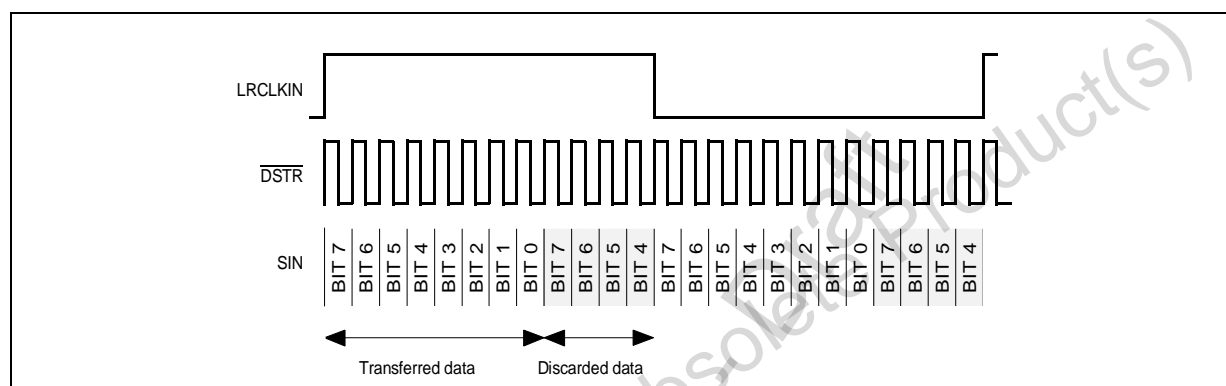


Example 2: Only the first 2 bytes are transferred to the STA310 because the number of slots is 20 (16 + 4). SIN and LRCLKIN are sampled on the falling edge of DSTR. The data is in delayed mode.

The register configuration is SIN_SETUP=3 and CAN_SETUP = DelayMode + LeftFirstChannel + FallingStrobe + AllSlot = 1 + 2 + 4 + 8 = 15.

This mode is a specific mode where only the first 16 data bits are transferred. The remaining bits are discarded.

The register configuration is SIN_SETUP = 3 and CAN_SETUP = DelayMode + FallingStrobe = 1 + 4 = 5.

#### 4.4.1.3 SPDIF Input

A true SPDIF Input **SPDIF** (PCM audio samples) or **IEC-61937** (compressed data) is selectable as a main serial input.

#### 4.4.1.4 Autodetected formats

The STA310 cut 2.0 is able the following audio format changes on the s/pdif input

**Table 5. Audio Format detection**

| BEFORE | AFTER |
|---|---|
| AC3 | PCM |
| AC3 | MPEG |
| MPEG | AC3 |
| MPEG | PCM |
| PCM | AC3 |
| PCM | MPEG |

### 4.4.1.5 Second Input

A second independent input allows to input bitstreams in serial mode.

This second input can be used, to input audio stream from a microphone, while we decode a data stream trough the main input.

### 4.4.2 Data parallel interface

Two ways are available to input data in parallel mode:

- Either through the parallel data bus, shared with the external controller,
- Or through the DATAIN register

### 4.4.2.1 Using the parallel data bus

In this mode the data must be presented on the 8-bit parallel host data bus D[7..0]. Note that this bus is shared with the external controller. On the rising clock of $\overline{DSTR}$ the data byte is sampled by the STA310. The signal $\overline{REQ}$ is used to signal when the input FIFO is full. When $\overline{REQ}$ is de-asserted the transfer must be stopped to avoid data loss.

After the $\overline{REQ}$ is de-asserted, the decoder is still able to accept data for a limited number of clock cycles.

The maximum number of data that can be transmitted with respect to the change of $\overline{REQ}$ is given by the following formula: Nbits = 23 - 6 * $F_{DSTR}$/33MHz, where: $F_{DSTR}$ is the $\overline{DSTR}$ clock frequency, (max is 33 MHz).

The signals $\overline{DSTR}$ and $\overline{DCSB}$ are used to make the distinction between Stream Data (strobed by $\overline{DSTR}$) and Control Data (strobed by $\overline{DCSB}$). To avoid conflicts, the $\overline{DSTR}$ signal and the $\overline{DCSB}$ signal must respect given timing constraints.

### 4.4.2.2 Using the DATAIN register

The data can be input by using the control parallel interface as if accessing any other register.

The signal $\overline{DCSB}$ is therefore used. When using this register to input data stream, there is no need to byte-align the data.

**Figure 8.**

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**Figure 9.**



### 4.5 Streams parsers

The parsing stage is operated by two parts: the packet parser and the audio parser.

The packet parser unpacks stream, sorts packets and transmit data to the audio parser. The audio parser verifies the stream syntax, extracts non-audio data and sends audio data to the frame buffer.

**Packet parser**

Before unpacking packets and transmitting data, the packet parser needs to detect the packet start by recognizing the packet synchronization word. It is possible to force the parser to search for two packet synchronization words before starting to unpack and transmit.

This is done by setting the register PACKET_LOCK to 1. Otherwise, the packet parser will start handling the stream once it has detected information matching the packet synchronization word.

The packet parser is also able to perform selective decoding: it can decode audio packets that are matching a specified Id. This Id is specified in AUDIO_ID and AUDIO_ID_EXt registers, and the function is enabled by setting the AUDIO_ID_EN register.

**Audio parser**

The audio parser needs to detect the audio synchronization word corresponding to the type of stream that must be decoded. It is possible to force the audio parser to detect more than one synchronization word before parsing.

This is done by setting the SYNC_LOCK register to a value between 1 and 3 - number of supplementary sync words to detect before considering to be synchronized.

The status of synchronization of both parsers is provided in the register SYNC_STATUS. Each time the synchronization status of one of the two parsers changes, the interrupt SYN is generated (if enabled) and the status can be read in SYNC_STATUS.

### 4.6 Decoding modes

#### 4.6.1 AC-3

The STA310 is Dolby Digital certified for class A products. The decoder must be programmed so to specify the stream format as AC-3 encoded: register DECODESEL = 0.
In the sections below are provided the modes specific to the AC-3 decoding.

#### 4.6.1.1 Compression modes

Four compression modes are provided in the STA310:

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- Custom A (also named custom 0 in Dolby specifications),
- Custom D (also named custom 1 in Dolby specifications),
- Line mode,
- RF mode.

These modes refer to different implementation of the dialog normalization and dynamic range control features. The mode is selected by programming the register COMP_MOD to the appropriate value.

**Line Mode**

In Line Mode (COMP_MOD = 2), the dialog normalization is always enabled. It is done by the decoder itself and the dialog is reproduced at a constant level.

The dynamic range control variable encoded in the bitstream is used and can be scaled by the two scaling registers HDR (for high-level cut compression) and LDR (for low-level boost compression). In case of 2/0 downmix, the high-level cut compression is not scalable.

**RF Mode**

In RF Mode (COMP_MOD=3), the dialog normalization is always performed by the decoder. The dialog is reproduced at a constant level.

The dynamic range control and heavy compression variables encoded in the bitstream are used, but the compression scaling is not allowed. This means that the HDR and LDR registers can not be used in this mode. A +11dB gain shift is applied on the output channels.

**Custom A Mode**

In Custom A mode (COMP_MOD=0), the dialog normalization is not performed by the decoder and must be done by another circuit externally.

The dynamic range control variable encoded in the bitstream is used and can be scaled by the two scaling registers HDR (for high-level cut compression) and LDR (for low-level boost compression).

**Custom D Mode**

In Custom D mode (COMP_MOD=1), the dialog normalization is performed by the decoder. The dynamic range control variable encoded in the bitstream is used and can be scaled by the two scaling registers HDR (for high-level cut compression) and LDR (for low-level boost compression).

### 4.6.1.2 Karaoke mode

The AC-3 decoder is karaoke aware and capable.

A karaoke bitstream can be composed of 5 channels: L for Left, R for Right, M for guide Melody, V1 for vocal track 1 and V2 for Vocal track 2.

- When in karaoke aware mode, the channels L,R and M are reproduced, and the channels V1 and V2 are reproduced at a level fixed by the bitstream.
- When in karaoke capable mode, it is possible to choose to reproduce one, two or none of the two incoming vocal tracks, V1 and V2.

The karaoke decoder is activated by the use of KARAMODE register, which specifies the downmix for the different modes. This register replaces DOWNMIX register. It is however possible to consider the incoming karaoke channels as any other multichannel stream and output it with a downmix specified in DOWNMIX register. For details, refer to the Digital Audio Compression AC-3 ATSC standard, annex C.

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### 4.6.1.3 Dual Mode

The Dual Mode corresponds to a mode where two completely independent mono program channels (e.g. bilingual) are encoded in the bitstream, referenced to as channel 1 and channel 2.

The possible ways to output channels on left/right outputs are:

- Output channel 1 on both L/R outputs,
- Output channel 2 on both L/R outputs,
- Mix channels 1 and 2 to monophonic and output on both L/R,
- Output channel 1 on Left output, and channel 2 on Right output.

This channels downmix is specified in the register DUALMODE.

### 4.6.2 MPEG

The STA310 is able to decode MPEG-1 layerI and layerII encoded data, as well as MPEG-2 layer I, layer II data without extension (i.e. 2-channel streams).

The MPEG input format should be specified in the DECODESEL register:

- DECODESEL=1 for MPEG1. The MC bit in MC_OFF register should be set.
- DECODESEL=2 for MPEG2. The MC bit in MC_OFF register should be set.

### 4.6.3 MP3

The STA310 is able to decoder MPEG2 layer III (MP3) data.

The MP3 input format aboved be specified in the DECODESEL register:

- DECODESEL=9 for MP3.

### 4.6.3.1 Dual Mode

The Dual Mode corresponds to a mode where two completely independent mono program channels (e.g. bilingual) are encoded in the 2-channel incoming bitstream, referenced to as channel 1 and channel 2.

The audio decoder allows to:

- Output channel 1 on both L/R outputs,
- Output channel 2 on both L/R outputs,
- Mix channels 1 and 2 to monophonic and output on both L/R,
- Output channel 1 on Left output, and channel 2 on Right output.

The output configuration is chosen by special downmix for dual mode through register MPEG_DUAL.

### 4.6.3.2 Decoding flow
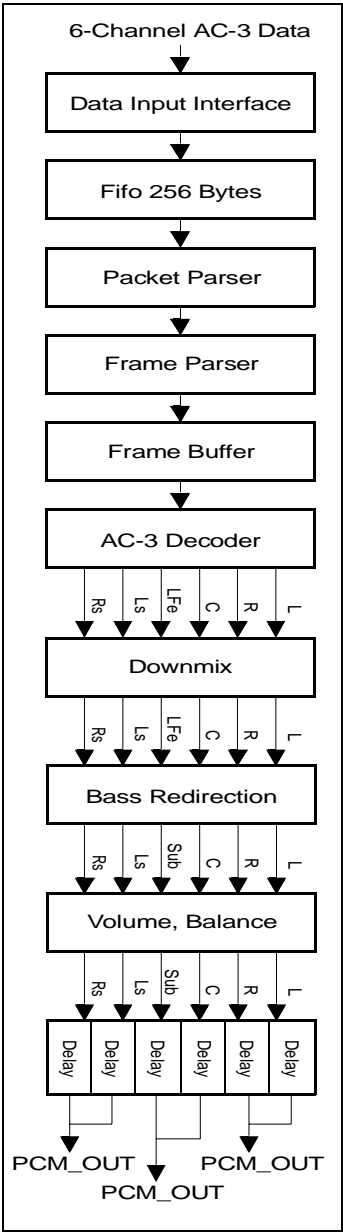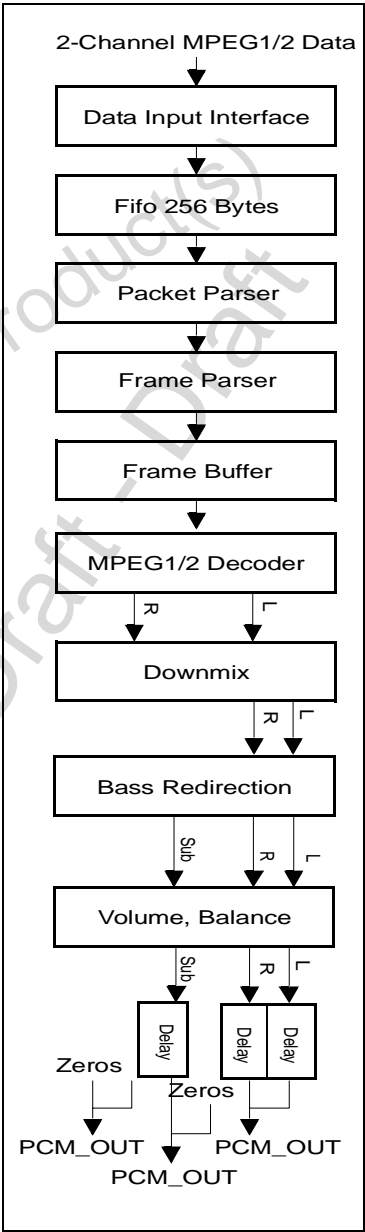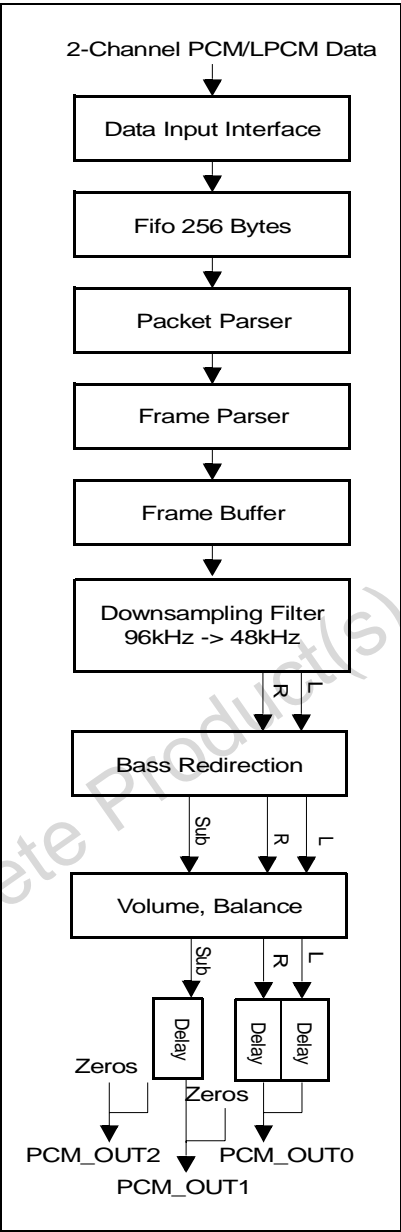
**Figure 10. AC-3 Decoding Flow**



6-Channel AC-3 Data → Data Input Interface → Fifo 256 Bytes → Packet Parser → Frame Parser → Frame Buffer → AC-3 Decoder → Downmix → Bass Redirection → Volume, Balance → Delay → PCM_OUT / PCM_OUT / PCM_OUT

**Figure 11. MPEG Decoding Flow**



2-Channel MPEG1/2 Data → Data Input Interface → Fifo 256 Bytes → Packet Parser → Frame Parser → Frame Buffer → MPEG1/2 Decoder → Downmix → Bass Redirection → Volume, Balance → Delay → Zeros → PCM_OUT / PCM_OUT / PCM_OUT

### 4.6.4 PCM/LPCM

The decoder supports PCM (2-channels) and LPCM Video (8-channels) and Audio (6-channels) streams. This is selected by DECODESEL=3.

### 4.6.4.1 Downsampling filter

When decoding PCM/LPCM streams encoded at 96kHz, it is possible to use a filter that downsamples the stream from 96kHz to 48kHz. The chip can not output streams at 96kHz. The register DWSMODE is used to configure the use of this filter.

**Figure 12. PCM/LPCM Decoding flow**



2-Channel PCM/LPCM Data → Data Input Interface → Fifo 256 Bytes → Packet Parser → Frame Parser → Frame Buffer → Downsampling Filter 96kHz -> 48kHz → Bass Redirection → Volume, Balance → Delay → Zeros → PCM_OUT2 / PCM_OUT1 / PCM_OUT0

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### 4.6.5 MLP

MLP is a lossless coding system for use on digital audio data originally represented as linear PCM. MLP is mandatory in DVD Audio. It allows transmission and storage of up to 6 channels. each up to 24 bits precision and with sample rates between 44.1 KHz and 192KHz.

- DECODESEL = 8

### 4.6.6 CDDA

- DECODESEL = 5

### 4.6.7 Beep Tone

- DECODESEL = 7

### 4.6.8 Pink noise generator

The pink noise generator can be used to position the speakers in the listening room so to benefit of the best listening conditions.

The decoder must be programmed so to generate pink noise by writing 4 in the DECODESEL register. The DOWNMIX register is used to select independently the channels on which the pink noise will be output.

When generating pink noise, the output configuration should be: OCFG=0 and PCM_SCALE=0.

**Figure 13. Pink Noise Generator Flow**
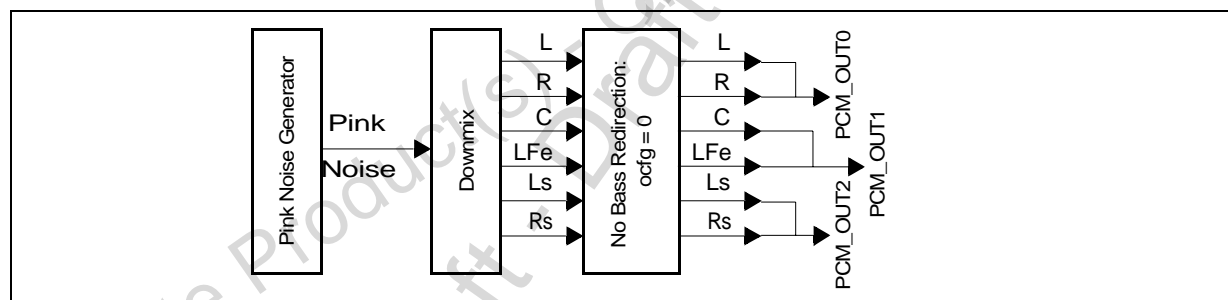


### 4.7  Post Processing
The following post processing alghorithms are available

### 4.7.1  Prologic

**Pro Logic Compatible Downmix**

The STA310 can decode an AC-3 multichannel bitstream and encode it to provide a 2-channel Pro Logic compatible output (Lt, Rt). These 2 channels are the result of a specific downmix referred to as Pro Logic compatible. This downmix is selected by the register DOWNMIX. The 2 channels can be used as the input of a Pro Logic decoder and player (e.g. home theatre).

**Pro Logic Decoding**

The STA310 can decode a 2-channel Pro Logic bitstream. The 2 channels could come from a CD player, an AC-3 2-channel bitstream or an MPEG1 bitstream. The 2-channel bitstream can be converted into a 4-channel output (L, R, C, S). The surround (S) is simultaneously sent on Ls and Rs channels. A Pro Logic downmix en-

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ables to configure which channels to output on PCM data. This is done through the register PL_DWN.

An auto-balance feature is available and activated through PL_AB register. The delay on surround channel is configurable thanks to the LSDLY register (while resetting the RSDLY register).

The bass redirection is performed after the Pro Logic decode. The same bass redirection configuration than those available in non-Pro Logic modes can be used except that the surround channels will not be added to the bass redirection. In the case of AC-3 or MPEG the STA310 is therefore capable of first decoding the AC-3 or MPEG stream then performing the Pro Logic decode.

### 4.7.2 Others

- Karaoke system
- Bass Management + Volume Control
- Deemphasis
- DC Remove

### 4.8 How to choose a decoder

To set up the device you have to select two registers.

The first one is DECODESEL for Audio data type,

The second one is STREAMSEL for Transport data type,

The STREAMSEL can be set-up as follows:

    0= PES
    1= PES DVD Video
    2= Packet MPEG1
    3= Elementary stream or IEC.60958
    4= reserved
    5= IEC.61937
    6= PES DVD Audio

So the possible configurations on listed in the following table:

**Table 6. Possible configurations:**

| STREAMSEL | DECODESEL | MODE |
|-----------|-----------|------|
| 0 | 0 | MPEG2 PES carrying Dolby Digital (ATSC) |
| 0 | 1 | MPEG2 PES carrying MPEG1 frames |
| 0 | 2 | MPEG2 PES carrying MPEG2 frames |
| 1 | 0 | MPEG2 PES carrying Dolby Digital frames for DVD Video |
| 1 | 2 | MPEG2 PES carrying MPEG2 frames for DVD Video |
| 1 | 3 | MPEG2 PES carrying Linear PCM frames for DVD Video |
| 1 | 1 | MPEG1 packet carrying MPEG1 frames |
| 3 | 0 | Dolby Digital frame elementary streams |
| 3 | 1 | MPEG1 frame elementary streams |
| 3 | 2 | MPEG2 frame elementary streams |
| 3 | 3 | Stereo PCM (16bits samples) |
| 3 | 4 | Pink Noise Generator |

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| STREAMSEL | DECODESEL | MODE |
|---|---|---|
| 3 | 5 | CDDA frames |
| 3 | 7 | Beep Tone Generator |
| 3 | 9 | MP3 frame elementary streams |
| 5 | 0 | IEC61937 Input with Dolby Digital frames |
| 5 | 1 | IEC61937 Input with MPEG1 frames |
| 5 | 2 | IEC61937 Input with MPEG2 frames |
| 6 | 3 | MPEG2 PES carrying Linear PCM for DVD Audio |
| 6 | 8 | MPEG2 PES carrying MPL for DVD Audio |

### 4.9  How to Program a Post Processing

### 4.9.1  2 registers for the mode:

PDEC (0x62) to define the type of PostProcessing

| PDEC | MODE |
|---|---|
| 0x01 | Prologic |
| 0x02 | MPEG 1/2 Dynamic Range |
| 0x08 | Double Stereo |
| 0x10 | DC Remove |
| 0x20 | Deemphasis filter |

### 4.9.2  1 or 2 registers to control the "PostProcessing"

Prologic decoder (PDEC = 0x01):

| PL ABL WS (0x64) | Effect |
|---|---|
| 1 | AutoBalance |
| 2 | WideSurround |
| **PL DOWNMIX (0x65)** | **Prologic DownMix** |
| 0,1,2 | Prologic not applied |
| 3 | 3/0 (L, R, C) |
| 4 | 2/1 (L, R, Ls) Phantom |
| 5 | 3/1 (L, R, Ls) |
| 6 | 2/2 (L, R, Ls, Rs) Phantom |
| 7 | 3/2 (L, C, R, Ls, Rs) |

**Remark:** When playing "Dolby Digital Prologic encoded", if PL_DOWNMIX is correctly set, Prologic decoder' is automatically applied even if the register "PDEC" different to 1.
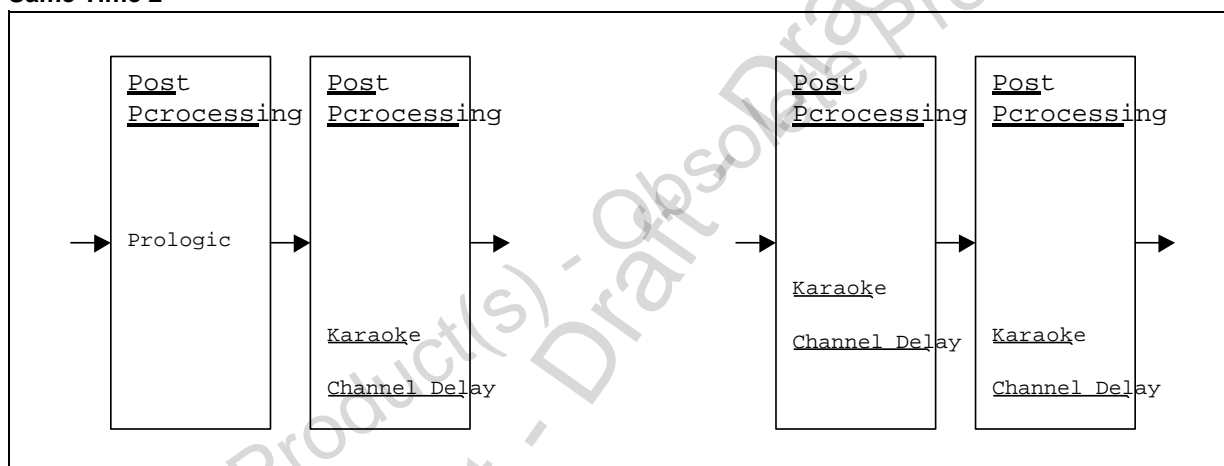
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### 4.10 What Can Be Processed at the Same Time

**Same Time 1**
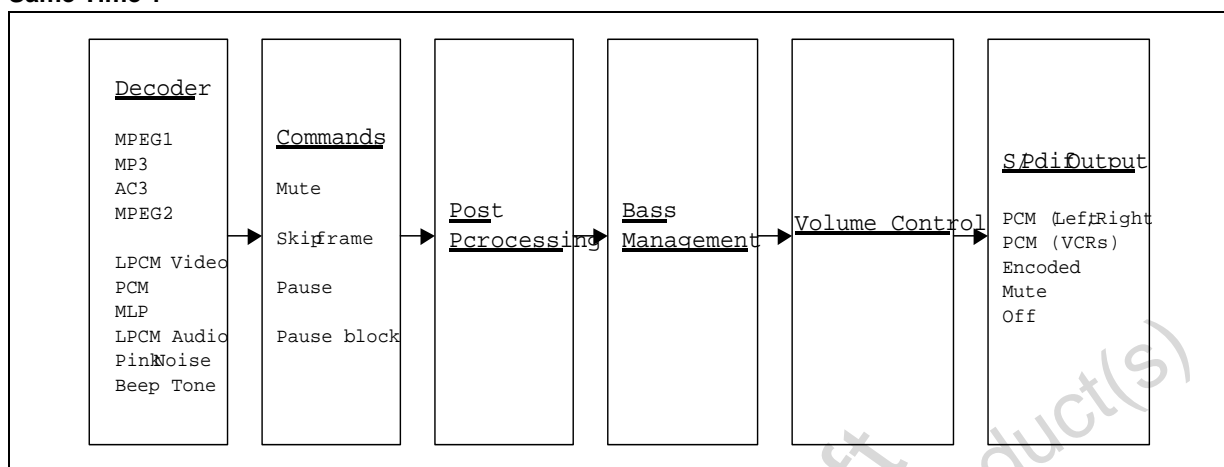


**Same Time 2**



## 5   PCM OUTPUT CONFIGURATIONS

### 5.1   Output configurations

The figure below shows the different configurations supported at PCM output stage. They are selected by the OCFG register contents.

- In configuration 1, 3 and 4, the main channels are attenuated by 18.5dB, and the LFE by 8.5dB before summing.
  After digital/analog conversion, the subwoofer preamplifier has to compensate for the different gains of the main channels and subwoofer.

- In configuration 2, the main channels are attenuated by 16dB and the LFE by 6dB before processing.

- In configuration 0, outputs are only scaled and rounded (see next section).

The same configurations will be used in case of a decoded Pro Logic program with the exception that the surround channels will not be added to the bass redirection (the surround channels of a Pro Logic program are band limited and bass is considered as leakage).

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**Figure 14. PCM Output Configurations**
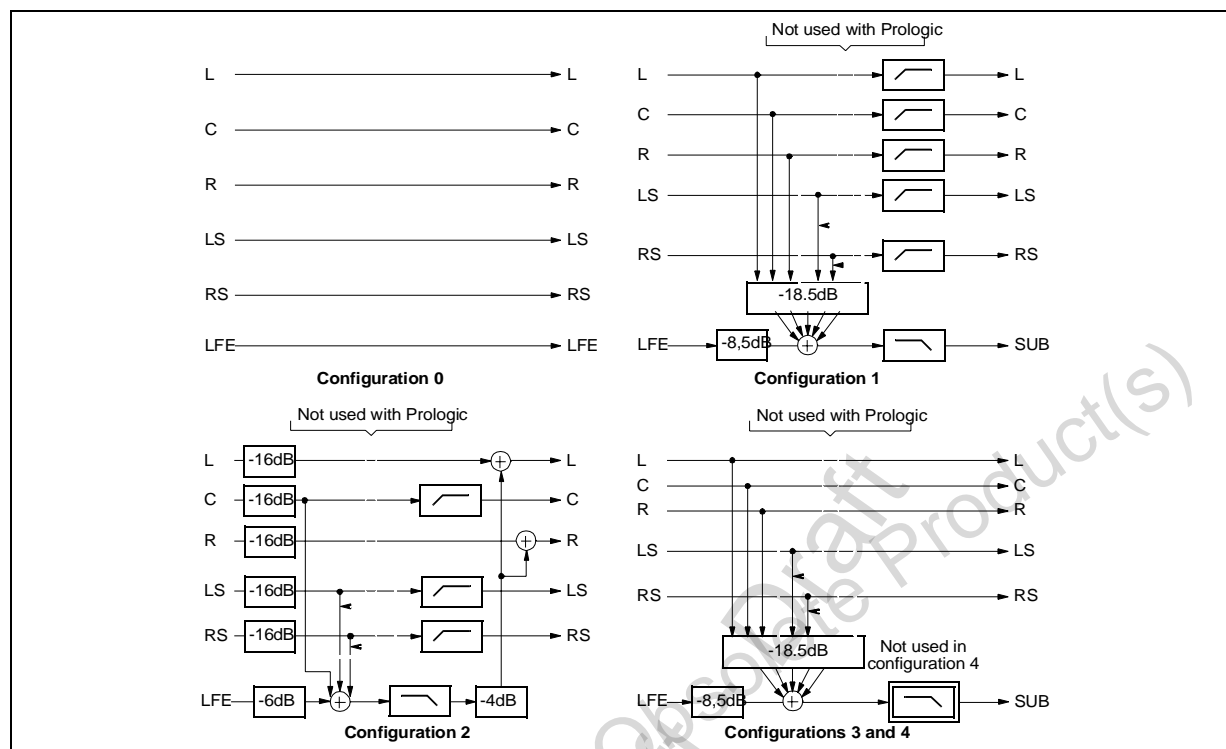


## 5.2 PCM scaling

PCM scaling is needed for every decoding mode (AC3, Pro Logic, MPEG, PCM). It is applied at the end of the filtering steps before PCM output, allowing maximum effective word width for most of the signal processing before.

Master volume (PCM_SCALE register) and balances (BAL_LR and BAL_SUR registers) are implemented for PCM scaling.

## 5.3 Output quantization

For optimal results for 16/18/20-bit DACs, a quantization with rounding is applied together with the PCM scaling.

The sample value is multiplied by a rounding factor and rounded to 24 bits. The result is then left shifted (4/6/8) for PCM output.

The output precision is selectable from the 16bits/word to 24 bits/word by configuring the field PREC in the register PCMCONF.

## 5.4 Interface and output formats

The decoded audio data are output in serial PCM format.

The interface consists of the following signals

| PCM_OUT0, 1, 2 | PCM data, output, |
| --- | --- |
| SCLK | Bit clock (or serial clock), output, |
| LRCLK | Word clock (or Left/Right channel select clock), output, |
| PCMCLK | PCM clock, input or output (see <CrossRef><BlueHT>Clocks <BlueHT>on page 11 for details). |

### 5.4.1  Output precision and format selection

Output precision is selectable from 16 bits/word to 24 bits/word by setting the output precision select, in the PC-MCONF (16-, 18-, 20- and 24-bit mode) register.

In 16-bit mode, data may be output either with the most significant bit first or least significant bit first. This is configured by the contents of the field ORD in the PCMCONF register.

When PCMCONF.PREC is more than 16 bits, 32 bits are output for each channel. In this configuration, the field FOR of register PCMCONF is used to select Sony or I²S- compatible format. The field DIF of PCMCONF is used to position the 18, 20 or 24 bits either at the beginning or at the end of each 32-bit frame.

**Figure 15. Output formats**
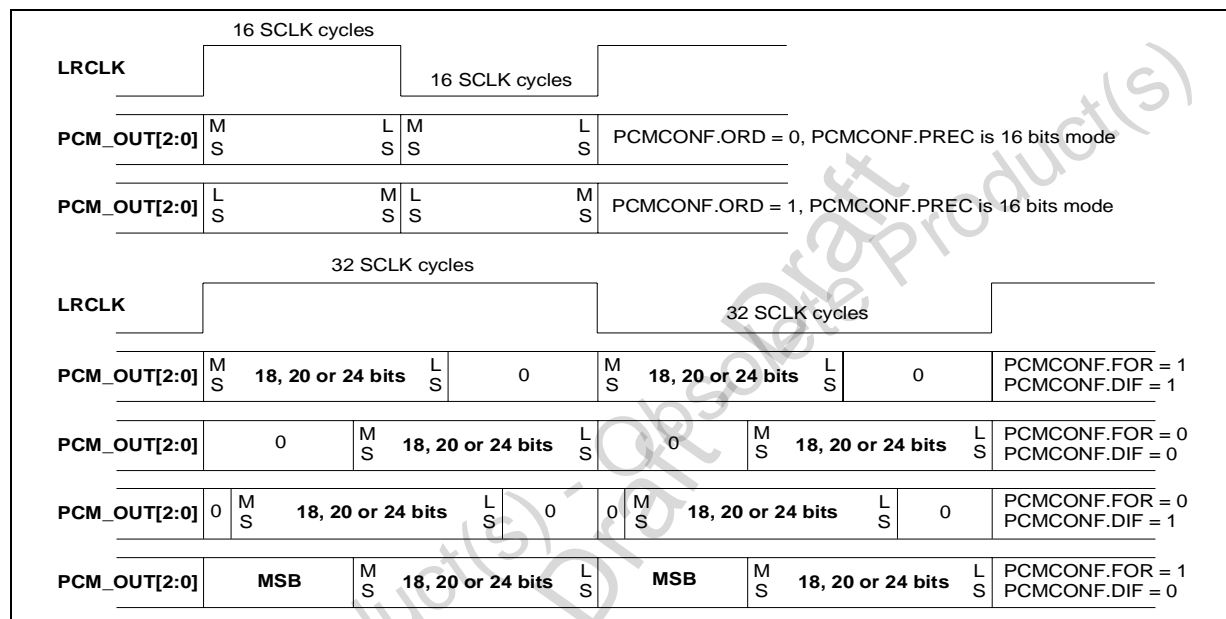


| M CONF.PEC | PCM CONF.ORD | PCM CONF.FOR | PCM CONF.DIF | DATA IN SAMPLE MEMORY DATA [23:0] | DATA SENT ON THE PCM SERIAL OUTPUT (LEFT BIT FIRST) |
|---|---|---|---|---|---|
| 0:16-bit mode | 1 | NA | NA | {d23-d8}-{8*0} | {d8-d23}: 16 bits |
| 0:16-bit mode | 0 | NA | NA | {d23-d8}-{8*0} | {d23-d8}: 16 bits |
| 1:18-bit mode | NA | 0 | 0 | {d23-d6}-{6*0} | {13*0}{0}{d23-d6}: 32 bits |
| 1:18-bit mode | NA | 0 | 1 | {d23-d6}-{6*0} | {0}{d23-d6}{13*0}: 32 bits |
| 1:18-bit mode | NA | 1 | 0 | {d23-d6}-{6*0} | {14*d23}{d26*d6}: 32 bits |
| 1:18-bit mode | NA | 1 | 1 | {d23-d6}-{6*0} | {d23-d6}{14*0}: 32 bits |
| 2:20-bit mode | NA | 0 | 0 | {d23-d4}-{4*0} | {11*0}{0}{d23-d4}: 32 bits |
| 2:20-bit mode | NA | 0 | 1 | {d23-d4}-{4*0} | {0}{d23-d4}{11*0}: 32 bits |
| 2:20-bit mode | NA | 1 | 0 | {d23-d4}-{4*0} | {12*d23}{d23-d4}: 32 bits |
| 2:20-bit mode | NA | 1 | 1 | {d23-d4}-{4*0} | {d23-d4}{12*0}: 32 bits |
| 3:24-bit mode | NA | 0 | 0 | {d23-d0} | {6*0}{0}{d23-d0}: 32 bits |
| 3:24-bit mode | NA | 0 | 1 | {d23-d0} | {0}{d23-d0}{7*0}: 32 bits |
| 3:24-bit mode | NA | 1 | 0 | {d23-d0} | {8*d23}{d23-d0}: 32 bits |
| 3:24-bit mode | NA | 1 | 1 | {d23-d0} | {d23-d0}{8*0}: 32 bits |

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How to read the above table:

The first 4 columns list the possible configurations for output formats on the PCM outputs. The 5th column gives the description of the internal 24-bit decoded, scaled and rounded audio samples as they are stored in memory. These 24 bits are referred to as d23, d22,..., d0, where MSB=d23, LSB=d0. The last column describes the sequence of bits that are output on PCM_OUT according to the selected format.

Example 1: in 16-bit mode, with PCMCONF.ORD=1: In memory, 24 bits are stored, where only the 16 MSB bits (d23, d22,... to d8) are significant and the 8 remaining bits are 0. This is noted: {d23-d8} {8*0}. The data are sent LSB first, i.e. d8 is sent first and d23 is sent last. This is noted {d8-d23}. 16 bits only are transmitted per channel.

Example 2: in 20-bit mode (PCMCONF.ORD field is meaningless in this mode), with PCMCONF.FOR=1 and PCMCONF.DIF=0: In memory, 24 bits are stored, where only the 20 MSB (d23 to d4) are significant and the remaining 4 LSB are 0.This is noted: {d23-d4} {4*0}. 32 bits are transmitted per channel on the PCM outputs: the 12 first transmitted bits are d23, the last bits are d23 to d4, where d23 is transmitted first. This is noted: {12*d23} {d23-d4}.

### 5.4.2 Clocks polarity selection

The polarity of the PCM serial output clock, SCLK and the polarity of the PCM word clock LRCLK are selected by the field SCL and INV respectively, in the PCMCONF register.

### 5.4.3 I²S format compatible outputs

To output I²S compatible data, the PCMCONF register must be configured as follows

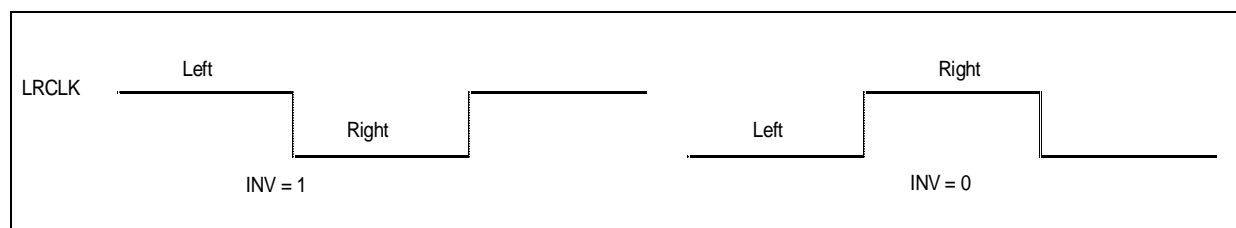| PCMCONF.DIF | = 1 | not right padded, |
| PCMCONF.FOR | = 0 | I²S format, |
| PCMCONF.INV | = 0 | do not invert LRCLK, |
| PCMCONF.SCL | = 0 | do not invert SCLK. |

### 5.4.4 Sony format compatible outputs

| PCMCONF.FOR | = 1 | Sony format, |
| PCMCONF.INV | = 1 | Invert LRCLK. |

**Figure 16. SCLK Polarity**
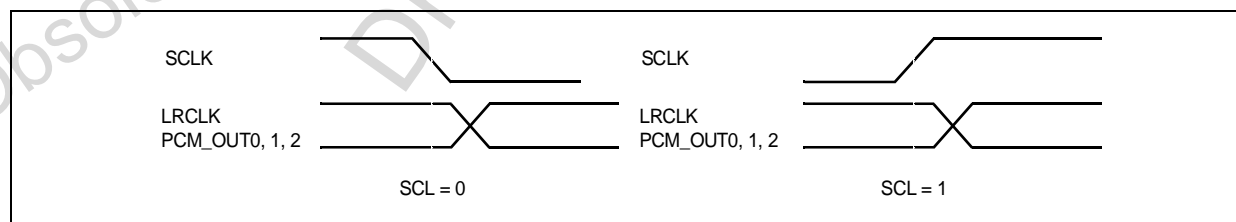


**Figure 17. LRCLK Polarity**

## 6    S/PDIF OUTPUT

The S/PDIF output pad is a TTL output pad with slew rate control. The output DC capability is 4 mA. The voltage drop is 3V. This output must be connected to a TTL driver before the transformer.

The S/PDIF output supports SPDIF and IEC-61937 standards. Several registers must be initialized to configure the SPDIF output:

- The category code must be entered in the IEC958_CAT register. It is related to the type of application. The category code is specified in the Digital Output Interface standard.
- The status bits that will be transmitted on the SPDIF output, must be programmed in the IEC958_STATUS register.
- IEC clock setting must be specified in the IEC958_CONF register.
- The data type dependent information can be specified in the IEC958_DTDI register.
- The S/PDIF type is selected through the IEC958_CMD register: the IEC unit can output decoded data (PCM mode), encoded data, or null data.

Note:   1.  The SPDIF output handles only 48kHz or 44.1kHz sample rates.

### 6.1  SPDIF output

When configured in SPDIF mode, the S/PDIF output is used to transmit either the L/R channels (PCMOUT1) or VCR_L/VCR_R (PCMOUT0).

The selection is done by choosing the PCM mode and AUX = 1 in the register SPDIF_CMD and resetting the COM status of SPDIF_STATUS register.

### 6.2  IEC-61937 output

When configured in IEC-61937 mode, the S/PDIF output is used to transmit encoded data taken directly from the frame buffer.

The selection is done by choosing the encoded mode (ENC mode) in the register IEC958_CMD and setting the bit COM in IEC958_STATUS register.

The decompressed data are output simultaneously on the PCM_OUT outputs.

Latency in software versions 6 and later

For software versions 6 and later, when choosing to output encoded S/PDIF data, a latency is automatically inserted between S/PDIF output and PCM outputs. The PCM outputs are delayed compared to the SPDIF output.

The latency value is defined by standards and applied when the auto-latency mode is selected.

AC3 decoding

$$\text{Latency} \quad = 1/\text{Fs} * (1/3 * \text{Framesize} + 256)$$
$$= 1/\text{Fs} * (32 * \text{Datarate}/\text{Fs} + 256)$$

MPEG decoding

$$\text{Latency} \quad = 1/\text{Fs} * (36 * \text{Datarate}/\text{Fs} + 96)$$

where Fs is the sampling frequency in kHz, Framesize is expressed in 16-bit words, Datarate is the bit rate in kbits per second.

The latency insertion can not be disabled however it can be programmed to values different from those required in the standard by selecting the user-programmable-latency mode (by setting the bit 7 of IEC858_CONF regis-

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ter). In this case, the latency is specified in the IEC958_LATENCY register.

Note that there are minimum and maximum values to respect

**Table 7.**

| AC-3 | | MPEG | |
|------|------|------|------|
| **Min. Latency** | **Max. Latency** | **Min. Latency** | **Max. Latency** |
| 256<br>samples / Fs | 1536<br>samples / Fs | 96<br>samples / Fs | 1152<br>samples / Fs |

If those limits are not respected, an error interrupt occurs corresponding to error type: LATENCY_TOO_BIG, which automatically makes the chip switch to auto_latency mode.

For software versions prior to 6, the latency is not implemented.

## 6.3  PCM null data

When configured in muted mode (in the IEC958_CMD register), the outputs are PCM null data. This can be used to synchronize the external IEC receiver.

## 7    INTERRUPTS

### 7.1  Interrupt register

The decoder can signal to the external controller that an interrupt has occurred during the execution.
The register INTE enables to select which interrupts will be generated and output on the IRQ output pin.

When an interrupt occurs, the signal IRQ is activated low and the controller can check which interrupt was detected by reading the register INT.

According to the type of interrupt detected, other information can be obtained by reading associated registers (such as stream header, type of error detected, PTS value).

### 7.2  IRQ Signal

This signal, IRQ, is a three-state line. This signal indicates (by going low) when an interrupt occurs. It returns to high level once the corresponding bit in the interrupt register has been cleared.

### 7.3  Error concealment

Errors are signaled as interrupts by the audio core. The error list is provided in. Most of the errors are automatically handled by the core, some require that software be changed.

AC-3 decoding errors:

Those errors are signaled in the ERROR register but handled directly by the core. Nothing can be done by the software. They signal that something wrong happened during the decoding. The core soft mutes the frame and continues to decode.

MPEG decoding errors:

Those errors are also signaled in the ERROR register but handled directly by the core. Nothing can be done by the software. They signal that something wrong happened during the decoding. The core soft mutes the frame and continues to decode. Only one error in this category indicates a programming error: if triggering the

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MPEG_EXT_CRC_ERROR, the bit MC_OFF must be set. This indicates that the decoder tries to decode more than 2 channels whereas the incoming stream contains only 2 channels.

Packet and audio synchronization errors:

Those errors are handled internally, and usually indicate that the incoming bitstream is incorrect or incorrectly input to the chip. In those cases, the decoder resets the corresponding parsing stage (packet or audio parser) then searches for the next correct frame.

Miscellaneous errors:

- LATENCY_TOO_BIG error indicates a problem of latency programming which is superior to the maximum authorized value.
  Change the latency value or switch to auto-latency mode to solve the problem. Other miscellaneous errors are internally handled.

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## 8    AUDIO/VIDEO SYNCHRONIZATION

### 8.1  Presentation time stamp detection

#### 8.1.0.1  $\overline{\text{PTS}}$ Signal

This signal, $\overline{\text{PTS}}$, is used to signal the detection of a Presentation Time Stamp in a stream, for audio/video synchronization. When a PTS is detected, the signal PTS goes low during one LRCLK period. It is generated while the PCM are output, so to enable the use of an external counter to synchronize the STA310 with a video decoder.

The signal is activated, even if PTS interrupt is not enabled.

### 8.1.1  PTS interrupt

When enabled through the INTE register, the interrupt PTS is generated when a PTS is detected. The interrupt is signalled on the $\overline{\text{IRQ}}$ output, which goes low. The $\overline{\text{IRQ}}$ signal is de-activated once the PTS bit has been cleared in INT register by reading the PTS Most Significant Bit.

### 8.1.2  PTS interrupt and signal relative timings

The $\overline{\text{IRQ}}$ configured as PTS interrupt is output before the $\overline{\text{PTS}}$ signal. The $\overline{\text{PTS}}$ signal is activated at last one period of LRCLK after the $\overline{\text{IRQ}}$ signal.

### 8.2  Frames skip capability

When the audio decoder is late compared to the video decoder, the decoder is able to skip frames. Writing 1 in the SKIP_FRAME register makes the decoder ignore the next incoming frame. Once skipping the frame, it continues to decode the stream, and the SKIP_FRAME register is automatically reset.

### 8.3  Frames repeat capability

When the audio decoder is ahead of the video decoder, the decoder can repeat frames. Writing 1 in the REPEAT_FRAME register makes the decoder repeat the current frame. Once repeating the frame, the chip plays the next incoming frame, and the REPEAT_FRAME register is reset.

## 9    REGISTER MANUAL

### 9.1  Introduction

The STA310 device contains 256 registers.

Two types of registers exist:

- From address 0x00 to 0x3F, the registers are real registers that can be initialized after reset.
- From address 0x40 to 0x100, they are memory locations. This means that the registers located at the address 0x40 to 0x100 can have different meanings and usage according to the mode in which the device operates.
  Be careful that they can not be hardware reset: they contain undefined values at reset and require to be initialized after each hardware reset.

In this document, only the user registers are described.

The undocumented registers are reserved. These registers must never be accessed (neither in Read nor in Write mode).

The Read only registers must never be written

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## 9.2  Register map by function

| Code | Description |
|------|-------------|
| (a) | Register modification is ALWAYS taken into account by the audio decoder. Any change to these registers is taken into account immediately. |
| (b) | Register modification is taken into account AFTER EVERY DECODED DATA BLOCK or JUST AFTER RESET (soft or hard). The decoded block is related to the granularity of the computation in the audio decoder software. A block is 256 samples in Dolby Digital, 96 samples in MPEG, 80 samples in LPCM/PCM. |
| (f) | Register modification is taken into account AFTER EVERY DATA FRAME. A frame is: 1152 samples in MPEG I/II, 1536 samples in Dolby Digital, 384 samples in MPEG-1 layer 1, 80 samples in LPCM/PCM. |
| (r) | Register modification is taken into account ONLY WHEN THE DSP IS RUN AFTER RESET (soft or hard). |
| (1) | The delay registers are updated when bit 0 of the     UPDATE register is set to 1. |
| (2) | The volume is updated when CHAN_IDX is set to the appropriate value. |
| (3) | The Karaoke mode is updated when     KAR_UPDATE is set to '1'. |

The following tables list the register map by address and function, then each audio decoder register is described individually

**Table 8.**

| Register function | HEX | DEC | Name |
|-------------------|-----|-----|------|
| VERSION | 0x00 | 0 | VERSION |
| | 0x01 | 1 | IDENT |
| | 0x71 | 113 | SOFT'VER |
| SETUP + INPUTS | 0x0C | 12 | SIN_SETUP (a) |
| | 0x0D | 13 | CAN_SETUP (a) |
| PCM CONFIGURATION | 0x54 | 84 | PCMDIVIDER (b) |
| | 0x55 | 85 | PCMCONF (b) |
| | 0x56 | 86 | PCMCROSS (b) |
| DAC AND PLL CONFIGURATION | 0x05 | 5 | SFREQ (f) |
| | 0x12 | 18 | PLLCTRL (f) |
| | 0x18 | 24 | PLLMASK (a) |
| | 0x0E | 14 | DATA IN |
| | 0x12 | 18 | PLLCTRL (f) |
| | 0x11 | 17 | PLL_DATA (a) |
| | 0x1D | 29 | PLL_CMD(f) |
| | 0x12 | 18 | PLL_ADD (f) |
| | 0xB5 | 181 | ENA_ALL FRACPLL |
| | 0xB6 | 182 | AU_PLL_FRACL_192 |
| | 0xB7 | 183 | AU_PLL_FRACH_192 |
| | 0xB8 | 184 | AU_PLL_XDIV_192 |
| | 0xB9 | 185 | AU_PLL_MDIV_192 |
| | 0xBA | 186 | AU_PLL_NDIV_192 |
| | 0xBB | 187 | AU_PLL_FRACL_176 |
| | 0xBC | 188 | AU_PLL_FRACH_176 |
| | 0xBD | 189 | AU_PLL_XDIV_176 |
| | 0xBE | 190 | AU_PLL_MDIV_176 |

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| Register function | HEX | DEC | Name |
|---|---|---|---|
| CHANNEL DELAY SETUP | 0x57 | 87 | LDLY (1) |
| | 0x58 | 88 | RDLY (1) |
| | 0x59 | 89 | CDLY (1) |
| | 0x5A | 90 | SUBDLY (1) |
| | 0x5B | 91 | LSDLY (1) |
| | 0x5C | 92 | RSDLY (1) |
| | 0x5D | 93 | UPDATE (f) |
| | 0xAF | 91 | LVDLY (1) |
| | 0xB0 | 92 | RVDLY (1) |
| SPDIF OUTPUT SETUP | 0x5E | 94 | SPDIF_CMD (r) |
| | 0x5F | 95 | SPDIF_CAT (f) |
| | 0x60 | 96 | SPDIF_CONF (b) |
| | 0x61 | 97 | SPDIF_STATUS (b) |
| | 0x75 | 117 | SPDIF_REP_TIME (b) |
| | 0x7E | 126 | SPDIF_LATENCY (f) |
| | 0x7F | 127 | SPDIF_DTDI (f) |
| COMMAND | 0x10 | 16 | SOFTRESET (a) |
| | 0x13 | 19 | PLAY (a) |
| | 0x14 | 20 | MUTE (a) |
| | 0x72 | 114 | RUN (a) |
| | 0x73 | 115 | SKIP_MUTE_CMD (f) |
| | 0x74 | 116 | SKIP_MUTE_VALUE(f) |
| INTERRUPT | 0x07, 08 | 7, 8 | INTE (a) |
| | 0x09, 0A | 9, 10 | INT (a) |
| INTERRUPT STATUS | 0x40 | 64 | SYNC_STATUS |
| | 0x41 | 65 | ANCCOUNT |
| | 0x42 | 66 | HEAD4 (f) |
| | 0x43 | 67 | HEAD3 (f) |
| | 0x44, 45 | 68, 69 | HEADLEN (f) |
| | 0x46 - 4A | 70 | PTS (f) |
| | 0x0F | 15 | ERROR |
| DECODING ALGORITHM | 0x4C | 76 | STREAMSEL (r) |
| | 0X4D | 77 | DECODSEL (r) |
| SYSTEM SYNCHRONIZATION | 0x4F | 79 | PACKET_LOCK (r) |
| | 0x50 | 80 | ID_EN (a) |
| | 0x51 | 81 | ID (a) |
| | 0x52 | 82 | ID_EXT (a) |
| | 0x53 | 83 | SYNC_LOCK (r) |
| POST DECODING AND PRO LOGIC | 0x62 | 98 | PDEC1 (b) |
| | 0xB1 | 177 | PDEC2 |
| | 0x64 | 100 | PL_AB (b) |
| | 0x65 | 101 | PL_DWNX (b) |
| | 0x66 | 102 | OCFG |
| | 0x70 | 112 | DWSMODE (b) |

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| Register function | HEX | DEC | Name |
|---|---|---|---|
| BASS REDIRECTION | 0x4E | 78 | VOLUME0 (2) |
| | 0x63 | 100 | VOLUME1 (2) |
| | 0x66 | 102 | OCFG (b) |
| | 0x67 | 103 | CHAN_IDX (b) |
| DOLBY DIGITAL CONFIGURATION | 0x68 | 104 | AC3_DECODE_LFE (b) |
| | 0X69 | 105 | AC3_COMP_MOD (b) |
| | 0x6A | 106 | AC3_HDR (b) |
| | 0x6B | 107 | AC3_LDR (b) |
| | 0x6C | 108 | AC3_RPC (b) |
| | 0x6D | 109 | AC3_KARAMODE (b) |
| | 0x6E | 110 | AC3_DUALMODE (b) |
| | 0x6F | 111 | AC3_DOWNMIX (b) |
| | 0x76 | 118 | AC3_STATUS0 (f) |
| | 0x77 | 119 | AC3_STATUS1 (f) |
| | 0x78 | 120 | AC3_STATUS2 (f) |
| | 0x79 | 121 | AC3_STATUS3 (f) |
| | 0x7A | 122 | AC3_STATUS4 (f) |
| | 0x7B | 123 | AC3_STATUS5 (f) |
| | 0x7C | 124 | AC3_STATUS6 (f) |
| | 0x7D | 125 | AC3_STATUS7 (f) |
| MPEG CONFIGURATION | 0x68 | 104 | MP_SKIP_LFE (b) |
| | 0x69 | 105 | MP_PROG_NUMBER (b) |
| | 0x6E | 106 | MP_DUALMODE (b) |
| | 0x6A | 110 | MP_DRC (b) |
| | 0x6C | 108 | MP_CRC_OFF (b) |
| | 0x6D | 109 | MP_MC_OFF (b) |
| | 0x6F | 111 | MP_DOWNMIX (b) |
| | 0x76 | 118 | MP_STATUS0 (f) |
| | 0x77 | 119 | MP_STATUS1 (f) |
| | 0x78 | 120 | MP_STATUS2 (f) |
| | 0x79 | 121 | MP_STATUS3 (f) |
| | 0x7A | 122 | MP_STATUS4 (f) |
| | 0x7B | 123 | MP_STATUS5 (f) |
| PINK NOISE GENERATION REGISTERS | 0x6F | 111 | PN_DOWNMIX |
| PCM BEEP-TONE CONFIGURATION | 0x68 | 104 | PCM_BTONE (b) |

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| Register function | HEX | DEC | Name |
|---|---|---|---|
| KARAOKE | 0x81 | 129 | KAR_MCh0VOL (3) |
| | 0x82 | 130 | KAR_MCh1VOL (3) |
| | 0x83 | 131 | KAR_KEYCONT (3) |
| | 0x84 | 132 | KAR_KEYVALUE (3) |
| | 0x85 | 133 | KAR_VCANCEL (3) |
| | 0x86 | 134 | KAR_VVALUE (3) |
| | 0x87 | 135 | KAR_MMUTE (3) |
| | 0x88 | 136 | KAR_VCh0VOL (3) |
| | 0x89 | 137 | KAR_VCh1VOL (3) |
| | 0x8A | 138 | KAR_DUET (3) |
| | 0x8B | 139 | KAR_DUETTHRESH (3) |
| | 0x8C | 140 | KAR_VOICE (3) |
| | 0x8D | 141 | KAR_VDELAY (3) |
| | 0x8E | 142 | KAR_VBAL (3) |
| | 0x8F | 143 | KAR_VMUTE (3) |
| | 0x90 | 144 | KAR_PLAY (3) |
| | 0x91 | 145 | KAR_MODE (3) |
| | 0x92 | 146 | KAR_DIN_CTL (3) |
| | 0x93 | 147 | KAR_UPDATE |
| SECOND SERIAL INPUT | 0x94 | 148 | SFREQ2 |
| | 0x95 | 149 | CANINPUT_MODE |
| LINEAR PCM (DVD AUDIO) REGISTERS | 0x6F | 111 | LPCMA_DOWNMIX |
| | 0x70 | 112 | LPCMA_FORCE_DWS |
| | 0x76 | 118 | LPCMA_STATUS0 |
| | 0x77 | 119 | LPCMA_STATUS1 |
| | 0x78 | 120 | LPCMA_STATUS2 |
| | 0x79 | 121 | LPCMA_STATUS3 |
| | 0x7A | 122 | LPCMA_STATUS4 |
| | 0x7B | 123 | LPCMA_STATUS5 |
| | 0x97 | 151 | LPCMA_DM_COEFT_0 |
| | 0x98 | 152 | LPCMA_DM_COEFT_1 |
| | 0x99 | 153 | LPCMA_DM_COEFT_2 |
| | 0x9A | 154 | LPCMA_DM_COEFT_3 |
| | 0x9B | 155 | LPCMA_DM_COEFT_4 |
| | 0x9C | 156 | LPCMA_DM_COEFT_5 |
| | 0x9D | 157 | LPCMA_DM_COEFT_6 |
| | 0x9E | 158 | LPCMA_DM_COEFT_7 |
| | 0x9F | 159 | LPCMA_DM_COEFT_8 |
| | 0xA0 | 160 | LPCMA_DM_COEFT_9 |
| | 0xA1 | 161 | LPCMA_DM_COEFT_10 |
| | 0xA2 | 162 | LPCMA_DM_COEFT_11 |
| | 0xA3 | 163 | LPCMA_DM_COEFT_12 |
| | 0xA4 | 164 | LPCMA_DM_COEFT_13 |
| LINEAR PCM (DVD VID & PCM) REGISTERS | 0x6F | 111 | LPCMV_DOWNMIX |

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| Register function | HEX | DEC | Name |
|---|---|---|---|
| | 0x70 | 112 | LPCMV_FORCE_DWS |
| | 0x76 | 118 | LPCMV_STATUS0 |
| | 0x77 | 119 | LPCMV_STATUS1 |
| | 0x78 | 120 | LPCMV_STATUS2 |
| | 0x97 | 151 | LPCMV_DM_COEFT_0 |
| | 0x98 | 152 | LPCMV_DM_COEFT_1 |
| | 0x99 | 153 | LPCMV_DM_COEFT_2 |
| | 0x9A | 154 | LPCMV_DM_COEFT_3 |
| | 0x9B | 155 | LPCMV_DM_COEFT_4 |
| | 0x9C | 156 | LPCMV_DM_COEFT_5 |
| | 0x9D | 157 | LPCMV_DM_COEFT_6 |
| | 0x9E | 158 | LPCMV_DM_COEFT_7 |
| | 0x9F | 159 | LPCMV_DM_COEFT_8 |
| | 0xA0 | 160 | LPCMV_DM_COEFT_9 |
| | 0xA1 | 161 | LPCMV_DM_COEFT_10 |
| | 0xA2 | 162 | LPCMV_DM_COEFT_11 |
| | 0xA3 | 163 | LPCMV_DM_COEFT_12 |
| | 0xA4 | 164 | LPCMV_DM_COEFT_13 |
| | 0xA8 | 168 | LPCMV_CH_ASSIGN |
| | 0xA9 | 169 | LPCMV_MULTI_CHS |
| DE-EMPHASIS REGISTER | 0xB5 | 181 | DEEMPH |
| AUXILLIARY OUTPUTS REGISTERS | 0xAE | 174 | VCR_MIX |
| | 0xAF | 175 | VCR_LDLY |
| | 0xB0 | 176 | VCR_RDLY |
| MISCELLANEOUS | 0x2B | 43 | BREAKPOINT |
| | 0x3A | 58 | CLOCKCMD |
| | 0xFF | 255 | INIT_RAM |
| SPDIF AUTODETECTION | 0xE0 | 224 | AUTODETECT_ENA |
| | 0xE1 | 225 | AUTODETECT_SENS |
| | 0xE2 | 226 | AUTODETECT_ALIGN |

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### 9.3   VERSION REGISTERS

**IDENT**

**Identify**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

Address: 0x01

Type: RO

Software Reset: 0x31

Hardware Reset: 0x31

Description:

IDENT is a read-only register and is used to identify the IC on an application board. IDENT always has the value "0x31".

**SOFTVER**

**Software version**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x71

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This SOFTVER register is the version of the code which is running on the device. This regiter is updated by the embedded software just after a soft reset of the device:

- For STA310 cut 1.0 the register contain the value 0x0A
- For STA310 cut 2.0 the register contain the value 0x14

Loading a patch into the STA310 will automatically change the register content.

Please contact ST to have the correct value according to the patch being used.

This register must be readonly after the STA310 has finished booting, in order to get a correct value (when INIT_RAM register hold the value 1)

**VERSION**

**Version**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Address: 0x00

Type: RO

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Software Reset: NA

Hardware Reset: NA

Description:

This version register is read only and is used to iden-
tify the audio hardware version. The version register
holds a number which refers to the cut number. The
version numbers are defined as below:

- STA310 cut 1.0, version number is : 0x10
- STA310 cut 2.0, version number is : 0x10

## 9.4   SETUP & INPUT REGISTERS

The STA310 can get receive an input bitstream either
from the I2s input or ffrom the Spdif input, the selec-
tion and the configuration is done through 2 registers
SIN_SETUP @ 12 and CAN_SETUP @ 13.

**SIN SETUP**

**Input data setup**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   | SPDIF | POL | IMODE [1...0] | |

Address: 0x0C

Type: R/W

Software Reset: NC

Hardware Reset: 0

Description:

This register is used to configure the input data inter-
face. The register must be setup before sending data
to the IC. The mapping of the register isescribed be-
low. Remember that the data must be sent to the de-
vice MSB first.

- **SPDIF** data frpm SPDIF when set to 1, data
  from main I$^2$S input.
- **POL** Polarity of the REQ signal. When set,
  the REQ pin is active low: data must be input
  when REQ is low. When reset, the REQ pin is
  active high and data must be input when REQ
  is high.
- **IMODE[1...0]** Input mode. Indicates which
  data input interface is used.

The configuration of the 3 possible interfaces is

shown below:

| IMODE[1:0] | Mode |
|---|---|
| 0 | Parallel input (DSTR+Data [7:0] + REQ) |
| 1 | Serial input (DSTR + SIN + REQ) |
| 2 | Reserved - Not used |
| 3 | A/D input (DSTR+LRCLKIN+REQ+SIN; SPDIF input; PCM input |

When the IC is configured in mode 1 or 3, the
CAN_SETUP register is used to configure the IC with
repect to the data format.

**CAN_SETUP**

**A/D converter setup**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   | S16 | SAM | FIR | PAD |

Address : 0x0D

Type: R/W

Software Reset: NC

Hardware Reset: 0

Description:

CAN_SETUP is used to configure the data serial in-
terface. The register is only taken into account when
the register sin_setup [1...0] = 3.

Also see SIN_SETUP register./

- **S16** When set, the slot count is 16. When re-
  set, the slot count is 32 but only the first 16
  are extracted.
- **SAM** When set data is sampled on the falling
  edge of the DSTR. When reset, the data is
  sampled on the rising edge of DSTR
- **FIR** When set the first channel (Left) is input
  when Lrclkin=1. When reset, the first channel
  is input when Lrclkin=0.
- **PAD** When set, data Lrclkin is delayed by one
  cycle (padding mode).

When the IC is configured with the S/PDIF input, reg-
ister CAN_SETUP must be set to 2

**DATAIN**

**Data input**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

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## STA310

Address : 0x0E

Type: WO

Software Reset: NA

Hardware Reset: NA

Description:

Data can be fed into the STa310 by using this register instead of the dedicated interface. there is no need to byte align the bitstream when using this register.

| PCM divider value | Mode description |
|---|---|
| 2 | DAC_PCMLK = 384 Fs, DAC is 32-bit mode |
| 1 | DAC_PCMLK = 256 Fs, DAC is 32-bit mode |

### PCMCONF

**PCM configuration**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | ODR | DIF | INV | FOR | SCL | PREC[1:0] | |

Address: 0x55

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

### 9.5  PCM CONFIGURATION RESISTERS
### PCMDIVIDER

**Divider for PCM clock**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Address : 0x54

Type: R/W

Software Reset: UND

Hardware Reset: UND

Description:

The PCM divider must be set according to the formula below, where DAC_SCLK is the bit clock for the DAC. When Div is set to 0, DAC_SCLK is equal to DAC_PCMCLK:

$$Div = (DAC\_PCMCLK/ (2 \times DAC\_SCLK)) -1$$

When the internal PLL is used, DAC_PCMCLK=384 x fs or 256 x fs. If DAC_PCMCLK = 384 x fs, the formula becomes:

$$Div = (192 \times Fs/DAC\_SCLK) -1$$

If DAC_SCLK is 32 x Fs (common case with the 16 bit DAC), Div must be set to 5.

| PCM divider value | Mode description |
|---|---|
| 5 | DAC_PCMCLK = 384Fs, DAC is 16-bit mode |
| 3 | DAC_PCMLK = 256 Fs, DAC is 16-bit mode |

| Bitfield | Description |
|---|---|
| ORD | PCM Order: This bit is significant only when in 16-bit mode. When set, LSB is sent first. When reset, MSB is sent first. |
| DIF | PCM_DIFF: This bit is not significant in 16-bit. When set, indicates that the bits are not right-padded in the slot. When reset, Ii is right padded. |
| INV | INV_LRCLK: When set the polarty of LRCLK is inverted: Left channel is output when LRCLK is high. When reset, the polarity of LRCLK is such that the left channel is outout when LRCLK is low. |
| FOR | FORMAT: This bit selects the data output format: When set, the Sony format is chosen. When reset 0 the format is IS format. |
| SCL | INV_SCLK: When set, the polarity of SCLK is inverted, the PCM outputs and LRCLK will be stable for the DACs on the falling edge of SCLK. When reset, PCM outputs and LRCLK are stable on the rising edge of SCLK. |
| PREC[1:0] | PCM Precision<br>0: 16 bit mode (16 slots)<br>1: 18 bit mode (32 slots)<br>2: 20 bit mode (32 slots)<br>3: 24 bit mode (32 slots) |

### PCMCROSS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VCR | | CLR[1:0] | | CSW[1:0] | | LRS[1:0] | |

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Address: 0x56

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

The PCMCROSS register only acts if bit PFC of register SPDIF_DTDI is set.

| Bitfield | Description |
|---|---|
| LRS[1:0] | Cross left and right surround. |
| CSW[1:0] | Cross centre and subwoofer. |
| CLR[1:0] | Cross left and right channels. **00**: Left channel is mapped on the left output, Right channel is mapped on the Right output. **01:** Left channel is duplicated on both outputs. **10:** Right channel is duplicated on both outputs. **11:** Right channel and Left channel are toggled. |
| VCR[1:0] | These 2 bits manage the VCR outputs. |

## 9.6 PDAC and PLL configuration registers
**SFREQ**

**Sampling frequency**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x05

Type: R/WS

Software Reset: NC

Hardware Reset: 0

Description:

This status register holds the code of the current sampling frequency. If the audio stream is encoded (Dolby Digital, MPEG) or packetized (DVD_LPCM), the sampling frequency is automatically read in the audio stream and written into this register by the audio DSP. The register is automatically updated by the DSP when it performs a down-sampling (for example, 96kHz to 48kHz).

The DSP resets SFREQ to 0.

For PCM stream or CDDA, this register is written to by the application. The value in SFREQ corresponds to the following frequencies:.

| Fs (KHz) | 46 | 44.1 | 32 | - | 96 | 88.2 | 64 | - | 24 | 22.05 |
|---|---|---|---|---|---|---|---|---|---|---|
| Value | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

| Fs (KHz) | 16 | - | 12 | 11.025 | 8 | - | 192 | 176.4 | 128 | - |
|---|---|---|---|---|---|---|---|---|---|---|
| Value | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |

**PLLCTRL**

**PLL Control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   | SYSCLSCK[1..0] | | OCLK[2..0] | | |

Address: 0x12

Type: R/W

Software Reset: NA

Hardware Reset: 0x19

Description:

| Bitfield | Value | Description | |
|---|---|---|---|
| OCLK [2:0] | | Configure PCMCLK source and direction | PCMCLK pad direction |
| | -01 | Audio master Clock from PCMLCK pad. | Input |
| | 011 | Audio master Clock from internal audio PLL | Input |
| | 111 | Audio master Clock from internal S/PDIF receiver | Input |
| | -00 | Forbidden | |
| | 010 | Audio master Clock from internal audio PLL | Output |
| | 110 | Audio master Clock from internal S/PDIF receiver | Output |
| SYSCLCK[1:0] | 0 | System Clock from CLK pad Output | |
| | 1 | System Clock from CLK pad divided by 2 | |
| | 2 | System Clock from internal system PLL | |
| | 3 | System Clock from internal system PLL divided by 2 | |

**PLL_DATA**

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### PLLData

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x11

Type: R/W

Software Reset: NA

Hardware Reset: 0

Description:

Data that must be written (has been read) at (from) the address specified by PLL_ADD.

### PLL_CMD
### PLL Command

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   | AUPLLCTL | SYSPLLCTL | RWCTL[1:0] | |

Address: 0x1D

Type: R/W

Software Reset: NA

Hardware Reset: 0

Description:

| Bitfield | Description |
|---|---|
| RWCTL [1:0] | Configure PCMCLK source and direction.<br>**00**: No action is performed on the configuration registers of the level 1<br>**01:** Read action of the configuration registers. During this phase, the content of a selectable (by PLL_ADD) register of the level 1 is copied into the PLL_DATA register.<br>**10:** Write action of the configuration registers. During .this phase, the content of a selectable (by PLL_ADD) register of the level 1 is copied into the PLL_DATA register.<br>**11:** Forbidden |
| SYSPLLCTL | System PLL coefficients transfert<br>**0:** No Transfer<br>**1:** Transfer the data between the level 1 and the level 2 for the system PLL |
| AUPLLCTL | Audio PLL coefficient transfert<br>**0:** No Transfer<br>**1:** Transfer the data between the level 1 and the level 2 for the audio PLL |

### PLL_ADD

### PLL Address

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   | ADDRESS | | | | |

Address: 0x12

Type: R/W

Software Reset: NA

Hardware Reset: 0

Description:

| Value | Address of PLLs configuration registers |
|---|---|
| Address | 2: Disable System PLL<br>3: System PLL frac Low<br>4: System PLL frac High<br>6: System PLL N divider<br>7: System PLL X divider<br>8: System PLL M divider<br>9: System PLL update<br>10: Disable Audio PLL<br>11: Audio PLL Frac Low<br>12: Audio PLL Frac High<br>14: Audio PLL N divider<br>15: Audio PLL X divider<br>16: Audio PLL M divider<br>17: udio PLL update |

### ENA_AU_FRACPLL
### Audio PLL Enable

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | ENA_PLL |

Address: 0xB5

Type: R/W

Software Reset: 1

Hardware Reset: 0

Description:

This register is used to enable the audio PLL of the STA310. This register must be always set to "1" after either a soft or hardware reset.

### AU_PLL_FRACL_192
### Frac Low Coefficient

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   | FRACL | | | | |

Address: 0xB6

Type: R/W

Software Reset: 0x34

Hardware Reset: UND

Description:

This register must contain a FRACL value that enables the audio PLL to generate a frequency of ofact*192KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_FRACH_192
**Frac High Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | FRACH | | | | |

Address: 0xB7

Type: R/W

Software Reset: 0xEC

Hardware Reset: UND

Description:

This register must contain a FRACH value that enables the audio PLL to generate a frequency of ofact*192KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_XDIV_192
**X Divider Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | XDIV | | | | |

Address: 0xB8

Type: R/W

Software Reset: 0x01

Hardware Reset: UND

Description:

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact*192KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_MDIV_192
**M Divider Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | MDIV | | | | |

Address: 0xB9

Type: R/W

Software Reset: 0x09

Hardware Reset: UND

Description:

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact*192KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_NDIV_192
**N Divider Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | NDIV | | | | |

Address: 0xBA

Type: R/W

Software Reset: 0x01

Hardware Reset: UND

Description:

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact*192KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK =

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384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_FRACL_176
**Frac Low Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | FRACL | | | | |

Address: 0xBB

Type: R/W

Software Reset: 0x3

Hardware Reset: UND

Description:

This register must contain a FRACL value that enables the audio PLL to generate a frequency of ofact*176KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_FRACH_176
**Frac High Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | FRACH | | | | |

Address: 0xBC

Type: R/W

Software Reset: 0x9

Hardware Reset: UND

Description:

This register must contain a FRACH value that enables the audio PLL to generate a frequency of ofact*176KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_XDIV_176

### X Divider Coefficient

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | XDIV | | | | |

Address: 0xBD

Type: R/W

Software Reset: 0x01

Hardware Reset: UND

Description:

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact*176KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_MDIV_176
**M Divider Coefficient**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | MDIV | | | | |

Address: 0xBE

Type: R/W

Software Reset: 0x09

Hardware Reset: UND

Description:

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact*176KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

### AU_PLL_NDIV_176

### N Divider Coefficient

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | NDIV | | | | |

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Address: 0xBF

Type: R/W

Software Reset: 0x01

Hardware Reset: UND

Description:

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact*176KHz for the PCMCK.

Default value at soft reset assume:

– Oversampling factor (ofact) = 384. PCMLCK = 384 x SF (where SF is the sampling frequency)

– External crystal provide a clock running at 27MHz

**INIT_RAM**

**STa310 boot Done**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | RAM_INIT |

Address: 0xFF

Type: RO

Software Reset: 1

Hardware Reset: 0

Description:

This register is used to signal when the STA310 has finished to boot. After a soft reset or a hardware reset, the host processor must wait until INIT_RAM hold the value "1".

The host can then start to configure the STA310 according to its application.

**PLLMASK**

**PCMCLK mask for half sampling frequency**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | HALF_FS |

Address: 0x18

Type: W

Software Reset: NC

Hardware Reset: 0

| Bitfield | Description |
|----------|-------------|
| HALF_FS | If the incoming bitstream is encoded with half sampling frequency, the device generates a PCM clock (for audio DAC)<br><br>**1:** At 256 x half_fs or 384 x half_fs (half_fs is equal to 24KHz, 22.05KHz, 16KHz).<br><br>**0:** At 256 x fs or 384 x fs (fs is equal to 48KHz, 44.1KHz, 32KHz).<br>This function is mainly use for DAC frequency adaptation. |

### 9.7  Channel delay set-up registers

The six delay setup registers are used to set the relative delays to the (up to) six loud speaker channels in order to give the sound effects of, for example, a large room or to compensate for the listener not being in the centre of the loud speaker system. The sum of the delays on the channels must be less than or equal to 35ms.

The unit for the register delay contents is a group of 16 samples.

Each register value is chosen using the expression:

desired channel delay'*'sampling frequency'/16 samples and taking care to ensure that the sum of the 'desired channel delays' is not more than 35ms.

For example, when the sampling frequency is 48kHz, the sum of the values programmed in the six delay registers must be less than or equal to:

35 ms * 48 KHz /16 samples = 105.

When only one surround channel is present (in Pro Logic or other mode), the right surround delay must be cleared, and the left delay channel is used for both surround channels.

**LDLY**

**Left channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x57

Type: R/W

Software Reset: NC

Hardware Reset: UND

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Delay on left channel, expressed in number of group of 16 samples. LDLY = delay (ms) * Fs (kHz) / 16

### RDLY

**Right channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x58

Type: R/W

Software Reset: NC

Hardware Reset:UND

Delay on right channel, expressed in number of group of 16 samples. RDLY = delay (ms)*Fs (kHz)/16

### CDLY

**Centre channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x59

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Delay on center channel, expressed in number of group of 16 samples. CDLY = delay (ms) * Fs (kHz) / 16

### SUBDLY

**Subwoofer channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x5A

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Delay on subwoofer channel, expressed in number of group of 16 samples. SUBDLY = delay (ms) * Fs (kHz) / 16

### LSDLY

**Left surround channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x5B

Type: R/W

Software Reset: NC

Hardware Reset: UND

Delay on left surround channel, expressed in number of group of 16 samples. LSDLY = delay (ms) * Fs (kHz) / 16

### RSDLY

**Right surround channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x5C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Delay on right surround channel, expressed in number of group of 16 samples. RSDLY = delay (ms) * Fs (kHz) / 16.

When only one surround channel is used, this register must be reset at initialization.

### LVDLY

**Left VCR channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0xAF

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Delay on left VCR channel, expressed in number of group of 16 samples.
LSDLY = delay (ms) * Fs (kHz) / 16

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**RVDLY**

**Right VCR channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0xB0

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Delay on right VCR channel, expressed in number of group of 16 samples. RSDLY = delay (ms) * Fs (kHz) / 16.

When only one VCR channel is used, this register must be reset at initialization.

**UPDATE**

**PCM delay update**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   | TM | DLY |

Address: 0x5D

Type: R/W

Software Reset: NC

Hardware Reset: UND

Software Reset: 0

Hardware Reset 0

Description:

| Bitfield | Description |
|---|---|
| DLY | This bit must be set to 1 to force the DSP to update its delays values (read from the audio delay registers).<br><br>**0:** Delay values held in the audio delay registers are NOT updated in the DSP (i.e. the DSP will keep the delay values set previously)<br><br>**1:** The delay values held in the audio delay registers are updated in the DSP (i.e. the DSP will use the new values). This bit is automatically reset to zero after it the update has been carried out. |
| TM | Set to "0" |

## 9.8  SPDIF output set-up

**SPDIF_CMD**

**SPDIF control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AUX | reserved | | | | | SPDIF_MODE[1:0] | |

Address: 0x5E

Type: R/W

This register controls the SPDIF mode:

Description:

| Bitfield | Description |
|---|---|
| SPDIF_MODE[1:0]<br>AUX = '0' | 00:  OFF, the IEC60958 is not working and the output line is idle,<br>01:  MUTE, the outputs are PCM null data,<br>10:  PCM, the outputs are PCM data and only the Left/Right channels are transmitted,<br>11:  EMC, in this "encoded" mode the compressed bitstream is transmitted in IEC61937 standard. |
| SPDIF_MODE[1:0]<br>AUX = '1' | 10:  PCM, the outputs are PCM data and only the "VCR" channels are transmitted.<br>All other values are reserved. |

**Category code**

**SPDIF_CAT**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CATCODE | | | | | | | |

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Address: 0x5F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

The table below defines the category codes, values not listed are reserved.

| Category code | Description | |
|---|---|---|
| 0 0 0 0 0 0 0 | General | |
| 1 0 0 0 0 0 0 | Experimental | |
| X X X 0 0 0 0 | Reserved | |
| X X X 1 0 0 0 | Solid State Memory | |
| 0 0 0 0 1 0 0 | Broadcast reception of dig. audio | Japan |
| 1 1 0 0 1 0 0 | Broadcast reception of dig. audio | United states |
| 0 0 0 1 1 0 0 | Broadcast reception of dig. audio | Europe |
| 1 0 0 0 1 0 0 | Broadcast reception of dig. audio | Electronic Software delivery |
| X X X X 1 0 0 | Broadcast reception of dig. audio | All other states are reserved |
| 0 0 0 0 0 1 0 | Digital / Digital converters and signal processing | PCM encoder/decoder |
| 0 1 0 0 0 1 0 | Digital / Digital converters and signal processing Digital / Digital | Digital sound sampler |
| 0 0 1 0 0 1 0 | converters and signal processing r | Digital signal mixe |
| 0 0 1 1 0 1 0 | Digital / Digital converters and signal processing | Sample rate converter |
| X X X X 0 1 0 | Digital / Digital converters and signal processing | All other states are reserved |
| X X 0 0 1 1 0 | A/D converter W/o copyright | |
| X X 1 0 1 1 0 | A/D converter W/ copyright (using copy and L bits) | |
| X X X 1 1 1 0 | Broadcast reception of dig. audio | |
| 0 0 0 0 0 0 1 | Laser optical CD - Compatible with IEC 908 | |
| 0 0 0 1 0 0 1 | Laser optical CD - Not compatible with IEC 908 (Magneto optical) | |
| X X X X 0 0 1 | Laser optical    All other states are reserved | |
| 0 0 0 0 1 0 1 | Musical instruments, microphones, etc. | Synthesizer |
| 0 0 0 1 1 0 1 | Musical instruments, microphones, etc. | Microphone |
| X X X X 1 0 1 | Musical instruments, microphones, etc. | All other states are reserved |
| 0 0 0 0 0 1 1 | Magnetic tape or disks | DAT |
| 0 0 0 1 0 1 1 | Magnetic tape or disks | Digital audio sound VCR |
| X X X X 0 1 1 | Magnetic tape or disks | All other states are reserved |
| X X X X 1 1 1 | Reserved | |
| 7<br>0<br>1 | Only cat. codes XXXX100, XXX1110, XXXX001 -> L bit<br>Original, commercially pre-recorded data<br>No indication of 1st generation or higher | |
| 7<br>0<br>1 | All other categories<br>No indication of 1st generation or higher<br>Original, commercially pre-recorded data | |

### SPDIF_CONF
### SPDIF PCMCLK divider

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LAT | SM=0 | RND | DIV[4:0] | | | | |

Address: 0x60

Type: R/W

Software Reset:NC

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Hardware: Reset:UND

Description:

| Bitfield | Description |
|---|---|
| DIV[4:0] | This field is the DAC_PCMCLK divider. It must be set according to the formula:<br>in 16 bit mode: IECDIV=(1+PCMDIV)/2-1; in 32 bit mode: IECDIV=PCMDIV |
| RND | This bit is used to have a "16-bit rounding" on the SPDIF (when in PCM mode):<br>0:  no rounding,<br>1:  rounding.<br>This bit has no effect on the precision of analogue data |
| SM | SYNC MUTE Mode, must be set to zero. |
| LAT | Configures the latency mode between the SPDIF output (in mode compressed) and the Audio output.<br>0: Auto-Latency: The latency is the transmission time for 2/3 of the payload, plus the time to decode an audio block.<br>For MPEG Auto-Latency, the latency is the following time depending of the sampling frequency in the incoming bitstream: MPEG 48KHz: 20.90ms, MPEG 44.1KHz: 22.95ms, MPEG 32KHz: 32.53ms.<br>1: User-programmable latency - the      SPDIF_LATENCY register is used. |

The table below shows the relationship between the value of the IEC divider and the value of the PCM divider.

| PCM Divider Value | Mode Description | IEC Divider Value |
|---|---|---|
| 5 | DAC_PCMCLK = 384Fs, DAC is 16-bit mode | 2 |
| 3 | DAC_PCMLK = 256 Fs, DAC is 16-bit mode | 1 |
| 2 | DAC_PCMLK = 384 Fs, DAC is 32-bit mode | 2 |
| 1 | DAC_PCMLK = 256 Fs, DAC is 32-bit mode | 1 |

## SPDIF_STATUS
### SPDIF status bit

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | SFR | | | PRE | COP | COM |

Address: 0x61

Type: R/W

Software Reset: NC

Hardware: Reset UND

Description:

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This register is used to set the value of the status bit in the IEC958 data stream.

| Bitfield | Description |
|----------|-------------|
| COM | Compress data bit.<br>1: compressed mode<br>0: non compressed mode. |
| COP | 1: copy allowed<br>0: copy not allowed |
| PRE | 1: output has pre-emphasis<br>0: output does not have pre-emphasis |
| SFR | 0000: if sampling frequency = 44.1KHz<br>0010: if sampling frequency = 48KHz<br>0011: if sampling frequency = 32KHz<br>1010: if sampling frequency = 96KHz |

**SPDIF_REP_TIME**

**SPDIF repetition time of a pause frame**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x75

Type: R/W

Software Reset: NC

Hardware: Reset: UND

Description:

In compressed mode, a burst of pause frames is sent when there are no more data to transmit (due to an error or a gap in the incoming bitstream, for example).

This register sets the size of a pause frame in IEC frames: Dolby Digital =4, MPEG=32 and DTS=3.

**SPDIF_LATENCY**

**Latency value**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Value | | | | | | | |

Address: 0x7E

Type: R/W

Software Reset: NC

Hardware: Reset: UND

Description:

If bit LAT of register SPDIF_CONF is set, a delay can be configured between the output of IEC61937 in compressed mode and the output of the audio decoder. To configure a latency (in unit of seconds) this register has to be set according the following formula:

Value = L x FS/8 where, L=Latency in s and FS=Sampling frequency in Hz

The minimum latency delay is 0; the maximum latency delay is the time to decode a frame:

| Bitfield | Description |
|---|---|
| Value | Dolby Digital: L = 1536 samples / Sampling frequency<br>MPEG:          L = 1152 samples / Sampling frequency |

## SPDIF_DTDI

**SPDIF data-type information**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PFC | DTD | | INF | | | | |

Address: 0x7F

Type: R/W

Software Reset: NC

Hardware: Reset: UND

Description::

| Bitfield | Description | | | | | |
|---|---|---|---|---|---|---|
| DTDI[4:0] | in Dolby Digital mode: | 4 | 3 | 2 | 1 | 0 |
| | | 0 | 0 | BSMOD [2..0] | | |
| | in MPEG mode: | 4 | 3 | 2 | 1 | 0 |
| | | 0 | 0 | 0 | DR | K |
| DTD | 1: Data-type dependent information used for the SPDIF in compressed mode, can be set by the user.<br>Refer to IEC958 standard for more information.<br><br>0: Transmitted DTDI are extracted from the stream. | | | | | |
| PFC | 1: PCMCROSS function enabled | | | | | |

## AUTODETECT_ENA

**S/PDIF Autodetection Enable**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | ENA |

Address: 0xE0

Type: R/W

Software Reset: 0

Hardware: Reset: UND

Description:

The feature is only available for STA310 cut 2.0. This register is used to enable the autodetection on the S/PDIF. When high, the autodetection is present. When low, autodetection is disable.

The STA310 cut 2.0 is able to detect the following audio format changes on the S?PDIF input.

| FROM | TO |
|---|---|
| AC3 | PCM |
| AC3 | MPEG |
| MPEG | AC3 |
| MPEG | PCM |
| PCM | AC3 |
| PCM | MPEG |

The host must respond to the RST and LCK interrupt in order for the STA310 to take into account the change of the audio format.

## AUTODETECT_SENS

**S/PDIF Autodetection Sensitivity**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | SENS | | | | |

Address: 0xE1

Type: R/W

Software Reset: 0

Hardware: Reset: UND

Description:

The feature is only available for STA310 cut 2.0. This register is used to configure the autodetection sensitivity. The lower is SENS, the faster is the autodetection. Typical value is 0.

## AUTODETECT_ ALIGN

**S/PDIF Autodetection Alignement**

Address: 0xE2

Type: R/W

Software Reset: 0

Hardware: Reset: UND

Description:

**STA310**

The feature is only available for STA310 cut 2.0. This register is used to configure the Left/Right sample alignement of the S/PDIF. Typical value is 10

■ When in idle mode, the PLAY value is not taken into account by the decoder.

■ When in init mode, the PLAY value is not taken into account by the decoder.

■ When in decode mode, PLAY enables the decoding, see table below:

### 9.9  Audio command registers
### SOFTRESET
**Soft reset**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x10

Type: W0

Software Reset: NA

Hardware: Reset: NA

Description:

When bit 0 of this register is set, a soft reset occurs.

The command registers and the interrupt registers listed below are cleared.

The decoder goes into idle mode and the volumes are cleared.

Command registers:
MUTE, RUN, PLAY, SKIP_MUTE_CMD and SKIP_MUTE_VALUE

Interrupt registers:
INTE, INT and ERROR

### PLAY
**Play**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | PLAY |

Address: 0x13

Type: R/W

Software Reset: 0

Hardware: Reset: 0

Description:

The PLAY command is treated according to the state of the decoder:

| PLAY value | MUTE value | DAC_SCLK, DAC_LRCLK state | DAC_PC MOUT | Decoding |
|---|---|---|---|---|
| 0 | 0 | Not running | 0 | No |
| 0 | 1 | Running | 0 | No |
| 1 | 0 | Running | Decoded samples | Yes |
| 1 | 1 | Running | 0 | Yes |

### MUTE
**Mute**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | MUTE |

Address: 0x14

Type: R/W

Software Reset: 0

Hardware: Reset: 0

Description:

The MUTE command is handled differently according to the state of the decoder:

■ When in idle mode after hardware reset, setting MUTE to "1" automatically runs the DAC_SCLK and DAC_LRCLK clocks and outputs them to the DACs.

■ When playing, setting MUTE to "1" mutes the PCM outputs.

■ The MUTE register has no effect on the SPDIF output.

### RUN
**RUN decoding**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   | RUN |

Address: 0x72

STA310

Type: R/W

Software Reset: 0

Hardware Reset: 0

Description:

This register enables to exit from idle mode. After a soft or hard reset the decoder is in idle mode. It stays in this mode until the RUN is set.

In run mode the decoder takes into account the state of all the configuration registers and begins to decode.

The RUN register can only be reset by the SOFTRESET command.

### SKIP_MUTE_CMD
### Skip or mute commands

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | MUTE | reserved | PAU | BLK | SKP | SMUT |

Address: 0x73

Type: R/W

Software Reset: 0

Hardware Reset: 0

Description:

This register cannot be used in MP3 decoding mode.The register is taken into account at a beginning of decoding a frame.

| Value | Description |
|---|---|
| SMUT, MUTE | If one or both of these bits is '1' then the decoder continues the normal decoding process, but the output samples are soft-muted to zero. When both these bits are '0' muting is disabled and the decoder plays the incoming frame. |
| SKP | Skip frame. The decoder skips the number of frames programmed in register |
| BLK | Pause block.  The decoder introduces a delay equal to the number of blocks programmed in register |
| PAU | The decoder is stopped whilst this bit is '1'. |
| Reserved | Set to '0'. |

### SKIP_MUTE_VALUE

### Skip frames or mutes blocks of frame

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address* + 0x74

Type: R/W

Software Reset: 0

Hardware Reset:0

Description:

The value in this register gives either the number of frames to skip or the number of blocks during which the decoder will be stopped. This is used in conjunction with register .

### 9.10 Interrupt register
### INTE
### Interrupt enable

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| @0x08 | | | | INTE[15:8] | | | | |
| @0x07 | | | | INTE[7:0] | | | | |

Address: 0x08 - 0x07

Type: R/W

Software Reset: 0

Hardware Reset: 0

Description:

This register is used to enable each interrupt independently. Setting a bit in the register enables the corresponding interrupt.

### INT
### Interrupt

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| @0x0A | | | | INTE[15:8] | | | | |
| @0x09 | | | | INTE[7:0] | | | | |

Address: 0x0A - 0x09

Type: RO

Software Reset: 0

Hardware Reset:0

## STA310

Description: These registers indicate which interrupt occurred. Provided an interrupt is enabled through the register INTE, if the corresponding bit of INT is set, the corresponding interrupt has occurred. The signal IRQ is activated whenever one of the bits of INT become set. Depending on the nature of the condition, clearing a bit in INT register is performed by either reading the MSB of INT register, or by reading the MSB of the associated condition registers (see below). This register is reset by software reset.
The table below shows the interrupt nature indicated by each bit..

| Bit Numer | Name | Condition Signalled |
|---|---|---|
| 0 | SYN | Change in Synchronization Status [1] |
| 1 | HDR | Valid Header Registered [1] |
| 2 | ERR | Error Detected [1] |
| 3 | SFR | Sampling frequency changed [2] |
| 4 | DEM | De-emphasis Changed [2] |
| 5 | BOF | First Bit of New Frame at Output Stage [2] |
| 6 | PTS | First Bit of New Frame with PTS at Output Stage [2] |
| 7 | ANC | Not implemented |
| 8 | PCM | PCM Output Underflow [2] |
| 9 | FBF | Frame Buffer Full: The frame buffer memory contains 2 frames: one decoded, and one parsed for next decoding |
| 10 | FBE | Frame Buffer Empty: The frame buffer memory contains 1 frame which begins to be decoded. The next frame begins to be parsed |

| Bit Numer | Name | Condition Signalled |
|---|---|---|
| 11 | FIO | FIFO Input has Overflowed [2] |
| 12 | RST[3] | The STA310 has detected a change in the incoming audio format. The soft Reset produce must be applied and the device must be re-initialized according to the new audio format detected. Registers DECODESEL (0x4d) and STREAMSEL (0x4c) contain the new audio format [1] |
| 13 | LCK[3] | A break has occurred in the S/PDIF stream causing the internal S/PDIF PLL to get unlocked. The soft reset procedure must be applied and the device must be re-initialized according to the current audio format decoding contained in the registers DECODESEL (0x4d) and SRTREAMSEL (0x4c). [1] |
| 14 | USD | Reserved |
| 15 | TBD | Reserved |

Notes:  1.  Cleared when a reset occurs or when the MSB of the interrupt register is read
2.  Cleared when a reset occurs or when the MSB of the corresponding register is read. Affected registers are listed in the following table
3.  Only available in STA310 cut 2.0

| Address | Name |
|---|---|
| 0x0F | ERROR |
| 0x40 | SYNCSTATUS |
| 0x41 | ANCCOUNT |
| 0x42 | HEAD 4 |
| 0x46 | PTS [32] |

### 9.11 Interrupt status registers
### SYNC_STATUS
### Synchronization status

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   | PAC | | FRA | |

*Address:* 0x40

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

This register indicates the status of the audio parser for synchronization. It is used in conjunction with PACKET_LOCK and SYNCK_LOCK registers. On read the synchronization status interrupt bit is cleared (INT.SYN is cleared).

| Bitfield | Description |
|---|---|
| FRA | Frame Status<br>0 0: Research audio synchronization<br>0 1: Wait for confirmation - a synchro word has been detected but the parser has not yet detected SYNC-LOCK+1    synchro words.<br>1 0: Synchronized - SYNC_LOCK + 1 synchro words have been detected<br>1 1: Not used |
| PAC | Packet Status<br>0 0: Research packet synchronization word<br>0 1: Wait for confirmation - - a synchro word has been detected but the parser has not yet detected<br>    PACKET_LOCK+1 synchro words.<br>1 0: Synchronized - PACKET_LOCK + 1 synchro words have been detected<br>1 1: Not used |

## ANCCOUNT
### Ancillary data

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|  |  |  |  |  |  |  |  |

*Address*: 0x41

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

This value gives the number of ancillary data in the stream. The ancillary data interrupt bit ANC of the register is cleared by a read.

## HEAD4
### HEADER 4 register

AC_3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | | BSMOD | |

MPEG_2

| 0 | 0 | 0 | 0 | 0 | 0 | DR | K |
|---|---|---|---|---|---|---|---|

OTHER

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

*Address:* 0x42

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

This register contains header data HEAD[31:24]. The contents depend on the type of the frame.HEAD4[7:3] = 00000, in all cases.

When the host reads this register, the corresponding interrupt bit (HDR) is cleared.

Dolby Digital

| Bitfield | Description |
|---|---|
| HEAD4[2:0] | BSMOD if an Dolby Digital frame |

MPEG-2

| Bitfield | Description |
|---|---|
| HEAD4[2] | 0 |
| HEAD4[1] | DR=1 Dynamic range exists |
| HEAD4[0] | K=0 in normal mode, K=1 in Karaoke mode. |

OTHER

In all other types of frame HEAD4[2:0] = "000"

## HEAD3
### HEADER 3 register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | DTYPE | | |

*Address:* 0x43

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

**STA310**

This register contains header data HEAD[23:16].HEAD3[7:5]="000", in all cases HEAD3[4:0] = DTYPE

DTYPE is the data type and is defined as follows:

| Bit | Description | |
|-----|-------------|---|
| DTYPE | 0000: | Null data or Linear PCM |
| | 0001: | Dolby Digital |
| | 0100: | MPEG-1 Layer I |
| | 0101: | MPEG-1 Layer II or MPEG-2 word extension |
| | 0110: | MPEG-2 Layer II with extension |
| | 1001: | MPEG-2 Layer II low sample rate |
| | (11) 1011: | DTS-1 (Frame Size 512) |
| | (12) 1100: | DTS-2 (Frame Size 1024) |
| | (13) 1101: | DTS-3 (Frame Size 2048) |

This register can not detect the data-type of data in a stream.

**HEADLEN**

**Frame length**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HEADLEN[15:8] | | | | | | | |
| HEADLEN[7:0] | | | | | | | |

*Address*: 0x44 - 0x45

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

The HEADLEN register contains the bit length of the compressed data frame HEAD[15:0]. HEADER registers are all updated as soon as the decoder begins to decode a frame.

**PTS**

**PTS**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| **0x46** | | | | | | | | PTS[32] |
| **0x47** | PTS[31:24] | | | | | | | |
| **0x48** | PTS[23:16] | | | | | | | |
| **0x49** | PTS[15:8] | | | | | | | |
| **0x4A** | PTS[7:0] | | | | | | | |

*Address:* 0x46 to 0x4A

Type: R/W

Software Reset: UND

Hardware Reset: UND

Description:

When the PTS interrupt is activated, a new PTS value is stored in this register. Once the PTS[32] value is read bit PTS of the PTS register is cleared.

**ERROR**

**ERROR code**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address* + 0x0F

Type: RO

Software Reset: 0

Hardware Reset:0

Description:

This is a status register, when read by the ST20, this and the corresponding interrupt register are cleared. This 7-bit register is ANDed with 0x7F to get the correct value. The value in the ERROR register indicates the type of error that has occurred. These errors are defined in the table below.

| Error Name | Value (decimal) |
|------------|-----------------|
| **Dolby Digital decoding** | |
| No error | 0 |
| EXPAND_DELTA_PAST_END_ARRAY | 1 |
| XDCALL_TRY_TO_REUSE_REMAT_FLG | 2 |
| XDCALL_TRY_TO_REUSE_COUPLING_STRA | 3 |
| XDCALL_CANT_COUPLE_IN_DUAL_MODE | 4 |
| XDCALL_TRY_TO_REUSE_CPL_LEAK | 5 |
| XDCALL_TRY_TO_REUSE_SNR | 6 |
| XDCALL_TRY_TO_REUSE_BIT_ALLOC | 7 |
| XDCALL_TRY_TO_REUSE_COUPLING_EXPONENT_STRA | 8 |
| XDCALL_TRY_TO_REUSE_EXPONENT_STRA | 9 |
| XDCALL_TRY_TO_REUSE_LFE_EXPONENT_STRA | 10 |
| XDCALL_CHBWCOD_IS_TOO_HIGH | 11 |

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| Error Name | Value (decimal) |
|---|---|
| BSI_ERR_REV | 12 |
| BSI_ERR_CHANS | 13 |
| CRC_NOT_VALID | 14 |
| Packet Synchronization | |
| SYNCHRO_PACKET_NOT_FOUND | 16 |
| BAD_MPEGI_RESERVED_WORD | 17 |
| BAD_MPEG2_RESERVED_WORD | 18 |
| BAD_LPCM_SYNCHRO | 19 |
| UNKNOWN_STREAM_ID | 20 |
| MARKER_ERROR | 21 |
| UNKNOWN_SUB_STREAM_ID | 22 |
| IEC958_INPUT_MISMATCH_CONF | 23 |
| IEC958_MPEG2_LAYERI_NOT_SUPPORTED | 24 |
| IEC958_PAUSE_FRAME_NOT_SUPPORTED | 25 |
| IEC958_BAD_DATA_TYPE_DEPENDANT | 26 |
| MISMATCH _HOST_SEL_CONFIGURATION | 27 |
| **Audio Synchronization** | |
| SYNCHRO_AUDIO_NOT_FOUND | 32 |
| BAD_CRC_AC3 | 33 |
| BAD_LPCM_QUANTIZATION_WORDLENGTH | 34 |
| BAD_AUDIO_SAMPLING_FREQUENCY | 35 |
| BAD_MPEG_LAYER | 36 |
| MPEG_BITRATE_FREE_FORMAT | 37 |
| NOT_SUPPORTED_AC-3_FRMSIZECOD | 38 |
| BAD_CRC_MPEG_EXTENDED | 39 |
| BAD_MPEG_EXTENDED_RESERVED_BIT | 40 |
| MPEG_EXTENDED_SYNC_NOT_FOUND | 41 |
| MPEG_EXTENDED_LENGTH_TOO_SMALL | 42 |
| BAD_SAMPLES_PER_CHANNEL | 44 |
| BAD_FRAME_BIT_SIZE | 45 |
| **MPEG Decoding** | |
| MPEG_EXTENSION_ERROR | 48 |
| MPEG_MC_MUTE | 49 |
| NOT USED | 50 |
| NOT USED | 51 |
| MPEG_LAYER_ERROR | 52 |
| MPEG_CHCONFIG_ERROR | 53 |
| MPEG_MC_PREDICTION_ERROR | 54 |
| MPEG_CRC_ERROR | 55 |
| MPEG_EXT_CRC_ERROR | 56 |
| MPEG_TOO_SMALL_FOR_MC_HEADER | 57 |

| Error Name | Value (decimal) |
|---|---|
| MPEG_BITRATE_ERROR | 58 |
| **MP3 Decoding** | |
| CRC_ERROR | 01 |
| DATA_AVAILABLE_ERROR | 02 |
| ANC_PARTIAL_READ_ERROR | 03 |
| ANC_NOT_READ_ERROR | 04 |
| BAD_ID_AND_IDEX_VALUES | 33 |
| LAYER_IS_NOR_LAYER3 | 34 |
| **BAD_audio_sampling_freq** | 35 |
| FREE_FORMAT_NOT_SUPPORTED | 36 |
| BIT_RATE_NOT_SUPPORTED | 37 |
| BIG_VALUE_ERROR | 48 |
| MODE_CHANGE_ERROR | 49 |
| FS_CHANGE_ERROR | 50 |
| **Miscellaneous** | |
| IEC_958_READ_ERROR | 64 |
| MPEG_FB_BYPASS_AREA_ERROR | 65 |
| SKIPPING_BITS_IN_FB_ERROR | 66 |
| LATENCY_TOO_BIG | 67 |
| SKIP_MUTE_ERROR | 68 |
| UNKNOW_SFREQ_FOR_LATENCY | 69 |
| LATENCY_TOO_SMALL | 70 |
| BAD_INPUT_CHAN | 71 |
| INVALID_ALPHA_COEFF | 72 |

### 9.12 Decoding algorithm registers

The table below shows how the STREAMSEL and DECODSEL registers should be programmed for different types of bitstream.

**Table 9.**
**STREAMSEL and DECODESEL programming definitions**

| STREAMSEL (0x4C) | DECODSEL (0x4D) | Mode |
|---|---|---|
| 0 | 0 | MPEG2 PES carrying Dolby Digital (ATSC) |
| 0 | 1 | MPEG2 PES carrying MPEG1 frames |
| 0 | 2 | MPEG2 PES carrying MPEG2 frames |
| 1 | 0 | MPEG2 PES carrying Dolby Digital frames for DVD video |

**STA310**

| 1 | 2 | MPEG2 PES carrying MPEG2 frames for DVD video |
|---|---|---|
| 1 | 3 | MPEG2 PES carrying linear PCM for DVD video |
| 2 | 1 | MPEG1 packet carrying MPEG1 audio |
| 3 | 0 | Dolby Digital frames elementary streams |
| 3 | 1 | MPEG1 frame elementary streams |
| 3 | 2 | MPEG2 frame elementary stream |
| 3 | 3 | Stereo PCM (16bits samples) and PCM2 channels |
| 3 | 4 | Pink noise generator |
| 3 | 5 | CDDA (Stereo PCM 16 bits samples) |
| 3 | 7 | Activate PCM beep tone |
| 3 | 9 | MP3 elementary streams |
| 5 | 0 | IEC61937 Input with Dolby Digital frames |
| 5 | 1 | IEC61937 Input with MPEG1 frames |
| 5 | 2 | IEC61937 Input with MPEG2 frames |
| 5 | 6 | IEC61937 Input with DTS frames |
| 6 | 3 | Linear PCM for DVD audio |

**DECODSEL**

**Decoding algorithm**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   | DEC |   |   |

*Address:* 0x4D

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register identifies the audio data-type.

| Bitfield | Description |
|---|---|
| DEC[3:0] | 0000: Dolby Digital Decoding<br>0001: MPEG1<br>0010: MPEG2<br>0011: PCM/LPCM<br>0100: PINK NOISE generator<br>0101: CD_DA<br>0111: PCM beep tone generator<br>1001: MP3 |

**STREAMSEL**

STREAM selection

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   | STRSEL |   |   |

*Address:* 0x4C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| STRSEL | 000: PES<br>001: PES DVD video<br>010: Packet MPEG1<br>011: Elementary Stream/IEC60958<br>100: Reserved<br>101: SPDIF IEC61937<br>110: PES DVD audio |

**9.13 System synchronization registers**
**PACKET_LOCK**

**Packet lock**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address:* 0x4F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register specifies the number of supplementary packet synchro words that the packet parser must detect before it is considered as synchronized, and can send data to the audio parser (max=1, min=0). In this way, stream data can not be sent to the audio parser instead of packet sync words.

PACKET_LOCK = 0: the packet parser is synchronized when it has detected one packet synchro word.

PACKET_LOCK = 1: the packet parser is synchronized when it has detected two packet synchro words.

### ID_EN
**Enable audio ID**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address:* 0x50

Type: R/W

Software Reset: NC

Hardware Reset:UND

Description:

If set to 1, the audio decoder decodes only the stream corresponding to the stream-id or sub-stream-id of the packet layer. This selection is done through AUDIO_ID or AUDIO_ID_EXT registers. If set to 0, the decoder decodes all the audio packets.

### ID
**Audio ID**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address* : 0x51

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

When decoding packets, it is possible to specify an identifier for a selected program. AUDIO_ID must be written with the packet ID. This feature is enabled when the register AUDIO_ID_EN is set, and only packets with matching ID are decoded.

For MPEG1 packets or PES, the 5 LSB bits are significant. For DVD PES (LPCM, Dolby Digital or MPEG), the 3 LSB bits are significant (see audio pack definition in DVD specifications).

These bits correspond to the stream number defined in the STREAM_ID field of the audio packet header, except for DVD, Dolby Digital or LPCM packets, where they correspond to the stream number defined in the SUB_STREAM_ID field.

### ID_EXT
**Audio extension**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address* + 0x52

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

The 3 LSB bits of this register are significant. In case of DVD MPEG2 audio with extension bitstream (see DVD specifications), this register is used to select the stream defined in the STREAM_ID of the packets containing MPEG2 extension bit stream data.

### SYNC_LOCK
**SYNC lock**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

Address: 0x53

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register specifies the number of supplementary audio synchro words that the audio parser must detect before it is considered as synchronized, and can send data to the decoder.

In this way, stream data can not be sent to the decoder instead of audio sync words. Max value = 3; min value = 0. SYNC_LOCK = 0, the audio parser is synchronized when it has detected one audio synchro word. SYNC_LOCK = n > 0, when the audio parser has detected one synchro word, it waits until it detects n supplementary audio sync words.

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When it has detected (SYNC_LOCK+1) sync words, it sends the data to the decoder.

### 9.14 Post decoding and pro logic registers PDEC1

**Post decoder register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VMAX | | DEM | DCF | DB | PVIRT | MPEG_DR | PL |

*Address:* 0x62

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register controls the post decoder operations.

| Bitfield | Description |
|---|---|
| PL | When high Pro Logic decoding is forced, when low the ProLogic decoder is automatically enabled when the stream contains the info that it is ProLogic encoded |
| MPEG_DR | When high enable MPEG dynamic range. |
| DB | When high the "double stereo" procedure is enabled. Double stereo is a copy of Left/Right channels on to Left/Right surround channels in order to have a pseudo 5-channel decoder effect. |
| DCF | When set the DC filter is activated.. When reset, it is disabled. |
| DEM | When set the de-emphasis filter is activated.. When reset, it is disabled. |

### PL_AB

**Pro Logic auto balance**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | PL_WS | PL_AB |

*Address* : 0x64

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| PL_AB | When high, select the auto-balance function (used to track out gin mismatches between Lt and Rt).When low, disable the autobalance function |
| PL_WS | When high, enable Wide Surround mode. The wide surround option is provided for users who plan to do further post-processing of the Pro Logic outputs, and want to fold the lowpass filtering of the surround channel into their downstream processing Lowpass filtering and B-type shelf filtering are both disabled. When low, disable ide surround mode. |

### PL_DWNX

**Pro Logic Decoder Downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | LFE_BYP | PL_DWNX[2:0] | | |

*Address* : 0x65

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| PL_DWNX [2:0] | 0,1,2: Pro Logic disabled<br>3: 3/0 (L, R, C) three stereo<br>4: 2/1 (L, R, Ls) phantom<br>5: 3/1 (L, C, R, Ls)<br>6: 2/2 (L, R, Ls, Rs) phantom<br>7: 3/2 (L, C, R, S, S) |
| LFE_BYP | 0:  LFE channel is clear<br>1:  LFE channel is bypassed |

Prologic decoder support only 4 sampling frequencies: 48KHz, 44.1KHz, 32KHz, 22.05KHz.

If we active prologic with sampling frequency different from those frequencies, the decoder will be automatically disable the prologic call.

### OCFG

**Output Configuration**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LFE_BYP | BOOST | | | | OCFG[2:0] | | |

*Address:* 0x66

Type: RW

Software Reset: NC

Hardware Reset: UND

Description:

6 output configurations are provided that redirects bass on subwoofer channel, and applies some filters on channels.

The description is provided in the output configuration section.

This register is used to indicate the output configuration chosen.

- LP means Low pass filter

- HP means High pass filter

| Bitfield | conf | Meaning | Description |
|---|---|---|---|
| OCFG[2:0] | | | Bass management configuration according to the bass direction scheme from Dolby. For configurations 2,3,4 the subwoofer can be output is bit LFE asset to high. For all other configurations, the LFE bit has no effect. |
| | 0 | ALL | All channels are rounded according to the selected output precision, (24b -> 16b, 24 -> 18b.) and scaled (volume control) only. |
| | 1 | LSW | Low frequencies are extracted from the six input channels and redirected to the subwoofer. SUB = LP(L+R+Ls+Rs+C+LFE).Low frequencies are removed from all channels L = HP(L), R = HP(R), C = HP(C), Ls = HP(Ls), Rs = HP(Rs). |
| | 2 | LLR | Low frequencies are extracted from C, LFE, Ls and Rs channels and redirected to left and right channels: C = HP (C), Rs = HP (Rs), Ls = HP(Ls), L = L + LP (C+LFE+Ls+Rs), R = R + LP(C+LFE+Ls+Rs). If subwoofer is output, SUB = LP (LFE+C+Ls+Rs). |
| | 3[1] | SLP | Low frequencies are redirected to the left, right and surround channels or cab be output on the subwoofer.<br>If sub-woofer is output, SUB = LFE, L = L + LP(C), R = R + LP(C), Ls = Ls, Rs = Rs<br>If sub-woofer is not output, L = L + LP(C) + LFE, R = R + LP(C) + LFE, Ls = Ls + LFE, Rs = Rs + LFE. |
| | 4 | SIMP | Simplified configuration. Low frequencies are exrtacted from C, Ls, Rs and LFE.<br>If subwoofer is output, SUB = LP(C+Ls+Rs) + LFE, L = L, R = R.<br>If sub-woofer is not output, SUB = LFE, L = L + (C+Ls+Rs), R = R + (C+Ls+Rs). |
| | 5 | BYP | BYPASS, All channels are directly routed to PCM outputs. |
| | 6 | | configuration 1 without filters. |
| BOOST[1] | Channel level, enables boost:<br>if OCFG_num = 2 :<br>  0 : No +12dB boost on left and right channels<br>  1 : +12dB boost on left and right channels<br><br>When configuration = 3 :<br>  If sub-woofer is output :<br>    0 : No +4dB boost on all channels<br>    1 : +4dB boost on all channels<br>  If sub-woofer is not output :<br>    0 : No +8dB boost on all channels<br>    1 : +8dB boost on all channels | | | |
| LFE_BYOP | 0; LFE channel is clear<br>1: LFE channel is bypassed | | | |

Note:   1. In configuration 3 with subwoofer enabled, the output of the subwoofer is 10dB greater than expected. Therefore when using this mode, the subwoofer output level needs to be attenuated 10dB in order to match the subwoofer output levels of other bass management configurations. In general be carefull while using the boost option since it has the potential of causing the woofer output to overload

**DWSMODE**

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**Downsampling filter**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address:* 0x70

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register controls the downsampling filter for the LPCM video, LPCM audio modes. When decoding a 96kHz DVD-LPCM stream, it might be necessary to downsample the stream to 48kHz**.**

| Value | Mode |
|---|---|
| 0 | Automatic (according to bitstream) |
| 1 | Force Downsampling |
| 2 | Suppress Downsampling |

### 9.15 Bass redirection registers
**VOLUME0**

**Volume of first channel**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | AVol0 | | | | |

*Address:* 0x4E

Type: RWS

Software Reset: 0

Hardware Reset: UND

Description:

This register reads or writes the attenuation that is applied to the channel selected by CHAN_IDX. The volume of the left channel can be set up with a 0.5dB step.

- If CHAN_IDX = 0, then VOLUME0 can be written with the attenuation that will be applied to Left channel.
- If CHAN_IDX = 1, then VOLUME0 can be written with the attenuation that will be applied to Center channel.

- If CHAN_IDX = 2, then VOLUME0 can be written with the attenuation that will be applied to Left Surround channel.
- If CHAN_IDX = 5, then reading VOLUME0 provides the attenuation that is applied to Left channel.
- If CHAN_IDX = 6, then reading VOLUME0 provides the attenuation that is applied to Center channel.
- If CHAN_IDX = 7, then reading VOLUME0 provides the attenuation that is applied to Left Surround channel.
- Other values of CHAN_IDX are reserved.

**VOLUME1**

**Volume of second channel**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | AVol1 | | | | |

*Address:* 0x63

Type: RWS

Software Reset: 0

Hardware Reset: UND

Description:

This register reads or writes the attenuation that is applied to the channel selected by CHAN_IDX. The volume of the right channel can be set up with a 0.5dB step.

- If CHAN_IDX = 0, then VOLUME1 can be written with the attenuation that will be applied to Right channel.
- If CHAN_IDX = 1, then VOLUME1 can be written with the attenuation that will be applied to Subwoofer channel.
- If CHAN_IDX = 2, then VOLUME1 can be written with the attenuation that will be applied to Right Surround channel.
- If CHAN_IDX = 5, then reading VOLUME1 provides the attenuation that is applied to Right channel.
- If CHAN_IDX = 6, then reading VOLUME1 provides the attenuation that is applied to Subwoofer channel.
- If CHAN_IDX = 7, then reading VOLUME1 provides the attenuation that is applied to Right Surround channel.
- Other values of CHAN_IDX are reserved.

**CHAN_IDX**

**Channel Index**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | CHAN_IDX | | |

*Address:* 0x67

Type: R/W

Software Reset: 4

Hardware Reset: UND

Description:

This register identifies the pair of channels and the type of access:

| Bitfield | value | Channel pair | Access | comment |
|---|---|---|---|---|
| CHAN_IDX | 0 | Left and Right | write | |
| | 1 | Center and Subwoofer | write | |
| | 2 | Left surround and right surround | write | |
| | 3 | reserved | reserved | |
| | 4 | no pair selected | none | Indicates that volume can be read or written |
| | 5 | Left and Right | read | |
| | 6 | Center and Subwoofer | read | |
| | 7 | Left surround and right surround | read | |

■ To read a volume, the register   CHAN_IDX must be set to the appropriate value. The DSP indicates that the attenuation is readable through registers   VOLUME0 and VOLUME1 by changing automatically the CHAN_IDX to value 4.

■ To write a volume, the attenuation of the pair of channel should be written in   VOLUME0 and VOLUME1 registers. Then the   CHAN_IDX register is written to the appropriate value. The attenuation is updated on the next audio block

and    CHAN_IDX value is automatically changed to 4.

### 9.16 Dolby Digital configuration registers

**AC3_DECODE_LFE**

**Decode LFE**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address:* 0x68

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

When this register is set to 1, the device decodes LFE channel (if present).

**AC3_COMP_MOD**

**Compression mode**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address* + 0x69

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

The value of this register defines the compression mode. In custom A mode, the dialog normalization function is not done by the audio decoder, it has to be done by an external analog part. In all other modes the normalization is done by audio decoder.

| Value | Meaning |
|---|---|
| 0 | Custom A (Analog) |
| 1 | Custom D (Digital) |
| 2 | Line Out |
| 3 | RF Mode |

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### AC3_HDR

**High dynamic range**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address:* 0x6A

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register corresponds to the Dynamic range scale factor for high level signals, also called cut factor in the Dolby specifications.

HDR = 255 * Cut Factor (in decimal), where the cut factor is a fractional number between 0 and 1. It is used to scale the dynamic range control word for high-level signals that would otherwise tend to be reduced.

When HDR = 0xff (cut factor = 1.0), the high level signals reduction is the one given in the stream.

A value of zero disables the high-level compression. This word is ignored if the compression mode is set to RF mode.

### AC3_LDR

**Low dynamic range**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address* : 0x6B

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register corresponds to the Dynamic range scale factor for low level signals, also called boost factor in the Dolby specifications.

LDR = 255 * BoostFactor (in decimal), where the boost factor is a fractional number between 0 and 1.0. The boost factor scales the dynamic range control-word for low-level signals that would otherwise tend to be amplified.

When LDR = 0xff (boost factor = 1.0), and the low

level signals amplification is maximum.

A value of zero disables the low-level amplification. This word is ignored if the compression mode is set to RF mode.

### AC3_RPC

**Repeat count**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address* + 0x6C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

When a CRC error is detected, previous blocks can be repeated or muted.

This register specifies the number of audio blocks to repeat before muting. If this is zero, then blocks are muted until the next frame is decoded

### AC3_KARAMODE

**Karaoke downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*AudioBaseAddress* + 0x6D

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

Downmix mode when a karaoke bit stream is received.

A Karaoke bitstream can be composed of 5 channels, which are: L (left), R (right), M (Music), V1(Vocal 1), V2 (Vocal 2).

There are two major modes when receiving a Karaoke bitstream: aware and capable.

When in 'aware' mode (   KARAMODE = 0), a predefined downmix is applied on all incoming channels.

When in 'capable' mode (   KARAMODE = 4, 5, 6, 7), the user can choose to reproduce or not the two in-

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coming vocal channels, V1 and V2.

An additional mode is added ( AC3_KARAMODE = 3) to allow multi-channel reproduction. In this case, the downmix specified by the AC3_DOWNMIX and AC3_DUALMODE registers is applied.

The following table summaries the different modes:

| Value | Mode | Comment |
|---|---|---|
| 0 | Aware | Left = L + clev*M + slev*V1, Right = R + clev*M + slev*V2 |
| 1 | | Not used |
| 2 | | Not used |
| 3 | Multichannel | Consider bitstream as multi-channel: Perform downmix according to DOWNMIX and DUALMODE registers |
| 4 | Capable | Do not reproduce V1, V2: Left = L + clev*M, Right = R + clev*M |
| 5 | | Reproduction V1 only: Left = L + clev*M + 0.707*V1, Right = R + clev*M + 0.707V1 |
| 6 | | Reproduction V2 only: Left = L + clev*M + 0.707*V2, Right = R + clev*M + 0.707V2 |
| 7 | | Reproduction V1, V2: Left = L + clev*M + V1, Right = R + clev*M + V2 |

**Left** = Output Channel,
**Right** = Output Channel, L, R, M, V1, V2 = Input Channels (coded in Dolby Digital karaoke bitstream),
**clev** = Center Mix Level (value provided in the bit-stream),

**slev** = Surround Mix Level (value provided in the bit-stream). For further information ref. to annex C of ATSC standard "Digital Audio Compression (AC-3)".

### AC3_DUALMODE
**Dual downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address*: 0x6E

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description

This register allows additional downmix to be set when in 2/0 output mode or when receiving a "Dual mode" incoming bitstream (example: A disk with 2 different languages on channel 1 and channel 2). In the following table, channel 1 and 2 represent the output channels after downmix performed with AC3_DOWNMIX.

This register enables Mono downmix when AC3_DOWNMIX = 2 and AC3_DUALMODE = 3.

| Value | Description |
|---|---|
| 0 | Output as Stereo |
| 1 | Output Channel 1 on both output L/R |
| 2 | Output Channel 2 on both output L/R |
| 3 | Mix Channel 1 and 2 to monophonic and output on both L/R |

### AC3_DOWNMIX
**Downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

*Address:* 0x6F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:.

| Value | Description |
|---|---|
| 0 | 2/0 Dolby Surround (LT, RT) |
| 1 | 1/0 (C) |
| 2 | 2/0 (L, R) |
| 3 | 3/0 (L, C, R) |
| 4 | (L, R, S) |
| 5 | 3/1 (L, C, R, S) |
| 6 | 2/2 (L, R, LS, RS - Dolby Phantom Mode |
| 7 | 3/2 (L, C, R, $L_S$, $R_S$) |

Note: in notation, 3/2 represents 3 front speakers and 2 surround speakers.

### AC3_STATUS0

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### Dolby Digital status register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Not used | fs_cod | | Bitrate code | | | | |

*AudioBaseAddress* + 0x76

Type: RO

Software Reset: NC

Hardware Reset:UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Bitrate code | Code identifying the bitrate. Bitrate[4..0] = frmsizecod[5..1] |
| fs_cod | Code identifying the sampling frequency |

### AC3_STATUS1

#### Dolby Digital status register 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | LFE | Acmod | | |

*Address:* 0x77

Type: RO

Software Reset: NC

Hardware Reset:UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Acmod | Audio coding mode. Indicates which channels are in use. |
| LFE | Indicates if LFe channel is present in the stream |

### AC3_STATUS2

### Dolby Digital status register 2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Bsmod | | | Bsid | | | | |

*Address* + 0x78

Type: RO

Software Reset: NC

Hardware Reset:UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Bsid | Bit stream identification, indicates the version of the standard |
| Bsmod | Bbit stream mode, indicates the type of service |

### AC3_STATUS3

#### Dolby Digital status register 3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | Cmixlevel | | SurMixlevel | |

*Address:* 0x79

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Cmixlevel | Downmix level of center channel |
| SurMixlevel | Downmix level of surround channel |

### AC3_STATUS4

**Dolby Digital status register 4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | Dsurmod | | Copyright | Origbs | Lancode |

*Address:* 0x7A

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Lancode | When at 1, indicates that a language code is provided in the stream |
| Origbs | When at 1, indicates that the stream is an original |
| Copyright | When at 1, indicates that the stream is protected by copyright |
| Dsurmod | In 2/0 mode, indicates if the stream is Dolby surround encoded |

### AC3_STATUS5
**Dolby Digital status register 5**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Lancode | | | | | | | |

*Address* : 0x7B

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains the code of the language of the audio service, extracted from the stream.

### AC3_STATUS6
**Dolby Digital status register 6**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | Dialog Normalization (see Dolby specifications) | | | | |

*Address:* 0x7C

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains the code indicating the dialog normalization level extracted from the stream.

### AC3_STATUS7
**Dolby Digital status register 7**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Room type | Mix level | | | | | | Audprodie |

*Address:* 0x7D

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| Audprodie | Audprodie: if set, indicates that room type and mix level are provided |
| Mix level | If audprodie is set, mix level indicates the sound level |
| Room type | If audprodie is set, mix level indicates the sound level |

### 9.17 MPEG configuration registers
**MP_SKIP_LFE**
**Channel skip**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

*Address* : 0x68

Type: R/W

Software Reset: 0x00

Hardware Reset: UND

Description:

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When this register is set to 1, the LFE channel is skipped. When this register is set to 0 the LFE channel is decoded (if present).

**MP_PROG_NUMBER**

**Program number**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | Prog |

*Address:* 0x69

Type: R/W

Software Reset: 0x00

Hardware Reset: UND

Description:

When the stream is in Second Stereo mode, this register specifies which program is played.

| Bitfield | Description |
|---|---|
| Prog | Select program #0 or #1 where 0: L0,R0 in front channels, 1: L2,R2 in front channels |

**MP_DUALMODE**

**MPEG setup dual mode**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Addres:* 0x6E

Type: R/W

Software Reset: 0x00

Hardware Reset: UND

The MPEG DUAL_MODE is active in downmix mode 1 and 9.

| Value | Description |
|---|---|
| 0 | Output as Stereo |
| 1 | Output Channel 1 on both outputs L/R |
| 2 | Output Channel 2 on both outputs L/R |
| 3 | Mix Channel 1 and 2 to monophonic, and output on both L/R |

**MP_DRC**

**Dynamic range control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | DRC |

*Address:* 0x6A

Type: R/W

Software Reset: 0x00

Hardware Reset: UND

Description;

When bit DRC=1, dynamic range control is enabled. The dynamic range is set according to the data transmitted in the DVD MPEG stream.

**MP_CRC_OFF**

**CRC check off**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address:* 0x6C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

When register is set to 1, the CRC in MPEG frame is not checked. When register is set to 0, the CRC in MPEG frame is checked if exists. If a CRC error occurs, the decoder soft mutes the frame (but does not stop).

**MP_MC_OFF**

**Multi-channel**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | DEN | Reserved | | | MC |

*Address:* 0x6D

Type: R/W

Software Reset: NC

Hardware Reset: UND

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Description:

| Bitfield | Description |
|---|---|
| MC | When MC=1, the multi-channel part of the bitstream is not decoded, only the MPEG-1 compatible bitstream is decoded. Bit MC must be set to 1 for an MPEG-1 bitstream. |
| DEN | De-normalization: set DEN=0 for MPEG1 signals, and set DEN=1 for MPEG2 multi-channel signals<br>When DEN=1, MPEG2 multi-channel signals L, C, R, LS and RS can be de-normalized. The signals must first be inverse-weighted then multiplied by the de-normalization factor. This undoes the attenuation carried out at the encoder side to avoid overload when calculating the compatible signals (see MPEG 13818-3 specifications). |

## MP_DOWNMIX
### MPEG downmix

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

*Address: 0x6F*

Type: R/W

Software Reset: 0x08

Hardware Reset: UND

Description:

In the table below, $L_O$, $R_O$, $C_O$, $Ls_O$, $Rs_O$ represent the output channels after downmix, and L, R, C, $L_S$, $R_S$ are the audio channels.

The coefficients $K_j$, $K_C$, $K_r$, $K_S$ depend on the number of input channels. In the above table, the equations are given for a 5 channels input bitstream. If the input bitstream does not contain five channels (L, C, R, $L_S$, $R_S$), the coefficient "Kj" corresponding to the channel not present is equal to 0.

If the MPEG bitstream contains only one surround channel (S), replace $(K_S \times (L_S + R_S))$, $(K_S \times L_S$ and

$(K_S \times R_S)$ by $(K_S \times S)$ in the above equations.

| Value | Output Mode | Comment |
|---|---|---|
| 0x00 | 1/0 (C) = Mono | $C_O = K_j \times L + C + K_r \times R + K_S (L_S + R_S)$ |
| 0x01 | 2/0 (L, R) = Stereo | $L_O = (L + K_C \times C + K_S \times L_S)/(1 + K_C + K_S)$,<br>$R_O = (R + K_C \times C + K_S \times R_S)/(1 + K_C + K_S)$ |
| 0x02 | 3/0 (L, C, R) | $L_O = L + K_S \times L_S$, $R_O = R + K_S \times R_S$, $C_O = C$ |
| 0x03 | 2/1 (L, R, S) | $L_O = L + K_C \times C$, $R_O = R + K_C \times C$, $Ls_O = Rs_O = K_S \times (L_S + R_S)$ |
| 0x04 | 3/1 (L, C, R, S) | $L_O = L$, $R_O = R$, $C_O = C$, $Ls_O = Rs_O = K_S \times (L_S + R_S)$ |
| 0x05 | 2/2 (L, R, $L_S$, $R_S$) | $L_O = L + K_C \times C$, $R_O = R + K_C \times C$, $Ls_O = L_S$, $Rs_O = R_S$ |
| 0x06 | 3/2 (L, C, R, $L_S$, $R_S$) | $L_O = L$, $R_O = R$, $C_O = C$, $Ls_O = L_S$, $Rs_O = R_S$ |
| 0x09 | 2/0 (Dolby surround $L_T$, $R_T$) | $L_T = (L + 0.707C - 0.707 \times 0.5 (LS + R_S)) /2.414$,<br>$R_T = (R + 0.707C + 0.707 \times 0.5 (L_S + R_S)) /2.414$ |
| 0x0A | 2/0 Karaoke capable: V1 ON, V2 ON | Lk = L + 0.707 A1 + 0.707 G, Rk = R + 0.707 A2 + 0.707 G |
| 0x0B | 2/0 Karaoke Capable: V1 ON, V2 OFF | Lk = L + 0.707 A1 + 0.707 G, Rk = R + 0.707 G |
| 0x0C | 2/0 Karaoke Capable: V1 OFF, V2 ON | Lk = L + 0.707 G, Rk = R + 0.707 A2 + 0.707 G |
| 0x0D | 2/0 Karaoke Capable: V1 OFF, V2 OFF | Lk = L + 0.707 G, Rk = R + 0.707 G |
| 0x0E | 2/0 Karaoke Capable: V1 ON, V2 OFF (Dolby Digital like) | Lk = L + 0.707 A1 + 0.707 G, Rk = R + 0.707 A1 + 0.707 G |
| 0x0F | 2/0 Karaoke Capable: V1 OFF, V2 ON (Dolby Digital like) | Lk = L + 0.707 A2 + 0.707 G, Rk = R + 0.707 A2 + 0.707 G |
| 0x1A | 3/0 Karaoke Capable: V1 ON, V2 ON | Lk = L + 0.707 A1, Ck = G, Rk = R + 0.707 A2 |

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| 0x1B | 3/0 Karaoke Capable: V1 ON, V2 OFF | Lk = L + 0.707 A1, Ck = G, Rk = R |
|------|------|------|
| 0x1C | 3/0 Karaoke Capable: V1 OFF, V2 ON | Lk = L, Ck = G, Rk = R + 0.707 A2 |
| 0x1D | 3/0 Karaoke Capable: V1 OFF, V2 OFF | Lk = L, Ck = G, Rk = R |
| 0x1E | 3/0 Karaoke Capable: V1 ON, V2 OFF (Dolby Digital like) | Lk = L, Ck = G + A1, Rk = R |
| 0x1F | 3/0 Karaoke Capable: V1 OFF, V2 ON (Dolby Digital like) | Lk = L, Ck = G + A2, Rk = R |

**MP_STATUS0**

**MPEG status register 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ID | LAY[1:0] | | P | BRI[3:0] | | | |

*Address* : 0x76

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

| Bitfield | Description |
|----------|-------------|
| BRI[3:0] | Bit rate index |
| P | Protection Bit |
| LAY[1:0] | Layer |
| ID | Identifier |

**MP_STATUS1**

**MPEG status register** 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SFR[1:0] | | PAD | PRI | MOD[1:0] | | MEX[1:0] | |

*Address:* 0x77

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

| Bitfield | Description |
|----------|-------------|
| MEX[1:0] | Mode Extension |
| MOD[1:0] | Mode |
| PRI | Private Bit |
| PAD | Padding Bit |
| SFR[1:0] | Sampling Frequency |

**MP_STATUS2**

**MPEG status register 2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| not used | | | | C | OCB | EMP[1:0] | |

Address: 0x78

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

| Bitfield | Description |
|----------|-------------|
| EMP[1:0] | Emphasis rate index |
| OCB | Original/Copy Bit |
| C | Copyright |

**MP_STATUS3**

**MPEG status register** 3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CEN[1:0] | | SUR[1:0] | | LFE | AMX | DEM[1:0] | |

*Address* : 0x79

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| DEM[1:0] | Dematrix procedure |
| AMX | Audio mix |
| LFE | LFE |
| SUR[1:0] | Surround |
| CEN[1:0] | Centre |

## MP_STATUS4
### MPEG status register 4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EXT | NML[2:0] | | | MFS | MLY | CIB | CIS |

Address: 0x7A

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| CIS | Copyright ID Start |
| CIB | Copyright ID Bit |
| MLY | Multi-lingual Layer |
| MFS | Multi-lingual FS |
| NML[2:0] | Number of Multi-lingual Channels |
| EXT | Extension bitstream present |

## MP_STATUS5
### MPEG status register 5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Address: 0x7B

Type: RO

Software Reset: UND

Hardware Reset: UND

Description:

The number of extended ancillary data bytes is contained in this register

## 9.18 Pink noise generation registers
## PN_DOWNMIX
### Pink noise downmix

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | RS | LS | LFE | C | R | L |

Address: 0x6F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Bitfield | Description |
|---|---|
| L | 1: Left channel contains pink noise<br>0: Left channel is forced to zero |
| R | 1: Right channel contains pink noise<br>0: Right channel is forced to zero |
| C | 1: Center channel contains pink noise<br>0: Center channel is forced to zero |
| LFE | 1: LFE channel contains pink noise<br>0: LFE channel is forced to zero |
| LS | 1: Left surround channel contain pink noise<br>0: Left surround channel is forced to zero |
| RS | 1: Right surround channel contains pink zero<br>0: Right surround channel is forced to zero |

After this processing, the OCFG stage is applied on these channels. OCFG must be configured to 0 and attenuation on all channels must be set to 10dB attenuation.

The other values must not be used because low frequency extraction must not be done when generating pink noise.

Pink noise selection is made through the STREAM-SEL and DECODSEL registers.

## 9.19 PCM beep-tone registers
## PCM_BTONE
### PCM beep tone frequency

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

*Address:* 0x68

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Type: R/W

Software Reset: 0

Hardware Reset: UND

Description:

The value in this register sets the PCM beep tone frequency according to the formula:

Beep_tone_frequency = (Fs/2)/(Register_value+1)

### 9.20 Karaoke registers

This section describes the registers which select the karaoke effects, for example: volume, chorus, echo, reverb and mute. Any change to these registers must be signalled to the DSP by writing 1 to the register.

### KAR_MCh0VOL

#### Music channel 0 (L) volume

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| value | | | | | | | |

Address: 0x81

Type: R/W

Reset value: 0xFF

Description;

This register contains the scaling factor applied to the left channel of the music input. It specifies a fractional multiplication factor whose value varies from 0 to 1.0:

Music Left channel = original music left channel scale_factor.

| Bitfield | Description |
|---|---|
| Value | 0x00: Scale factor 0 = left channel mute<br>0x7F: Scale factor 0.5 = half restitution of left channel<br>0xFF: Scale factor 1.0 = full restitution of left channel |

### KAR_MCh1VOL

#### Music channel 1 (R) volume

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| value | | | | | | | |

Address: 0x82

Type: R/W

Reset value: 0xFF

Description:

This register has the same function as KAR_MCh0VOL for the right music channel.

### KAR_KEYCONT

#### Key control (Pitch Shift) ON/OFF

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | PSHIFT |

**Address: 0x83**

Type: R/W

Reset value: 0

Description:.

| Bitfield | Description |
|---|---|
| PSHIFT | 0: pitch shift disabled, 1: pitch shift enabled |

### KAR_KEYVALUE

#### Key value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| KEYVALUE | | | | | | | |

Address: 0x84

Type: R/W

Reset value: 0x00

Description:

The pitch shift can be changed from -3.5 to 3.5 tones, in steps of 1/4 tone. This register sets the number of tones according to the following table:

| Key control (tone) | -1/4 | -1/2 | -3/4 | -1 | -1.16 | -1.34 | -1.58 | -1.93 | -2.49 | -3.5 |
|---|---|---|---|---|---|---|---|---|---|---|
| KEYVALUE (decimal) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

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| Key control (tone) | 1/4 | 1/2 | 3/4 | 1 | 1.16 | 1.34 | 1.58 | 1.93 | 2.49 | 3.5 |
|---|---|---|---|---|---|---|---|---|---|---|
| KEYVALUE (decimal) | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |

### KAR_VCANCEL

**Voice cancellation ON/OFF**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | VCANCEL |

Address: 0x85

Type: R/W

Reset value: 0

Description:

| Bitfield | Description |
|---|---|
| VCANCELL | 0: voice cancellation off, 1: voice cancellation on |

### KAR_VVALUE

**Degree of voice cancellation**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | LEVEL[2:0] | | |

Address: 0x86

Type: R/W

Reset value: 0x0

Description:

When the voice cancellation is enabled by the KAR_VCANCEL register, KAR_VVALUE specifies the extent of the voice cancellation according to the following table:

| Bitfield | Description |
|---|---|
| LEVEL[2:0] | 0: cut-band filter with 40dB attenuation at 700Hz 1: cut-band filter with 35dB attenuation at 700Hz 2: cut-band filter with 32dB attenuation at 700Hz 3: cut-band filter with 27dB attenuation at 700Hz 4: cut-band filter with 23dB attenuation at 700Hz |

### KAR_MMUTE

**Music channel mute**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | MUTE |

Address: 0x87

Type: R/W

Reset value:0

Description:

This register mutes the music channel.

| Bitfield | Description |
|---|---|
| MUTE | 0: not muted,   1: muted |

### KAR_VCh0VOL

**Voice channel 0 (L) volume**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Value | | | | | | | |

Address: 0x88

Type: R/W

Reset value: 0xFF

Description:

This register has the same function as KAR_MCh0VOL for the left voice channel instead of the left music channel.

### KAR_VCh1VOL

**Voice channel 1 (R) volume**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Value | | | | | | | |

Address: 0x89

Type: R/W

Reset value: 0xFF

Description:

This register has the same function as KAR_MCh0VOL for the right voice channel instead of the left music channel.

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### KAR_DUET
**Duet ON/OFF switch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | DUET |

Address: 0x8A

Type: R/W

Reset value: 0

Description:

The value in this register sets the duet function on or off. When selected, the duet function is configured by register KAR_DUETTHRESH.

| Bitfield | Description |
|---|---|
| DUET | 0: duet off and 1: duet on |

### KAR_DUETTHRESH
**Duet threshold control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DUETTHRESHOLD[7:0] | | | | | | | |

Address + 0x8B

Type: R/W

Reset delay: 0

Description:

When the Duet function is enabled by the KAR_DUET register, this register specifies the amplitude of the voice line below which the voice is cancelled. If the amplitude of the voice line is below this threshold, the recorded voice is played instead. The value of DUETTHRESHOLD ranges from 0 to 255, full scale signal.

### KAR_VOICE
**Selection of voice effects**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | MIX | VOICEEFF[1:0] | |

Address: 0x8C

Type: R/W

Reset delay: 0x0

Description:

| Bitfield | Description |
|---|---|
| VOICEEFF | Selecte the voice effects: <br> 0: No effect is applied to the voice input <br> 1: Echo is applied to the voice inputs, tuned by registers KAR_VDELAY and KAR_VBAL <br> 2: Chorus is applied to the voice inputs, tuned by registers KAR_VDELAY and KAR_VBAL <br> 3: Reverb is applied to the voice inputs, tuned by register KAR_VDELAY. |
| MIX | Voice channel mixing: <br> 0: No mix, voice is output on centre channell <br> 1: Mix music and voice channels into music channel. |

### KAR_VDELAY
**Programmable delay/decay music effects**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Value | | | | | | | |

Address: 0x8D

Type: R/W

Reset value: 0x0

Description:

The value in this register specifies the delay used for voice input effects. The delay can be set in the range from 0 to 2048/Fs seconds (where Fs is the sampling frequency in KHz).

'desired time delay' = ( 2048 / Fs) * ( Value / 256)

which gives:

KAR_VDELAY value = (Fs / 8) * 'desired time delay

For reverberation effects, this register gives the decay factor,which can vary within the range 0 to 1.0.

### KAR_VBAL
**Programmable mix for echo and chorus effects**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BALANCE[7:0] | | | | | | | |

Address: 0x8E

Type: R/W

Reset value: 0x3F

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Description:

This register sets the balance between the original sound and its delayed version for the echo and chorus effects according to the formula.

echo (or chorus) output = original_sound * (1 - balance) + delayed_sound * balance

where balance = Balance[7:0] / 255

where balance can vary in the range of 0 to 1. A balance limit of 0.5 is recommended. BALANCE[7:0] = balance * 255.

## KAR_VMUTE
**Voice channel mute**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | MUTE |

Address: 0x8F

Type: R/W

Reset value: 0x00

Description:

This register mutes the voice channel: '0' means not muted and '1' means muted.

## KAR_PLAY
**Mute of voice and music**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | PLAY |

Address: 0x90

Type: R/W

Reset value: 0x01

Description:

This register mutes the voice and the music channels simultaneously: PLAY = '0' means muted and '1' means playing. The registers  and KAR_VMUTE have priority for muting.

## KAR_MODE
**Operating mode selection**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | KAR_MODE[1:0] | |

Address + 0x91

Type: R/W

Reset value: 0x01

Description:

This register specifies the working mode of the Karaoke module.

| Bitfield | Description |
|---|---|
| KAR_MODE [1:0] | **00:** Karaoke processor in waiting mode. This is the default mode after a hardware reset, total or partial software reset. This mode is used to programme all the registers at first initialization. |
| | **01:** Karaoke processor running. |
| | **10:** Partial Software reset. This resets the internal DSP program but keep the register configuration as it was before the partial reset. When the partial reset is finished, KAR_MODE[1:0] is automatically set to '01'. |
| | **11:** Total Software reset. The program is reset and the registers values are changed back to their reset default values. |

## KAR_DIN_CTL
**Control of voice channel**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | JUSTIF | DELAY | WS_POL | CLK_POL | WS[1:0] | | DINEN |

Address: 0x92

Type: R/W

Reset Value: 0x00

Description:

This register specifies the input format for configuring

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the handling of the second input.

| Bitfield | Description |
|---|---|
| DINEN | DIN enable: 0: disabled, 1: enabled |
| WS[1:0] | PCM precision: 00: 16-bit mode, 01: 18-bit mode, 10: 20-bit mode, 11: 24-bit mode |
| CLK_POL | 0: Data and WS change on clockalling edge<br>1: Data and WS change on clockising edge |
| WS_POL | 0: Left data word = WS low, right data word = WS high<br>1: Left data word = WS high, right data word = WS low |
| DELAY | 0: First bit of data occurs on transition of WS<br>1: First bit of data occurs with 1 clock cycle delay (I2S compatible) |
| JUSTIF | 0: Left padded, 1: Right padded |

### KAR_UPDATE

**Change active Karaoke functions**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | UPDATE |

Address: 0x93

Type: R/W

Reset Value: 0

Description:

This register loads the new Karaoke configuration into the internal registers when UPDATE is set to '1'. When the bit is reset to '0' the system continues in the configuration last loaded.

### 9.21 Second serial input registers
### SFREQ2

**Sampling frequency of voice channel**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Value | |

Address: 0x94

Type: RO

Reset Value: 0

Description:

This register sets the sampling frequency, Fs, of the incoming PCM stream.

| Fs (KHz) | 48 | 44.1 | 32 | - | 96 | 88.2 | 64 | - | 24 | 22.05 |
|---|---|---|---|---|---|---|---|---|---|---|
| Value (decimal) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

| Fs (KHz) | 16 | - | 12 | 11.025 | 8 | - | 192 | 176.4 | 128 | - |
|---|---|---|---|---|---|---|---|---|---|---|
| Value (decimal) | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |

### CANINPUT_MODE

**Selection of input data format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SWAP | MODE[6;0] | | | | | | |

Address: 0x95

Type: R/W

Reset Value: 0x00

Description;

This register specifies the input format for configuring the handling of the second input.

| Bitfield | Description |
|---|---|
| MODE [6:0] | 0: 16 slots mode<br>1: 16 slots mode, LSB first<br>2: 32 slots mode, left aligned<br>3: 32 slots mode, right aligned<br>4: 32 slots mode, I2S mode<br>5: 32 slots mode, sign extended<br>6: 32 slots mode, 8-bit data<br>7: 32 slots mode16-bit data |
| SWAP | Channel swap: 0: Left channel first, 1: Right channel firs |

### 9.22 Linear PCM (DVD audio) registers
### LPCMA_DOWNMIX

**Downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Value | |

*Address*: 0x6F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description;:.

| Value | Description |
|-------|-------------|
| 0 | Downmix not applied |
| 1 | Force downmix 2/0 |
| 2 | Downmix 2/0 is applied if the flags down_mix_code_validity AND stereo_playback_mode are both '0' in the bitstream |

The notation, 2/0 represents 2 front speakers and no surround speakers.

### LPCMA_FORCE_DWS
**Downsampling 192 to 96KHz**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Value | |

*Address* : 0x70

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register selects whether downsampling is used for input streams requiring sampling frequencies of 192KHz or 176.4KHz. When 'automatic' is selected, register is automatically updated to correspond to the new output frequency.

| Bitfield | Description |
|----------|-------------|
| Value | 00: Automatic (if Fs = 192KHz or 176.4KHz) 01: Automatic (if Fs = 192KHz or 176.4KHz) 10: No downsampling |

### LPCMA_DM_COEFT_0
Downmix phase coefficients 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | PH_1L | PH_2L | PH_3L | PH_4L | PH_5L | Reserved | |

*Address* : 0x97

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the phase coefficients for channels mixing to Lmix. The input signal is inverted when PH_xL = '0' and non-inverted when '1'.

### LPCMA_DM_COEFT_1
**Downmix phase coefficients** 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PH_0R | 0 | PH_2R | PH_3R | PH_4R | PH_5R | Reserved | |

*Address:* 0x98

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the phase coefficients for channels mixing to Rmix. The input signal is inverted when PH_xR = '0' and non-inverted when '1'.

### LPCMA_DM_COEFT_2
**Downmix gain coefficients** 2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_0L | | | | | | | |

*Address:* 0x99

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Lf to Lmix. See the note after register

### LPCMA_DM_COEFT_3
**Downmix gain coefficients** 3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_0R | | | | | | | |

*Address* : 0x9A

Type: R/W

Software Reset: NC

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Hardware Reset: UND

Description:

This register sets the mixing gain for Lf to Rmix. See the note after register

### LPCMA_DM_COEFT_4
**Downmix gain coefficients 4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_1L | | | | | | | |

*Address:* 0x9B

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Rf to Lmix. See the note after register
<BlueHT>LPCMA_DM_COEFT_13.

### LPCMA_DM_COEFT_5
**Downmix gain coefficients 5**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_1R | | | | | | | |

*Address:* 0x9C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Rf to Rmix.

See the note after register
<BlueHT> LPCMA_DM_COEFT_13.

### LPCMA_DM_COEFT_6
**Downmix gain coefficients 6**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_2L | | | | | | | |

*Address:* 0x9D

Type: R/W

Software Reset: NC
Hardware Reset: UND

Description:

This register sets the mixing gain for C to Lmix. See the note after register .

### LPCMA_DM_COEFT_7
**Downmix gain coefficients 7**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_2R | | | | | | | |

*Address:* 0x9E

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for C to Rmix. See the note after register

### LPCMA_DM_COEFT_8
**Downmix gain coefficients 8**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_3L | | | | | | | |

*Address:* 0x9F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Ls / S to Lmix. See the note after register

### LPCMA_DM_COEFT_9
**Downmix gain coefficients 9**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_3R | | | | | | | |

*Address* : 0xA0

Type: R/W

Software Reset: NC

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Hardware Reset: UND

Description:

This register sets the mixing gain for Ls / S to Rmix. See the note after register

### LPCMA_DM_COEFT_10
**Downmix gain coefficients 10**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_4L | | | | | | | |

*Address* : 0xA1

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Rs to Lmix. See the note after register .

### LPCMA_DM_COEFT_11
**Downmix gain coefficients 11**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_4R | | | | | | | |

*Address:* 0xA2

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for Rs to Rmix. See the note after register
LPCMA_DM_COEFT_12

**Downmix gain coefficients 12**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_5L | | | | | | | |

*Address:* 0xA3

Type: R/W

Software Reset: NC

Hardware Reset: UND

This register sets the mixing gain for LFE to Lmix. See the note after register .

### LPCMA_DM_COEFT_13
**Downmix gain coefficients 13**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COEF_5R | | | | | | | |

*Address:* 0xA4

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register sets the mixing gain for LFE to Rmix

Note: For DVD audio, the real coefficient value, alpha[x], applied to channel x is calculated with the following formulae:

$$alpha[x] = 2^{-(COEF\_xL/30)} \quad 0 < COEF\_xL \ 199$$
$$alpha[x] = 2^{-((COEF\_xL - 100)/30)} \quad 200 < COEF\_xL \ 254$$
$$alpha[x] = 0 \quad COEF\_xL \ 255$$

### LPCMA_STATUS0
**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EMPH ASIS | Reser ved | STERE O_PB | DWNMX _VALID | DOWN_MIX_CODE [3:0] | | | |

*Address:* 0x76

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| DOWN_MIX_CODE | Identifying code |
| DWNMX_VALID | DOWN_MIX_CODE valid |
| STEREO_PB | Stereo playback mode |
| EMPHASIS | Emphasis flag |

### LPCMA_STATUS1
**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| QUANTIZATION_WORD_L ENGTH_1[3:0] | | | | QUANTIZATION_WORD_L ENGTH_2[3:0] | | | |

*ST*

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*Address:* 0x77

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| QUANTIZATION_WORD _LENGTH_2[3:0] | Quantization word length for group 2 |
| QUANTIZATION_WORD _LENGTH_1[3:0] | Quantization word length for group 1 |

### LPCMA_STATUS2

**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SAMPLING_FREQUENCY _1[3:0] | | | | SAMPLING_FREQUENCY_ 2[3:0] | | | |

*Address:* 0x78

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| SAMPLING_FREQU ENCY_2[3:0] | Sampling frequency for group 2 |
| SAMPLING_FREQU ENCY_1[3:0] | Sampling frequency for group 1 |

### LPCMA_STATUS3

**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | MULTI_CHANNEL_TYPE[3:0] | | | |

*Address: 0x79*

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| MULTI_CHANNEL_TYPE[3:0] | |

### LPCMA_STATUS4

**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BIT_SHIFT_OF_CHANNEL _GR2[3:0] | | | | CHANNEL_ASSIGNMENT [3:0] | | | |

*Address:* 0x7A

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains bit stream information extracted from the stream.

| Bitfield | Description |
|---|---|
| CHANNEL_ASSIGNMENT[3:0] | |
| BIT_SHIFT_OF_CHANNEL_GR2[3:0] | |

### LPCMA_STATUS5

**Linear PCM (DVD audio) status register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DYNAMIC_RANGE_CONTROL[7:0] | | | | | | | |

*Address:* 0x7B

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This register contains information, extracted from the stream, for the dynamic range control.

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## 9.23 Linear PCM (DVD video and PCM) registers

**LPCMV_DOWNMIX**

**Downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Value | |

*Address* : 0x6F

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description;.

| Value | Description |
|---|---|
| 0 | Downmix not applied |
| 1 | Force downmix 2/0 |

The notation, 2/0 represents 2 front speakers and no surround speakers.

**LPCMV_FORCE_DWS**

**Downsampling 96 to 48KHz**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Value | |

*Address:* 0x70

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register selects whether downsampling is used for input streams requiring a sampling frequency of 96KHz.

When 'automatic' is selected, register is automatically updated to correspond to the new output frequency.

| Bitfield | Description |
|---|---|
| Value | 00: Automatic (if Fs = 96KHz)<br>01: Automatic (if Fs = 96KHz)<br>10: No downsampling |

**LPCMV_DM_COEFT_0**

**Downmix phase coefficients** 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PH_0L | PH_1L | PH_2L | PH_3L | PH_4L | PH_5L | Reserved | |

*Address:* 0x97

Type: R/W

Software Reset:NC

Hardware Reset: UND

Description:

This register sets the phase coefficients for channels mixing to Lmix. The input signal is inverted when PH_xL = '0' and non-inverted when '1'.

**LPCMV_DM_COEFT_1**

**Downmix phase coefficients 1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PH_0R | PH_1R | PH_2R | PH_3R | PH_4R | PH_5R | Reserved | |

*Address:* x98

Type: R/W

Software Reset:NC

Hardware Reset: UND

Description:

This register sets the phase coefficients for channels mixing to Rmix. The input signal is inverted when PH_xR = '0' and non-inverted when '1'.

**LPCMV_DM_COEFT_2**

**Downmix gain coefficients 2**

For details see register 0x99

**LPCMV_DM_COEFT_3**

**Downmix gain coefficients 3**

For details see register 0x9A

**LPCMV_DM_COEFT_4**

Downmix gain coefficients 4

For details see register 0x9B

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**LPCMV_DM_COEFT_5**

**Downmix gain coefficients 5**

For details see register 0x9C

**PCMV_DM_COEFT_6**

**Downmix gain coefficients 6**

For details see register 0x9D

**LPCMV_DM_COEFT_7**

**Downmix gain coefficients 7**

For details see register 0x9E

**LPCMV_DM_COEFT_8**

**Downmix gain coefficients 8**

For details see register 0x9F

**LPCMV_DM_COEFT_9**

**Downmix gain coefficients 9**

For details see register 0xA0

**PCMV_DM_COEFT_10**

 **Downmix gain coefficients 10**

For details see register 0xA1

**LPCMV_DM_COEFT_11**

**Downmix gain coefficients 11**

For details see register 0xA2

**LPCMV_DM_COEFT_12**

**Downmix gain coefficients 12**

For details see register 0xA3

**LPCMV_DM_COEFT_13**

**Downmix gain coefficients 13**

For details see register 0xA4

Note: For DVD video & PCM, the real coefficient value, alpha[x], applied to channel x is calculated with the following formulae:

$$alpha[x] = 2^{-(x+(y/30))} \quad 0<Y,29 \quad 0<X,7$$

COEF_xL = register bits [b7,b6,b5,b4,b3,b2,b1,b0]

X = register bits[b7,b6,b5]

Y = register bits[b4,b3,b2,b1,b0]

**LPCMV_STATUS0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EMPH_FLAG | MUTE_FLAG | Reserved | FRAME_NUM | | | | |

*Address:* 0x76

Type: R/W

Reset Value: UND

Description:

| Bitfield | Description |
|---|---|
| FRAME_NUM | frame number of the first access unit in the group of audio frames |
| Reserved | Set to 0 |
| MUTE_FLAG | 0: mute off, 1: mute on |
| EMPH_FLAG | Emphasis status after the first access unit: 0: emphasis off; 1: emphasis on |

**LPCMV_STATUS1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Word_Length | | Samp_Freq | | Reserved | Channels | | |

*Address* :0x77

Type: R/W

Reset Value: UND

Description:

| Bitfield | Description |
|---|---|
| Channels | Number of audio channels:000=1 channel (mono), 001=2 channels (stereo), 010=3 channels, 011=4 channels, 100=5 channels,101=6 channels, 110=7 channels, 111=8 channels |
| Reserved | Set to 0 |
| Samp_Freq | Sampling frequency: 00=48kHz, 01=96kHz, 10=reserved, 11=reserved |
| Word_Length | Audio sample length: 00=16 bits, 01=20 bits, 10=24 bits, 11=reserved |

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## PCMV_STATUS2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | Dyn_Range_Control | | | | |

*Address* : 0x78

Type: RW

Reset Value: UND

Description:

This register sets the dynamic range compression from the first access unit. For the hexadecimal value 0x80, dynamic range control is not set. For all other values, the dynamic range control is $(24.082 - 6.0206 * X - 0.2007 * Y)$dB, where $X$ = dynamic_range_control[7..5] and $Y$ = dynamic_range_control[4..0].

## LPCMV_CH_ASSIGN

**Channel assignment**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | Value | | | | |

*Address:* 0xA8

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Value | Description |
|---|---|
| Value (decimal) | This register configures the audio channels: See "DVD Specifications for Read-Only Disc", Part 4 AUDIO SPECIFICATIONS, Version 1.0, March 1999, Table C.1-2. |

## PCMV_MULTI_CHS

**Multi channels**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | Value |

*Address:* 0xA9

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

| Value | Description |
|---|---|
| Value (decimal) | This register configures the multi channel structure for the output channels:<br>0: Stereo<br>1: Multi channels |

## 9.24 MLP registers
## MLP_CRC
**CRC check**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | SU_P | MA_S | MS_C | RH_C |

*Address:* 0x6C

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register controls the four different CRCs in MLP. If the check is false, an error is returned (error numbers 80-83 in register and the outputs of all 6 channels are muted

| Bitfield | Description |
|---|---|
| RH_C | 1: Check of 'Restart_Header_CRC' enable |
| MS_C | 1: Check of 'Major_Sync_CRC' enable |
| MA_C | 1: Check of 'Max_Shift' enable |
| SU_P | 1: Check of 'Substream_Parity' enable |

## MLP_DOWNMIX
**Downmix**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DWNMIX[7:0] | | | | | | | |

*Address:* 0x6F

Type: R/W

Software Reset: NC

Hardware Reset: UND

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Description:

This register controls the MLP downmix.

| Bitfield | Description |
|----------|-------------|
| DWNMIX [7:0] | 0x00: 2/0 (L / R)<br>0x01: 2/0[a] (Lo / Ro) (according to bitstream0)<br>0x02: 3/0 (L, R, C)<br>0x03: 2/1 (L, R, S)<br>0x04: 3/1 (L, C, R, S)<br>0x05: 2/2 (L, R, Ls, Rs)<br>0x06: 3/3 (L, C, R, Ls, Rs)<br>For all other values there is no downmix. |

(a)  Downmix 1/0 (one channel only) is
     forbidden in DVD audio

**MLP_DRC**

**Dynamic range control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | DRC[7:0] | | | | |

*Address* : 0x6A

Type: R/W

Software Reset: NC

Hardware Reset:: UND

Description:

When this register = 0x00, the dynamic range control is disabled. When 0x01, the dynamic range control is enabled and the DRC information in the MLP stream is used.

**MLP_FORCE_DWS**

**Downsampling 192 to 96kHz or 176.4 to 88.2kHz**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | Reserved | | | Value | |

*Address:* 0x70

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

This register selects whether downsampling is used for input streams requiring sampling frequencies of 192KHz or 176.4KHz. When 'automatic' is selected, register is automatically updated to correspond to the new output frequency.

| Bitfield | Description |
|----------|-------------|
| Value | 00: Automatic (if Fs = 192KHz or 176.4KHz)<br>01: Automatic (if Fs = 192KHz or 176.4KHz)<br>10: No downsampling |

**MLP_LFE**

**Decode LFE**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | LFE[7:0] | | | | |

*Address:* 0x68

Type: R/W

Software Reset: NC

Hardware Reset: UND

Description:

When this register = 0x00, LFE is not decoded and when 0x01, LFE is decoded.

**MLP_STATUS0**

**MLP status 0 register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | Reserved | | | | FS_CODE[4:0] | | |

*Address:* 0x76

Type: R/W

Software Reset: NC

Hardware Reset: UND

Type:

This status register contains the sampling frequency codes..

| Bitfield | Description |
|----------|-------------|
| FS_CODE[4:0] | This list gives the codes and the corresponding sampling frequency.<br>0x09: 44.1KHz<br>0x0A: 48KHz<br>0x0D: 88.2KHz<br>0x0E: 96KHz<br>0x11: 176.4KHz<br>0x12: 192KHz<br>0x1F: Undefined<br>The remaining codes are reserved. |

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## MLP_STATUS1

**MLP status 1 register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | CH_ASSIGN[4:0] | | | | |

*Address* : 0x77

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This status register contains the channel assignment.

| Bitfield | Description |
|----------|-------------|
| CH_ASSIGN[4:0] | This gives the channel assignment: See "DVD Specifications for Read-Only Disc", Part 4 AUDIO SPECIFICATIONS, Version 1.0, March 1999, Table C.1-1. |

## MLP_STATUS2

**MLP status 2 register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | NSUBSTR[3:0] | | | |

*Address:* 0x78

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This status register contains the number of sub-streams present in the audio frame.

## MLP_STATUS3

**MLP status 3 register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | SUBSTR_CODE[3:0] | | | |

*Address:*: 0x79

Type: RO

Software Reset: NC

Hardware Reset: UND

Description:

This status register contains the sub-stream information codes..

| Bitfield | Description |
|----------|-------------|
| SUBSTR_CODE [3:0] | 2-channel decoder: bit0 = '1': sub-stream 0 is decoded bit1 = '1': a simplified decoder can be used for sub-stream 0 6-channel decoder: bit2 = '1': sub-stream 0 is decoded bit3 = '1': sub-stream 1 is decoded |

## 9.25 De-emphasis register

**DEEMPH**

**De-emphasis**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | D[1:0] | |

*Address:* 0xB5

Type: R/WS

Software Reset: NC

Hardware Reset: UND

Description:

This register is used in MPEG, DVD_LPCM or CDDA modes; it is not supported in Dolby Digital.

In MPEG and DVD_LPCM modes, its register value is extracted from the bitstream. When the emphasis status changes (by setting bit DEM of the register), an interrupt is generated. In CDDA mode, the register value must be updated by the application.

The de-emphasis filter specified here is applied only if bit DEM of the register is set.

| Bitfield | Description |
|----------|-------------|
| D[1:0] | 00: none, 01: 50/15µs, 10: reserved, 11: CCITT J.17 |

## 9.26 Auxilliary outputs registers

**VCR_MIX**

**VCR outputs**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | STEREO | PRL | reserved | COPY | 3D_VCR |

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*Address:* 0xAE

Type: R/WS??

Software Reset: NC

Hardware Reset: 0

Description:

| Bitfield | Description |
|----------|-------------|
| 3D_VCR | This bit selects "3-D sound" on the VCR channels using SRS processing (depending on the PDEC registers and ):<br>0: Standard sound (disable "3-D sound"),<br>1: Enable "3-D sound". |
| COPY | This bit is used to copy "Left/Right" channels to "VCR" channels:<br>0: no copy,<br>1: copy enable. |
| PRL | This bit enables a "ProLogic downmix" on the "VCR" channels:<br>0: Disable,<br>1: Enable. |
| STEREO | This bit enables a "2/0 downmix" on the "VCR" channels:<br>0: Disable,<br>1: Enable. |

Note:   1.  To have both "3-D sound" on the "VCR" and "Left/Right" channels, the setup is:
VCR_MIX = 0x02 and PDEC = 0x40 for SRS processing,

### VCR_LDLY

**VCR left channel delay**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LEFT_VCR_DELAY | | | | | | | |

*Address:* 0xAF

Type: R/WS??

Software Reset: NC

Hardware Reset: 0

Description:

This register contains the VCR left channel value. See note after next register description.

### VCR_RDLY

VCR right channel delay

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RIGHT_VCR_DELAY | | | | | | | |

*Address:* 0xAF

Type: R/WS??

Software Reset: NC

Hardware Reset: 0

Description:

This register contains the VCR right channel delay value. The values for LEFT_VCR_DELAY and RIGHT_VCR_DELAY are taken into account only when register.bit .DLY = '1'.

### 9.27 Miscellaneous
**BREAKPOINT**
**To be defined**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

*Address* + 0x2B

Type: R/W

Software Reset: NC

Hardware Reset: 0

Description:

This register must be set to 0x08.

### CLOCKCMD
**To be defined**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

*Address:* 0x3A

Type: R/W

Software Reset: NC

Hardware Reset: 0

Description:

This register must be set to 0x00.

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**INIT_RAM**

**RAM initialization**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | Reserved | | | | RAM_INIT |

*Address* : 0xFF

Type: RO

Software Reset: 1

Hardware Reset: 0

Description:

The register is used to signal when the STA310 has finished to boot.

After a soft reset or a hardware reset, or a hardware reset, the host processor must wait until INIT_RAM hold the value "1".

the host can then start to configure the STA310 according to its application

**APPENDIX A OVERVIEW OF THE CHIP**

This **STA310** is based on a very high performances low power general purpose DSP core, MMDSP+, and a set of dedicated peripherals. Internal audio and system PLL allows to configure the chip for a wide range of audio frequencies and DSP processing power (1 to 100 Mips).

**A.1 Architectural Block Diagram**
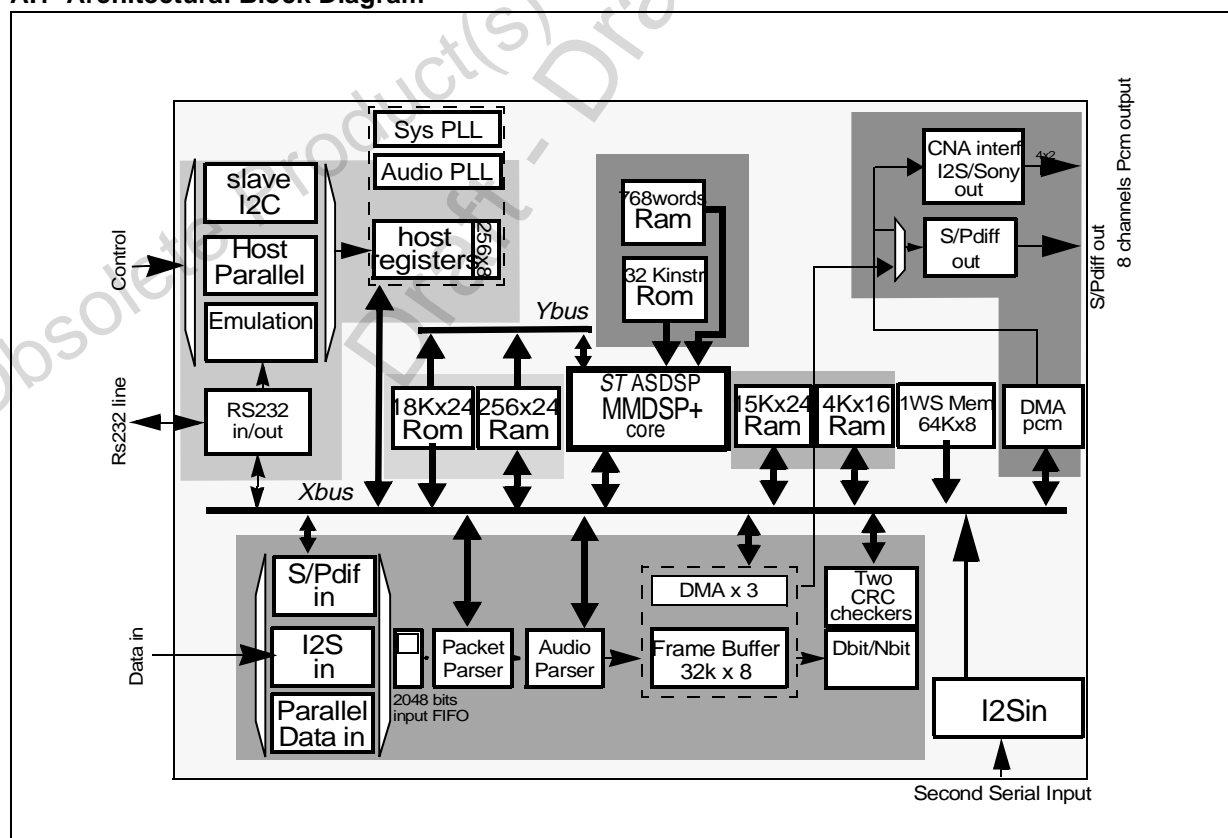
**STA310**

**A.2  Description of the architecture**

The MMDSP+ DSP core can access 5 banks of RAM/ROM memories:

- the 32K instruction ROM,

- the 768 words instruction development RAM,

- X_memory 19K x 24 RAM,

- Y_memory 18 K x 24 ROM,

- Y_memory 1K x 24 RAM.

The DSP core can also access some dedicated and general purpose peripherals. These peripherals (called MMIO peripherals) are mapped as memory locations of the X memory space of the MMDSP+ DSP core. On top of the front-end dedicated ones, the list of the peripherals is the following:

- Four PCM out *I2S/Sony* (16,18,20,24 bits) serial output interfaces are provided to connect, typically, to external DACs. This interface and the Audio PLL provide the Oversampling clocks and the serial clocks necessary to interface the DACs .This interface provides up to 8 independent audio channels. A "DMA PCM" MMIO block makes the link between the X data memory of the DSP core (which can store the audio samples) and the *I2S/Sony* serial interfaces. This MMIO block is a DMA (Direct Memory Access) and handles automatically the transfer of data by blocks. This peripheral implements also an hardware mechanism to support delayed channels. Each channel can de delayed (resolution 1 sample) by a programmable number of data samples. This function is totally transparent to the user.

- A 256 x 8 address space is shared between the MMDSP+ core (as MMIO peripheral) and the external world of the STA310 through the I2C Slave interface or the Host parallel interface. This area is divided mainly in 2 parts:

  a 192 x 8 general purpose RAM area,

  a 64 x (1 to 8 bits) area of specific registers.

- The two PLLs (Audio PLL and System PLL) can be controlled by the DSP itself (thru the MMIO bus) or by the external world of the STA310 (thru the I2C Slave I/F or the Host parallel I/F).

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| DIM. | mm | | | inch | | |
|------|-----|-----|-----|-----|-----|-----|
|      | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A    |      |      | 1.60 |      |      | 0.063 |
| A1   | 0.05 |      | 0.15 | 0.002 |      | 0.006 |
| A2   | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B    | 0.22 | 0.32 | 0.38 | 0.009 | 0.013 | 0.015 |
| C    | 0.09 |      | 0.20 | 0.003 |      | 0.008 |
| D    |      | 16.00 |     |      | 0.630 |      |
| D1   |      | 14.00 |     |      | 0.551 |      |
| D3   |      | 12.35 |     |      | 0.295 |      |
| e    |      | 0.65 |      |      | 0.0256 |     |
| E    |      | 16.00 |     |      | 0.630 |      |
| E1   |      | 14.00 |     |      | 0.551 |      |
| E3   |      | 12.35 |     |      | 0.486 |      |
| L    | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1   |      | 1.00 |      |      | 0.0393 |     |
| K    | 3.5°(min.), 7°(max.) | | | | | |

## OUTLINE AND MECHANICAL DATA
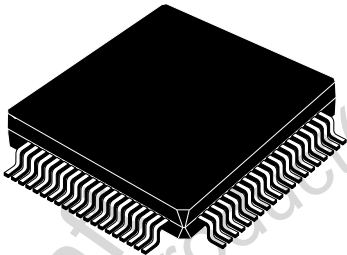


## TQFP80
## (14x14x1.40mm)



TQFP80L
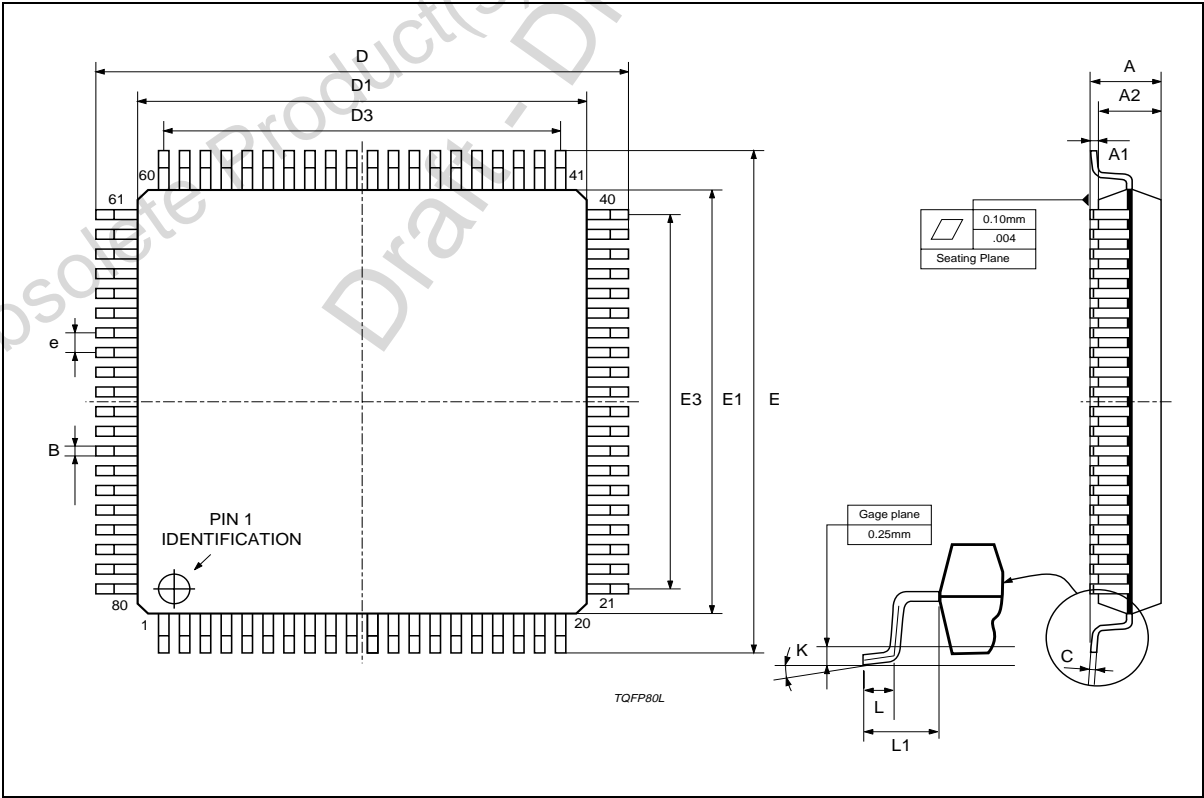
**STA310**

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