

Automotive-grade N-channel 80 V, 3.15 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

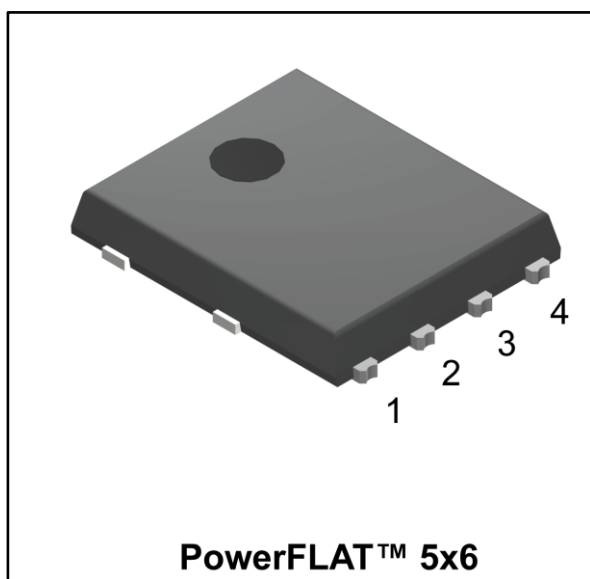
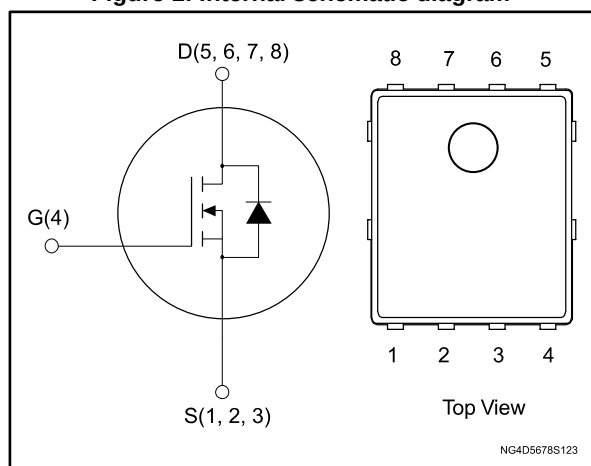


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL135N8F7AG	80 V	3.6 mΩ	120 A	135 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL135N8F7AG	135N8F7	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT™ 5x6 WF type C package information.....	9
	4.2 PowerFLAT™ 5x6 WF packing information	12
5	Revision history	14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	120	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	98	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	480	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	26	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	19	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	104	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	135	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.8	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.2	J
T_{stg}	Storage temperature range	-55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

- (1) This value is rated according to R_{thj-c}
 (2) Pulse width is limited by safe operating area
 (3) This value is rated according to $R_{thj-pcb}$
 (4) Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 13\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^{\circ}\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	1.1	

Notes:

- (1) When mounted on a 1-inch² FR-4 board, 2oz Cu, $t < 10\text{ s}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	80			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
		V _{GS} = 0 V, V _{DS} = 80 V, T _j = 125 °C ⁽¹⁾			10	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 13 A		3.15	3.6	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 40 V, f = 1 MHz, V _{GS} = 0 V	-	6800	-	pF
C _{oss}	Output capacitance		-	1350	-	
C _{rss}	Reverse transfer capacitance		-	95	-	
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 26 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	103	-	nC
Q _{gs}	Gate-source charge		-	35	-	
Q _{gd}	Gate-drain charge		-	28	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 13 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	30	-	ns
t _r	Rise time		-	28	-	
t _{d(off)}	Turn-off delay time		-	73	-	
t _f	Fall time		-	30	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 26\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 64\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	47		ns
Q_{rr}	Reverse recovery charge		-	66		nC
I_{RRM}	Reverse recovery current		-	2.8		A

Notes:

(1) Pulse width is limited by safe operating area

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

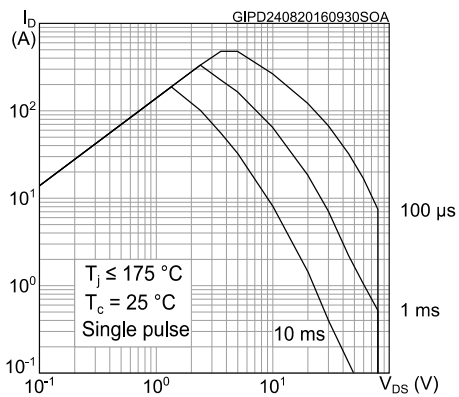


Figure 3: Thermal impedance

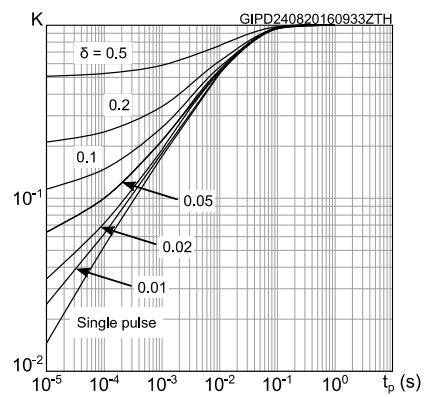


Figure 4: Output characteristics

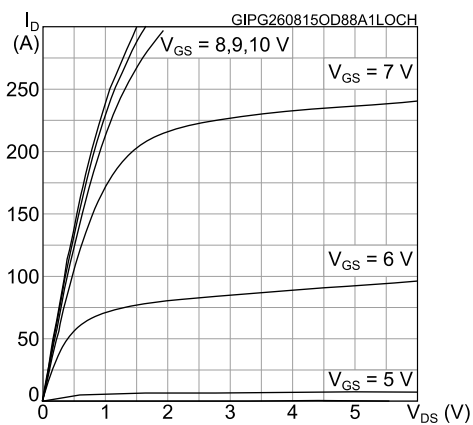


Figure 5: Transfer characteristics

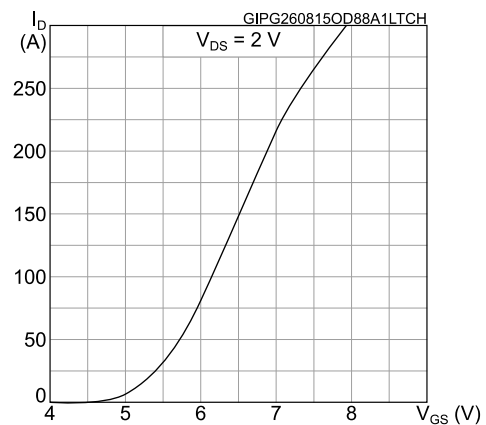


Figure 6: Gate charge vs gate-source voltage

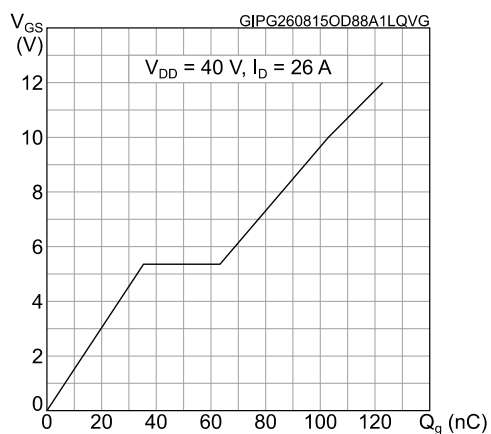


Figure 7: Static drain-source on-resistance

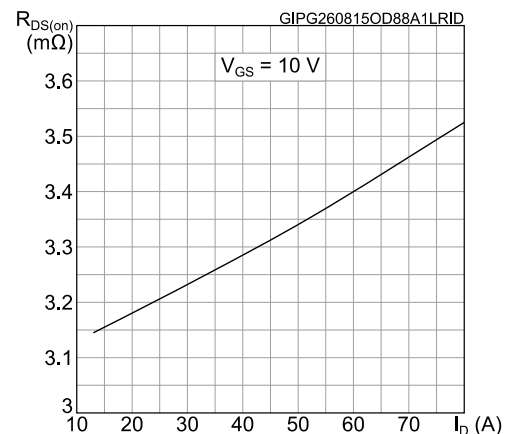


Figure 8: Capacitance variations

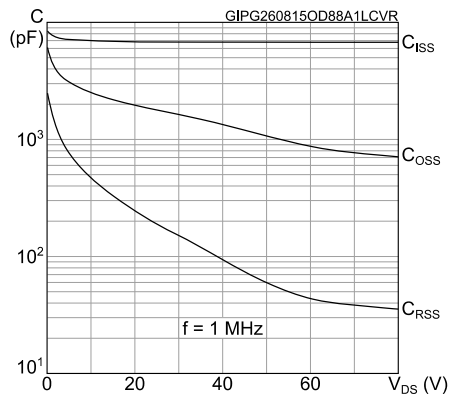


Figure 9: Normalized gate threshold voltage vs temperature

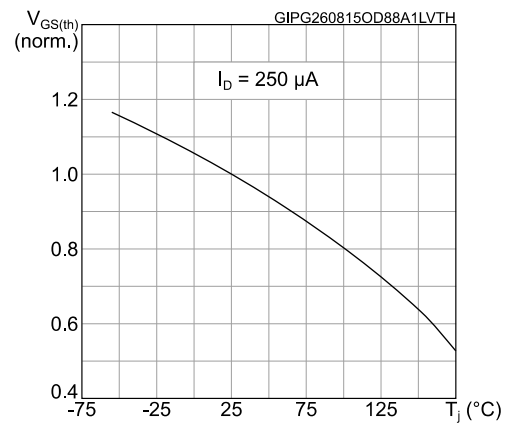


Figure 10: Normalized on-resistance vs temperature

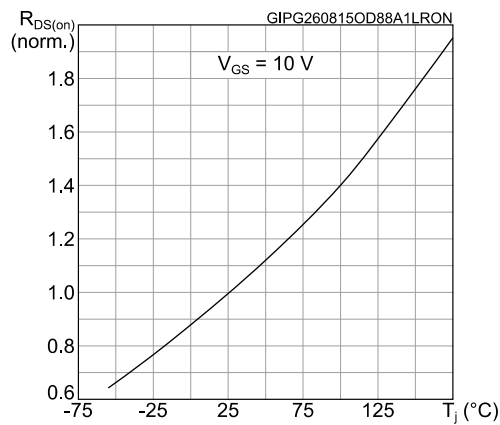
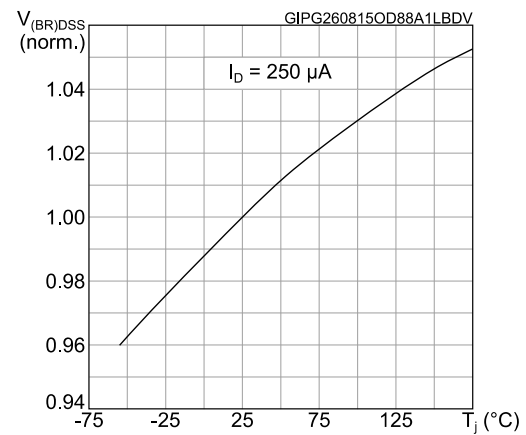
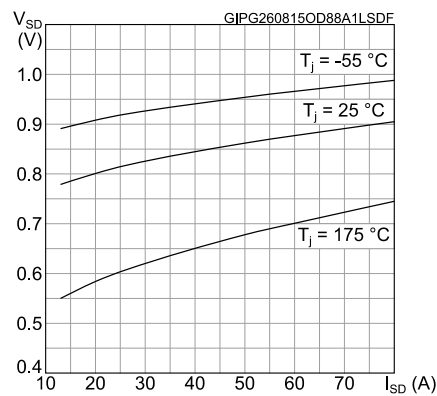
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times



Figure 14: Test circuit for gate charge behavior



Figure 15: Test circuit for inductive load switching and diode recovery times



Figure 16: Unclamped inductive load test circuit



Figure 17: Unclamped inductive waveform



Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

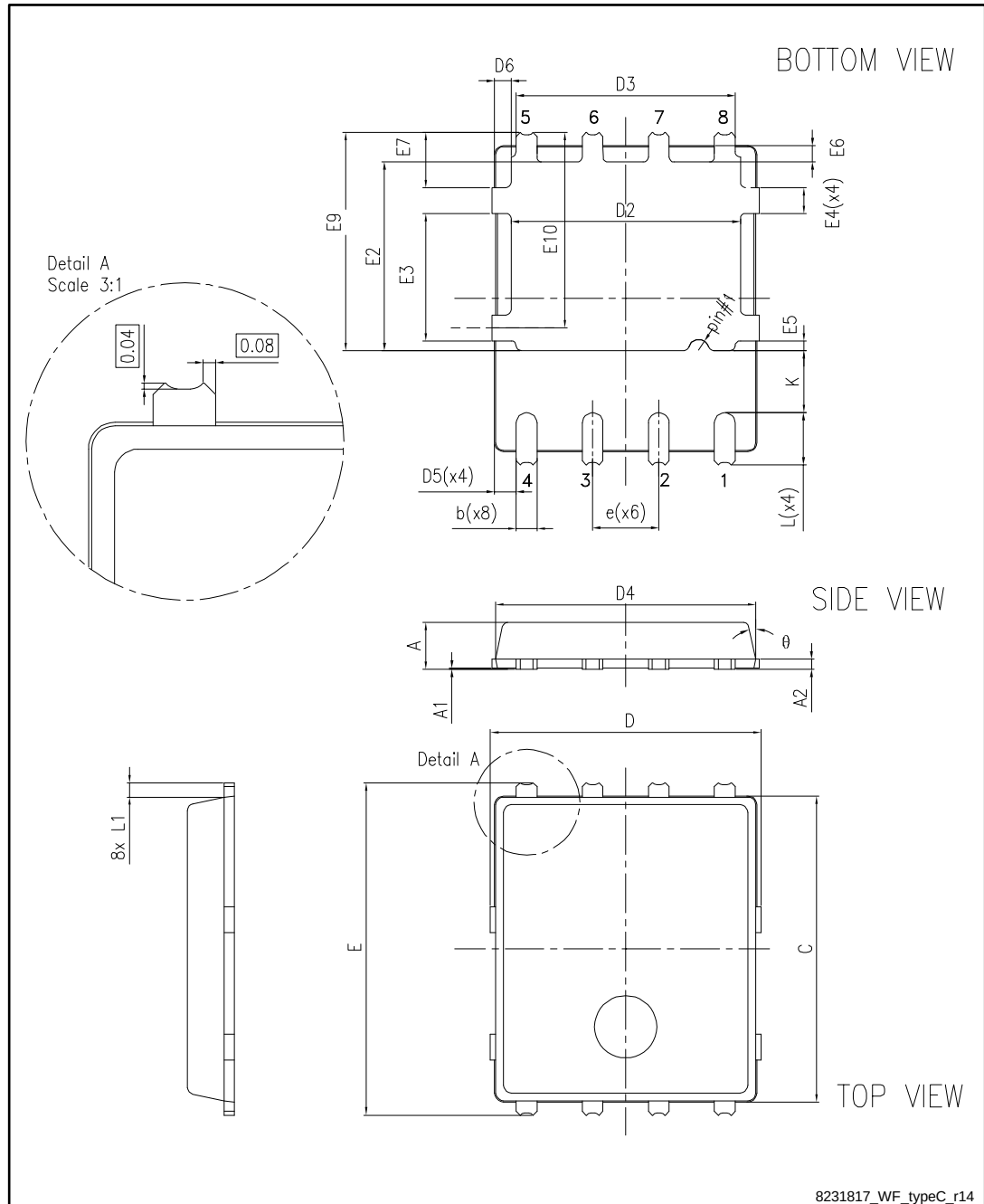
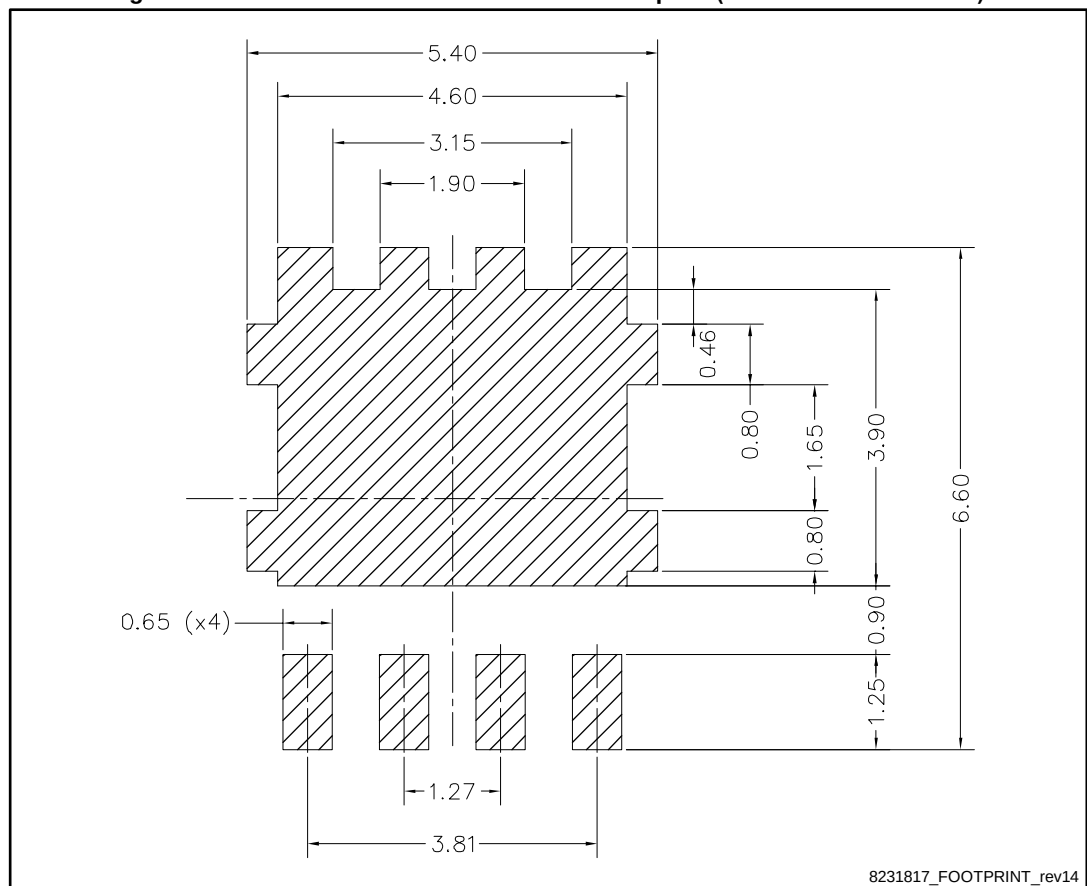


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

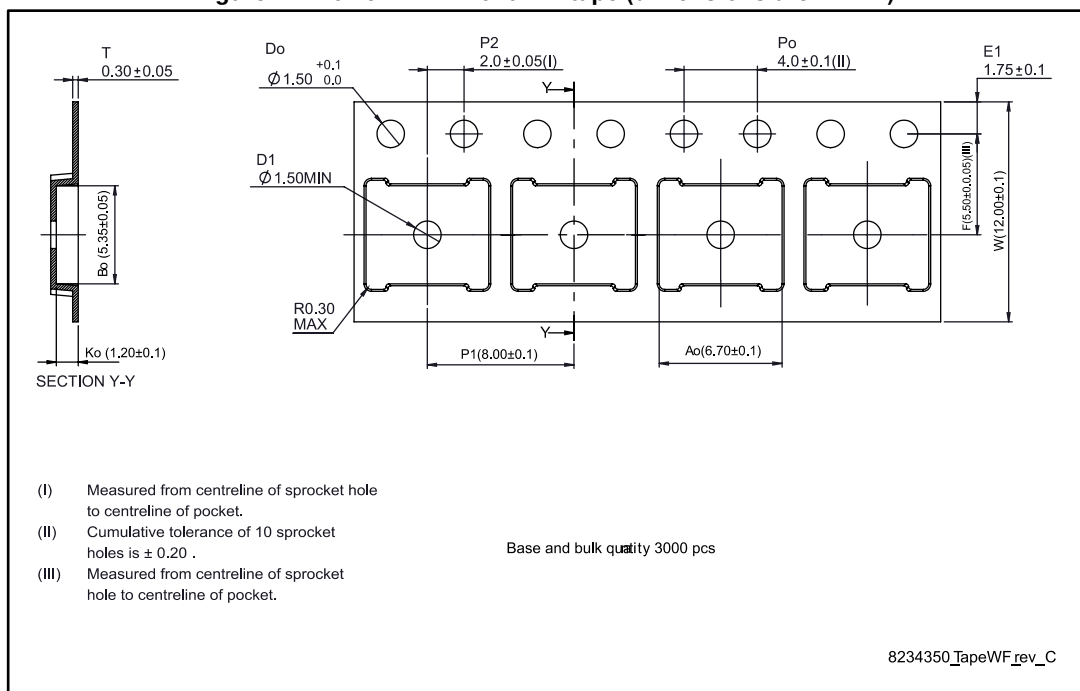


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

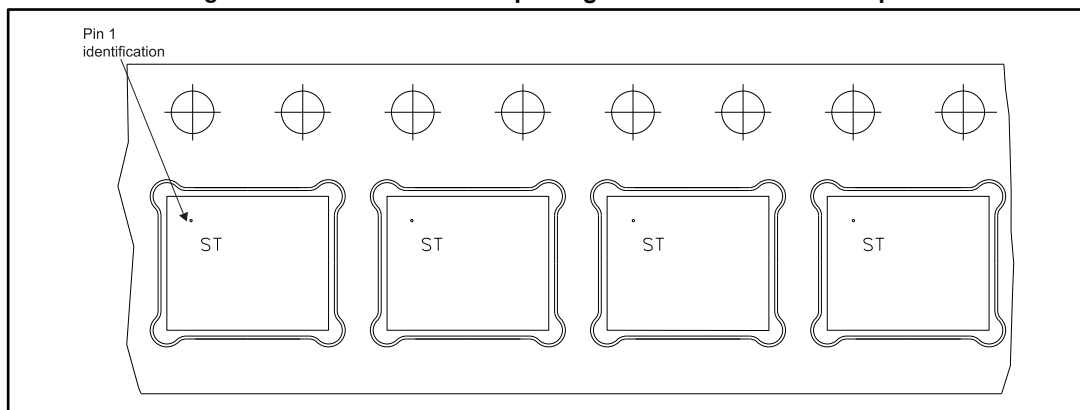
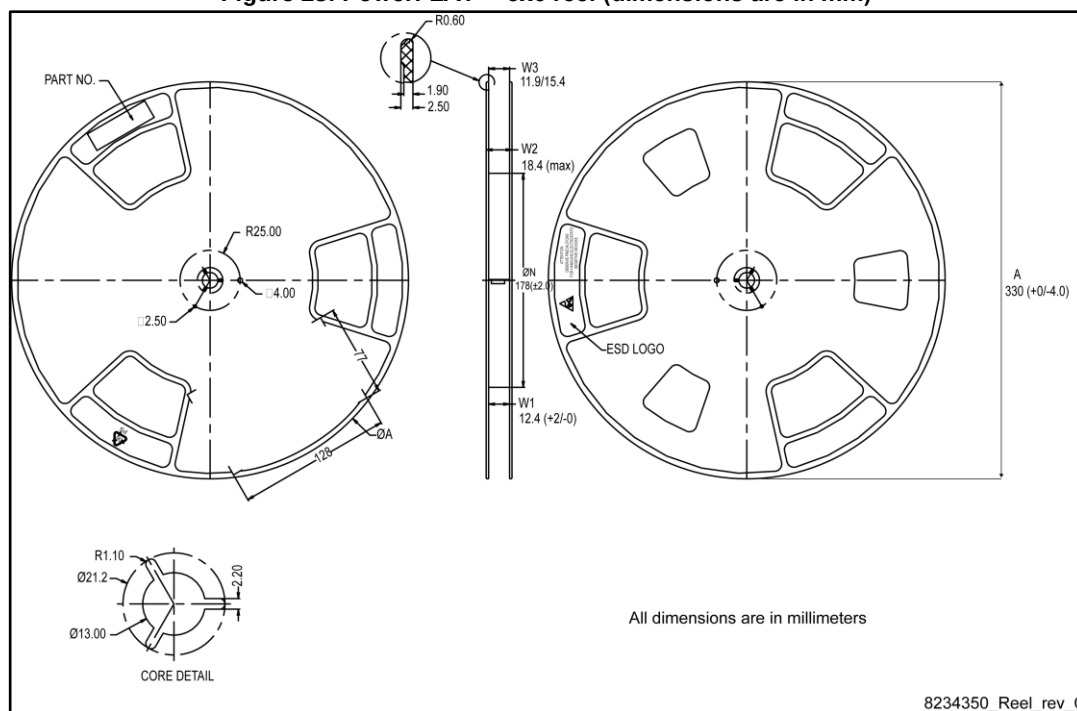


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
07-Sep-2015	1	First release.
15-Sep-2015	2	Minor text edits. On cover page: - updated Title and Features.
26-Jan-2016	3	Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Section 4.1: "PowerFLAT™ 5x6 WF type C package information"</i> .
16-Sep-2016	4	Updated the silhouette, the title and the features in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Figure 2: "Safe operating area"</i> and <i>Figure 3: "Thermal impedance"</i> . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved