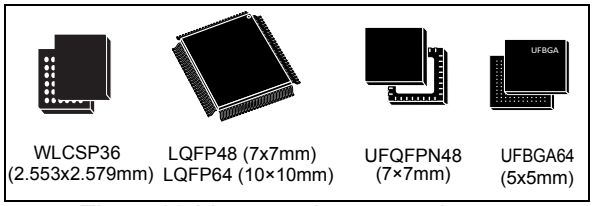
# STM32F410x8 STM32F410xB

## Arm®-Cortex®-M4 32b MCU+FPU, 125 DMIPS, 128KB Flash, 32KB RAM, 9 TIMs, 1 ADC, 1 DAC, 1 LPTIM, 9 comm. interfaces

**Datasheet - production data**

## Features

- **Includes ST state-of-the-art patented technology**
- Dynamic Efficiency Line with eBAM (enhanced Batch Acquisition Mode)
  - 1.7 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait state execution from flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 128 Kbytes of flash memory
  - 512 bytes of OTP memory
  - 32 Kbytes of SRAM
- Clock, reset, and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD, and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 89 µA/MHz (peripheral off)
  - Stop (flash in Stop mode, fast wake-up time): 40 µA typ @ 25 °C; 49 µA max @25 °C
  - Stop (flash in deep power down mode, slow wake-up time): down to 6 µA @ 25 °C; 14 µA max @25 °C
  - Standby: 2.4 µA @25 °C / 1.7 V without RTC; 12 µA @85 °C @1.7 V
  - $V_{BAT}$ supply for RTC: 1 µA @25 °C
- 1×12-bit, 2.4 MSPS ADC: up to 16 channels
- 1×12-bit D/A converter
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 9 timers
  - One low-power timer (available in Stop mode)
  - One 16-bit advanced motor-control timer
  - Three 16-bit general-purpose timers
  - One 32-bit timer up to 100 MHz with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Two watchdog timers (independent window)
  - SysTick timer.
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 50 I/O ports with interrupt capability
  - Up to 45 fast I/Os up to 100 MHz
  - Up to 49 5 V-tolerant I/Os
- Up to 9 communication interfaces
  - Up to 3x $I^2C$ interfaces (SMBus/PMBus) including 1x $I^2C$ fast mode at 1 MHz
  - Up to 3 USARTs (2 x 12.5 Mbit/s, 1 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPI/I2Ss (up to 50 Mbit/s SPI or I2S audio protocol)
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages are ECOPACK2 compliant




WLCSP36 (2.553x2.579mm) | LQFP48 (7x7mm) LQFP64 (10×10mm) | UFQFPN48 (7×7mm) | UFBGA64 (5x5mm)

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F410x8 | STM32F410T8, STM32F410C8, STM32F410R8 |
| STM32F410xB | STM32F410TB, STM32F410CB, STM32F410RB |



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# 1 Introduction

This datasheet provides the description of the STM32F410x8/B microcontrollers.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32F410x8 and STM32F410xB errata sheet (ES0325), available from *www.st.com*.

*Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

# 2 Description

The STM32F410x8/B devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all Arm single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F410x8/B belong to the STM32 Dynamic Efficiency™ product line (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F410x8/B incorporate high-speed embedded memories (up to 128 Kbytes of Flash memory, 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, one AHB bus and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, one 12-bit DAC, a low-power RTC, three general-purpose 16-bit timers, one PWM timer for motor control, one general-purpose 32-bit timers and one 16-bit low-power timer. They also feature standard and advanced communication interfaces.

- Up to three $I^2C$s
- Three SPIs
- Three $I^2S$s

  To achieve audio class accuracy, the $I^2S$ peripherals can be clocked via the internal PLL or via an external clock to allow synchronization.
- Three USARTs.

The STM32F410x8/B are offered in 5 packages ranging from 36 to 64 pins. The set of available peripherals depends on the selected package.

The STM32F410x8/B operate in the – 40 to +125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F410x8/B microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub

**Table 2. STM32F410x8/B features and peripheral counts**

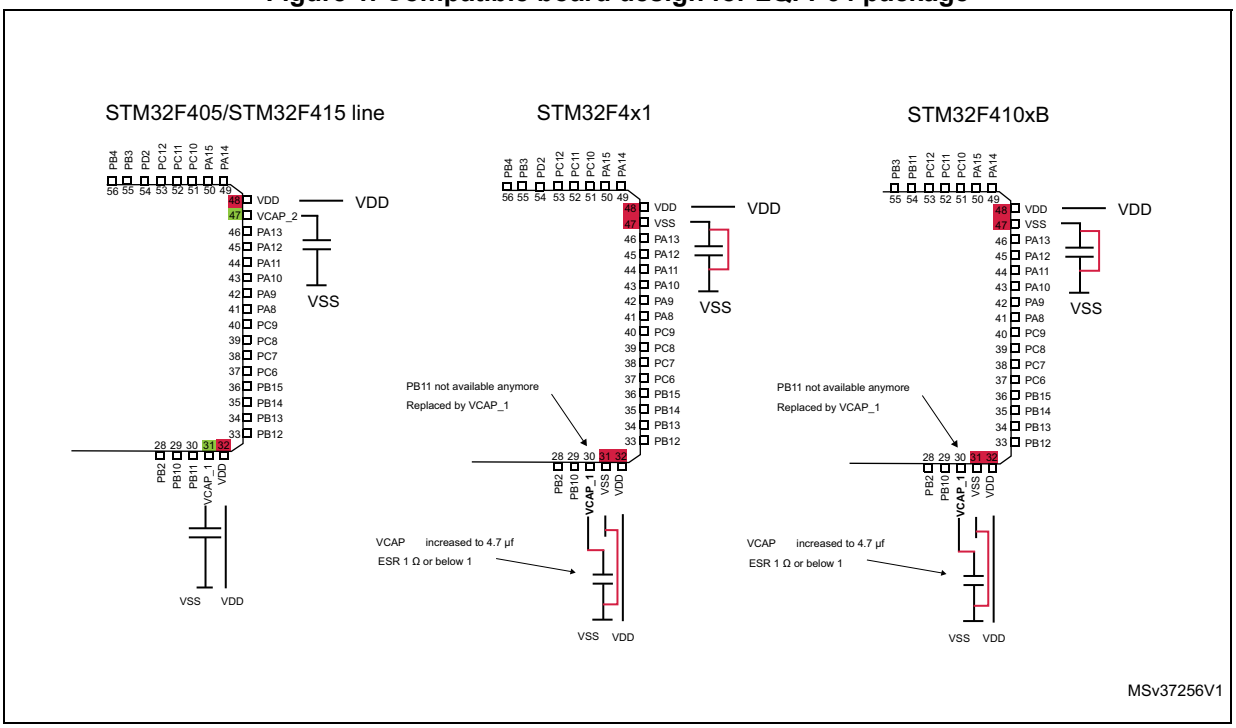
| Peripherals | | STM32 F410 T8Y | STM32 F410 TBY | STM32 F410 C8U | STM32 F410 CBU | STM32 F410 C8T | STM32 F410 CBT | STM32 F410 R8T | STM32 F410 RBT | STM32 F410 R8I | STM32 F410 RBI |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 64 | 128 | 64 | 128 | 64 | 128 | 64 | 128 | 64 | 128 |
| SRAM in Kbytes | System | 32 | | | | | | | | | |
| Timers | General-purpose | 4 | | | | | | | | | |
| | Low-power timer | 1 | | | | | | | | | |
| | Advanced-control | 1 | | | | | | | | | |
| Random number generator | | 1 | | | | | | | | | |
| Communication interfaces | SPI/ $I^2S$ | 1 | 3 | | | | | | | | |
| | $I^2C$ | 2 | 3 | | | | | | | | |
| | USART | 2 | 3 | | | | | | | | |
| GPIOs | | 23 | 36 | | | | | 50 | | | |
| 12-bit ADC Number of channels | | 1 | | | | | | | | | |
| | | 4 | 10 | | | | | 16 | | | |
| 12-bit DAC Number of channels | | 1<br>1 | | | | | | | | | |
| Maximum CPU frequency | | 100 MHz | | | | | | | | | |
| Operating voltage | | 1.7 to 3.6 V | 1.8 to 3.6 V | | | 1.7 to 3.6 V | | 1.8 to 3.6 V | | 1.7 to 3.6 V | |
| Operating temperatures | | Ambient temperatures: – 40 to +85 °C / – 40 to + 105 °C / – 40 to + 125 °C | | | | | | | | | |
| | | Junction temperature: –40 to + 130 °C | | | | | | | | | |
| Package | | WLCSP36 | UFQFPN48 | | | LQFP48 | | LQFP64 | | UFBGA64 | |

## 2.1 Compatibility with STM32F4 series

The STM32F410x8/B are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

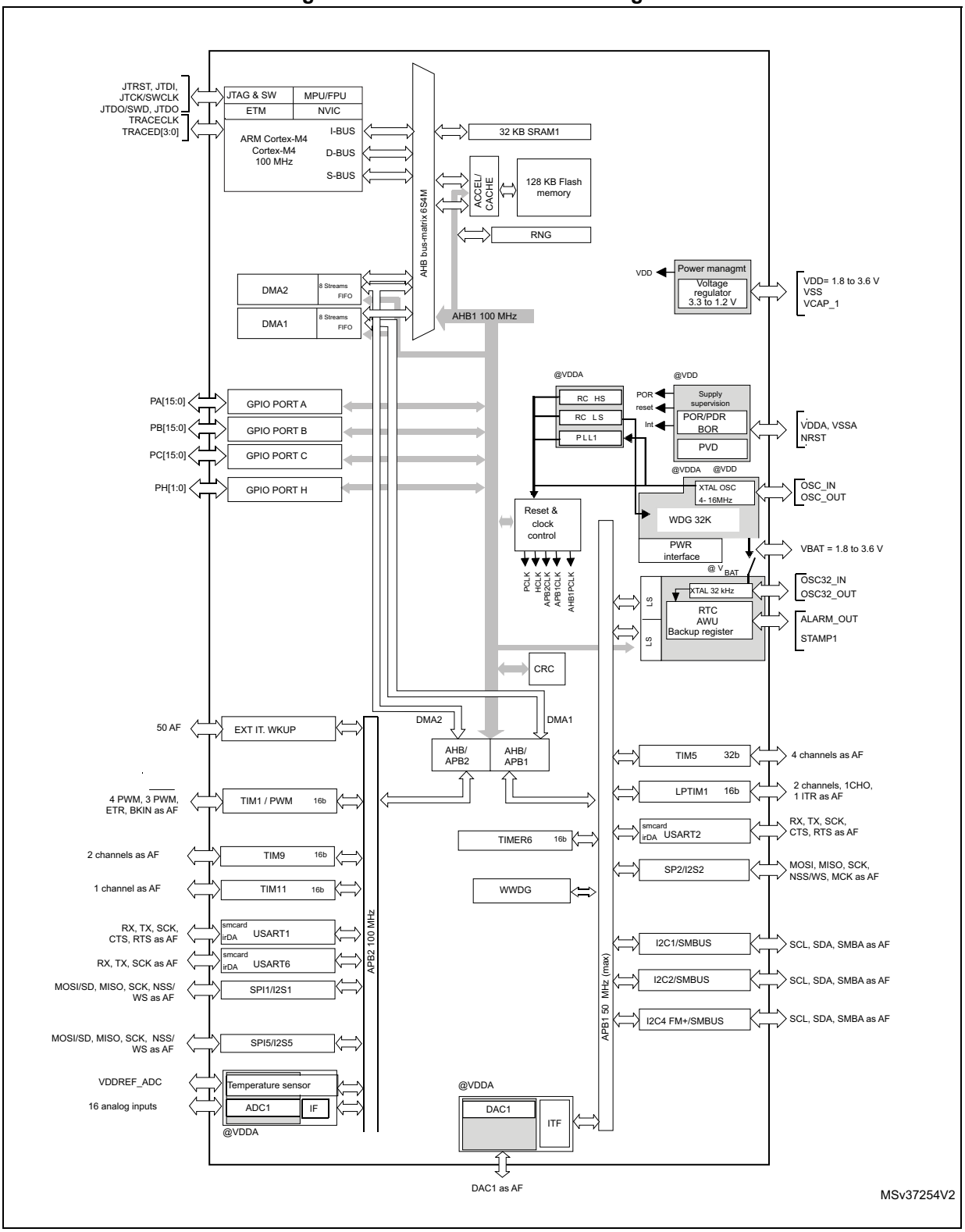
The STM32F410x8/B can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

**Figure 1. Compatible board design for LQFP64 package**




1. For STM32F410xB devices, pin 54 is bonded to PB11 instead of PD2.

**Figure 2. STM32F410x8/B block diagram**




1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 100 MHz.

# 3 Functional overview

## 3.1 Arm® Cortex®-M4 with FPU core with embedded Flash and SRAM

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F410x8/B devices are compatible with all Arm tools and software.

*Figure 2* shows the general block diagram of the STM32F410x8/B.

*Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.*

## 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

## 3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the I2S directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F410x8/B BAM to allow the best power efficiency.

## 3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.5 Embedded Flash memory

The devices embed up to 128 Kbytes of Flash memory available for storing programs and data, plus 512 bytes of OTP memory organized in 16 blocks which can be independently locked.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.18: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

## 3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

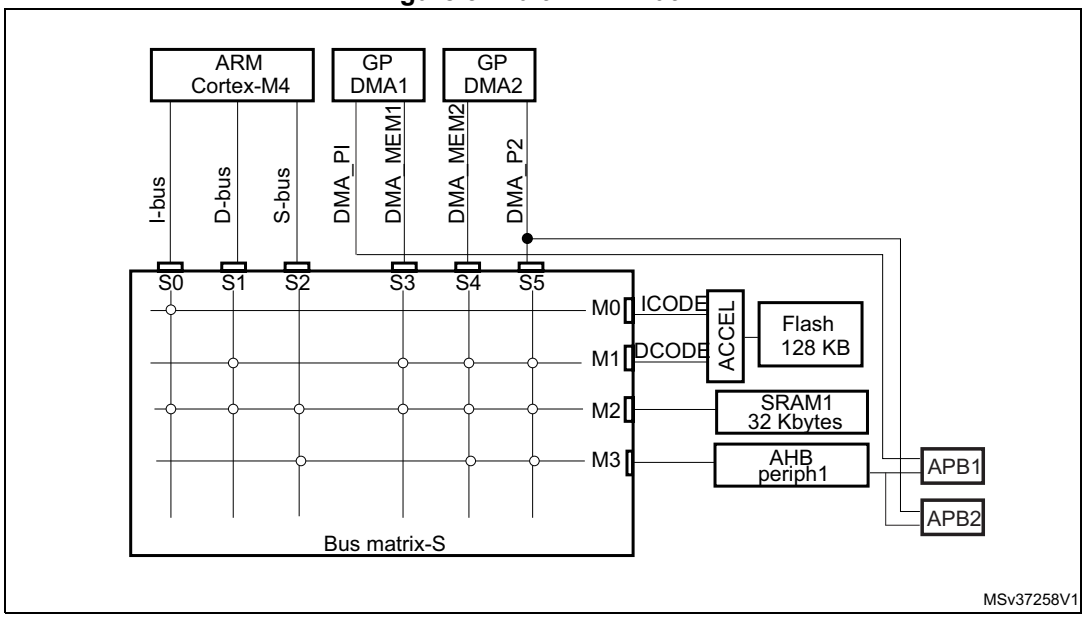
## 3.7 Embedded SRAM

All devices embed 32 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

## 3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 3. Multi-AHB matrix**




## 3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$
- USART
- General-purpose, basic and advanced-control timers TIMx
- ADC
- DAC.

## 3.10 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 50 GPIOs can be connected to the 16 external interrupt lines.

## 3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the AHB bus, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB bus and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

## 3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using the interfaces described in *Table 3*.

Refer to *Table 9: STM32F410x8/B pin definitions*) for the GPIOs available on the selected package.

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

**Table 3. Embedded bootloader interfaces**

| Package | USART1 | USART2 | I2C1 | I2C2 | I2C4 FM+ | SPI1 | SPI3 |
|---|---|---|---|---|---|---|---|
| WLCSP36 | X | PA2/PA3 | PB6/PB7 | X | PB10/PB3 | PA15/PA5 /PB4/PB5 | X |
| UFQFPN48 | PA9/PA10 | | | X | PB14/PB15 | PA4/PA5/ PA6/PA7 | X |
| LQFP64 | | | | PB10/PB11 | | | PB12/PB13 /PC2/PC3 |

## 3.14 Power supply schemes

- $V_{DD}$ = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through $V_{DD}$ pins. Requires the use of an external power supply supervisor connected to the VDD and PDR_ON pins.
- $V_{SSA}$, $V_{DDA}$ = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively, with decoupling technique.
- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.15 Power supply supervisor

### 3.15.1 Internal reset ON

This feature is available for $V_{DD}$ operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for an external reset circuit.

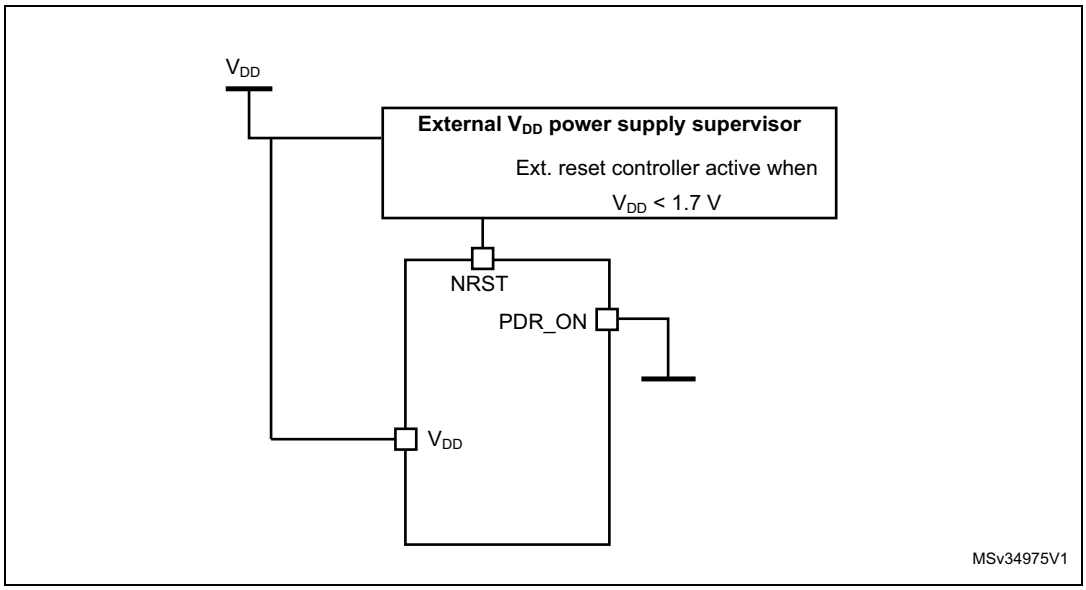
The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.15.2 Internal reset OFF

This feature is available on WLCSP36 package only. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor $V_{DD}$ and should set the device in reset mode when $V_{DD}$ is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

**Figure 4. Power supply supervisor interconnection with internal reset OFF(1)**




1. The PRD_ON pin is available on WLCSP36 package only.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.

## 3.16 Voltage regulator

The regulator has three operating modes:

– Main regulator mode (MR)
– Low power regulator (LPR)
– Power-down

The three power modes configured by software:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

An external ceramic capacitor should be connected to the $V_{CAP_1}$ pin.

### 3.16.1 Internal power supply supervisor availability

**Table 4. Regulator ON/OFF and internal power supply supervisor availability**

| Package | Power supply supervisor ON | Power supply supervisor OFF |
|---|---|---|
| UFQFPN48 | Yes | No |
| WLCSP36 | Yes<br>PDR_ON set to VDD | Yes<br>PDR_ON set to $V_{SS}$(1) |
| LQFP64 | Yes | No |

1. An external power supervisor must be used (refer to *Section 3.15.2: Internal reset OFF*).

## 3.17 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 bytes of user application data when $V_{DD}$ power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.18: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the $V_{DD}$ supply when present or from the $V_{BAT}$ pin.

## 3.18 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The RTC and the low-power timer (LPTIM1) can remain active in Stop mode. They can consequently be used to wake up the device from this mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, LPTIM1, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 3.19 $V_{BAT}$ operation

The VBAT pin allows to power the device $V_{BAT}$ domain from an external battery, an external super-capacitor, or from $V_{DD}$ when no external battery and an external super-capacitor are present.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The VBAT pin supplies the RTC and the backup registers.

*Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation. When PDR_ON pin is not connected to $V_{DD}$ (internal Reset OFF), the $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.*

## 3.20 Timers and watchdogs

The devices embed one advanced-control timer, four general purpose timers, one low power timer, two watchdog timers and one SysTick timer.

All timer counters can be frozen in debug mode.

*Table 5* compares the features of the advanced-control and general-purpose timers.

**Table 5. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complemen-tary output | Max. interface clock (MHz) | Max. timer clock (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced -control | TIM1 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 100 | 100 |
| General purpose | TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 50 | 100 |
| | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 100 | 100 |
| | TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 100 | 100 |
| Basic | TIM6 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 50 | 100 |
| Low-power | LPTIM1 | 16-bit | Up | Between 1 and 128 | No | 2 | No | 50 | 100 |

### 3.20.1 Advanced-control timers (TIM1)

The advanced-control timer (TIM1) can be seen as three-phase PWM generator multiplexed on 4 independent channels. It has complementary PWM outputs with programmable inserted dead times. It can also be considered as a complete general-purpose timer. Its 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, it has the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 supports independent DMA request generation.

### 3.20.2 General-purpose timers (TIM5, TIM9 and TIM11)

There are three synchronizable general-purpose timers embedded in the STM32F410x8/B (see *Table 5* for differences).

- **TIM5**

  The STM32F410x8/B devices includes a full-featured general-purpose timer, TIM5. TIM5 timer is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. It features four independent channels for input capture/output compare, PWM or one-pulse mode output.

  TIM5 can operate in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

  TIM5 general-purpose timer can be used to generate PWM output.

  All TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9 and TIM11**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM11 features one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM5 full-featured general-purpose timer or used as simple time bases.

### 3.20.3 Basic timer (TIM6)

This timer is mainly used for DAC triggering and waveform generation. It can also operate as generic 16-bit timers.

TIM6 supports independent DMA request generation.

### 3.20.4 Low-power timer (LPTIM1)

The devices embed one low-power timer. This timer features an independent clock and runs in Stop mode if it is clocked by LSE, LSI or by an external clock. It is able to wake up the system from Stop mode.

The low-power timer main features are the following:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI or APB1 clock
  - External clock source over LPTIM input (working even when no internal clock source is running and used by pulse-counter applications).
- Programmable digital glitch filter
- Encoder mode
- Active in Stop mode.

### 3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.21 Inter-integrated circuit interface ($I^2C$)

The devices feature up to three $I^2C$ bus interfaces which can operate in multimaster and slave modes:

- One $I^2C$ interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Two $I^2C$ interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All $I^2C$ interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

**Table 6. Comparison of I2C analog and digital filters**

| | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |

## 3.22 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 12.5 Mbit/s. The USART2 interface communicates at up to 6.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

**Table 7. USART feature comparison**

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X(1) | X | X | X | X | 6.25 | 12.5 | APB2 (max. 100 MHz) |
| USART2 | X | X(1) | X | X(1) | X | X(1) | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| USART6 (1) | X | N.A | X | X(1)(2) | X | X(1)(2) | 6.25 | 12.5 | APB2 (max. 50 MHz) |

1. Not available on WLCSP36 package.
2. Not available on UFQFPN48 package.

## 3.23 Serial peripheral interface (SPI)

The devices feature three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 and SPI5 can communicate at up to 50 Mbit/s, SPI2 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

## 3.24 Inter-integrated sound ($I^2S$)

Three standard $I^2S$ interfaces (multiplexed with SPI1 to SPI5) are available. They can be operated in master or slave mode, in simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. All the I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All $I^2Sx$ can be served by the DMA controller.

## 3.25 True random number generator (RNG)

All devices embed an RNG that is a true random number generator, providing full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

## 3.26 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

## 3.27 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1 or TIM5 timer.

## 3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 3.29 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel can be used to convert a digital signal into an analog voltage signal output. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- 8-bit or 12-bit monotonic output
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation

- Triangular-wave generation
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channel is triggered through TIM6 update output that is also connected to different DMA channels.

## 3.30 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

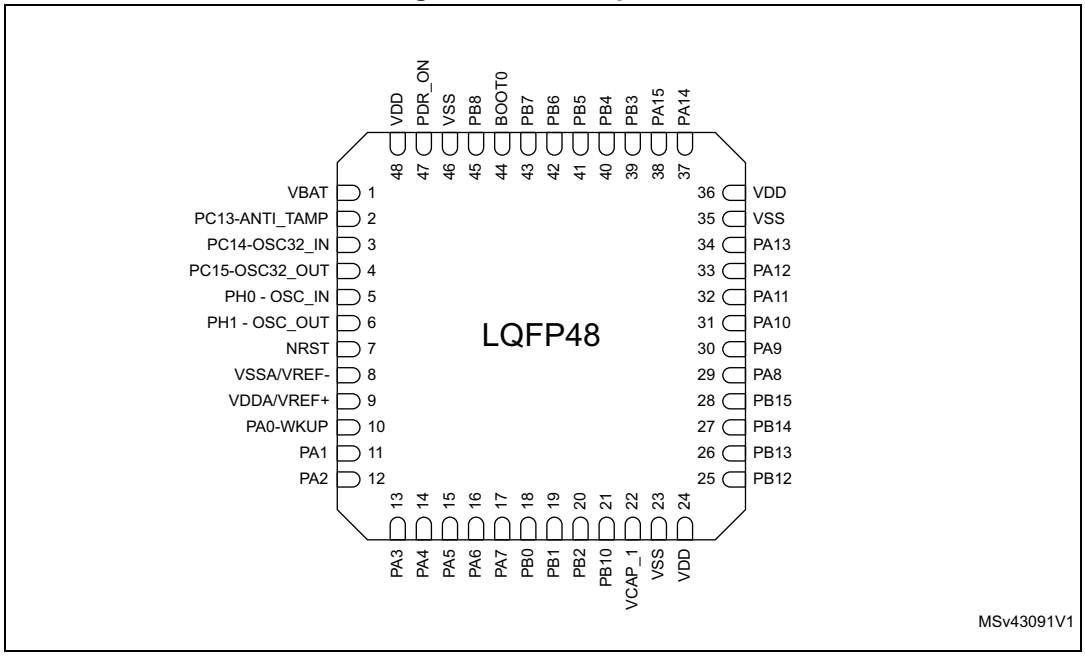
## 3.31 Embedded Trace Macrocell™

The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F410x8/B through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

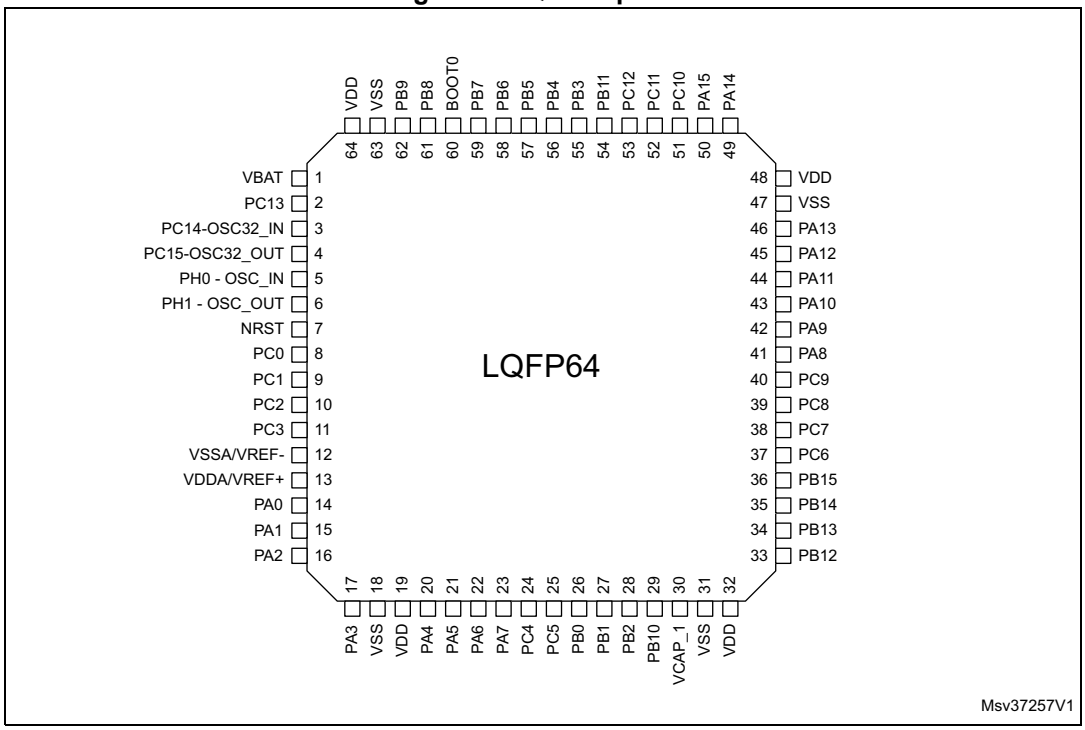
# 4 Pinouts and pin description

**Figure 5. LQFP48 pinout**



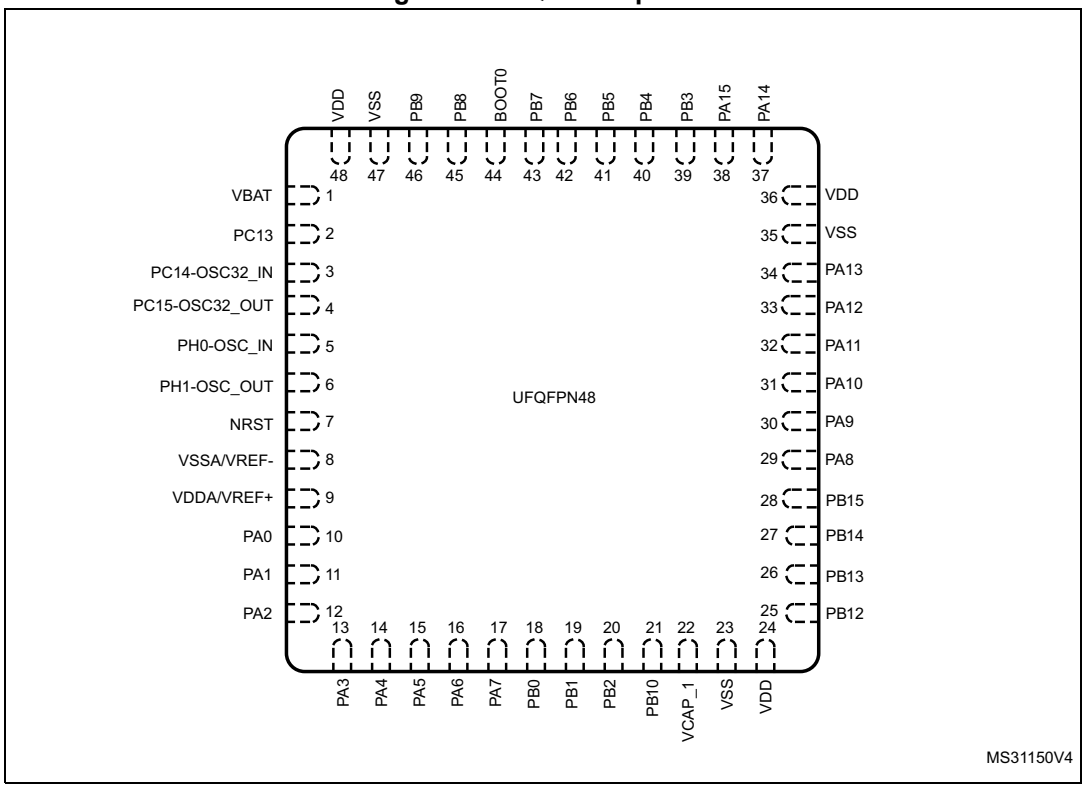

1. The above figure shows the package top view.

**Figure 6. LQFP64 pinout**



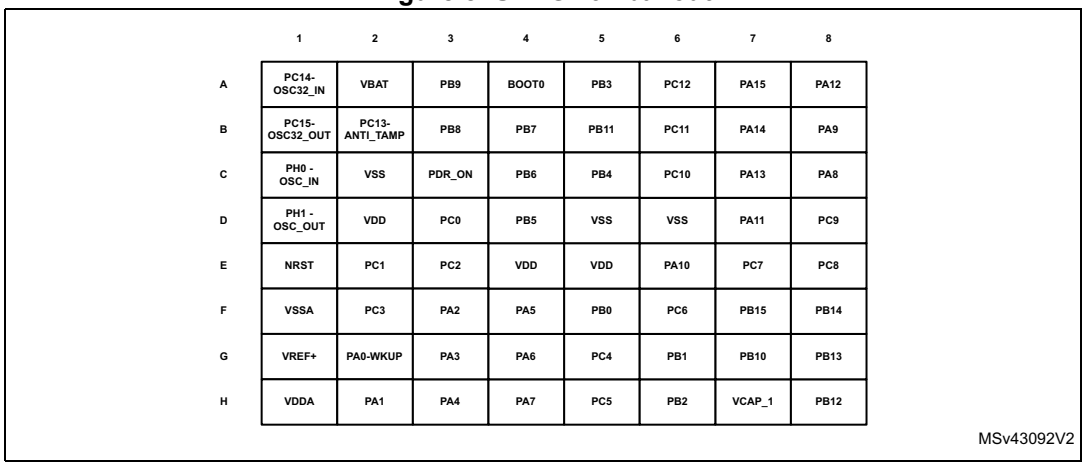

1. The above figure shows the package top view.

**Figure 7. UFQFPN48 pinout**



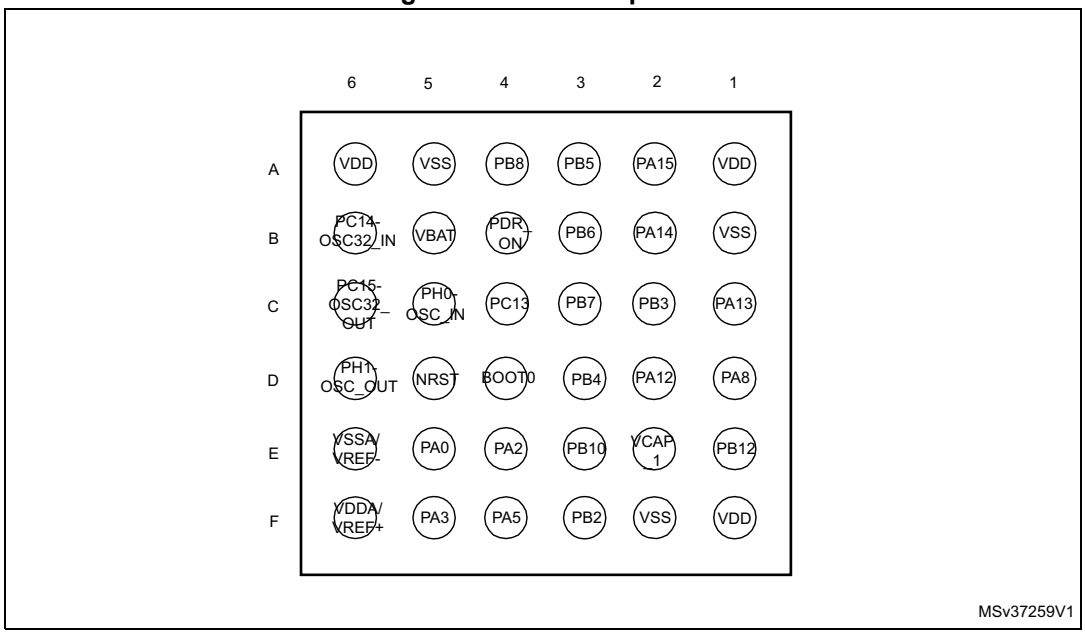

1. The above figure shows the package top view.

**Figure 8. UFBGA64 ballout**




1. The above figure shows the package top view.

**Figure 9. WLCSP36 pinout**




1. The above figure shows the package bump side.

**Table 8. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input/output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | TC | Standard 3.3 V I/O |
| | B | Dedicated BOOT0 pin |
| | NRST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Alternate functions | Functions selected through GPIOx_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 9. STM32F410x8/B pin definitions**

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP36 | LQFP48 | UFQFPN48 | LQFP64 | UFBGA64 | | | | | | |
| B5 | 1 | 1 | 1 | A2 | VBAT | S | - | - | - | VBAT |
| - | - | - | - | C2 | VSS | S | - | - | - | - |
| C4 | 2 | 2 | 2 | B2 | PC13 | I/O | FT | (2)(3) | EVENTOUT | RTC_TAMP1, RTC_OUT, RTC_TS |
| B6 | 3 | 3 | 3 | A1 | PC14-OSC32_IN | I/O | FT | (2)(3)(4) | EVENTOUT | OSC32_IN |
| C6 | 4 | 4 | 4 | B1 | PC15-OSC32_OUT | I/O | FT | (2)(4) | EVENTOUT | OSC32_OUT |
| - | - | - | - | D2 | VDD | S | - | - | - | - |
| C5 | 5 | 5 | 5 | C1 | PH0 - OSC_IN | I/O | FT | (4) | EVENTOUT | OSC_IN |
| D6 | 6 | 6 | 6 | D1 | PH1 - OSC_OUT | I/O | FT | (4) | EVENTOUT | OSC_OUT |
| D5 | 7 | 7 | 7 | E1 | NRST | NRST | - | - | - | - |
| - | - | - | 8 | D3 | PC0 | I/O | FT | - | LPTIM1_IN1, EVENTOUT | ADC1_10, WKUP2 |
| - | - | - | 9 | E2 | PC1 | I/O | FT | - | LPTIM1_OUT, EVENTOUT | ADC1_11, WKUP3 |
| - | - | - | 10 | E3 | PC2 | I/O | FT | - | LPTIM1_IN2, SPI2_MISO, EVENTOUT | ADC1_12 |
| - | - | - | 11 | F2 | PC3 | I/O | FT | - | LPTIM1_ETR, SPI2_MOSI/I2S2_SD, EVENTOUT | ADC1_13 |
| E6 | 8 | 8 | 12 | F1 | VSSA/VREF- | S | - | - | - | - |
| F6 | 9 | 9 | 13 | - | VDDA/VREF+ | S | - | - | - | - |
| - | - | - | - | G1 | VREF+ | S | - | - | - | - |
| - | - | - | - | H1 | VDDA | S | - | - | - | - |
| E5 | 10 | 10 | 14 | G2 | PA0 | I/O | FT | - | TIM5_CH1, USART2_CTS, EVENTOUT | ADC1_0, WKUP1 |
| - | 11 | 11 | 15 | H2 | PA1 | I/O | FT | - | TIM5_CH2, USART2_RTS, EVENTOUT | ADC1_1 |

Table 9. STM32F410x8/B pin definitions (continued)

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP36 | LQFP48 | UFQFPN48 | LQFP64 | UFBGA64 | | | | | | |
| E4 | 12 | 12 | 16 | F3 | PA2 | I/O | FT | - | TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, EVENTOUT | ADC1_2 |
| F5 | 13 | 13 | 17 | G3 | PA3 | I/O | FT | - | TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, EVENTOUT | ADC1_3 |
| - | - | - | 18 | D5 | VSS | S | - | - | - | - |
| - | - | - | 19 | E4 | VDD | S | - | - | - | - |
| - | 14 | 14 | 20 | H3 | PA4 | I/O | FT | - | SPI1_NSS/I2S1_WS, USART2_CK, EVENTOUT | ADC1_4 |
| F4 | 15 | 15 | 21 | F4 | PA5 | I/O | TC | - | SPI1_SCK/I2S1_CK, EVENTOUT | ADC1_5, DAC_OUT1 |
| - | 16 | 16 | 22 | G4 | PA6 | I/O | FT | - | TIM1_BKIN, SPI1_MISO, I2S2_MCK, EVENTOUT | ADC1_6 |
| - | 17 | 17 | 23 | H4 | PA7 | I/O | FT | - | TIM1_CH1N, SPI1_MOSI/I2S1_SD, EVENTOUT | ADC1_7 |
| - | - | - | 24 | G5 | PC4 | I/O | FT | - | TIM9_CH1, EVENTOUT | ADC1_14 |
| - | - | - | 25 | H5 | PC5 | I/O | FT | - | TIM9_CH2, I2C4_SMBA, EVENTOUT | ADC1_15 |
| - | 18 | 18 | 26 | F5 | PB0 | I/O | FT | - | TIM1_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT | ADC1_8 |
| - | 19 | 19 | 27 | G6 | PB1 | I/O | TC | - | TIM1_CH3N, SPI5_NSS/I2S5_WS, EVENTOUT | ADC1_9 |
| F3 | 20 | 20 | 28 | H6 | PB2 | I/O | FT | - | LPTIM1_OUT, EVENTOUT | BOOT1 |

Table 9. STM32F410x8/B pin definitions (continued)

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP36 | LQFP48 | UFQFPN48 | LQFP64 | UFBGA64 | | | | | | |
| E3 | 21 | 21 | 29 | G7 | PB10 | I/O | FT | - | I2C2_SCL, SPI2_SCK/I2S2_CK, I2S1_MCK, I2C4_SCL, EVENTOUT | - |
| E2 | 22 | 22 | 30 | H7 | VCAP_1 | S | - | - | - | - |
| F2 | 23 | 23 | 31 | D6 | VSS | S | - | - | - | - |
| F1 | 24 | 24 | 32 | E5 | VDD | S | - | - | - | - |
| E1 | 25 | 25 | 33 | H8 | PB12 | I/O | FT | - | TIM1_BKIN, TIM5_CH1, I2C2_SMBA, SPI2_NSS/I2S2_WS, EVENTOUT | - |
| - | 26 | 26 | 34 | G8 | PB13 | I/O | FT | - | TIM1_CH1N, I2C4_SMBA, SPI2_SCK/I2S2_CK, EVENTOUT | - |
| - | 27 | 27 | 35 | F8 | PB14 | I/O | FT | - | TIM1_CH2N, I2C4_SDA, SPI2_MISO, EVENTOUT | - |
| - | 28 | 28 | 36 | F7 | PB15 | I/O | FT | - | RTC_50Hz, TIM1_CH3N, I2C4_SCL, SPI2_MOSI/I2S2_SD, EVENTOUT | - |
| - | - | - | 37 | F6 | PC6 | I/O | FT | - | TRACECLK, I2C4_SCL, I2S2_MCK, USART6_TX, EVENTOUT | - |
| - | - | - | 38 | E7 | PC7 | I/O | FT | - | I2C4_SDA, SPI2_SCK/I2S2_CK, I2S1_MCK, USART6_RX, EVENTOUT | - |
| - | - | - | 39 | E8 | PC8 | I/O | FT | - | USART6_CK, EVENTOUT | - |
| - | - | - | 40 | D8 | PC9 | I/O | FT | - | MCO_2, I2C4_SDA, I2S2_CKIN, EVENTOUT | - |

Table 9. STM32F410x8/B pin definitions (continued)

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP36 | LQFP48 | UFQFPN48 | LQFP64 | UFBGA64 | | | | | | |
| D1 | 29 | 29 | 41 | C8 | PA8 | I/O | FT | - | MCO_1, TIM1_CH1, I2C4_SCL, USART1_CK, EVENTOUT | - |
| - | 30 | 30 | 42 | B8 | PA9 | I/O | FT | - | TIM1_CH2, USART1_TX, EVENTOUT | - |
| - | 31 | 31 | 43 | E6 | PA10 | I/O | FT | - | TIM1_CH3, SPI5_MOSI/I2S5_SD, USART1_RX, EVENTOUT | - |
| - | 32 | 32 | 44 | D7 | PA11 | I/O | FT | - | TIM1_CH4, USART1_CTS, USART6_TX, EVENTOUT | - |
| D2 | 33 | 33 | 45 | A8 | PA12 | I/O | FT | - | TIM1_ETR, SPI5_MISO, USART1_RTS, USART6_RX, EVENTOUT | - |
| C1 | 34 | 34 | 46 | C7 | PA13 | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| B1 | 35 | 35 | 47 | D5 | VSS | S | - | - | - | - |
| - | 36 | 36 | 48 | - | VDD | S | - | - | - | - |
| A1 | - | - | - | - | VDD | S | - | - | - | - |
| B2 | 37 | 37 | 49 | B7 | PA14 | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| A2 | 38 | 38 | 50 | A7 | PA15 | I/O | FT | - | JTDI, SPI1_NSS/I2S1_WS, USART1_TX, EVENTOUT | - |
| - | - | - | 51 | C6 | PC10 | I/O | FT | - | TRACED0, TIM5_CH2, EVENTOUT | - |
| - | - | - | 52 | B6 | PC11 | I/O | FT | - | TRACED1, TIM5_CH3, EVENTOUT | - |
| - | - | - | 53 | A6 | PC12 | I/O | FT | - | TRACED2, TIM11_CH1, EVENTOUT | - |

**Table 9. STM32F410x8/B pin definitions (continued)**

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP36 | LQFP48 | UFQFPN48 | LQFP64 | UFBGA64 | | | | | | |
| - | - | - | 54 | B5 | PB11 | I/O | FT | - | TRACED3, TIM5_CH4, I2C2_SDA, I2S2_CKIN, EVENTOUT | - |
| C2 | 39 | 39 | 55 | A5 | PB3 | I/O | FT | - | JTDO-SWO, I2C4_SDA, SPI1_SCK/I2S1_CK, USART1_RX, I2C2_SDA, EVENTOUT | - |
| D3 | 40 | 40 | 56 | C5 | PB4 | I/O | FT | - | JTRST, SPI1_MISO, EVENTOUT | - |
| A3 | 41 | 41 | 57 | D4 | PB5 | I/O | FT | - | LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI/I2S1_SD, EVENTOUT | - |
| B3 | 42 | 42 | 58 | C4 | PB6 | I/O | FT | - | LPTIM1_ETR, I2C1_SCL, USART1_TX, EVENTOUT | - |
| C3 | 43 | 43 | 59 | B4 | PB7 | I/O | FT | - | LPTIM1_IN2, I2C1_SDA, USART1_RX, EVENTOUT | - |
| D4 | 44 | 44 | 60 | A4 | BOOT0 | I | B | - | - | VPP |
| A4 | 45 | 45 | 61 | B3 | PB8 | I/O | FT | - | LPTIM1_OUT, I2C1_SCL, SPI5_MOSI/I2S5_SD, EVENTOUT | - |
| - | - | 46 | 62 | A3 | PB9 | I/O | FT | - | TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C2_SDA, EVENTOUT | - |
| A5 | 46 | 47 | 63 | - | VSS | S | - | - | - | - |
| B4 | 47 | - | - | C3 | PDR_ON | I | FT | - | - | - |
| A6 | 48 | 48 | 64 | - | VDD | S | - | - | - | - |

1. Function availability depends on the chosen device.

2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F410x8/Breference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

**Table 10. Alternate function mapping**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/LPTIM1 | TIM5 | TIM9/ TIM11 | I2C1/I2C2 /I2C4 | SPI1/I2S1/S PI2/I2S2 | SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5 | USART1/ USART2 | USART6 | I2C2/ I2C4 | - | - | - | - | - | SYS_AF |
| Port A | PA0 | - | - | TIM5_ CH1 | - | - | - | - | USART2_ CTS | - | - | - | - | - | - | - | EVENTOUT |
| | PA1 | - | - | TIM5_ CH2 | - | - | - | - | USART2_ RTS | - | - | - | - | - | - | - | EVENTOUT |
| | PA2 | - | - | TIM5_ CH3 | TIM9_ CH1 | - | I2S2_ CKIN | - | USART2_ TX | - | - | - | - | - | - | - | EVENTOUT |
| | PA3 | - | - | TIM5_ CH4 | TIM9_ CH2 | - | I2S2_MCK | - | USART2_ RX | - | - | - | - | - | - | - | EVENTOUT |
| | PA4 | - | - | - | - | - | SPI1_NSS/ I2S1_WS | - | USART2_ CK | - | - | - | - | - | - | - | EVENTOUT |
| | PA5 | - | - | - | - | - | SPI1_SCK/ I2S1_CK | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA6 | - | TIM1_BKIN | - | - | - | SPI1_MISO | I2S2_MCK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA7 | - | TIM1_CH1N | - | - | - | SPI1_MOSI /I2S1_SD | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA8 | MCO_1 | TIM1_CH1 | - | - | I2C4_ SCL | - | - | USART1_ CK | - | - | - | - | - | - | - | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | - | - | - | USART1_ TX | - | - | - | - | - | - | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | SPI5_MOSI /I2S5_SD | USART1_ RX | - | - | - | - | - | - | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | - | - | USART1_ CTS | USART6 _TX | - | - | - | - | - | - | EVENTOUT |
| | PA12 | - | TIM1_ETR | - | - | - | - | SPI5_MISO | USART1_ RTS | USART6 _RX | - | - | - | - | - | - | EVENTOUT |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA15 | JTDI | - | - | - | - | SPI1_NSS/ I2S1_WS | - | USART1_ TX | - | - | - | - | - | - | - | EVENTOUT |

**Table 10. Alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/LPTIM1 | TIM5 | TIM9/ TIM11 | I2C1/I2C2 /I2C4 | SPI1/I2S1/S PI2/I2S2 | SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5 | USART1/ USART2 | USART6 | I2C2/ I2C4 | - | - | - | - | - | SYS_AF |
| Port B | PB0 | - | TIM1_CH2N | - | - | - | - | SPI5_SCK/ I2S5_CK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | - | - | - | - | SPI5_NSS/ I2S5_WS | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB2 | - | LPTIM1_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO-SWO | - | - | - | I2C4_ SDA | SPI1_SCK/I 2S1_CK | - | USART1_ RX | - | I2C2_ SDA | - | - | - | - | - | EVENTOUT |
| | PB4 | JTRST | - | - | - | - | SPI1_MISO | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB5 | - | LPTIM1_IN1 | - | - | I2C1_ SMBA | SPI1_MOSI /I2S1_SD | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB6 | - | LPTIM1_ETR | - | - | I2C1_ SCL | - | - | USART1_ TX | - | - | - | - | - | - | - | EVENTOUT |
| | PB7 | - | LPTIM1_IN2 | - | - | I2C1_ SDA | - | - | USART1_ RX | - | - | - | - | - | - | - | EVENTOUT |
| | PB8 | - | LPTIM1_OUT | - | - | I2C1_ SCL | - | SPI5_MOSI /I2S5_SD | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB9 | - | - | - | TIM11_ CH1 | I2C1_ SDA | SPI2_NSS/ I2S2_WS | - | - | - | I2C2_ SDA | - | - | - | - | - | EVENTOUT |
| | PB10 | - | - | - | - | I2C2_ SCL | SPI2_SCK/ I2S2_CK | I2S1_MCK | - | - | I2C4_ SCL | - | - | - | - | - | EVENTOUT |
| | PB11 | TRACED3 | - | TIM5_ CH4 | - | I2C2_ SDA | I2S2_CKIN | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB12 | - | TIM1_BKIN | TIM5_ CH1 | - | I2C2_ SMBA | SPI2_NSS/ I2S2_WS | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | I2C4_ SMBA | SPI2_SCK /I2S2_CK | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | - | I2C4_ SDA | SPI2_MISO | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB15 | RTC_ 50Hz | TIM1_CH3N | - | - | I2C4_ SCL | SPI2_MOSI /I2S2_SD | - | - | - | - | - | - | - | - | - | EVENTOUT |

**Table 10. Alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/LPTIM1 | TIM5 | TIM9/ TIM11 | I2C1/I2C2 /I2C4 | SPI1/I2S1/S PI2/I2S2 | SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5 | USART1/ USART2 | USART6 | I2C2/ I2C4 | - | - | - | - | - | SYS_AF |
| Port C | PC0 | - | LPTIM1_IN1 | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC1 | - | LPTIM1_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC2 | - | LPTIM1_IN2 | - | - | - | SPI2_MISO | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC3 | - | LPTIM1_ETR | - | - | - | SPI2_MOSI /I2S2_SD | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC4 | - | - | - | TIM9_ CH1 | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC5 | - | - | - | TIM9_ CH2 | I2C4_ SMBA | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC6 | TRACE CLK | - | - | - | I2C4_ SCL | I2S2_MCK | - | - | USART6 _TX | - | - | - | - | - | - | EVENTOUT |
| | PC7 | - | - | - | - | I2C4_ SDA | SPI2_SCK/ I2S2_CK | I2S1_MCK | - | USART6 _RX | - | - | - | - | - | - | EVENTOUT |
| | PC8 | - | - | - | - | - | - | - | - | USART6 _CK | - | - | - | - | - | - | EVENTOUT |
| | PC9 | MCO_2 | - | - | - | I2C4_ SDA | I2S2_CKIN | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC10 | TRACED0 | - | TIM5_ CH2 | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC11 | TRACED1 | - | TIM5_ CH3 | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC12 | TRACED2 | - | - | TIM11_ CH1 | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| Port H | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

# 5 Memory mapping

The memory map is shown in *Figure 10*.

**Figure 10. Memory map**

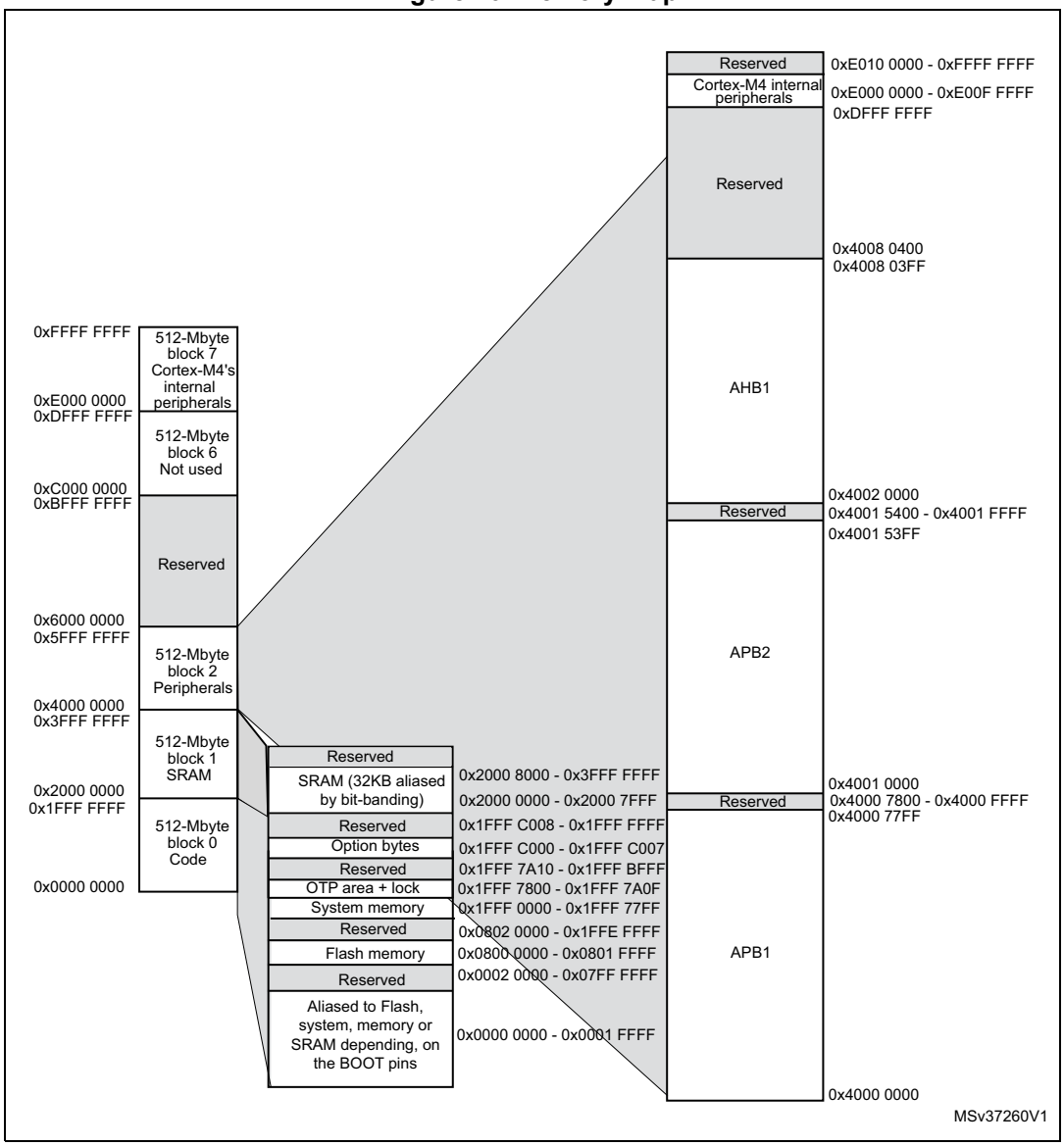


**Table 11. STM32F410x8/B register boundary addresses(1)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| - | 0xE010 0000 - 0xFFFF FFFF | Reserved |
| Cortex®-M4 | 0xE000 0000 - 0xE00F FFFF | Cortex-M4 internal peripherals |
| - | 0x5000 0000 - 0xDFFF FFFF | Reserved |
| AHB1 | 0x4008 0400 - 0x4FFF FFFF | Reserved |
| | 0x4008 0000 - 0x4008 03FF | RNG |
| | 0x4002 6800 - 0x4007 FFFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 5000 - 0x4002 4FFF | Reserved |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0x4002 3400 - 0x4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2800 - 0x4002 2FFF | Reserved |
| | 0x4002 2400 - 0x4002 27FF | LPTIM1 |
| | 0x4002 2000 - 0x4002 23FF | Reserved |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 0C00 - 0x4002 1BFF | Reserved |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

**Table 11. STM32F410x8/B register boundary addresses(1)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| APB2 | 0x4001 5400- 0x4001 FFFF | Reserved |
| | 0x4001 5000 - 0x4001 53FF | SPI5/I2S5 |
| | 0x4001 4C00- 0x4001 4FFF | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | TIM11 |
| | 0x4001 4400 - 0x4001 47FF | Reserved |
| | 0x4001 4000 - 0x4001 43FF | TIM9 |
| | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | 0x4001 3400 - 0x4001 37FF | Reserved |
| | 0x4001 3000 - 0x4001 33FF | SPI1/I2S1 |
| | 0x4001 2400 - 0x4001 2FF | Reserved |
| | 0x4001 2000 - 0x4001 23FF | ADC1 |
| | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | 0x4001 1400 - 0x4001 17FF | USART6 |
| | 0x4001 1000 - 0x4001 13FF | USART1 |
| | 0x4001 0400 - 0x4001 0FFF | Reserved |
| | 0x4001 0000 - 0x4001 03FF | TIM1 |

**Table 11. STM32F410x8/B register boundary addresses(1)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| APB1 | 0x4000 7800 - 0x4000 FFFF | Reserved |
| | 0x4000 7400 - 0x4000 77FF | DAC |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6400 - 0x4000 6FFF | Reserved |
| | 0x4000 6000 - 0x4000 63FF | I2C4 FM+ |
| | 0x4000 5C00 - 0x4000 5FFF | Reserved |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 4800 - 0x4000 53FF | Reserved |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | Reserved |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | Reserved |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 1400 - 0x4000 27FF | Reserved |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0000 - 0x4000 0BFF | Reserved |

1. The gray color is used for reserved boundary address.

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 1.7 V ≤$V_{DD}$ ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

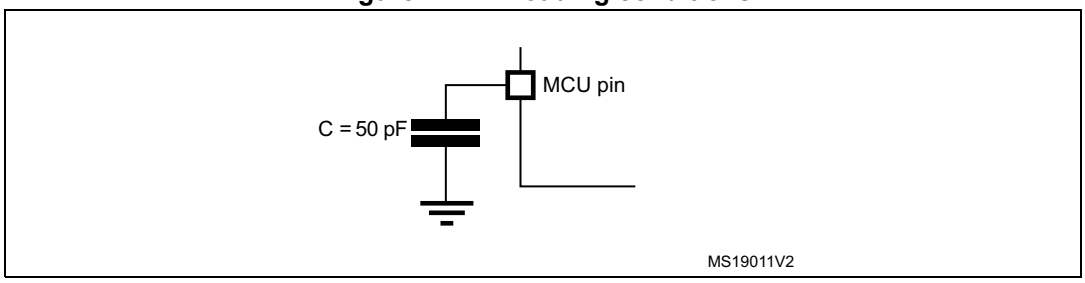
### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

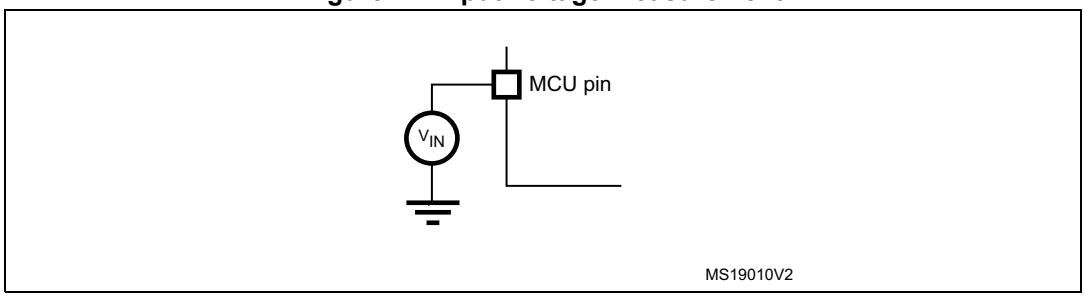
**Figure 11. Pin loading conditions**



### 6.1.5 Pin input voltage

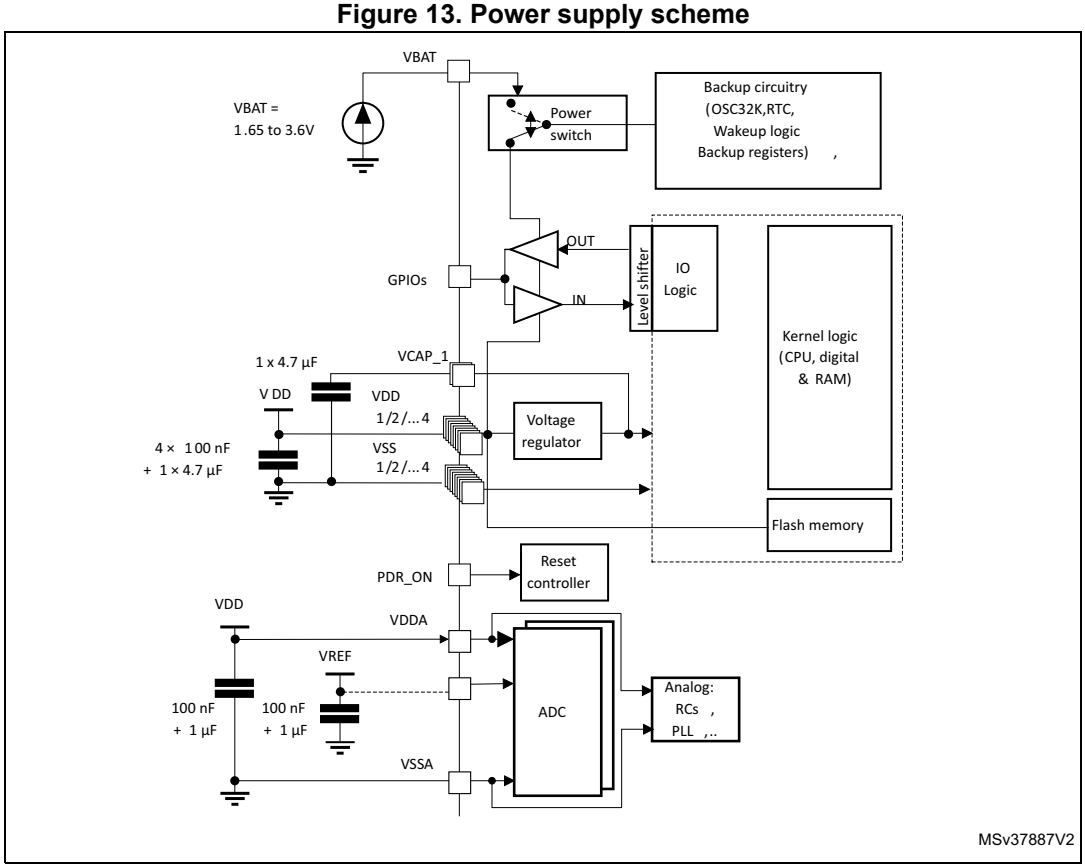
The input voltage measurement on a pin of the device is described in *Figure 12*.

**Figure 12. Input voltage measurement**



### 6.1.6 Power supply scheme

**Figure 13. Power supply scheme**

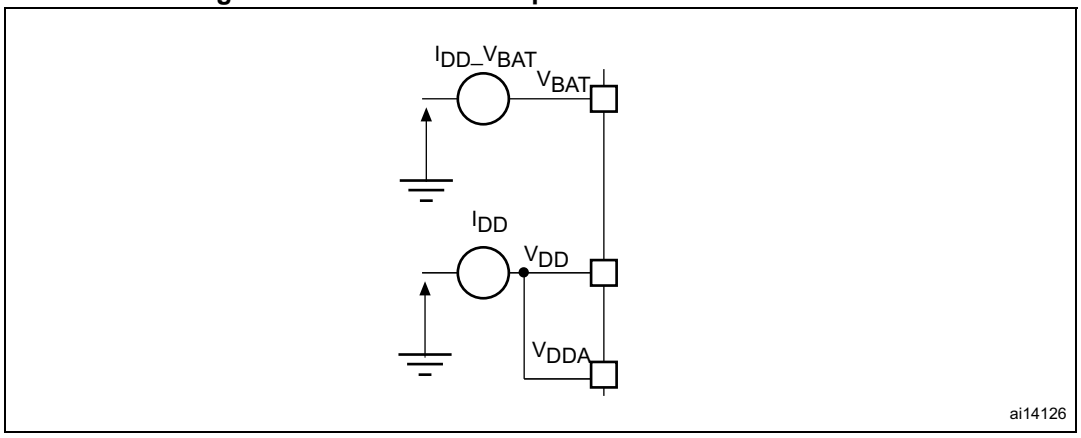



1. To connect PDR_ON pin, refer to *Section 3.15: Power supply supervisor*.

**Caution:** Each power supply pair (for example $V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 12: Voltage characteristics*, *Table 13: Current characteristics*, and *Table 14: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard; extended mission profiles are available on demand.

**Table 12. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD}$ and $V_{BAT}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT and TC pins(2) | $V_{SS}$–0.3 | Min(Min($V_{DD}$, $V_{DDA}$)+ 3.6 V, 5.5 V) | |
| | Input voltage on any other pin | $V_{SS}$–0.3 | 4.0 | |
| | Input voltage for BOOT0 | $V_{SS}$ | 9.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins including $V_{REF-}$ | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)* | | V |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum value must always be respected. Refer to *Table 13* for the maximum allowed injected current values.

**Table 13. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD_x}$ power lines (source)(1) | 160 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS_x}$ ground lines (sink)(1) | -160 | |
| $I_{VDD}$ | Maximum current into each $V_{DD_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS_x}$ ground line (sink)(1) | -100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/O and control pin | -25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | -120 | |
| $I_{INJ(PIN)}$ (3) | Injected current on FT and TC pins (4) | –5/+0 | |
| | Injected current on NRST and B pins (4) | | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 14. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 130 | |
| $T_{LEAD}$ | Maximum lead temperature during soldering (WLCSP36, LQFP48, LQFP64, UFQFPN48, UFBGA64) | see note (1) | |

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 15. General operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01 | 0 | - | 64 | MHz |
| | | Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10 | 0 | - | 84 | |
| | | Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11 | 0 | - | 100 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | - | 50 | MHz |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | - | 100 | MHz |
| $V_{DD}$ | Standard operating voltage | - | 1.7(1) | - | 3.6 | V |
| $V_{DDA}$(2)(3) | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$(4) | 1.7(1) | - | 2.4 | V |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | 2.4 | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.65 | - | 3.6 | V |
| $V_{12}$ | Regulator ON: 1.2 V internal voltage on VCAP_1 pins | VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz | 1.08 | 1.14 | 1.20 | V |
| | | VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz | 1.20 | 1.26 | 1.32 | |
| | | VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz | 1.26 | 1.32 | 1.38 | |
| $V_{12}$ | Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1 pins | Max frequency 64 MHz | 1.10 | 1.14 | 1.20 | V |
| | | Max frequency 84 MHz | 1.20 | 1.26 | 1.32 | |
| | | Max frequency 100 MHz | 1.26 | 1.32 | 1.38 | |
| $V_{IN}$ | Input voltage on RST, FT and TC pins | 2 V ≤ $V_{DD}$ ≤ 3.6 V | –0.3 | - | 5.5 | V |
| | | $V_{DD}$ ≤ 2 V | –0.3 | - | 5.2 | |
| | Input voltage on BOOT0 pin | - | 0 | - | 9 | |

**Table 15. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum allowed package power dissipation at $T_A$ = 85 °C (range 6) or 105 °C (range 7) | LQFP48 | - | - | 364 | mW |
| | | LQFP64 | - | - | 435 | |
| | | UFQFPN48 | - | - | 606 | |
| | | WLCSP36 | - | - | 328 | |
| | | UFBGA64 | - | - | 253 | |
| | Power dissipation at $T_A$ = 125 °C for range 3 | LQFP48 | - | - | 91 | |
| | | LQFP64 | - | - | 108 | |
| | | UFQFPN48 | - | - | 151 | |
| | | WLCSP36 | - | - | 81 | |
| | | UFBGA64 | - | - | 63 | |
| $T_A$ | Ambient temperature for range 6 | Maximum power dissipation | –40 | - | 85 | °C |
| | | Low power dissipation | –40 | - | 105 | |
| | Ambient temperature for range 7 | Maximum power dissipation | –40 | - | 105 | |
| | | Low power dissipation | –40 | - | 125 | |
| | Ambient temperature for range 3 | Maximum power dissipation | -40 | - | 110 | |
| | | Low power dissipation | -40 | - | 130 | |
| $T_J$ | Junction temperature range | Range 6 | –40 | - | 105 | |
| | | Range 7 | –40 | - | 125 | |
| | | Range 3 | –40 | - | 130 | |

1. $V_{DD}/V_{DDA}$ minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. If VREF+ pin is present, it must respect the following condition: VDDA-VREF+ < 1.2 V.
4. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.

**Table 16. Features depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum Flash memory access frequency with wait states (1)(2) | I/O operation | Clock output frequency on I/O pins(3) | Possible Flash memory operations |
|---|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(4) | Conversion time up to 1.2 Msps | 16 MHz(5) | 100 MHz with 6 wait states | – No I/O compensation | up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1.2 Msps | 18 MHz | 100 MHz with 5 wait states | – No I/O compensation | up to 30 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2.4 Msps | 24 MHz | 100 MHz with 4 wait states | – I/O compensation works | up to 50 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V | Conversion time up to 2.4 Msps | 30 MHz | 100 MHz with 3 wait states | – I/O compensation works | – up to 100 MHz when $V_{DD}$ = 3.0 to 3.6 V<br>– up to 50 MHz when $V_{DD}$ = 2.7 to 3.0 V | 32-bit erase and program operations |

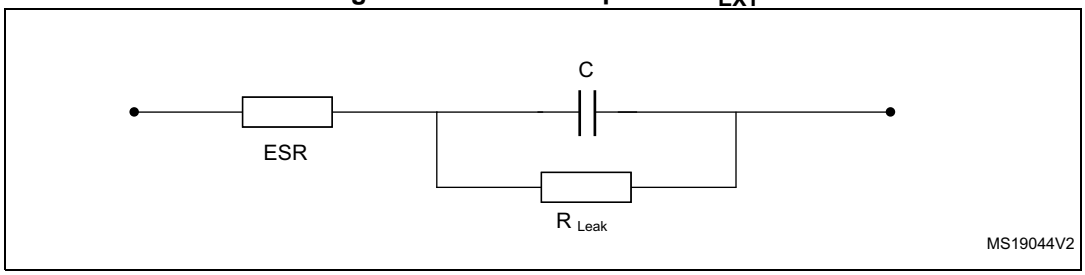
1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to *Table 57: I/O AC characteristics* for frequencies vs. external load.
4. $V_{DD}/V_{DDA}$ minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
5. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

### 6.3.2 VCAP_1 external capacitor

Stabilization for the main regulator is achieved by connecting the external capacitor $C_{EXT}$ to the VCAP_1 pin.

$C_{EXT}$ is specified in *Table 17*.

**Figure 15. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

**Table 17. VCAP_1 operating conditions**

| Symbol | Parameter | Conditions |
|---|---|---|
| CEXT | Capacitance of external capacitor | 4.7 µF |
| ESR | ESR of external capacitor | < 1 Ω |

### 6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for $T_A$.

**Table 18. Operating conditions at power-up / power-down (regulator ON)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | |

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for $T_A$.

**Table 19. Operating conditions at power-up / power-down (regulator OFF)(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | Power-up | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | Power-down | 20 | ∞ | |
| $t_{VCAP}$ | $V_{CAP_1}$ rise time rate | Power-up | 20 | ∞ | |
| | $V_{CAP_1}$ fall time rate | Power-down | 20 | ∞ | |

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when $V_{DD}$ reach below 1.08 V.

### 6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 20* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage @ 3.3V.

**Table 20. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | |
| | | PLS[2:0]=101 (falling edge) | 2.75 | 2.84 | 3.02 | |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | |
| $V_{PVDhyst}$(2) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60(1) | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | |
| $V_{PDRhyst}$(2) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | |
| $V_{BOR2}$ | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | |
| | | Rising edge | 2.53 | 2.59 | 2.63 | |
| $V_{BOR3}$ | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | |
| | | Rising edge | 2.85 | 2.92 | 2.97 | |
| $V_{BORhyst}$(2) | BOR hysteresis | - | - | 100 | - | mV |
| $T_{RSTTEMPO}$(2)(3) | POR reset timing | - | 0.5 | 1.5 | 3.0 | ms |

**Table 20. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{RUSH}$(2) | In-Rush current on voltage regulator power-on (POR or wakeup from Standby) | - | - | 160 | 200 | mA |
| $E_{RUSH}$(2) | In-Rush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD}$ = 1.7 V, $T_A$ = 125 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

1. The product behavior is specified by design down to the minimum $V_{POR/PDR}$ value, not tested in production.
2. Specified by design, not tested in production.
3. The reset timing is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is fetched by the user application code.

## 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both $f_{HCLK}$ frequency and VDD ranges (refer to *Table 16: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and a maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 21. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | $T_A$= 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 17.4 | 18.3 | 19.1 | 19.4 | 20.2 | mA |
| | | | 84 | S2 | 168 | 14.1 | 14.8 | 15.4 | 15.8 | 16.6 | |
| | | | 64 | S3 | 128 | 9.8 | 10.3 | 10.7 | 11.0 | 11.7 | |
| | | | 50 | S3 | 100 | 7.7 | 8.1 | 8.5 | 8.8 | 9.5 | |
| | | | 25 | S3 | 100 | 4.1 | 4.4 | 4.7 | 5.0 | 5.7 | |
| | | | 20 | S3 | 160 | 3.5 | 3.8 | 4.1 | 4.4 | 5.1 | |
| | | HSI, PLL off, all peripherals enabled(3)(4) | 16 | S3 | off | 2.5 | 2.6 | 2.9 | 3.2 | 4.0 | |
| | | | 1 | S3 | off | 0.4 | 0.5 | 0.8 | 1.2 | 2.0 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 11.8 | 12.5 | 12.9 | 13.3 | 14.1 | |
| | | | 84 | S2 | 168 | 9.6 | 10.1 | 10.4 | 10.8 | 11.6 | |
| | | | 64 | S3 | 128 | 6.7 | 7.2 | 7.4 | 7.7 | 8.4 | |
| | | | 50 | S3 | 100 | 5.3 | 5.6 | 5.9 | 6.2 | 6.9 | |
| | | | 25 | S3 | 100 | 2.9 | 3.1 | 3.3 | 3.7 | 4.4 | |
| | | | 20 | S3 | 160 | 2.5 | 2.7 | 2.9 | 3.2 | 3.9 | |
| | | HSI, PLL off, all peripherals disabled(3) | 16 | S3 | off | 1.7 | 1.9 | 2.1 | 2.4 | 3.2 | |
| | | | 1 | S3 | off | 0.3 | 0.4 | 0.7 | 1.1 | 1.9 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | $T_A$= 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 17.7 | 19.1 | 19.3 | 19.7 | 20.5 | mA |
| | | | 84 | S2 | 168 | 14.4 | 15.3 | 15.7 | 16.0 | 16.8 | |
| | | | 64 | S3 | 128 | 10.1 | 10.6 | 11.0 | 11.3 | 12.0 | |
| | | | 50 | S3 | 100 | 8.0 | 8.4 | 8.8 | 9.1 | 9.8 | |
| | | | 25 | S3 | 100 | 4.4 | 4.7 | 4.9 | 5.2 | 5.9 | |
| | | | 20 | S3 | 160 | 3.8 | 4.1 | 4.3 | 4.6 | 5.3 | |
| | | HSI, PLL off, all peripherals enabled(3)(4) | 16 | S3 | off | 2.5 | 2.6 | 2.9 | 3.2 | 4.0 | |
| | | | 1 | S3 | off | 0.4 | 0.5 | 0.8 | 1.2 | 2.0 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 12.1 | 13.1 | 13.1 | 13.5 | 14.3 | |
| | | | 84 | S2 | 168 | 9.8 | 10.6 | 10.7 | 11.0 | 11.8 | |
| | | | 64 | S3 | 128 | 7.0 | 7.4 | 7.6 | 7.9 | 8.6 | |
| | | | 50 | S3 | 100 | 5.6 | 5.9 | 6.1 | 6.4 | 7.2 | |
| | | | 25 | S3 | 100 | 3.1 | 3.3 | 3.5 | 3.9 | 4.8 | |
| | | | 20 | S3 | 160 | 2.8 | 3.0 | 3.2 | 3.5 | 4.4 | |
| | | HSI, PLL off, all peripherals disabled(3) | 16 | S3 | off | 1.7 | 1.8 | 2.1 | 2.4 | 3.3 | |
| | | | 1 | S3 | off | 0.4 | 0.4 | 0.7 | 1.1 | 1.8 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 23. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 15.7 | 16.5 | 16.5 | 16.9 | 17.8 | mA |
| | | | 84 | S2 | 168 | 12.7 | 13.3 | 13.4 | 13.8 | 14.6 | |
| | | | 64 | S3 | 128 | 8.8 | 9.3 | 9.4 | 9.7 | 10.6 | |
| | | | 50 | S3 | 100 | 7.0 | 7.4 | 7.5 | 7.8 | 8.6 | |
| | | | 25 | S3 | 100 | 3.9 | 4.1 | 4.3 | 4.7 | 5.6 | |
| | | | 20 | S3 | 160 | 3.4 | 3.6 | 3.8 | 4.2 | 5.1 | |
| | | HSI, PLL OFF, all peripherals enabled(3)(4) | 16 | S3 | off | 2.4 | 2.5 | 2.8 | 3.2 | 4.1 | |
| | | | 1 | S3 | off | 0.6 | 0.7 | 1.0 | 1.4 | 2.3 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 10.1 | 10.7 | 10.8 | 11.2 | 12.0 | |
| | | | 84 | S2 | 168 | 8.2 | 8.6 | 8.7 | 9.1 | 10.0 | |
| | | | 64 | S3 | 128 | 5.7 | 6.1 | 6.2 | 6.6 | 7.4 | |
| | | | 50 | S3 | 100 | 4.6 | 4.9 | 5.0 | 5.4 | 6.3 | |
| | | | 25 | S3 | 100 | 2.6 | 2.8 | 3.0 | 3.4 | 4.3 | |
| | | | 20 | S3 | 160 | 2.4 | 2.5 | 2.8 | 3.1 | 4.0 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | S3 | off | 1.7 | 1.8 | 2.1 | 2.4 | 3.3 | |
| | | | 1 | S3 | off | 0.6 | 0.6 | 1.0 | 1.4 | 2.2 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 16.3 | 17.3 | 17.1 | 17.5 | 18.4 | mA |
| | | | 84 | S2 | 168 | 13.2 | 14.1 | 14.0 | 14.3 | 15.2 | |
| | | | 64 | S3 | 128 | 9.3 | 10.0 | 9.9 | 10.2 | 11.1 | |
| | | | 50 | S3 | 100 | 7.4 | 8.0 | 8.0 | 8.3 | 9.2 | |
| | | | 25 | S3 | 100 | 4.2 | 4.7 | 4.8 | 5.0 | 5.9 | |
| | | | 20 | S3 | 160 | 3.7 | 4.2 | 4.3 | 4.6 | 5.5 | |
| | | HSI, PLL OFF, all peripherals enabled(3)(4) | 16 | S3 | off | 2.4 | 2.8 | 3.0 | 3.4 | 4.3 | |
| | | | 1 | S3 | off | 0.6 | 1.0 | 1.2 | 1.5 | 2.4 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 10.6 | 11.4 | 11.4 | 11.7 | 12.6 | |
| | | | 84 | S2 | 168 | 8.7 | 9.4 | 9.3 | 9.7 | 10.6 | |
| | | | 64 | S3 | 128 | 6.2 | 6.8 | 6.8 | 7.1 | 7.9 | |
| | | | 50 | S3 | 100 | 5.0 | 5.5 | 5.5 | 5.8 | 6.8 | |
| | | | 25 | S3 | 100 | 2.9 | 3.4 | 3.5 | 3.8 | 4.7 | |
| | | | 20 | S3 | 160 | 2.7 | 3.1 | 3.2 | 3.5 | 4.4 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | S3 | off | 1.7 | 2.1 | 2.3 | 2.6 | 3.5 | |
| | | | 1 | S3 | off | 0.6 | 0.9 | 1.1 | 1.5 | 2.4 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 24.7 | 26.3 | 26.5 | 27.0 | 28.0 | mA |
| | | | 84 | S2 | 168 | 21.6 | 23.0 | 23.2 | 23.7 | 24.7 | |
| | | | 64 | S3 | 128 | 15.9 | 17.0 | 17.1 | 17.6 | 18.6 | |
| | | | 50 | S3 | 100 | 13.1 | 14.2 | 14.3 | 14.7 | 15.7 | |
| | | | 25 | S3 | 100 | 7.5 | 8.2 | 8.3 | 8.7 | 9.7 | |
| | | | 20 | S3 | 160 | 6.5 | 7.1 | 7.2 | 7.5 | 8.5 | |
| | | HSI, PLL OFF, all peripherals enabled(3)(4) | 16 | S3 | off | 4.7 | 5.3 | 5.5 | 5.9 | 6.9 | |
| | | | 1 | S3 | off | 0.8 | 1.2 | 1.6 | 1.9 | 2.9 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 19.1 | 20.5 | 20.7 | 21.3 | 22.3 | |
| | | | 84 | S2 | 168 | 17.1 | 18.3 | 18.6 | 19.1 | 20.1 | |
| | | | 64 | S3 | 128 | 12.8 | 13.8 | 14.0 | 14.5 | 15.5 | |
| | | | 50 | S3 | 100 | 10.7 | 11.7 | 11.8 | 12.2 | 13.2 | |
| | | | 25 | S3 | 100 | 6.3 | 7.0 | 7.1 | 7.4 | 8.3 | |
| | | | 20 | S3 | 160 | 5.4 | 6.0 | 6.2 | 6.5 | 7.4 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | S3 | off | 4.0 | 4.5 | 5.0 | 5.1 | 6.0 | |
| | | | 1 | S3 | off | 0.8 | 1.1 | 1.5 | 1.8 | 2.7 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 24.2 | 26.2 | 25.7 | 26.5 | 27.6 | mA |
| | | | 84 | S2 | 168 | 20.0 | 21.8 | 21.4 | 22.1 | 23.1 | |
| | | | 64 | S3 | 128 | 15.8 | 17.2 | 17.0 | 17.7 | 18.7 | |
| | | | 50 | S3 | 100 | 13.3 | 16.5 | 14.4 | 15.0 | 16.0 | |
| | | | 25 | S3 | 100 | 7.5 | 9.5 | 8.3 | 8.8 | 9.8 | |
| | | | 20 | S3 | 160 | 6.7 | 8.2 | 7.3 | 7.7 | 8.6 | |
| | | HSI, PLL OFF, all peripherals enabled(3)(4) | 16 | S3 | off | 5.1 | 6.4 | 5.7 | 6.2 | 7.1 | |
| | | | 1 | S3 | off | 0.8 | 1.0 | 1.3 | 1.7 | 2.6 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 18.6 | 23.0 | 23.4 | 23.9 | 24.9 | |
| | | | 84 | S2 | 168 | 15.5 | 19.3 | 19.9 | 20.4 | 21.4 | |
| | | | 64 | S3 | 128 | 12.7 | 16.1 | 16.7 | 17.0 | 18.0 | |
| | | | 50 | S3 | 100 | 10.9 | 13.9 | 14.3 | 14.7 | 15.7 | |
| | | | 25 | S3 | 100 | 6.3 | 8.1 | 8.4 | 8.7 | 9.7 | |
| | | | 20 | S3 | 160 | 5.6 | 7.2 | 7.3 | 7.6 | 8.4 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | S3 | off | 4.3 | 5.5 | 5.8 | 6.2 | 7.1 | |
| | | | 1 | S3 | off | 0.8 | 1.0 | 1.3 | 1.6 | 2.5 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, all peripherals enabled(3)(4) | 100 | S1 | 200 | 27.1 | 28.9 | 28.9 | 29.5 | 30.5 | mA |
| | | | 84 | S2 | 168 | 23.2 | 24.8 | 24.9 | 25.5 | 26.5 | |
| | | | 64 | S3 | 128 | 17.0 | 18.3 | 18.4 | 18.8 | 19.8 | |
| | | | 50 | S3 | 100 | 13.6 | 14.7 | 14.7 | 15.2 | 16.2 | |
| | | | 25 | S3 | 100 | 7.5 | 8.2 | 8.3 | 8.7 | 9.7 | |
| | | | 20 | S3 | 160 | 6.5 | 7.1 | 7.2 | 7.5 | 8.5 | |
| | | HSI, PLL OFF, all peripherals enabled(3)(4) | 16 | S3 | off | 4.7 | 5.3 | 5.5 | 5.9 | 6.9 | |
| | | | 1 | S3 | off | 0.8 | 1.2 | 1.4 | 1.8 | 2.8 | |
| | | External clock, all peripherals disabled(3) | 100 | S1 | 200 | 21.5 | 23.0 | 23.2 | 23.8 | 24.8 | |
| | | | 84 | S2 | 168 | 18.7 | 20.0 | 20.3 | 20.8 | 21.8 | |
| | | | 64 | S3 | 128 | 14.0 | 15.1 | 15.2 | 15.7 | 16.7 | |
| | | | 50 | S3 | 100 | 11.2 | 12.2 | 12.3 | 12.7 | 13.7 | |
| | | | 25 | S3 | 100 | 6.3 | 7.0 | 7.1 | 7.4 | 8.4 | |
| | | | 20 | S3 | 160 | 5.4 | 6.0 | 6.2 | 6.5 | 7.5 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | S3 | off | 4.0 | 4.5 | 4.8 | 5.1 | 6.1 | |
| | | | 1 | S3 | off | 0.8 | 1.1 | 1.4 | 1.7 | 2.7 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 28. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode | 100 | S1 | 200 | 8.0 | 8.2 | 9.0 | 9.4 | 10.2 | mA |
| | | | 84 | S2 | 168 | 6.5 | 6.7 | 7.4 | 7.7 | 8.5 | |
| | | | 64 | S3 | 128 | 4.6 | 4.7 | 5.2 | 5.5 | 6.3 | |
| | | | 50 | S3 | 100 | 3.7 | 3.9 | 4.3 | 4.6 | 5.4 | |
| | | | 25 | S3 | 100 | 2.2 | 2.3 | 2.6 | 2.9 | 3.8 | |
| | | | 20 | S3 | 160 | 2.1 | 2.2 | 2.5 | 2.8 | 3.6 | |
| | | All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 1.1 | 1.2 | 1.5 | 1.9 | 2.7 | |
| | | | 1 | S3 | off | 0.3 | 0.4 | 0.7 | 1.1 | 1.9 | |
| | | All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON | 100 | S1 | 200 | 8.4 | 8.7 | 9.5 | 9.9 | 10.7 | |
| | | | 84 | S2 | 168 | 6.9 | 7.1 | 7.7 | 8.1 | 8.9 | |
| | | | 64 | S3 | 128 | 4.9 | 5.1 | 5.5 | 5.9 | 6.7 | |
| | | | 50 | S3 | 100 | 4.0 | 4.2 | 4.6 | 4.9 | 5.7 | |
| | | | 25 | S3 | 100 | 2.5 | 2.6 | 2.9 | 3.2 | 4.0 | |
| | | | 20 | S3 | 160 | 2.4 | 2.5 | 2.7 | 3.1 | 3.9 | |
| | | All peripherals enabled(3), HSI, PLL OFF, Flash memory ON | 16 | S3 | off | 1.4 | 1.4 | 1.8 | 2.2 | 3.0 | |
| | | | 1 | S3 | off | 0.6 | 0.6 | 1.0 | 1.3 | 2.0 | |

**Table 28. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 3.6 V (continued)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz) (1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ (continued) | Supply current in **Sleep mode** (continued) | All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode | 100 | S1 | 200 | 2.2 | 2.3 | 2.6 | 3.0 | 3.8 | mA |
| | | | 84 | S2 | 168 | 1.8 | 1.9 | 2.2 | 2.6 | 3.4 | |
| | | | 64 | S3 | 128 | 1.4 | 1.5 | 1.8 | 2.1 | 2.9 | |
| | | | 50 | S3 | 100 | 1.2 | 1.3 | 1.6 | 1.9 | 2.7 | |
| | | | 25 | S3 | 100 | 0.9 | 1.0 | 1.3 | 1.7 | 2.5 | |
| | | | 20 | S3 | 160 | 1.0 | 1.2 | 1.4 | 1.7 | 2.5 | |
| | | All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 0.3 | 0.4 | 0.7 | 1.1 | 1.9 | |
| | | | 1 | S3 | off | 0.3 | 0.3 | 0.7 | 1.0 | 1.8 | |
| | | All peripherals disabled, External clock, PLL ON, Flash memory ON | 100 | S1 | 200 | 2.6 | 2.7 | 3.0 | 3.4 | 4.2 | |
| | | | 84 | S2 | 168 | 2.2 | 2.3 | 2.6 | 3.0 | 3.8 | |
| | | | 64 | S3 | 128 | 1.8 | 1.9 | 2.1 | 2.5 | 3.3 | |
| | | | 50 | S3 | 100 | 1.5 | 1.6 | 1.9 | 2.2 | 3.1 | |
| | | | 25 | S3 | 100 | 1.2 | 1.4 | 1.6 | 2.0 | 2.8 | |
| | | | 20 | S3 | 160 | 1.3 | 1.4 | 1.7 | 2.0 | 2.8 | |
| | | All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 0.6 | 0.6 | 1.0 | 1.3 | 2.0 | |
| | | | 1 | S3 | off | 0.5 | 0.6 | 0.9 | 1.3 | 2.0 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 29. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz)(1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | All peripherals enabled(3) (4), External clock, PLL ON, Flash memory in Deep power down mode | 100 | S1 | 200 | 7.7 | 7,9 | 8,8 | 9,2 | 10.0 | mA |
| | | | 84 | S2 | 168 | 6.2 | 6,4 | 7,1 | 7,5 | 8.3 | |
| | | | 64 | S3 | 128 | 4.3 | 4,5 | 5,0 | 5,3 | 6.1 | |
| | | | 50 | S3 | 100 | 3.4 | 3,6 | 4,0 | 4,4 | 5.2 | |
| | | | 25 | S3 | 100 | 2.0 | 2,1 | 2,4 | 2,7 | 3.5 | |
| | | | 20 | S3 | 160 | 1.8 | 1,9 | 2,3 | 2,6 | 3.4 | |
| | | All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 1.1 | 1,2 | 1,5 | 1,9 | 2.7 | |
| | | | 1 | S3 | off | 0.3 | 0,4 | 0,7 | 1,0 | 1.8 | |
| | | All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON | 100 | S1 | 200 | 8.1 | 8,4 | 9,3 | 9,7 | 10.5 | |
| | | | 84 | S2 | 168 | 6.6 | 6,8 | 7,5 | 7,9 | 8.7 | |
| | | | 64 | S3 | 128 | 4.7 | 4,8 | 5,4 | 5,7 | 6.5 | |
| | | | 50 | S3 | 100 | 3.8 | 3,9 | 4,4 | 4,7 | 5.5 | |
| | | | 25 | S3 | 100 | 2.3 | 2,4 | 2,7 | 3,1 | 3.9 | |
| | | | 20 | S3 | 160 | 2.1 | 2,2 | 2,6 | 2,9 | 3.7 | |
| | | All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory ON | 16 | S3 | off | 1.4 | 1,5 | 1,8 | 2,2 | 3.0 | |
| | | | 1 | S3 | off | 0.5 | 0,6 | 1,0 | 1,3 | 2.0 | |

**Table 29. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 1.7 V (continued)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Voltage scale | PLL VCO (MHz)(1) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$= 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD}$ (continued) | Supply current in **Sleep mode** (continued) | All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode | 100 | S1 | 200 | 1.9 | 2,0 | 2,4 | 2,7 | 3.5 | mA |
| | | | 84 | S2 | 168 | 1.6 | 1,7 | 2,0 | 2,4 | 3.2 | |
| | | | 64 | S3 | 128 | 1.1 | 1,2 | 1,5 | 1,9 | 2.7 | |
| | | | 50 | S3 | 100 | 0.9 | 1,0 | 1,3 | 1,7 | 2.5 | |
| | | | 25 | S3 | 100 | 0.7 | 0,8 | 1,1 | 1,4 | 2.2 | |
| | | | 20 | S3 | 160 | 0.8 | 0,8 | 1,2 | 1,5 | 2.3 | |
| | | All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 0.3 | 0,4 | 0,7 | 1,0 | 1.8 | |
| | | | 1 | S3 | off | 0.2 | 0,3 | 0,6 | 1,0 | 1.8 | |
| | | All peripherals disabled, External clock, PLL ON, Flash memory ON | 100 | S1 | 200 | 2.3 | 2,4 | 2,9 | 3,3 | 4.0 | |
| | | | 84 | S2 | 168 | 2.0 | 2,1 | 2,4 | 2,8 | 3.6 | |
| | | | 64 | S3 | 128 | 1.5 | 1,6 | 1,9 | 2,3 | 3.1 | |
| | | | 50 | S3 | 100 | 1.3 | 1,4 | 1,7 | 2,0 | 2.8 | |
| | | | 25 | S3 | 100 | 1.0 | 1,1 | 1,4 | 1,7 | 2.5 | |
| | | | 20 | S3 | 160 | 1.0 | 1,2 | 1,5 | 1,8 | 2.6 | |
| | | All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode | 16 | S3 | off | 0.6 | 0,6 | 1,0 | 1,4 | 2.1 | |
| | | | 1 | S3 | off | 0.5 | 0,6 | 0,9 | 1,3 | 2.0 | |

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Evaluated by characterization, not tested in production.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

**Table 30. Typical and maximum current consumptions in Stop mode - $V_{DD}$ = 1.7 V**

| Symbol | Conditions | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C(1) | $T_A$ = 85 °C | $T_A$ = 105 °C(1) | $T_A$ = 125 °C(1) | |
| $I_{DD_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 105.6 | 117.1 | 385.1 | 665.7 | 1270.0 | µA |
| | | Low power regulator usage | 39.5 | 48.7 | 287.5 | 548.4 | 1070.0 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 77.8 | 87.5 | 351.3 | 630.1 | 1222.0 | |
| | | Low power regulator usage | 11.0 | 20.0 | 254.2 | 512.0 | 1006.0 | |
| | | Low power low voltage regulator usage | 6.1 | 13.6 | 217.0 | 442.5 | 941.0 | |

1. Evaluated by characterization, not tested in production.

**Table 31. Typical and maximum current consumption in Stop mode - $V_{DD}$=3.6 V**

| Symbol | Conditions | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C(1) | $T_A$ = 85 °C | $T_A$ = 105 °C(1) | $T_A$ = 125 °C(1) | |
| $I_{DD_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 108.6 | 126 | 392.8 | 675.4 | 1280.0 | µA |
| | | Low power regulator usage | 41.03 | 50.31 | 290.9 | 554.2 | 1077.0 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 80.32 | 94.0 | 357.0 | 639.5 | 1232.0 | |
| | | Low power regulator usage | 12.41 | 21.5 | 258.1 | 518.1 | 1010.0 | |
| | | Low power low voltage regulator usage | 7.53 | 15.2 | 221.6 | 449.2 | 947.0 | |

1. Evaluated by characterization, not tested in production.

**Table 32. Typical and maximum current consumption in Standby mode - $V_{DD}$= 1.7 V**

| Symbol | Parameter | Conditions | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C(1) | $T_A$ = 85 °C | $T_A$ = 105 °C(1) | $T_A$ = 125 °C(1) | |
| $I_{DD_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE) and RTC ON | 2.1 | 2.9 | 6.5 | 18.2 | 60.0 | µA |
| | | RTC and LSE OFF | 1.2 | 1.9 | 5.5 | 17.1 | 59.0 | |

1. Evaluated by characterization, not tested in production.

**Table 33. Typical and maximum current consumption in Standby mode - $V_{DD}$= 3.6 V**

| Symbol | Parameter | Conditions | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C(1) | $T_A$ = 85 °C | $T_A$ = 105 °C(1) | $T_A$ = 125 °C(1) | |
| $I_{DD_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE) and RTC ON | 3.4 | 4.3 | 8.9 | 22.8 | 65.0 | µA |
| | | RTC and LSE OFF | 2.5 | 3.3 | 7.8 | 21.6 | 64.0 | |

1. Evaluated by characterization, not tested in production.

**Table 34. Typical and maximum current consumptions in $V_{BAT}$ mode (LSE and RTC ON, LSE low- drive mode)**

| Symbol | Parameter | Conditions(1) | Typ | | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| | | | $V_{BAT}$ = 1.7 V | $V_{BAT}$= 2.4 V | $V_{BAT}$ = 3.3 V | $V_{BAT}$ = 3.6 V | | | |
| $I_{DD_VBAT}$ | Backup domain supply current | Low-speed oscillator (LSE in low-drive mode) and RTC ON | 0.7 | 0.8 | 1.1 | 2.8 | 4.2 | 5.6 | µA |
| | | Low-speed oscillator (LSE in high-drive mode) and RTC ON | 1.4 | 1.6 | 1.9 | 4.2 | 7.0 | 8.6 | |
| | | RTC and LSE OFF | 0.1 | 0.1 | 0.1 | 2.0 | 4.0 | 5.8 | |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a $C_L$ of 6 pF for typical values.
2. Evaluated by characterization, not tested in production.

**Figure 16. Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSE oscillator in "low power" mode selection**

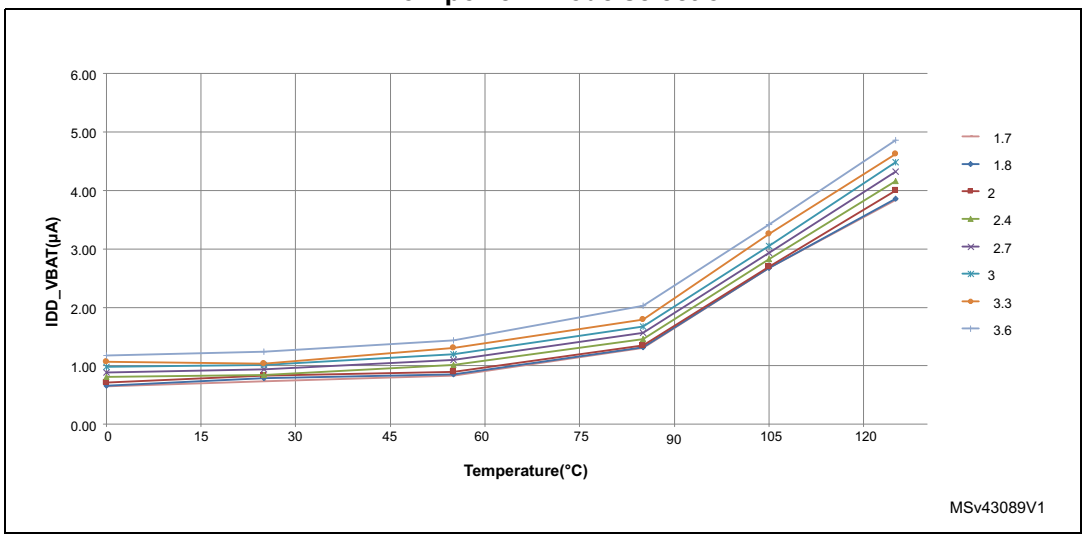
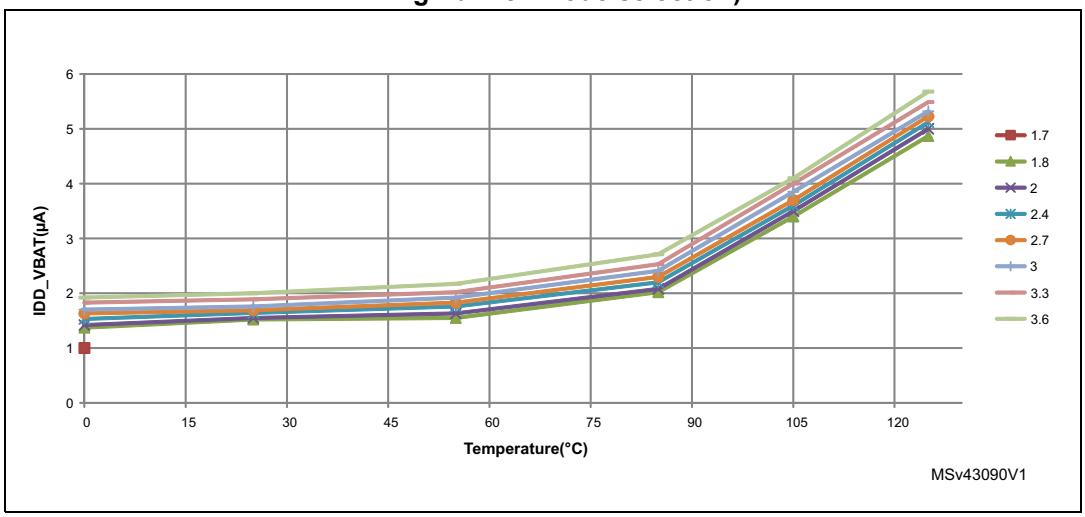


**Figure 17. Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSE oscillator in "high-drive" mode selection)**




## I/O system current consumption

### The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull resistors generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 55: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O

pin circuitry and to charge/discharge the internal and external capacitive load connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 35. Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| IDDIO | I/O switching current | $V_{DD}$ = 3.3 V<br>C = $C_{INT}$ | 2 MHz | 0.05 | mA |
| | | | 8 MHz | 0.15 | |
| | | | 25 MHz | 0.45 | |
| | | | 50 MHz | 0.85 | |
| | | | 60 MHz | 1.00 | |
| | | | 84 MHz | 1.40 | |
| | | | 90 MHz | 1.67 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 0 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.10 | |
| | | | 8 MHz | 0.35 | |
| | | | 25 MHz | 1.05 | |
| | | | 50 MHz | 2.20 | |
| | | | 60 MHz | 2.40 | |
| | | | 84 MHz | 3.55 | |
| | | | 90 MHz | 4.23 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ =10 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.20 | |
| | | | 8 MHz | 0.65 | |
| | | | 25 MHz | 1.85 | |
| | | | 50 MHz | 2.45 | |
| | | | 60 MHz | 4.70 | |
| | | | 84 MHz | 8.80 | |
| | | | 90 MHz | 10.47 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.25 | |
| | | | 8 MHz | 1.00 | |
| | | | 25 MHz | 3.45 | |
| | | | 50 MHz | 7.15 | |
| | | | 60 MHz | 11.55 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.32 | |
| | | | 8 MHz | 1.27 | |
| | | | 25 MHz | 3.88 | |
| | | | 50 MHz | 12.34 | |

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 36. Peripheral current consumption**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Voltage scale1 | Voltage scale2 | Voltage scale3 | |
| **AHB**1 (up to 100 MHz) | GPIOA | 1.68 | 1.62 | 1.42 | µA/MHz |
| | GPIOB | 1.67 | 1.60 | 1.41 | |
| | GPIOC | 1.63 | 1.56 | 1.39 | |
| | GPIOH | 0.61 | 0.61 | 0.52 | |
| | CRC | 0.31 | 0.32 | 0.25 | |
| | DMA1(1) | 1.67N + 3.12 | 1.60N + 2.96 | 1.43N + 2.64 | |
| | DMA2(1) | 1.59N + 2.83 | 1.52N + 2.65 | 1.36N + 2.41 | |
| | RNG | 0.90 | 0.88 | 0.75 | |
| APB1 (up to 50 MHz) | APB1 to AHB | 0,78 | 0,74 | 0,63 | µA/MHz |
| | TIM5 | 13,38 | 12,76 | 11,41 | |
| | TIM6 | 2,14 | 1,98 | 1,75 | |
| | LPTIM | 8,22 | 7,88 | 7,06 | |
| | WWDG | 0,64 | 0,64 | 0,56 | |
| | SPI2/I2S2 | 2,42 | 2,33 | 2,06 | |
| | USART2 | 3,38 | 3,29 | 2,91 | |
| | I2C1 | 3,46 | 3,33 | 2,97 | |
| | I2C2 | 3,50 | 3,31 | 2,97 | |
| | I2C4 | 4,82 | 4,64 | 4,09 | |
| | PWR | 0,66 | 0,64 | 0,62 | |
| | DAC | 0,84 | 0,81 | 0,78 | |

**Table 36. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Voltage scale1 | Voltage scale2 | Voltage scale3 | |
| APB2 (up to 100 MHz) | APB2 to AHB | 0,22 | 0,19 | 0,17 | µA/MHz |
| | TIM1 | 6,62 | 6,36 | 5,66 | |
| | USART1 | 3,19 | 3,10 | 2,77 | |
| | USART6 | 3,10 | 2,99 | 2,66 | |
| | ADC1 | 3,35 | 3,25 | 2,88 | |
| | SPI1/I2S1 | 1,82 | 1,77 | 1,58 | |
| | SYSCFG | 0,83 | 0,81 | 0,72 | |
| | EXTI | 0,92 | 0,88 | 0,80 | |
| | TIM9 | 2,90 | 2,81 | 2,48 | |
| | TIM11 | 2,13 | 2,06 | 1,81 | |
| | SPI5/I2S5 | 1,88 | 1,83 | 1,59 | |
| Bus matrix | | 1.91 | 1.82 | 1.64 | |

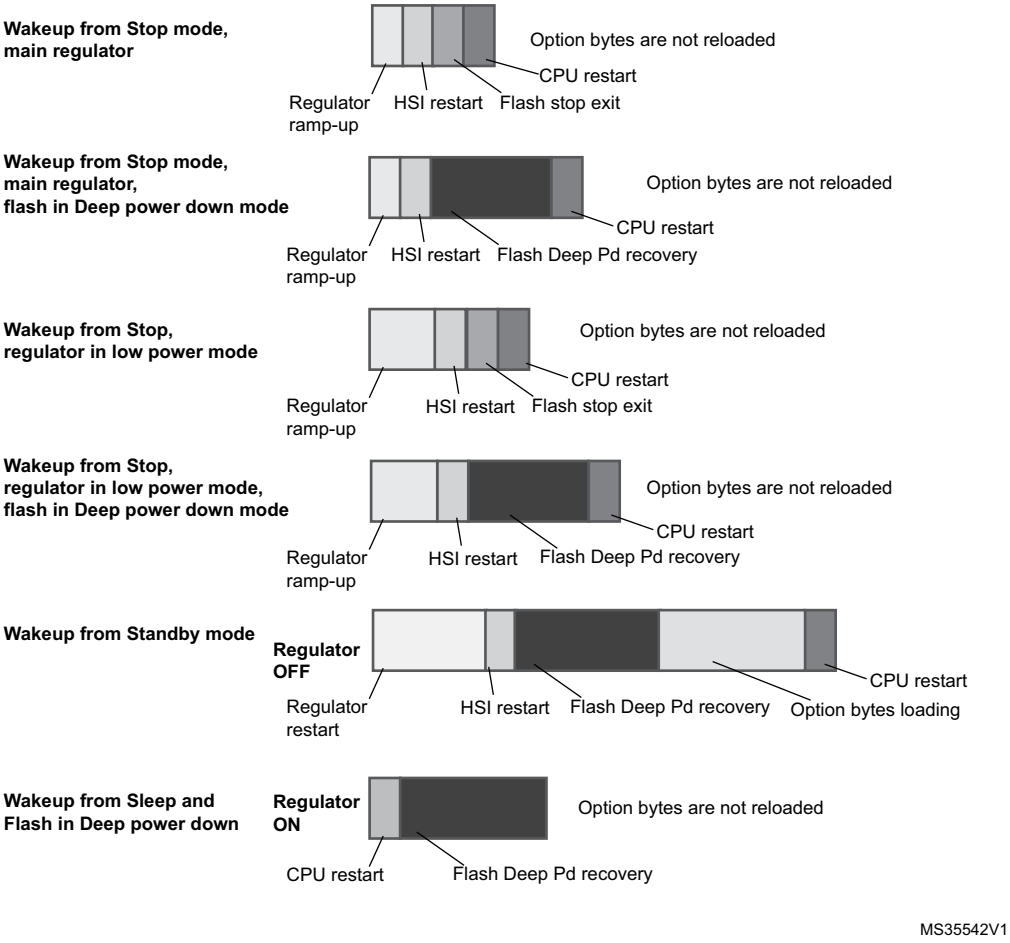
1. Valid if all the DMA streams are activated (please refer to the reference manual RM0401).

### 6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

**Figure 18. Low-power mode wakeup**




All timings are derived from tests performed under ambient temperature and $V_{DD}$=3.3 V.

**Table 37. Low-power mode wakeup timings(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{WUSLEEP}$(2) | Wakeup from Sleep mode | - | - | 4 | 6 | CPU clock cycles |
| $t_{WUSLEEPFDSM}$(2) | | Flash memory in Deep power down mode | - | - | 40,0 | µs |
| $t_{WUSTOP}$(2) | Wakeup from Stop mode, code execution from Flash memory | Main regulator | - | 12.9 | 15.0 | |
| | | Main regulator, Flash memory in Deep power down mode | - | 104.9 | 115.0 | |
| | | Regulator in low-power mode(3) | - | 20.8 | 25.0 | |
| | | Regulator in low-power mode, Flash memory in Deep power down mode | - | 112.9 | 120.0 | |
| | Wakeup from Stop mode, code execution from RAM | Main regulator, Flash memory in Stop or Deep power down mode | - | 4.9 | 7.0 | |
| | | Regulator in low-power mode, Flash memory in Stop or Deep power down mode(3) | - | 12.8 | 20.0 | |
| $t_{WUSTDBY}$(2)(4) | Wakeup from Standby mode | - | - | 316.8 | 350.0 | |
| $t_{WUFLASH}$ | Wakeup of Flash memory | From Flash_Stop mode | - | - | 10.0 | |
| | Wakeup of Flash memory | From Flash Deep power down mode | - | - | 40.0 | |

1. Evaluated by characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. The specification is valid for wakeup from regulator in low power mode or in low power low voltage mode, since the timing difference is negligible.
4. $t_{WUSTDBY}$ maximum value is given at - 40 °C.

## 6.3.8 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 55*. However, the recommended clock input waveform is shown in *Figure 19*.

The characteristics given in *Table 38* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 15*.

**Table 38. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | External user clock source frequency(1) | - | 1 | - | 50 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 10 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Specified by design, not tested in production.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 55*. However, the recommended clock input waveform is shown in *Figure 20*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 15*.

**Table 39. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE_ext}$ | User External clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{f(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Specified by design, not tested in production.

**Figure 19. High-speed external clock source AC timing diagram**

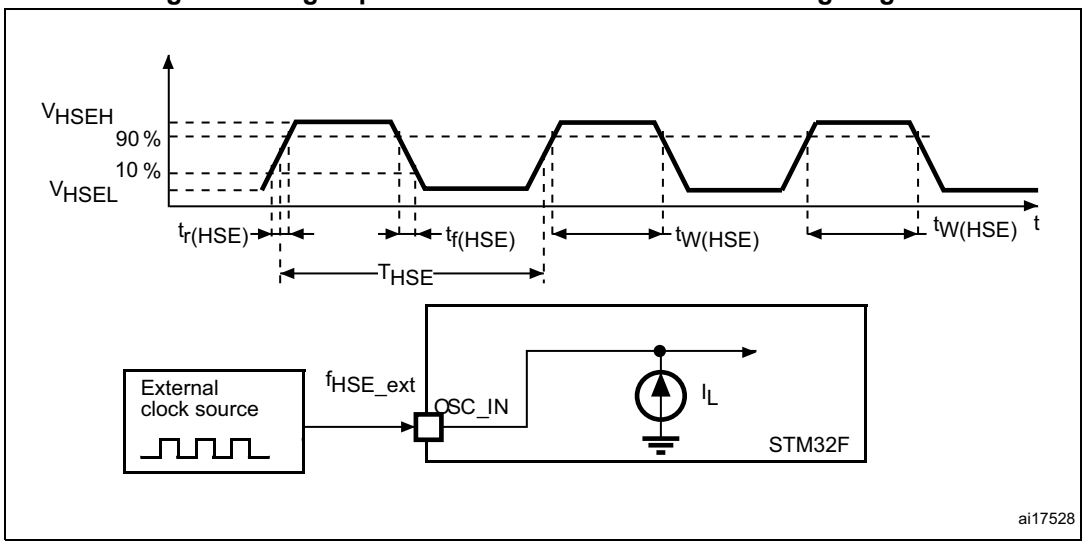
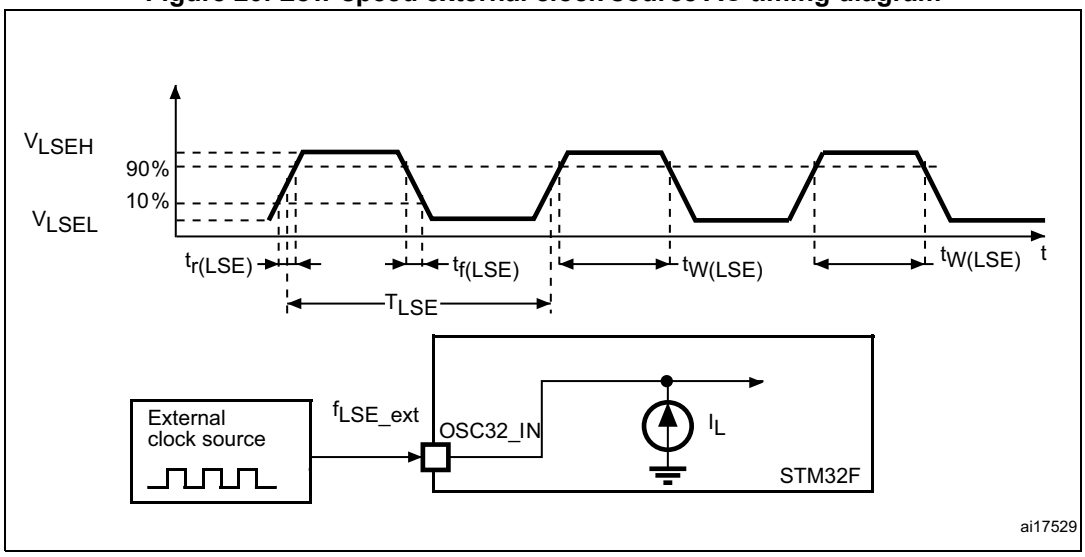



**Figure 20. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE 4-26 MHz oscillator characteristics(1)**

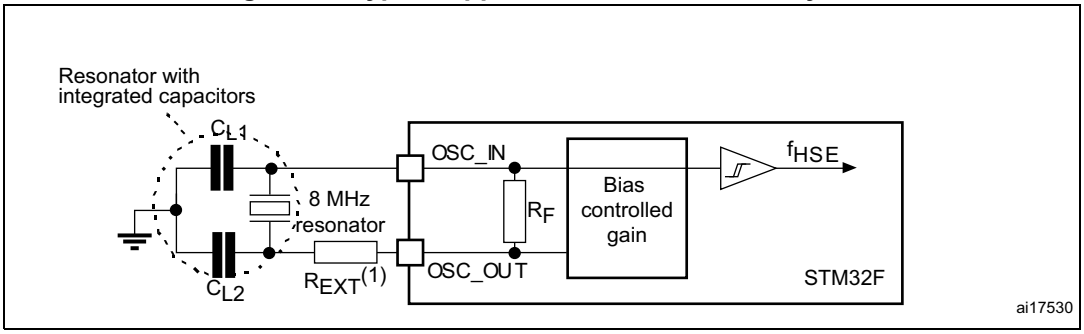
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC_IN}$ | Oscillator frequency | - | 4 | - | 26 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=5 pF @25 MHz | - | 450 | - | µA |
| | | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=10 pF @25 MHz | - | 530 | - | |
| $G_{m_crit_max}$ | Maximum critical crystal $g_m$ | Startup | - | - | 1 | mA/V |
| $t_{SU(HSE)}$(2) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Specified by design, not tested in production.
2. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 21. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

**Table 41. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

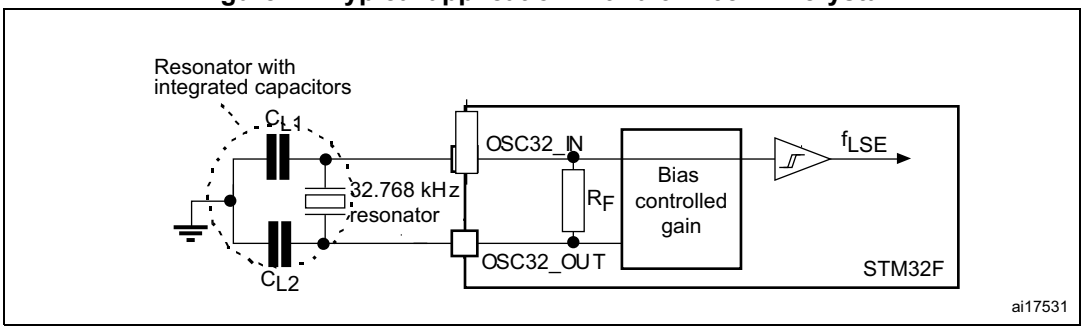
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 18.4 | - | MΩ |
| $I_{DD}$ | LSE current consumption | Low-power mode (default) | - | - | 1 | µA |
| | | High-drive mode | - | - | 3 | |
| $G_m$_crit_max | Maximum critical crystal $g_m$ | Startup, low-power mode | - | - | 0.56 | µA/V |
| | | Startup, high-drive mode | - | - | 1.50 | |
| $t_{SU(LSE)}$ (2) | startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Specified by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. Evaluated by characterization, and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

*For information about the LSE high-power mode, refer to the reference manual RM0401.*

**Figure 22. Typical application with a 32.768 kHz crystal**



## 6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*.

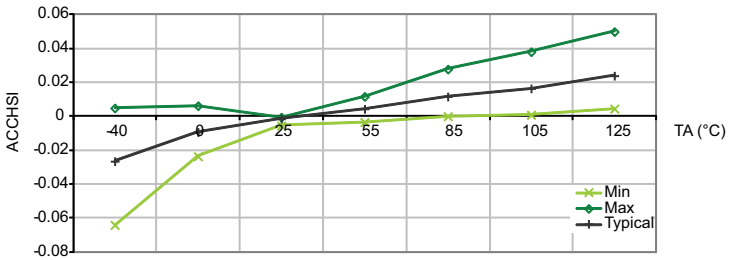
### High-speed internal (HSI) RC oscillator

**Table 42. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | | - | 16 | - | MHz |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register(2) | | - | - | 1 | % |
| | | Factory-calibrated | $T_A$ = –40 to 125 °C(3) | –8 | - | 5.5 | % |
| | | | $T_A$ = –10 to 85 °C(3) | –4 | - | 4 | % |
| | | | $T_A$ = 25 °C(4) | –1 | - | 1 | % |
| $t_{su(HSI)}$(2) | HSI oscillator startup time | - | | - | 2.2 | 4 | µs |
| $I_{DD(HSI)}$(2) | HSI oscillator power consumption | - | | - | 60 | 80 | µA |

1. $V_{DD}$ = 3.3 V, PLL OFF, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Specified by design, not tested in production.
3. Evaluated by characterization, not tested in production.
4. Factory calibrated non-soldered parts.

**Figure 23. $ACC_{HSI}$ versus temperature**




MS30492V2

1. Evaluated by characterization, not tested in production.

### Low-speed internal (LSI) RC oscillator

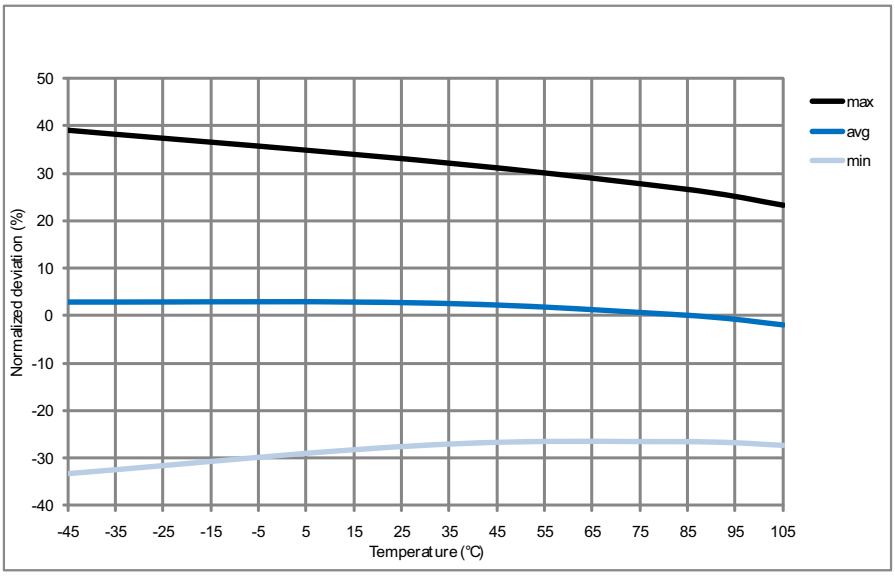
**Table 43. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | 15 | 40 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Evaluated by characterization, not tested in production.

3. Specified by design, not tested in production.

**Figure 24. $ACC_{LSI}$ versus temperature**




## 6.3.10 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*.

**Table 44. Main PLL characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL_IN}$ | PLL input clock(1) | - | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLL_OUT}$ | PLL multiplier output clock | - | | 24 | - | 100 | MHz |
| $f_{PLL48_OUT}$ | 48 MHz PLL multiplier output clock | - | | - | 48 | 75 | MHz |
| $f_{VCO_OUT}$ | PLL VCO output | - | | 100 | - | 432 | MHz |
| $t_{LOCK}$ | PLL lock time | VCO freq = 100 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Cycle-to-cycle jitter | System clock 100 MHz | RMS | - | 25 | - | ps |
| | | | peak to peak | - | ±150 | - | |
| | Period Jitter | | RMS | - | 15 | - | |
| | | | peak to peak | - | ±200 | - | |

**Table 44. Main PLL characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(PLL)}$(4) | PLL power consumption on VDD | VCO freq = 100 MHz<br>VCO freq = 432 MHz | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLL)}$(4) | PLL power consumption on VDDA | VCO freq = 100 MHz<br>VCO freq = 432 MHz | 0.30<br>0.55 | - | 0.40<br>0.85 | |

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Specified by design, not tested in production.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Evaluated by characterization, not tested in production.

### 6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 51: EMI characteristics for fHSE = 8 MHz and fHCLK = 64 MHz*). It is available only on the main PLL.

**Table 45. SSCG parameter constraints**

| Symbol | Parameter | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $f_{Mod}$ | Modulation frequency | - | - | 10 | kHz |
| md | Peak modulation depth | 0.25 | - | 2 | % |
| MODEPER * INCSTEP | (Modulation period) * (Increment Step) | - | - | $2^{15}$-1 | - |

1. Specified by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL_IN} / (4 \times f_{Mod})]$$

$f_{PLL_IN}$ and $f_{Mod}$ must be expressed in Hz.

As an example:

If $f_{PLL_IN}$ = 1 MHz, and $f_{MOD}$ = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

$f_{VCO_OUT}$ must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[((2^{15}-1)\times 2\times 240)/(100\times 5\times 250)] = 126\text{md(quantitazed)}\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER}\times \text{INCSTEP}\times 100\times 5)/((2^{15}-1)\times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250\times 126\times 100\times 5)/((2^{15}-1)\times 240) = 2.002\%\text{(peak)}$$

*Figure 25* and *Figure 26* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{PLL_OUT}$ nominal.

$T_{mode}$ is the modulation period.

md is the modulation depth.

**Figure 25. PLL output clock waveforms in center spread mode**

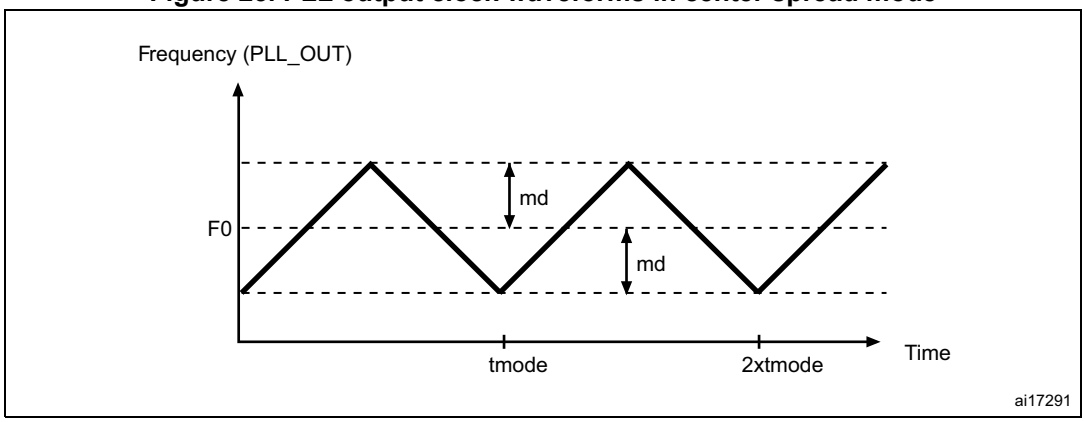
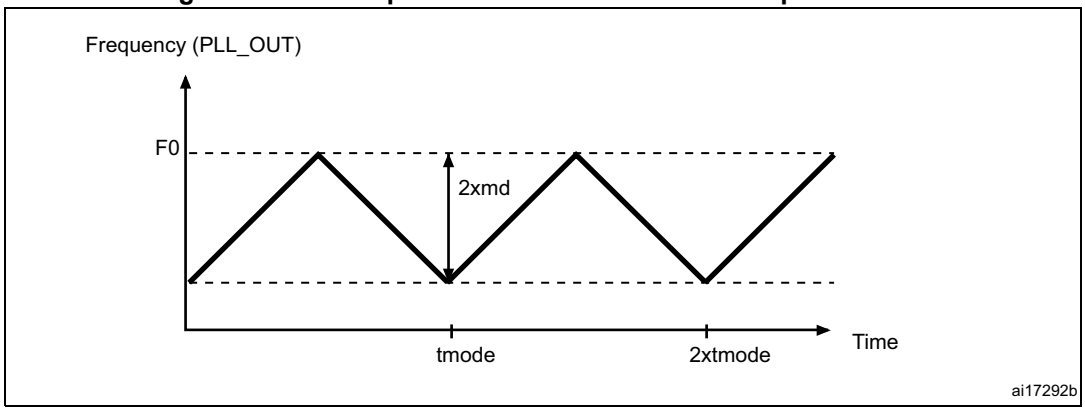



**Figure 26. PLL output clock waveforms in down spread mode**



## 6.3.12 Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 46. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode, $V_{DD}$ = 1.7 V | - | 5 | - | mA |
| | | Write / Erase 16-bit mode, $V_{DD}$ = 2.1 V | - | 8 | - | |
| | | Write / Erase 32-bit mode, $V_{DD}$ = 3.3 V | - | 12 | - | |

**Table 47. Flash memory programming**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word programming time | Program/erase parallelism (PSIZE) = x 8/16/32 | - | 16 | 100(2) | µs |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 400 | 800 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 300 | 600 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 250 | 500 | |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1200 | 2400 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 700 | 1400 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 550 | 1100 | |
| $t_{ME}$ | Mass erase time | Program/erase parallelism (PSIZE) = x 8 | - | 2 | 4 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 1.4 | 2.8 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 1 | 2 | |
| $V_{prog}$ | Programming voltage | 32-bit program operation | 2.7 | - | 3.6 | V |
| | | 16-bit program operation | 2.1 | - | 3.6 | V |
| | | 8-bit program operation | 1.7 | - | 3.6 | V |

1. Evaluated by characterization, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

**Table 48. Flash memory programming with $V_{PP}$ voltage**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Double word programming | $T_A$ = 0 to +40 °C<br>$V_{DD}$ = 3.3 V<br>$V_{PP}$ = 8.5 V | - | 16 | 100(2) | µs |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | | - | 230 | - | ms |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | | - | 490 | - | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | | - | 875 | - | |
| $t_{ME}$ | Mass erase time | | - | 3.50 | - | s |
| $V_{prog}$ | Programming voltage | - | 2.7 | - | 3.6 | V |
| $V_{PP}$ | $V_{PP}$ voltage range | - | 7 | - | 9 | V |
| $I_{PP}$ | Minimum current sunk on the $V_{PP}$ pin | - | 10 | - | - | mA |
| $t_{VPP}$(3) | Cumulative time during which $V_{PP}$ is applied | - | - | - | 1 | hour |

1. Specified by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. $V_{PP}$ should only be connected during programming/erasing.

**Table 49. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_A$ = - 40 to +85 °C (6 suffix versions)<br>$T_A$ = - 40 to +105 °C (7 suffix versions)<br>$T_A$ = - 40 to +125 °C (3 suffix versions) | 10 | Kcycle |
| tRET | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 1 kcycle(2) at $T_A$ = 125 °C | 3 | |
| | | 10 kcycle(2) at $T_A$ = 55 °C | 20 | |

1. Evaluated by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

## 6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 50. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP64, $T_A$ = +25 °C, $f_{HCLK}$ = 100 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP64, $T_A$ = +25 °C, $f_{HCLK}$ = 100 MHz, conforms to IEC 61000-4-4 | 4A |

In noisy environments, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are PA14 and PA15.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 51. EMI characteristics for $f_{HSE}$ = 8 MHz and $f_{HCLK}$ = 64 MHz**

| Symbol | Parameter | Conditions | Monitored frequency band | Value | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak(1) | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP64 package compliant with IEC 61967-2 | 0.1 MHz to 30 MHz | 7 | dBµV |
| | | | 30 MHz to 130 MHz | -1 | |
| | | | 130 MHz to 1 GHz | 8 | |
| | | | 1 GHz to 2 GHz | 7 | |
| | Level(2) | | 0.1 MHz to 2 GHz | 2.5 | - |

1. Refer to AN1709 “EMI radiated test” chapter.
2. Refer to AN1709 “EMI level classification” chapter.

## 6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 52. ESD absolute maximum ratings(1)**

| Symbol | Ratings | Conditions | | Class | Maximum value(2) | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to ANSI/JEDEC JS-001 | | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD STM5.3.1 | UFQFPN48 | 4 | 500 | |
| | | | WLCSP36 | 3 | 250 | |
| | | | LQFP48 | 4 | 500 | |
| | | | LQPF64 | 4 | 500 | |
| | | | UFBGA64 | TBD | TBD | |

1. TBD stands for “to be defined”.
2. Evaluated by characterization, not tested in production.

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 53. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +125 °C conforming to JESD78A | II level A |

## 6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 54*.

**Table 54. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 pin | - 0 | NA | mA |
| | Injected current on NRST pin | - 0 | NA | |
| | Injected current on PB3, PB4, PB5, PB6, PB7, PB8, PB9, PC13, PC14, PC15, PH1, PDR_ON, PC0, PC1, PC2, PC3 | - 0 | NA | |
| | Injected current on any other FT pin | - 5 | NA | |
| | Injected current on any other pins | - 5 | + 5 | |

1. NA = not applicable.

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

## 6.3.16 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under the conditions summarized in *Table 15*. All I/Os are CMOS and TTL compliant.

*Note: For information on GPIO configuration, refer to the application note AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption", available from www.st.com.*

**Table 55. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | FT, TC and NRST I/O input low level voltage | 1.7 V≤$V_{DD}$≤3.6 V | - | - | 0.3$V_{DD}$ | V |
| | BOOT0 I/O input low level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, - 40 °C≤$T_A$ ≤ 125 °C | - | - | 0.1$V_{DD}$+0.1(1) | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤ 125 °C | - | - | | |
| $V_{IH}$ | FT, TC and NRST I/O input high level voltage(4) | 1.7 V≤$V_{DD}$≤3.6 V | 0.7$V_{DD}$ | - | - | V |
| | BOOT0 I/O input high level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, -40 °C≤$T_A$ ≤ 125 °C | 0.17$V_{DD}$+ 0.7 | - | - | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤ 125 °C | | | | |
| $V_{HYS}$ | FT, TC and NRST I/O input hysteresis | 1.7 V≤$V_{DD}$≤3.6 V | - | 10% $V_{DD}$(2) | - | V |
| | BOOT0 I/O input hysteresis | 1.75 V≤$V_{DD}$ ≤3.6 V, - 40 °C≤$T_A$ ≤ 125 °C | - | 100 | - | mV |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤ 125 °C | | | | |
| $I_{lkg}$ | I/O input leakage current(3) | $V_{SS}$ ≤$V_{IN}$ ≤$V_{DD}$ | - | - | ±1 | µA |
| | I/O FT/TC input leakage current (4) | $V_{IN}$ = 5 V | - | - | 3 | |

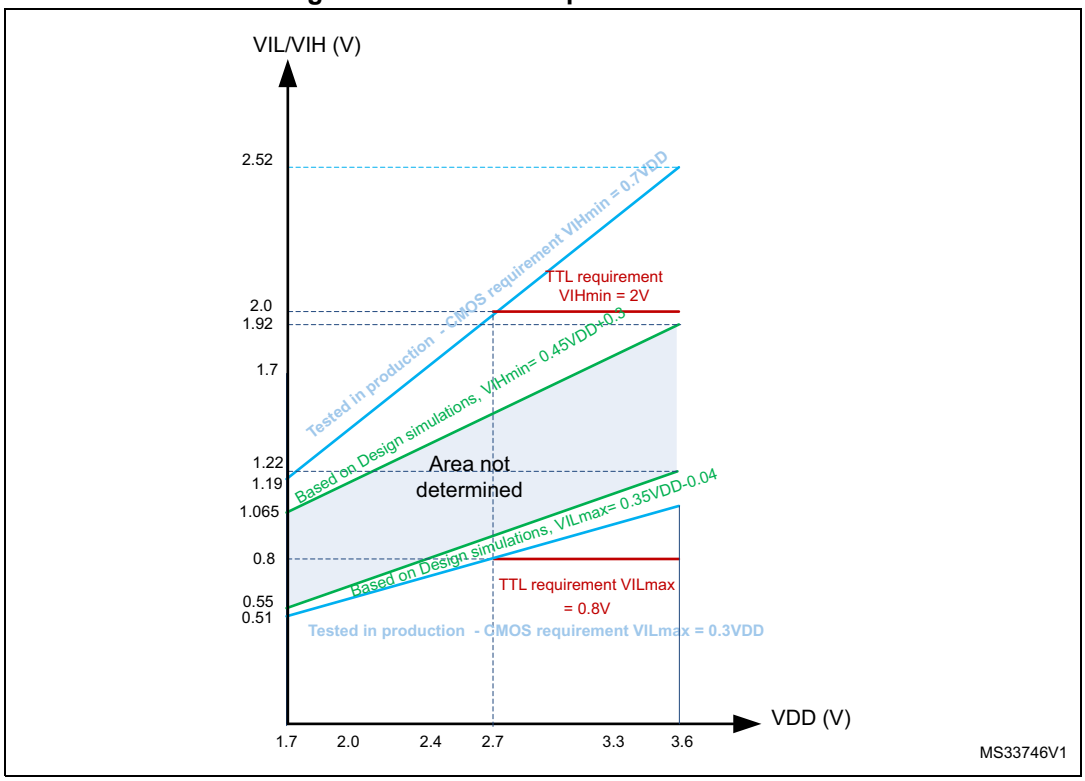
**Table 55. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(5) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(6) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $C_{IO}$(7) | I/O pin capacitance | | - | - | 5 | - | pF |

1. Specified by design, not tested in production.
2. With a minimum of 200 mV.
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 54: I/O current injection susceptibility*
4. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 54: I/O current injection susceptibility*
5. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
6. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
7. Hysteresis voltage between Schmitt trigger switching levels. Evaluated by characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 27*.

**Figure 27. FT/TC I/O input characteristics**




### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 13*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 13*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*. All I/Os are CMOS and TTL compliant.

**Table 56. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2) $I_{IO}$ = +8 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4 | - | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2) $I_{IO}$ =+8 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 1.3(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–1.3(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +6 mA 1.8 V ≤$V_{DD}$ ≤3.6 V | - | 0.4(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA 1.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4(5) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4(5) | - | |
| $V_{OLFM}$(1) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$ = +20 mA 2.7 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | V |
| | | $I_{IO}$ = +10 mA 1.8 V ≤$V_{DD}$ ≤3.6 V | - | 0.4 | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 13*. and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 13* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Evaluated by characterization, not tested in production.
5. Specified by design, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 28* and *Table 57*, respectively.

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*.

**Table 57. I/O AC characteristics(1)(2)**

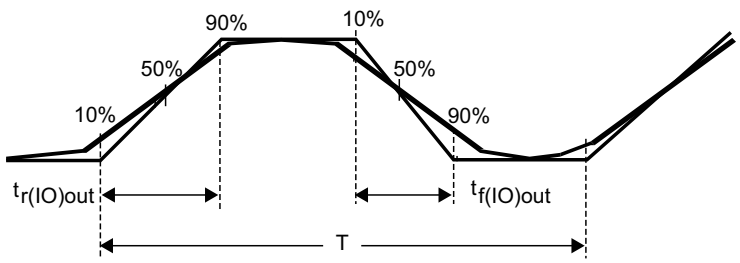
| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.70 V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$≥ 1.7 V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 4 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.7 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.70 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 12.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ ≥2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50(4) | MHz |
| | | | $C_L$ = 40 pF, $V_{DD}$ ≥ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100(4) | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD}$≥ 2.70 V | - | - | 6 | ns |
| | | | $C_L$ = 40 pF, $V_{DD}$≥ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 6 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100(4) | MHz |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 4 | |

**Table 57. I/O AC characteristics(1)(2) (continued)**

| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| FM+ | Fmax | Maximum frequency | $C_L$ = 50 pF, 1.6 ≤ $V_{DD}$ ≥ 3.6 V | - | - | 1 | MHz |
| | Tf | Output high to low level fall time | | - | - | 5 | ns |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | - | ns |

1. Evaluated by characterization, not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 28*.
4. For maximum frequencies above 50 MHz and $V_{DD}$ > 2.4 V, the compensation cell should be used.

**Figure 28. I/O AC characteristics definition**




Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

## 6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 55*).

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*. Refer to *Table 55: I/O static characteristics* for the values of VIH and VIL for NRST pin.

**Table 58. NRST pin characteristics**

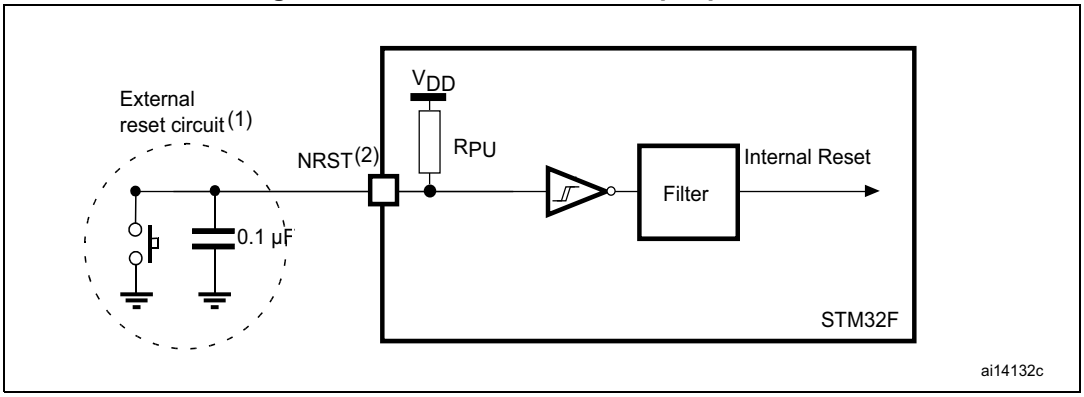
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(1) | $V_{IN}$ = $V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | - | - | - | 100 | ns |

**Table 58. NRST pin characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | $V_{DD}$ > 2.7 V | 300 | - | - | ns |
| $T_{NRST_OUT}$ | Generated reset pulse duration | Internal Reset source | 20 | - | - | µs |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Specified by design, not tested in production.

**Figure 29. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 58*. Otherwise the reset is not taken into account by the device.

## 6.3.18 TIM timer characteristics

The parameters given in *Table 59* are specified by design and not tested in production.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 59. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 100 MHz | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | | 0 | 50 | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | $f_{TIMxCLK}$ = 100 MHz | 0.0119 | 780 | µs |

**Table 59. TIMx characteristics(1)(2) (continued)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{MAX_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 100 MHz | - | 51.1 | S |

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Specified by design, not tested in production.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I²C characteristics are described in *Table 60*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.

**Table 60. I²C characteristics**

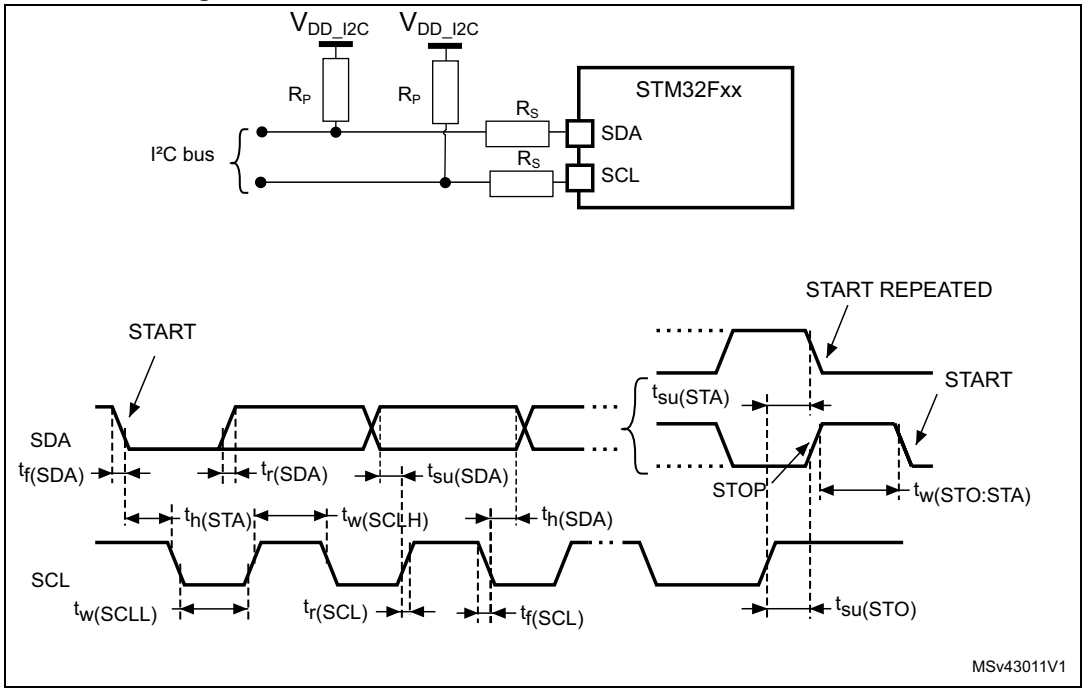
| Symbol | Parameter | Standard mode I²C(1)(2) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3450(3) | 0 | 900(4) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | µs |

**Table 60. I²C characteristics (continued)**

| Symbol | Parameter | Standard mode I²C(1)(2) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard fast mode | 0 | 50(5) | 0 | 50(5) | ns |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. Specified by design, not tested in production.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP}$ (max)

**Figure 30. I²C bus AC waveforms and measurement circuit**




1. $R_S$ = series protection resistor.
2. $R_P$ = external pull-up resistor.
3. $V_{DD_I2C}$ is the I2C bus power supply.

**Table 61. SCL frequency ($f_{PCLK1}$= 50 MHz, $V_{DD}$ = $V_{DD_I2C}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = $I^2C$ speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

**Table 62. SCL frequency ($f_{PCLK1}$= 42 MHz.,$V_{DD}$ = $V_{DD_I2C}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = $I^2C$ speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

### FMPI$^2$C characteristics

The FMPI2C characteristics are described in *Table 63*.

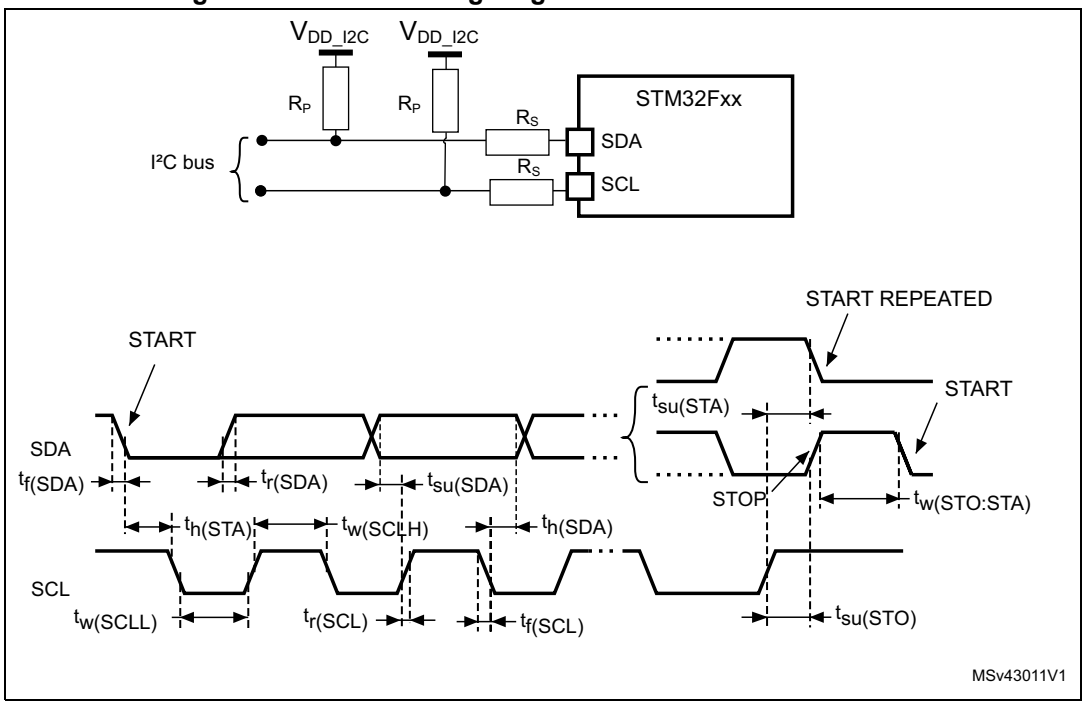
Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 63. FMPI$^2$C characteristics(1)**

| - | Parameter | Standard mode | | Fast mode | | Fast+ mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{FMPI2CC}$ | $F_{MPI2CCLK}$ frequency | 2 | - | 8 | - | 17<br>16(2) | - | us |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | 0.5 | - | |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | 0.26 | - | |
| $t_{su(SDA)}$ | SDA setup time | 0.25 | - | 0.10 | - | 0.05 | - | |
| $t_{H(SDA)}$ | SDA data hold time | 0 | - | 0 | - | 0 | - | |
| $t_{v(SDA,ACK)}$ | Data, ACK valid time | - | 3.45 | - | 0.9 | - | 0.45 | |
| $t_{r(SDA)}$<br>$t_{r(SCL)}$ | SDA and SCL rise time | - | 0.100 | - | 0.30 | - | 0.12 | |
| $t_{f(SDA)}$<br>$t_{f(SCL)}$ | SDA and SCL fall time | - | 0.30 | - | 0.30 | - | 0.12 | |
| $t_{h(STA)}$ | Start condition hold time | 4 | - | 0.6 | - | 0.26 | - | |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | 0.26 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4 | - | 0.6 | - | 0.26 | - | |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | 0.5 | - | |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode | - | - | 0.05 | 0.09 | 0.05 | 0.09 | |
| $C_b$ | Capacitive load for each bus Line | - | 400 | - | 400 | - | 550(3) | pF |

1. Evaluated by characterization, not tested in production.
2. When tr(SDA,SCL)<=110 ns.
3. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

**Figure 31. FMPI$^2$C timing diagram and measurement circuit**




## SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 64. SPI dynamic characteristics(1)**

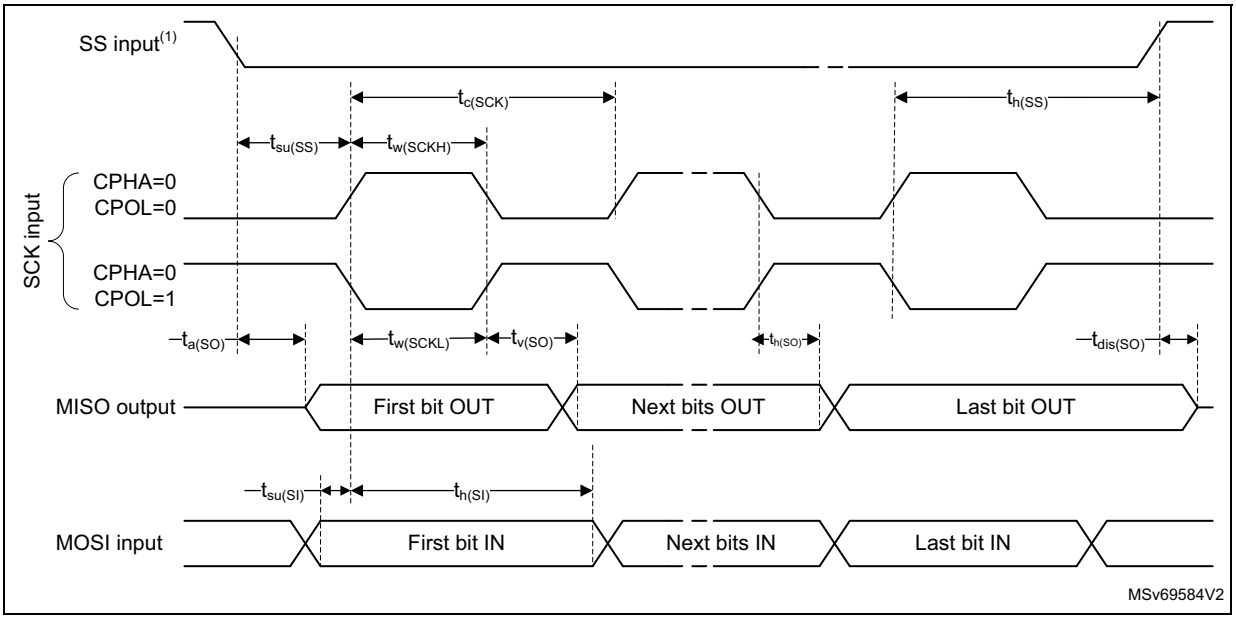
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master full duplex/receiver mode,<br>2.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 42 | MHz |
| | | Master full duplex/receiver mode,<br>3.0 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Master transmitter mode<br>1.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Master mode<br>1.7 V < $V_{DD}$ < 3.6 V<br>SPI1/2/3/4/5 | - | - | 25 | |
| | | Slave transmitter/full duplex mode<br>2.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 38(2) | |
| | | Slave receiver mode,<br>1.8 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Slave mode,<br>1.8 V < $V_{DD}$ < 3.6 V<br>SPI1/2/3/4/5 | - | - | 25 | |
| Duty(SCK) | Duty cycle of SPI clock frequency | Slave mode | 30 | 50 | 70 | % |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$ | SCK high and low time | Master mode, SPI presc = 2 | $T_{PCLK}$ - 1.5 | $T_{PCLK}$ | $T_{PCLK}$ +1.5 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | $3T_{PCLK}$ | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | $2T_{PCLK}$ | - | - | ns |
| $t_{su(MI)}$ | Data input setup time | Master mode | 4 | - | - | ns |
| $t_{su(SI)}$ | | Slave mode | 2.5 | - | - | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 7.5 | - | - | ns |
| $t_{h(SI)}$ | | Slave mode | 3.5 | - | - | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode | 7 | - | 21 | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 5 | - | 12 | ns |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge),<br>2.7 V < $V_{DD}$ < 3.6 V | - | 11 | 13 | ns |
| | | Slave mode (after enable edge),<br>1.7 V < $V_{DD}$ < 3.6 V | - | 11 | 18.5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge),<br>1.7 V < $V_{DD}$ < 3.6 V | 8 | - | - | ns |

**Table 64. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 4 | 6 | ns |
| $t_{h(MO)}$ | Data output hold time | Master mode (after enable edge) | 0 | - | - | ns |

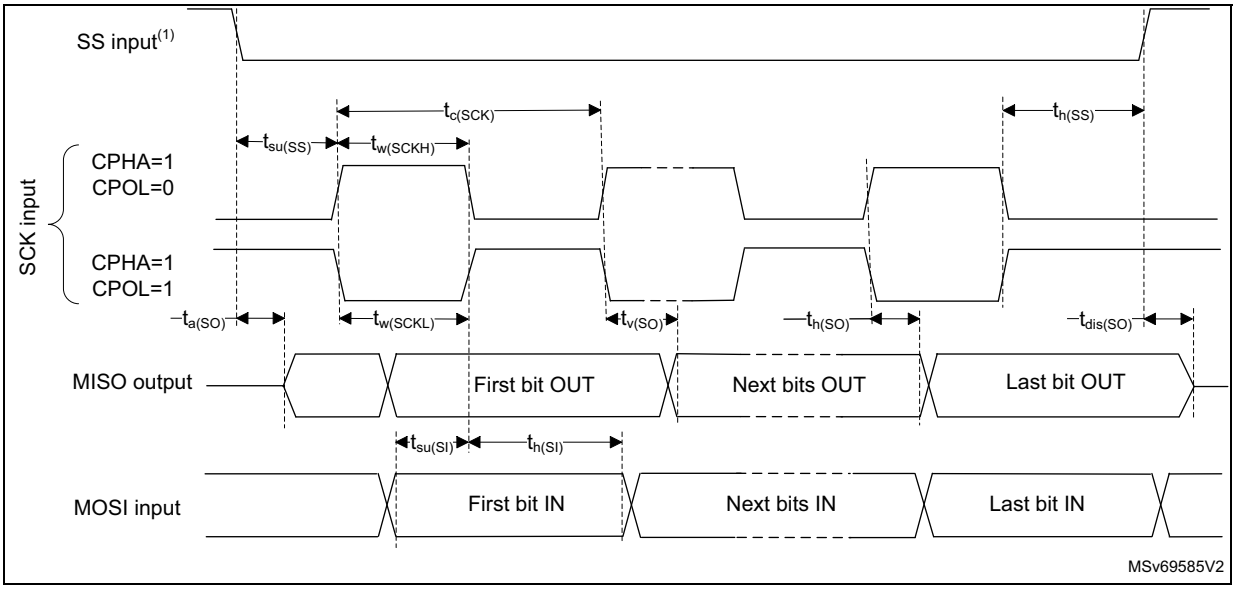
1. Evaluated by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

**Figure 32. SPI timing diagram - slave mode and CPHA = 0**



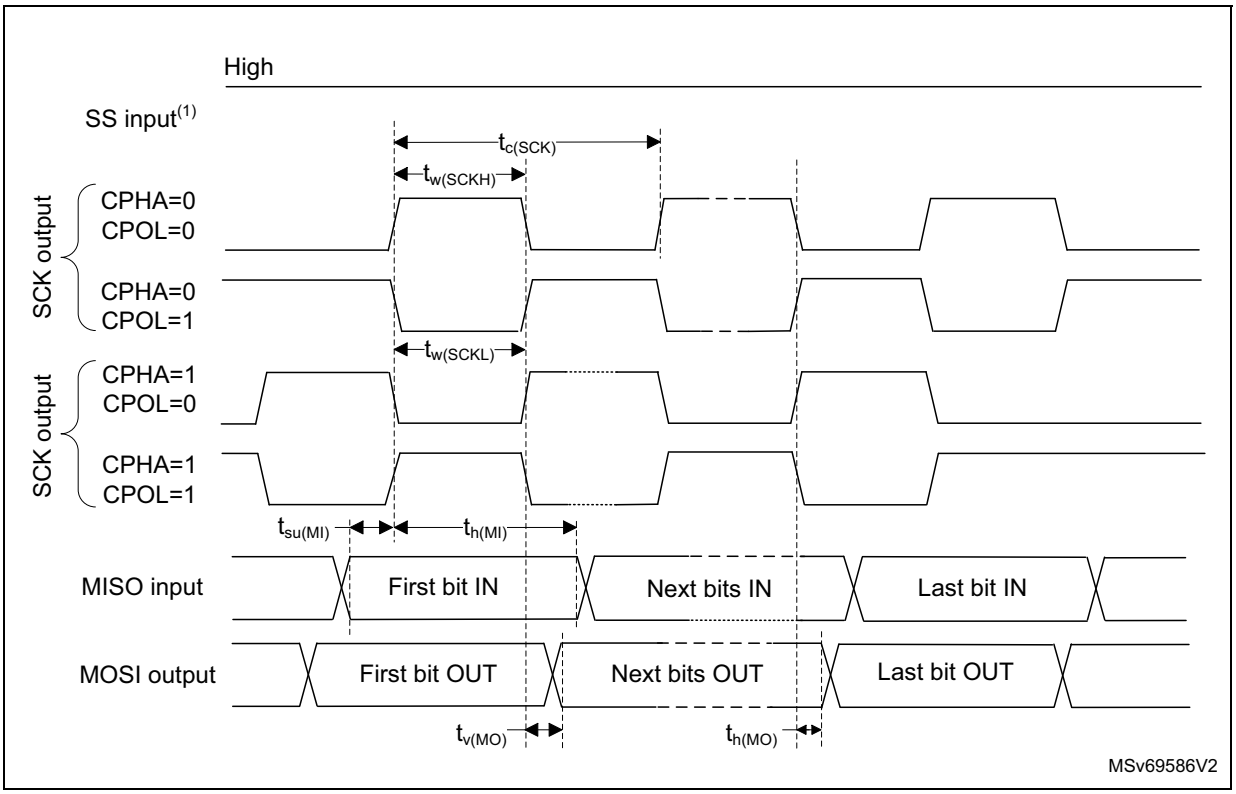

1. The SS input polarity can be configured to active low or active high.

**Figure 33. SPI timing diagram - slave mode and CPHA = 1**



1. The SS input polarity can be configured to active low or active high.

**Figure 34. SPI timing diagram - master mode**




1. The SS input polarity can be configured to active low or active high.

### I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

**Table 65. I²S dynamic characteristics(1)**

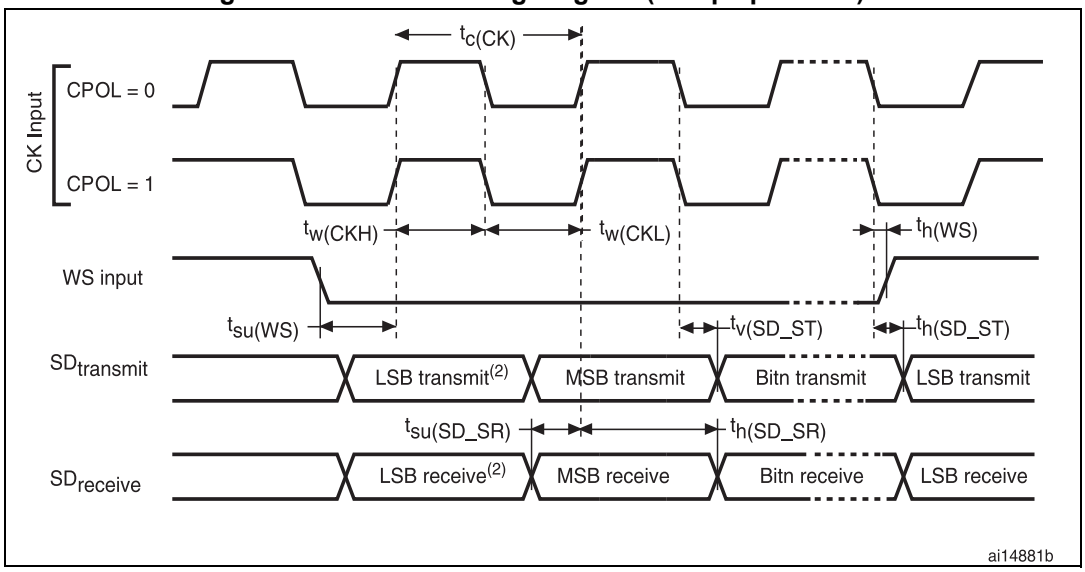
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main clock output | - | 256x8K | 256xFs(2) | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave data: 32 bits | - | 64xFs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(WS)}$ | WS valid time | Master mode | 0 | 7 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 1.5 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 1.5 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 3 | - | |
| $t_{su(SD_MR)}$ | Data input setup time | Master receiver | 1 | - | |
| $t_{su(SD_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{h(SD_MR)}$ | Data input hold time | Master receiver | 7 | - | |
| $t_{h(SD_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{v(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 20 | |
| $t_{v(SD_MT)}$ | | Master transmitter (after enable edge) | - | 6 | |
| $t_{h(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 8 | - | |
| $t_{h(SD_MT)}$ | | Master transmitter (after enable edge) | 2 | - | |

1. Evaluated by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

*Note: Refer to the I2S section of RM0401 reference manual for more details on the sampling frequency ($F_S$).*

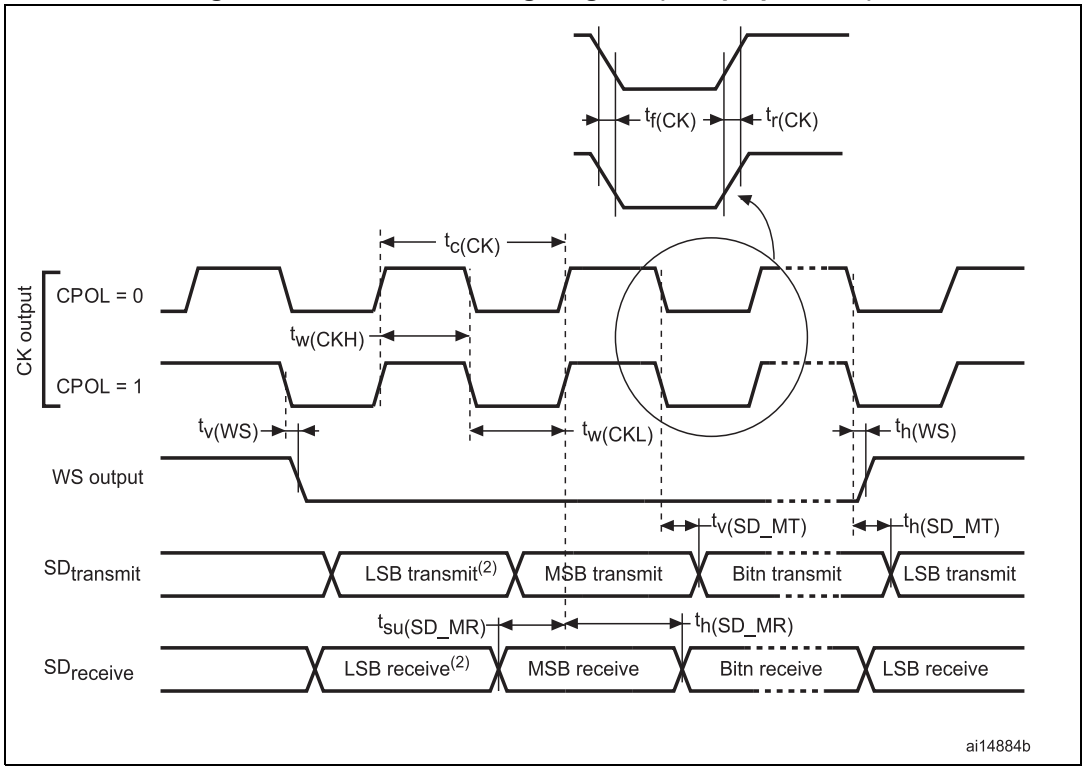
*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Figure 35. I²S slave timing diagram (Philips protocol)(1)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 36. I²S master timing diagram (Philips protocol)(1)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### 6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 15*.

**Table 66. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | $V_{DDA} - V_{REF+} < 1.2$ V | 1.7(1) | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 1.7(1) | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | - | 0 | - | |
| $f_{ADC}$ | ADC clock frequency | $V_{DDA}$ = 1.7(1) to 2.4 V | 0.6 | 15 | 18 | MHz |
| | | $V_{DDA}$ = 2.4 to 3.6 V | 0.6 | 30 | 36 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 30 MHz, 12-bit resolution | - | - | 1764 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2)(4) | Sampling switch resistance | - | - | - | 6 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | 4 | 7 | pF |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | - | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | - | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | - | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |

**Table 66. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msps |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msps |
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | - | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | - | - | 1.6 | 1.8 | mA |

1. $V_{DDA}$ minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Evaluated by characterization, not tested in production.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 66*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} = \frac{(k-0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

**Table 67. ADC accuracy at $f_{ADC}$ = 18 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =18 MHz<br>$V_{DDA}$ = 1.7 to 3.6 V<br>$V_{REF}$ = 1.7 to 3.6 V<br>$V_{DDA}$ – $V_{REF}$ < 1.2 V | ±3 | ±4 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±1 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±2 | ±3 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Evaluated by characterization, not tested in production.

**Table 68. ADC accuracy at $f_{ADC}$ = 30 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 30 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V, $V_{DDA}-V_{REF}$ < 1.2 V | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±4 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Evaluated by characterization, not tested in production.

**Table 69. ADC accuracy at $f_{ADC}$ = 36 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =36 MHz, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V $V_{DDA}-V_{REF}$ < 1.2 V | ±4 | ±7 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±3 | ±6 | |
| ED | Differential linearity error | | ±2 | ±3 | |
| EL | Integral linearity error | | ±3 | ±6 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Evaluated by characterization, not tested in production.

**Table 70. ADC dynamic accuracy at $f_{ADC}$ = 18 MHz - limited test conditions(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =18 MHz $V_{DDA}$ = $V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C | 10.3 | 10.4 | - | bits |
| SINAD | Signal-to-noise and distortion ratio | | 64 | 64.2 | - | dB |
| SNR | Signal-to-noise ratio | | 64 | 65 | - | |
| THD | Total harmonic distortion | | - | -72 | -67 | |

1. Evaluated by characterization, not tested in production.

**Table 71. ADC dynamic accuracy at $f_{ADC}$ = 36 MHz - limited test conditions(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 36 MHz $V_{DDA}$ = $V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C | 10.6 | 10.8 | - | bits |
| SINAD | Signal-to noise and distortion ratio | | 66 | 67 | - | dB |
| SNR | Signal-to noise ratio | | 64 | 68 | - | |
| THD | Total harmonic distortion | | - | -72 | -70 | |

1. Evaluated by characterization, not tested in production.

*Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

**Figure 37. ADC accuracy characteristics**

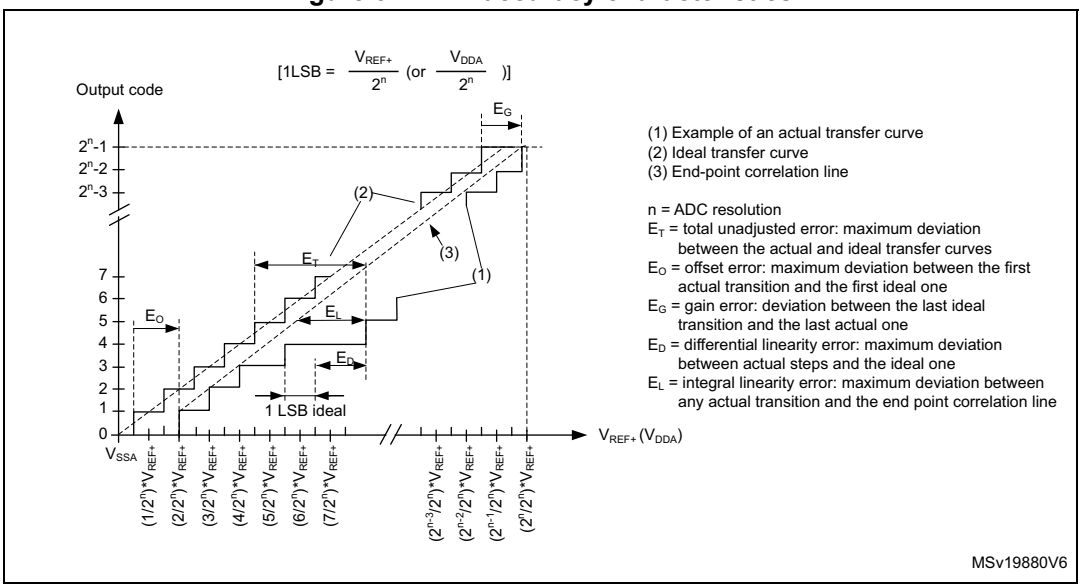
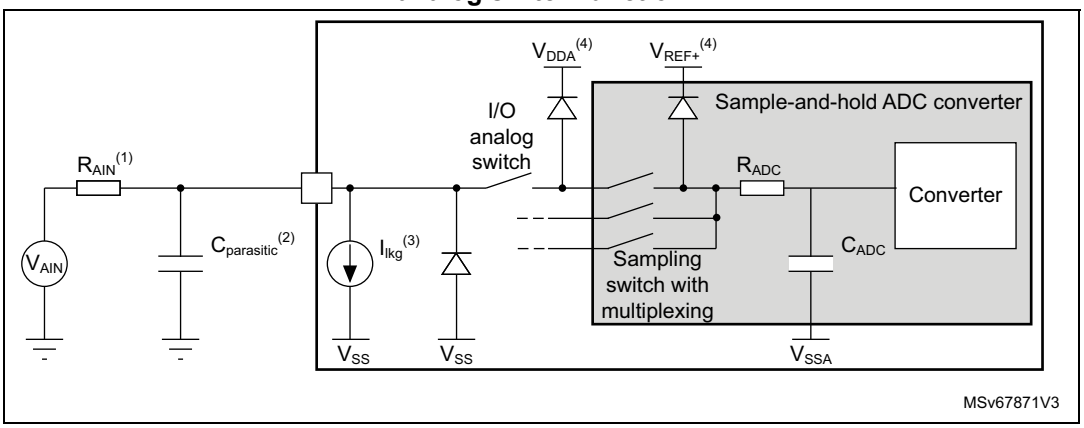



**Figure 38. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function**

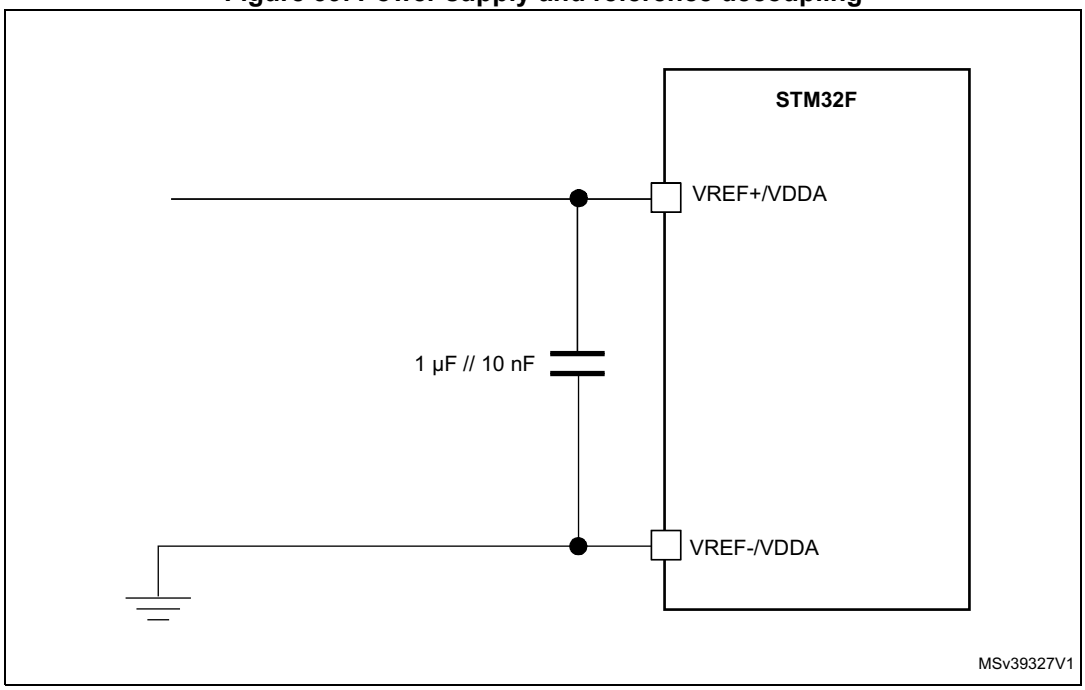



1. Refer to *Table 66: ADC characteristics* for the values of $R_{AIN}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 55: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ must be reduced.
3. Refer to *Table 55: I/O static characteristics* for the value of $I_{lkg}$.
4. Refer to *Figure 13: Power supply scheme*.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 39*. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 39. Power supply and reference decoupling**




## 6.3.21 Temperature sensor characteristics

**Table 72. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | - | 2.5 | - | mV/°C |
| $V_{25}$(1) | Voltage at 25 °C | - | 0.76 | - | V |
| $t_{START}$(2) | Startup time | - | 6 | 10 | µs |
| $T_{S_temp}$(2) | ADC sampling time when reading the temperature (1 °C accuracy) | 10 | - | - | µs |

1. Evaluated by characterization, not tested in production.
2. Specified by design, not tested in production.

**Table 73. Temperature sensor calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2C - 0x1FFF 7A2D |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2E - 0x1FFF 7A2F |

### 6.3.22 $V_{BAT}$ monitoring characteristics

**Table 74. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 4 | - | - |
| Er(1) | Error on Q | –1 | - | +1 | % |
| $T_{S_vbat}$(2) | ADC sampling time when reading the $V_{BAT}$ 1 mV accuracy | 5 | - | - | µs |

1. Specified by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.23 Embedded reference voltage

The parameters given in *Table 75* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 15*.

**Table 75. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | - 40 °C < $T_A$ < + 125 °C | 1.18 | 1.21 | 1.24 | V |
| $T_{S_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | 10 | - | - | µs |
| $V_{RERINT_s}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ± 10m V | - | 3 | 5 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | - | - | 30 | 50 | ppm/°C |
| $t_{START}$(2) | Startup time | - | - | 6 | 10 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Specified by design, not tested in production.

**Table 76. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$ = 3.3 V | 0x1FFF 7A2A - 0x1FFF 7A2B |

### 6.3.24 DAC electrical characteristics

**Table 77. DAC characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.7(1) | - | 3.6 | V | - |
| $V_{REF+}$ | Reference supply voltage | - | | 1.7(1) | - | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| $V_{SSA}$ | Ground | - | | 0 | - | 0 | V | - |
| $R_{LOAD}$(2) | Resistive load | DAC output buffer ON | $R_{LOAD}$ connected to $V_{SSA}$ | 5 | - | - | kΩ | - |
| | | | $R_{LOAD}$ connected to $V_{DDA}$ | 25 | - | - | kΩ | - |
| $R_O$(2) | Impedance output with buffer OFF | - | | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$(2) | Capacitive load | - | | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer ON | - | | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x1C7) to (0xE38) at $V_{REF+}$ = 1.7 V |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer ON | - | | - | - | $V_{DDA}$ – 0.2 | V | |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer OFF | - | | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer OFF | - | | - | - | $V_{REF+}$ – 1LSB | V | |
| $I_{VREF+}$(4) | DAC DC $V_{REF}$ current consumption in quiescent mode (Standby mode) | - | | - | 170 | 240 | µA | With no load, worst code (0x800) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| | | - | | - | 50 | 75 | | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |

**Table 77. DAC characteristics (continued)**

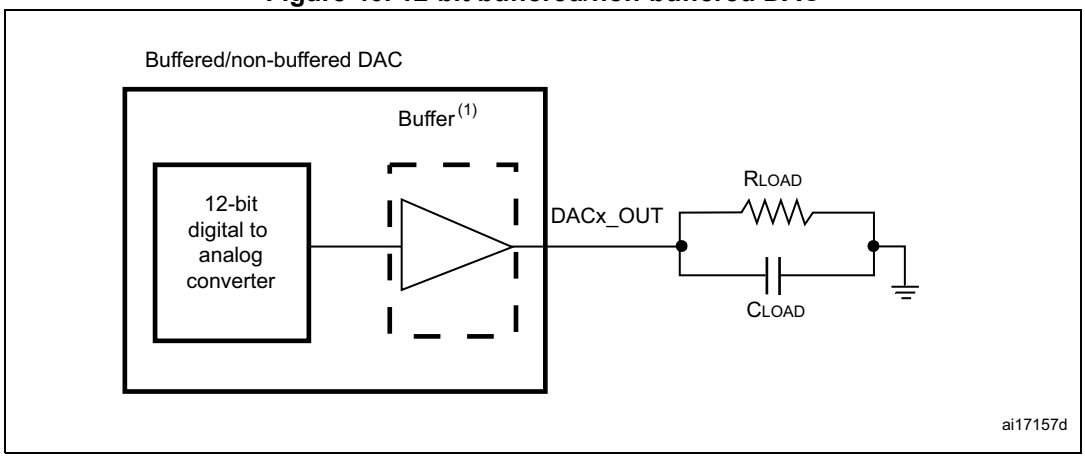
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|
| $I_{DDA}$(4) | DAC DC VDDA current consumption in quiescent mode(3) | - | - | 280 | 380 | µA | With no load, middle code (0x800) on the inputs |
| | | - | - | 475 | 625 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| DNL(4) | Differential non linearity Difference between two consecutive code-1LSB) | - | - | - | ±0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | - | ±2 | LSB | Given for the DAC in 12-bit configuration. |
| INL(4) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration. |
| Offset(4) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}$/2) | - | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error(4) | Gain error | - | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(4) | Total Harmonic Distortion Buffer ON | - | - | 3 | 6 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| THD(4) | - | - | - | - | - | dB | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate(2) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |

**Table 77. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|
| $t_{WAKEUP}$(4) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ (2) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | - | - | - –67 | - 40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Specified by design, not tested in production.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Evaluated by characterization, not tested in production.

**Figure 40. 12-bit buffered/non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

## 6.3.25 RTC characteristics

**Table 78. RTC characteristics**

| Symbol | Parameter | Conditions | Min | Max |
|---|---|---|---|---|
| - | $f_{PCLK1}$/RTCCLK frequency ratio | Any read/write operation from/to an RTC register | 4 | - |

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 7.1 Device marking

Refer to technical note "*Reference device marking schematics for STM32 microcontrollers and microprocessors*" (TN1433), available from www.st.com, for the location of pin 1/ball A1 as well as the location and orientation of the marking areas versus pin 1/ball A1.

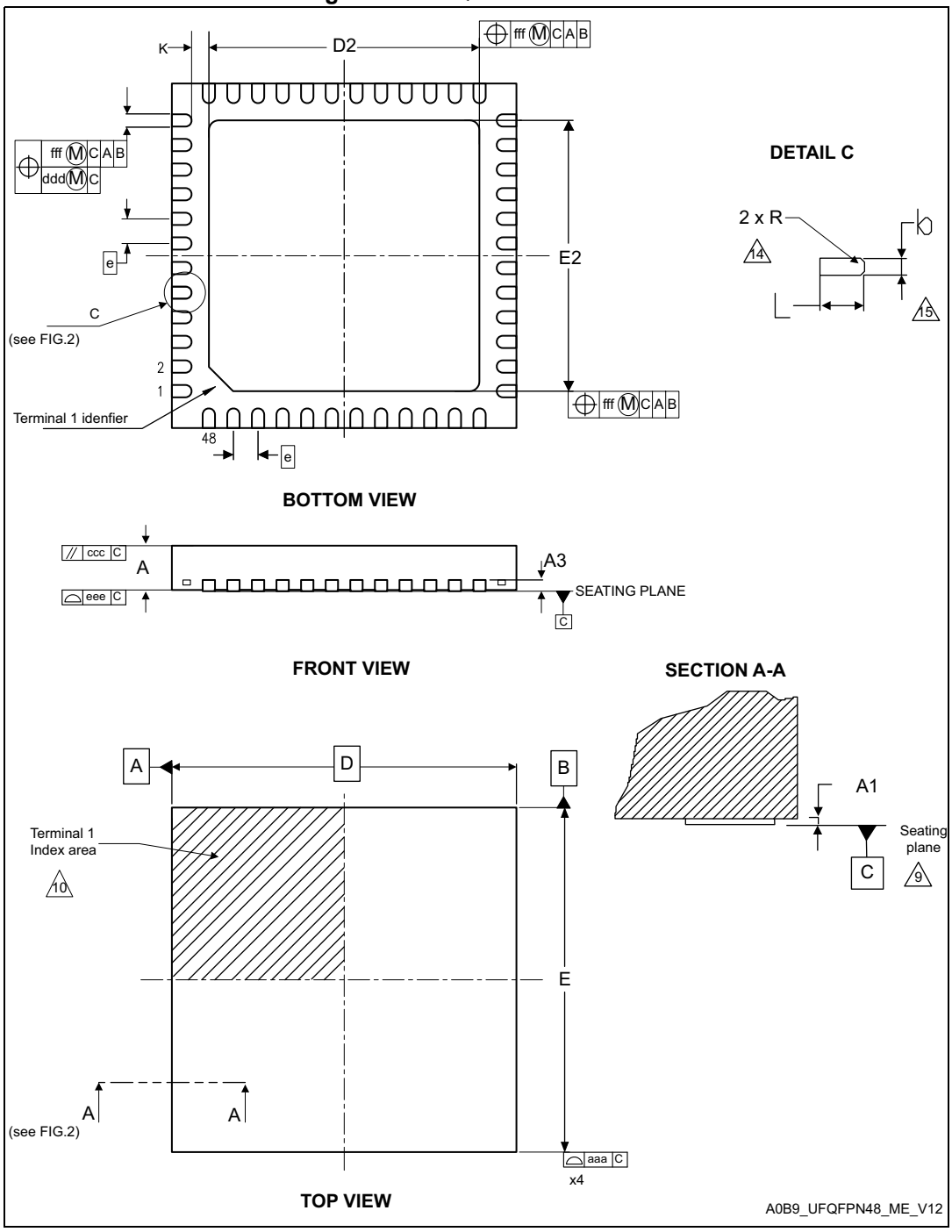
Parts marked as "ES" or "E", or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

## 7.2 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

**Figure 41. UFQFPN48 – Outline**



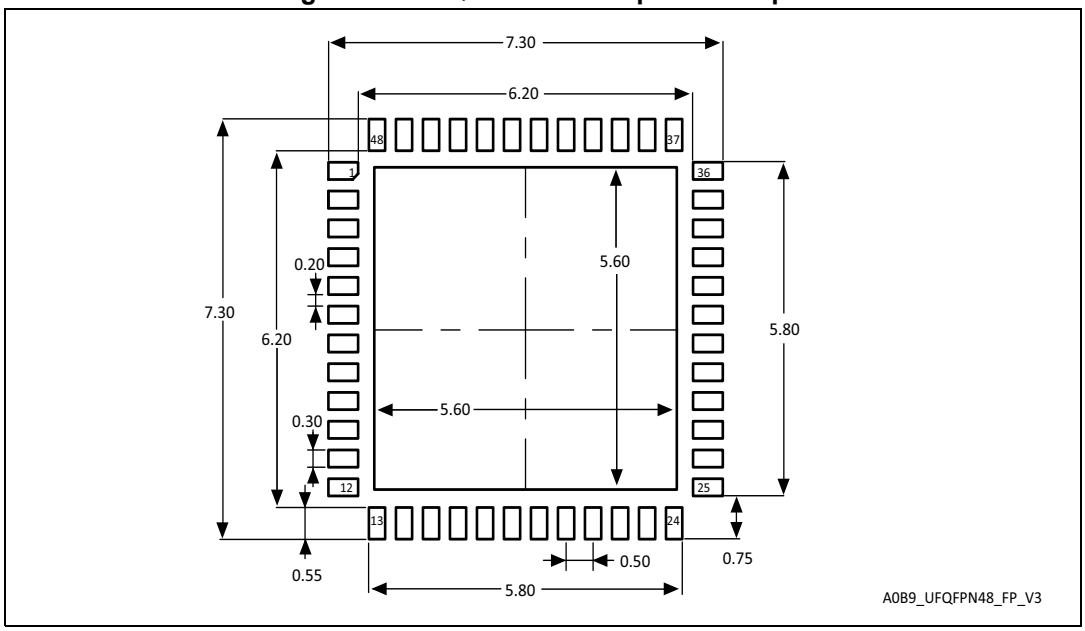

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 79. UFQFPN48 – Mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.50 | 0.55 | 0.60 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.00 | - | 0.05 | 0.0000 | - | 0.0020 |
| b | 0.18 | 0.25 | 0.30 | 0.0071 | 0.0098 | 0.0118 |
| D[2] | 7.00 BSC | | | 0.2756 BSC | | |
| D2[3] | 5.50 | 5.60 | 5.70 | 0.2165 | 0.2205 | 0.2244 |
| E[2] | 7.00 BSC | | | 0.2756 BSC | | |
| E2[3] | 5.50 | 5.60 | 5.70 | 0.2165 | 0.2205 | 0.2244 |
| e | 0.50 BSC | | | 0.0197 BSC | | |
| N | 48 | | | | | |
| L | 0.30 | - | 0.50 | 0.0118 | - | 0.0197 |
| R | 0.10 | - | - | 0.0039 | - | - |
| aaa | 0.15 | | | 0.0059 | | |
| bbb | 0.10 | | | 0.0039 | | |
| ccc | 0.10 | | | 0.0039 | | |
| ddd | 0.05 | | | 0.0020 | | |
| eee | 0.08 | | | 0.0031 | | |
| fff | 0.10 | | | 0.0039 | | |

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

**Figure 42. UFQFPN48 – Footprint example**




1. Dimensions are expressed in millimeters.

## 7.3 LQFP48 package information (5B)

This LQFP is a 48-pin, 7 x 7 mm low-profile quad flat package.

*Note: See list of notes in the notes section.*

**Figure 43. LQFP48 - Outline(15)**

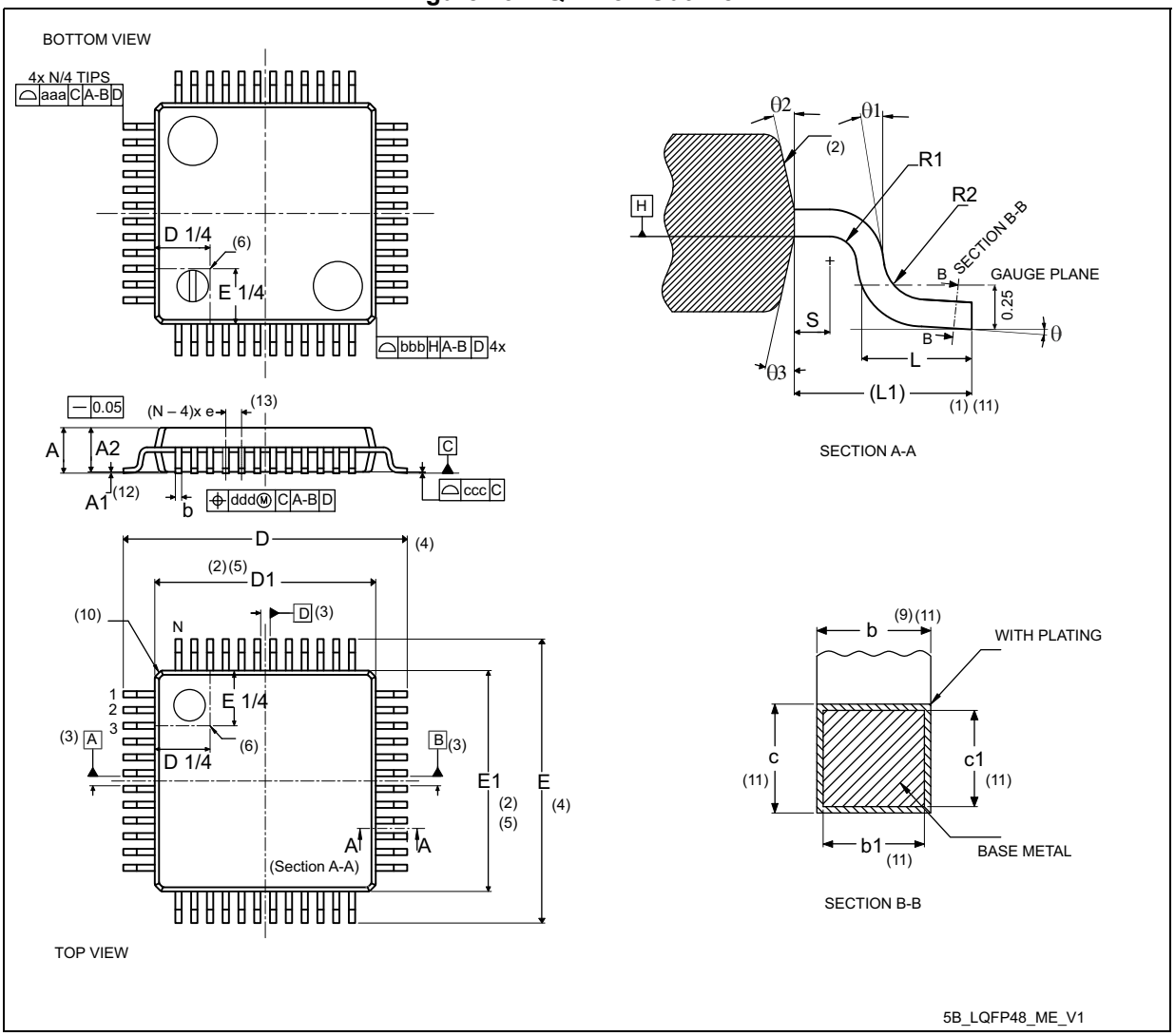


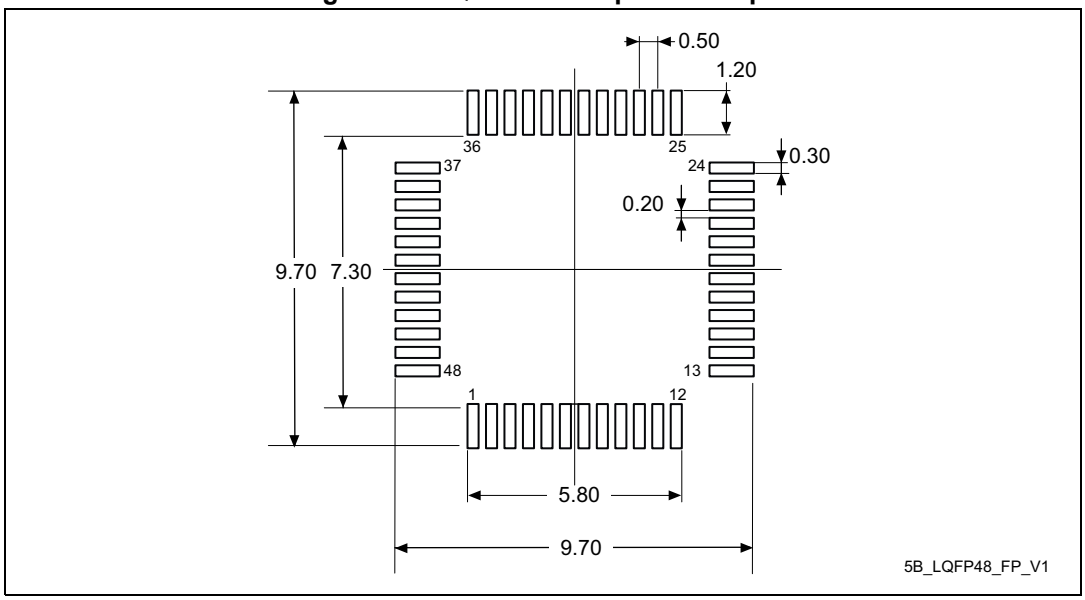
**Table 80. LQFP48 - Mechanical data**

| Symbol | millimeters | | | inches[14] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.0630 |
| A1[12] | 0.05 | - | 0.15 | 0.0020 | - | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b[9][11] | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| b1[11] | 0.17 | 0.20 | 0.23 | 0.0067 | 0.0079 | 0.0090 |
| c[11] | 0.09 | - | 0.20 | 0.0035 | - | 0.0079 |
| c1[11] | 0.09 | - | 0.16 | 0.0035 | - | 0.0063 |
| D[4] | 9.00 BSC | | | 0.3543 BSC | | |
| D1[2][5] | 7.00 BSC | | | 0.2756 BSC | | |
| E[4] | 9.00 BSC | | | 0.3543 BSC | | |
| E1[2][5] | 7.00 BSC | | | 0.2756 BSC | | |
| e | 0.50 BSC | | | 0.1970 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | 1.00 REF | | | 0.0394 REF | | |
| N[13] | 48 | | | | | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | - | - | 0° | - | - |
| θ2 | 10° | 12° | 14° | 10° | 12° | 14° |
| θ3 | 10° | 12° | 14° | 10° | 12° | 14° |
| R1 | 0.08 | - | - | 0.0031 | - | - |
| R2 | 0.08 | - | 0.20 | 0.0031 | - | 0.0079 |
| S | 0.20 | - | - | 0.0079 | - | - |
| aaa[1][7] | 0.20 | | | 0.0079 | | |
| bbb[1][7] | 0.20 | | | 0.0079 | | |
| ccc[1][7] | 0.08 | | | 0.0031 | | |
| ddd[1][7] | 0.08 | | | 0.0031 | | |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

**Figure 44. LQFP48 - Footprint example**




1. Dimensions are expressed in millimeters.

## 7.4 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

*Note: See list of notes in the notes section.*

**Figure 45. LQFP64 - Outline(15)**

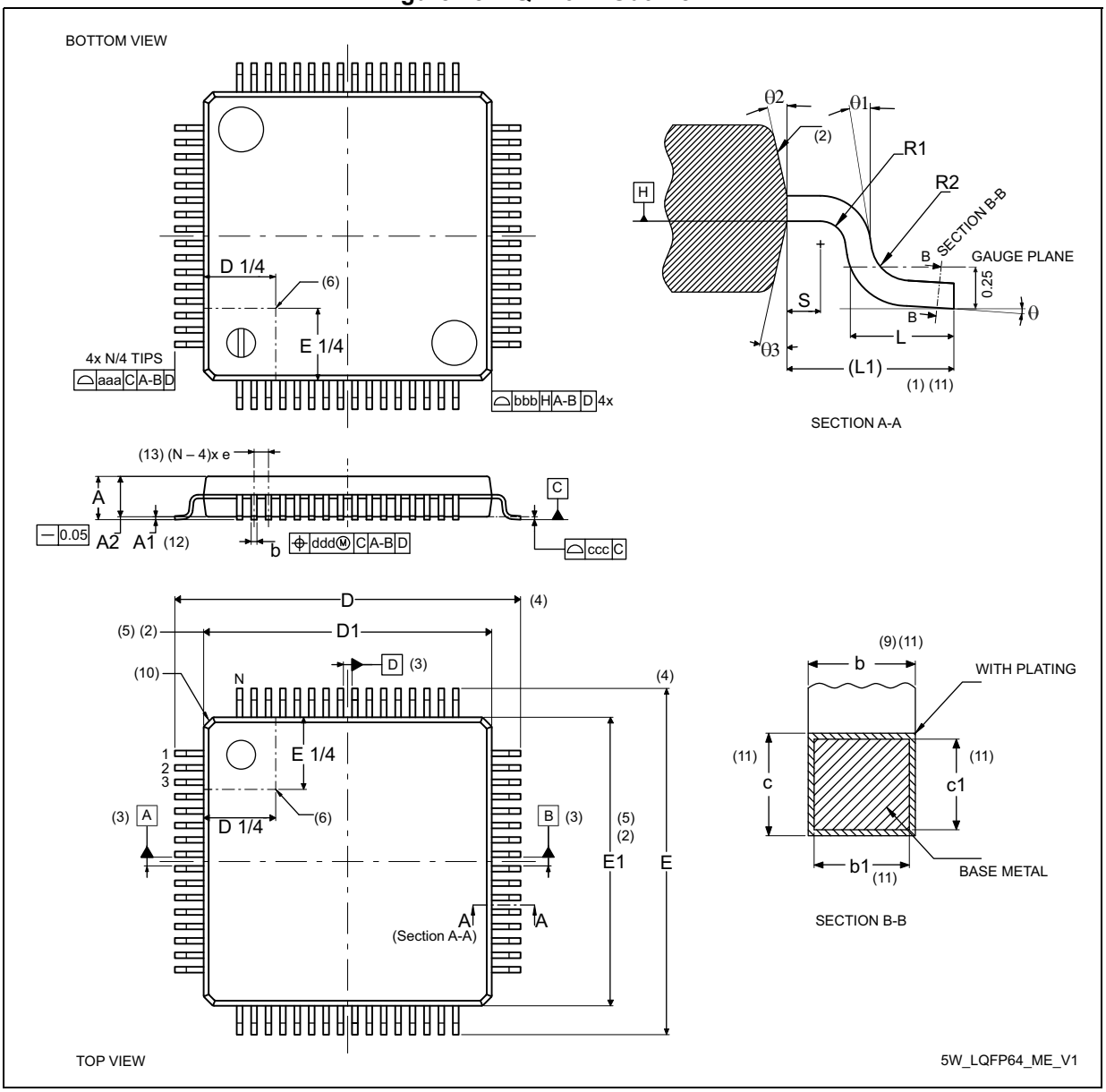


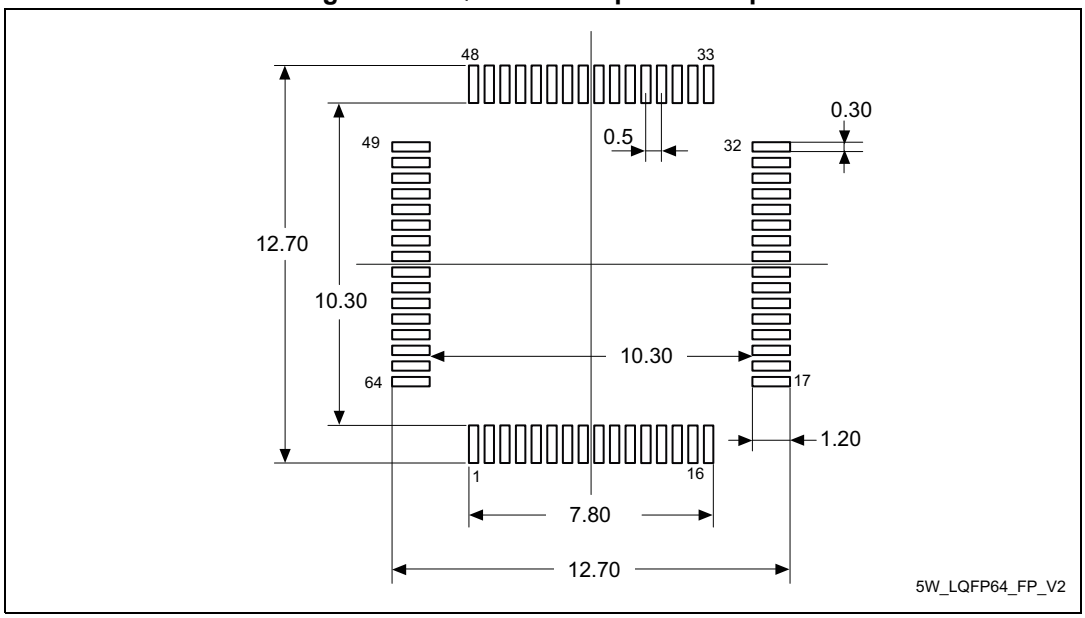
**Table 81. LQFP64 - Mechanical data**

| Symbol | millimeters | | | inches[14] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.0630 |
| A1[12] | 0.05 | - | 0.15 | 0.0020 | - | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0570 |
| b[9][11] | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| b1[11] | 0.17 | 0.20 | 0.23 | 0.0067 | 0.0079 | 0.0091 |
| c[11] | 0.09 | - | 0.20 | 0.0035 | - | 0.0079 |
| c1[11] | 0.09 | - | 0.16 | 0.0035 | - | 0.0063 |
| D[4] | 12.00 BSC | | | 0.4724 BSC | | |
| D1[2][5] | 10.00 BSC | | | 0.3937 BSC | | |
| E[4] | 12.00 BSC | | | 0.4724 BSC | | |
| E1[2][5] | 10.00 BSC | | | 0.3937 BSC | | |
| e | 0.50 BSC | | | 0.1970 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | 1.00 REF | | | 0.0394 REF | | |
| N[13] | 64 | | | | | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | - | - | 0° | - | - |
| θ2 | 10° | 12° | 14° | 10° | 12° | 14° |
| θ3 | 10° | 12° | 14° | 10° | 12° | 14° |
| R1 | 0.08 | - | - | 0.0031 | - | - |
| R2 | 0.08 | - | 0.20 | 0.0031 | - | 0.0079 |
| S | 0.20 | - | - | 0.0079 | - | - |
| aaa[1] | 0.20 | | | 0.0079 | | |
| bbb[1] | 0.20 | | | 0.0079 | | |
| ccc[1] | 0.08 | | | 0.0031 | | |
| ddd[1] | 0.08 | | | 0.0031 | | |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

**Figure 46. LQFP64 - Footprint example**




1. Dimensions are expressed in millimeters.

## 7.5 UFBGA64 package information (A019)

This UFBGA is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 47. UFBGA64 – Outline(13)**

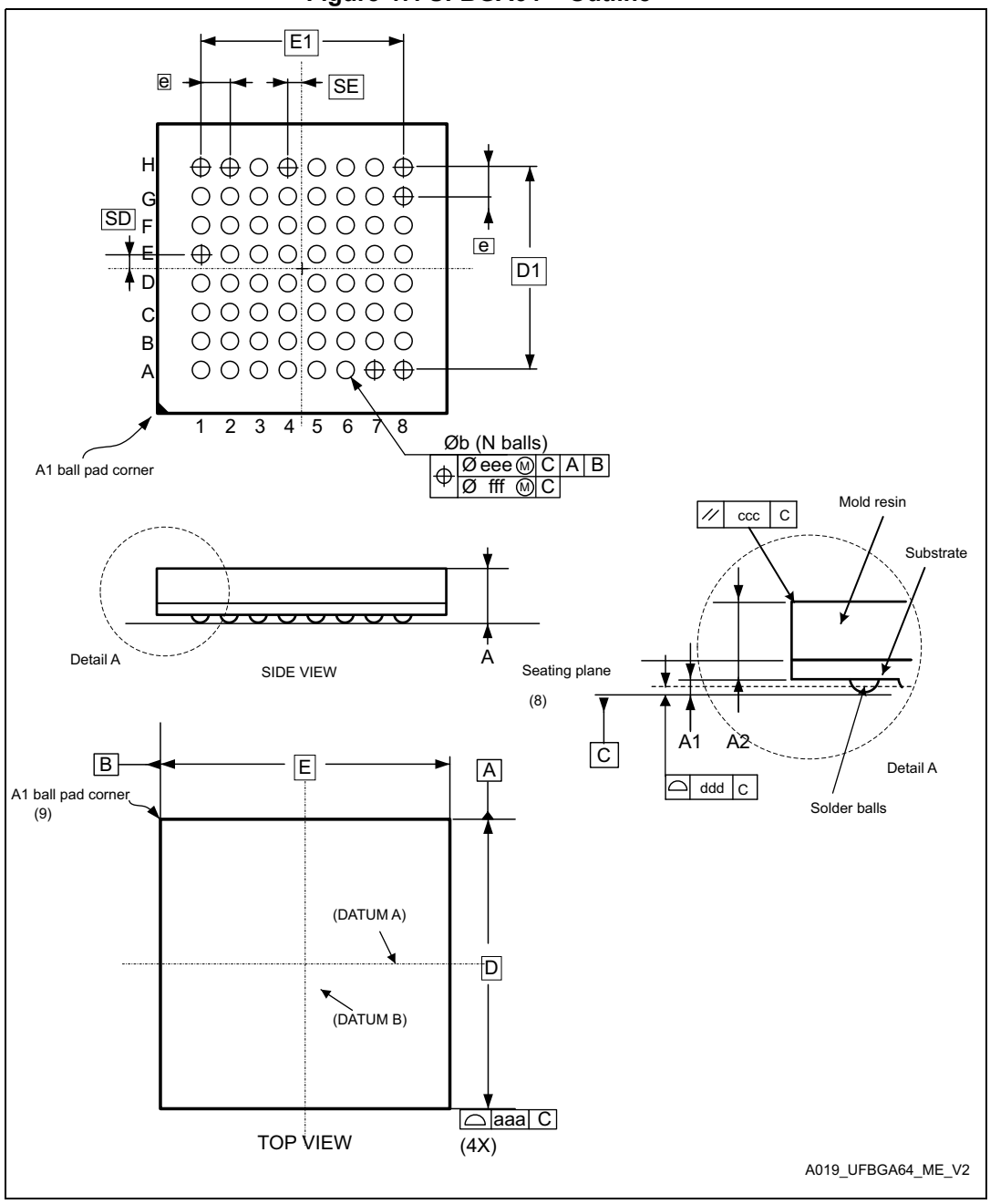


**Table 82. UFBGA64 – Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 0.60 | - | - | 0.0236 |
| A1[4] | 0.05 | - | - | 0.0020 | - | - |
| A2 | - | 0.43 | - | - | 0.0169 | - |
| b[5] | 0.23 | 0.28 | 0.33 | 0.0090 | 0.0110 | 0.0130 |
| D[6] | 5.00 BSC | | | 0.1969 BSC | | |
| D1 | 3.50 BSC | | | 0.1378 BSC | | |
| E | 5.00 BSC | | | 0.1969 BSC | | |
| E1 | 3.50 BSC | | | 0.1378 BSC | | |
| e[9] | 0.50 BSC | | | 0.0197 BSC | | |
| N[11] | 64 | | | | | |
| SD[12] | 0.25 BSC | | | 0.0098 BSC | | |
| SE[12] | 0.25 BSC | | | 0.0098 BSC | | |
| aaa | 0.15 | | | 0.0059 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.08 | | | 0.0031 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.05 | | | 0.0020 | | |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.5 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

**Figure 48. UFBGA64 – Footprint example**

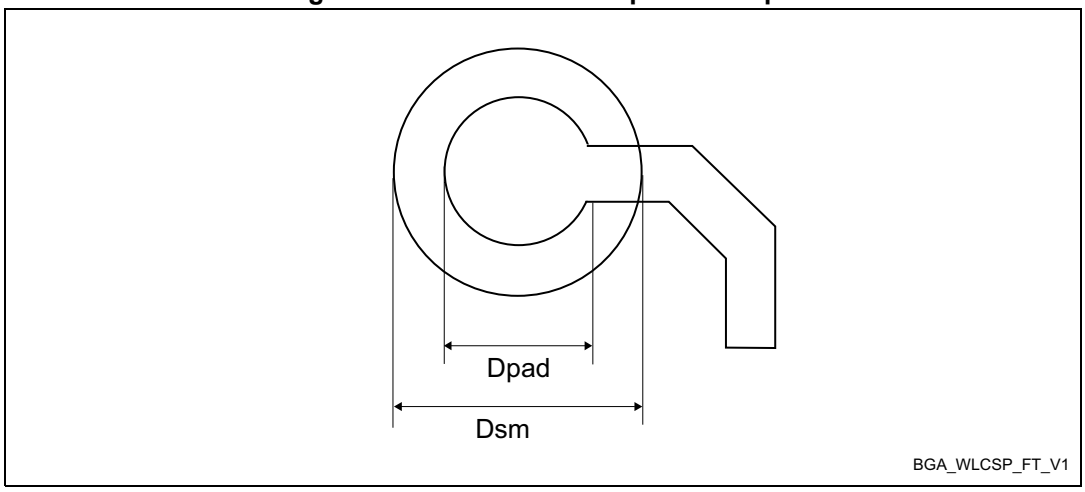
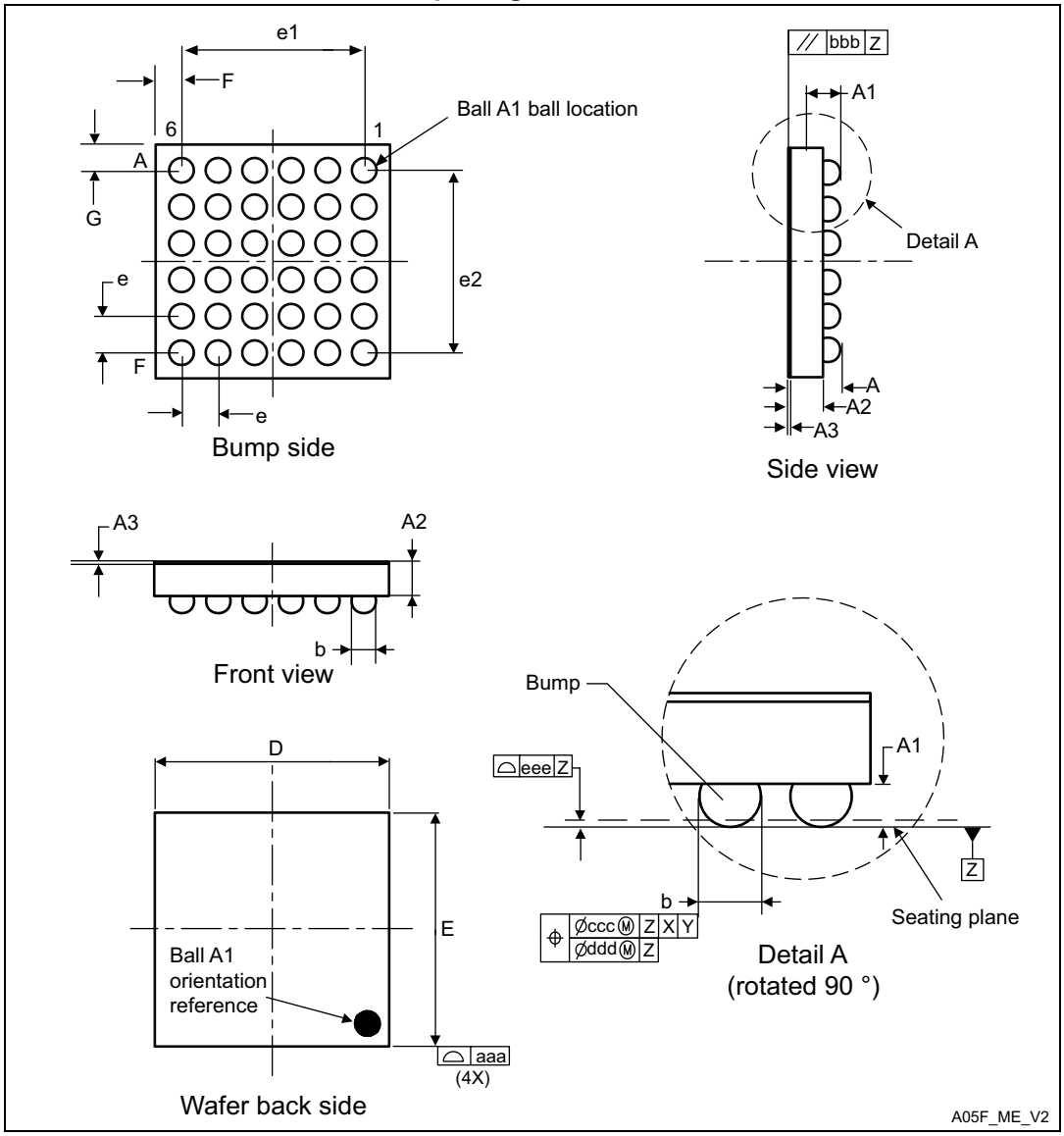



**Table 83. UFBGA64 - Example of PCB design rules (0.5 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.5 mm |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

## 7.6 WLCSP36 package information

**Figure 49. WLCSP36 - 36-ball, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package outline**



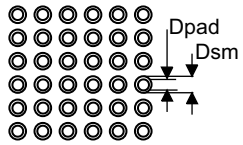

1. Drawing is not to scale.

**Table 84. WLCSP36 - 36-ball, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.170 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 2.518 | 2.553 | 2.588 | 0.1012 | 0.1026 | 0.1039 |
| E | 2.544 | 2.579 | 2.614 | 0.1050 | 0.1064 | 0.1078 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 2.000 | - | - | 0.0787 | - |
| e2 | - | 2.000 | - | - | 0.0787 | - |
| F | - | 0.2765 | - | - | 0.0119 | - |
| G | - | 0.2895 | - | - | 0.0138 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 50. WLCSP36 - 36-ball, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**




A05F_FP_V1

**Table 85. WLCSP36 recommended PCB design rules (0.4 mm pitch)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.225 mm |

**Table 85. WLCSP36 recommended PCB design rules (0.4 mm pitch) (continued)**

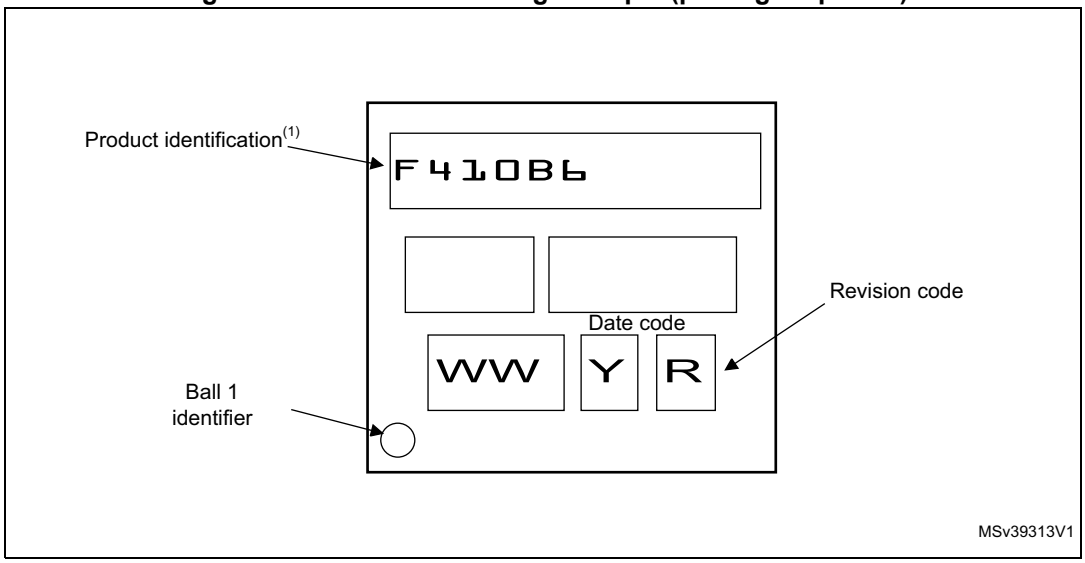
| Dimension | Recommended values |
|---|---|
| Dsm | 0.290 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

### WLCSP36 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 51. WLCSP36 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 15: General operating conditions on page 52*.

The maximum chip-junction temperature, $T_J$ max., in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + (PD max x $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- PD max is the sum of $P_{INT}$ max and $P_{I/O}$ max (PD max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 86. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP48 | 55 | °C/W |
| | **Thermal resistance junction-ambient** LQFP64 | 46 | |
| | **Thermal resistance junction-ambient** UFQFPN48 | 33 | |
| | **Thermal resistance junction-ambient** WLCSP36 | 61 | |
| | **Thermal resistance junction-ambient** UFBGA64 | 79 | |

### 7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

# 8 Part numbering

**Table 87. Ordering information scheme**

Example: STM32 F 410 C B Y 6 TR

**Device family**

STM32 = Arm®-based 32-bit microcontroller

**Product type**

F = General-purpose

Device subfamily

410 = 410 line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

**Flash memory size**

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

**Package**

I = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

**Temperature range**

6 = Industrial temperature range, - 40 to 85 °C

7 = Industrial temperature range, - 40 to 105 °C

3 = Industrial temperature range, - 40 to 125 °C

Packing

TR = tape and reel

No character = tray or tube

# Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BRO) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- VBAT functionality is no more available and VBAT pin should be connected to VDD.

## A.1 Operating conditions

**Table 88. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait state ($f_{Flashmax}$) | Maximum Flash memory access frequency with no wait states(1) (2) | I/O operation | Possible Flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ = 1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz(4) | 100 MHz with 6 wait states | No I/O compensation | 8-bit erase and program operations only |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART Accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART Accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.15.1: Internal reset ON*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

# Appendix B Application block diagrams

## B.1 Sensor Hub application example

**Figure 52. Sensor hub application example 1**

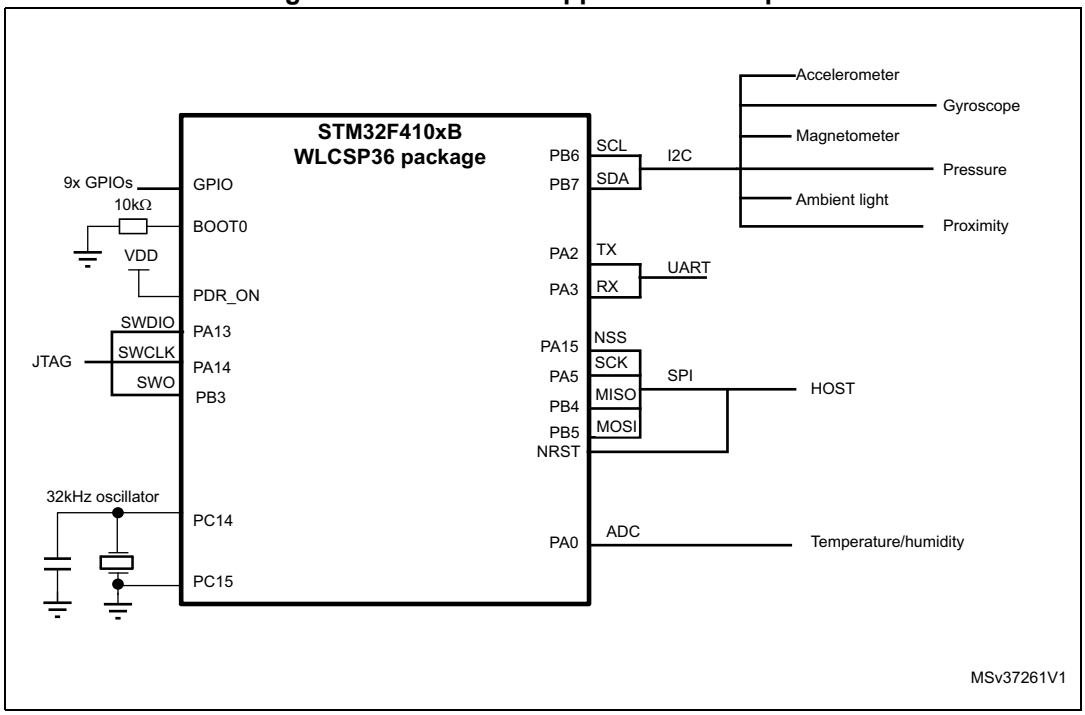
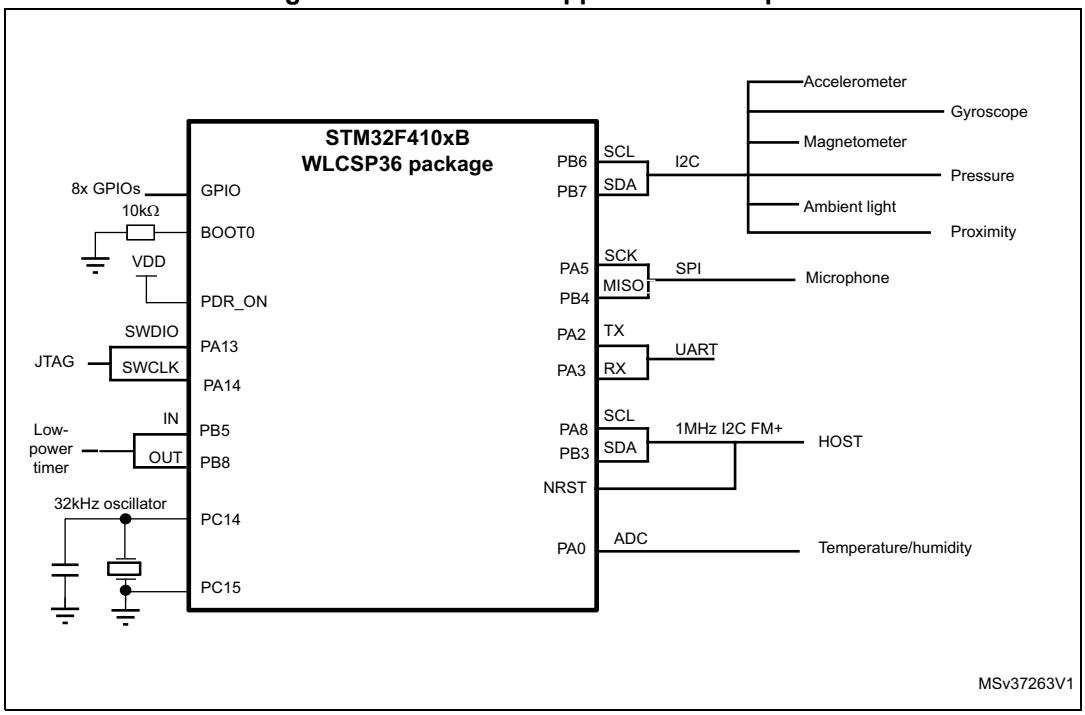



**Figure 53. Sensor hub application example 2**

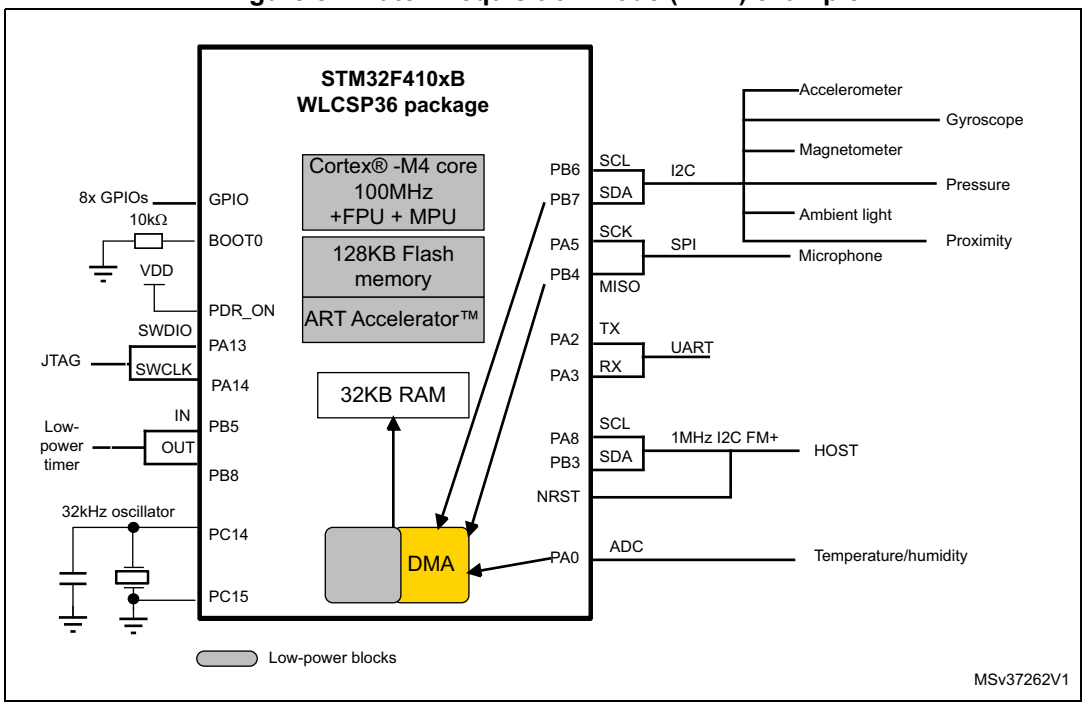


## B.2 Batch Acquisition Mode (BAM) example

Data is transferred through the DMA from interfaces into the internal SRAM while the rest of the MCU is set in low power mode.

- Code execution from RAM before switching off the Flash.
- Flash is set in power down and flash interface (ART accelerator™) clock is stopped.
- The clocks are enabled only for the required interfaces.
- MCU core is set in sleep mode (core clock stopped waiting for interrupt).
- Only the needed DMA channels are enabled and running.

**Figure 54. Batch Acquisition Mode (BAM) example**



# 9 Important security notice

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# Revision history

**Table 89. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 28-Sep-2015 | 1 | Initial release. |
| 07-Dec-2015 | 2 | Junction temperature range changed to –40 to + 110 °C for WLCSP49 package.<br>Updated *Figure 7: UFQFPN48 pinout*. |
| 10-Aug-2016 | 3 | Updated:<br>– *Table 2: STM32F410x8/B features and peripheral counts*<br>– *Table 9: STM32F410x8/B pin definitions*<br>– *Table 14: Thermal characteristics*<br>– *Table 15: General operating conditions*<br>– *Table 20: Embedded reset and power control block characteristics*<br>– Tables from *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V* to *Table 34: Typical and maximum current consumptions in $V_{BAT}$ mode (LSE and RTC ON, LSE low- drive mode)*<br>– *Table 42: HSI oscillator characteristics*<br>– *Table 43: LSI oscillator characteristics*<br>– *Table 49: Flash memory endurance and data retention*<br>– *Table 52: ESD absolute maximum ratings*<br>– *Table 55: I/O static characteristics*<br>– *Table 66: ADC characteristics*<br>– *Table 75: Embedded internal reference voltage*<br>– *Table 77: DAC characteristics*<br>– *Table 87: Ordering information scheme*<br>– *Figure 16: Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSE oscillator in "low power" mode selection*<br>– *Section 7: Package information*<br>Added:<br>– *Figure 5: LQFP48 pinout*<br>– *Figure 8: UFBGA64 ballout*<br>– *Figure 49: LQFP48 marking example (package top view)*<br>– *Figure 55: UFBGA64 marking example (package top view)* |

**Table 89. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 06-Mar-2017 | 4 | Updated:<br>– *Features*<br>– *Section 3.20: Timers and watchdogs*<br>– *Table 9: STM32F410x8/B pin definitions*<br>– *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V*<br>– *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V*<br>– *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD}$ = 3.6 V*<br>– *Table 28: Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 3.6 V*<br>– *Table 31: Typical and maximum current consumption in Stop mode - $V_{DD}$=3.6 V*<br>– *Table 34: Typical and maximum current consumptions in $V_{BAT}$ mode (LSE and RTC ON, LSE low- drive mode)* |
| 04-Apr-2017 | 5 | The maximum current consumption at 30 °C has been redefined to be in line with the actual silicon performance. For a typical customer application the impact on the average current consumption will be insignificant.<br>Updated:<br>– *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V*<br>– *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V*<br>– *Table 23: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD}$ = 1.7 V*<br>– *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD}$ = 3.6 V*<br>– *Table 25: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 3.6 V*<br>– *Table 26: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD}$ = 1.7 V*<br>– *Table 27: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD}$ = 3.6 V*<br>– *Table 37: Low-power mode wakeup timings*<br>– *Figure 30: $I^2C$ bus AC waveforms and measurement circuit*<br>– *Figure 31: FMP$I^2C$ timing diagram and measurement circuit* |

**Table 89. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 15-Dec-2017 | 6 | Updated:<br>– *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V*<br>– *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V*<br>– *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD}$ = 3.6 V*<br>– *Table 28: Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 3.6 V*<br>– *Table 31: Typical and maximum current consumption in Stop mode - $V_{DD}$=3.6 V*<br>– *Table 33: Typical and maximum current consumption in Standby mode - $V_{DD}$= 3.6 V*<br>– *Table 87: Ordering information scheme* |
| 13-Jan-2025 | 7 | Updated:<br>– Cover page<br>– *Section 1: Introduction*<br>– *Section 3.25: True random number generator (RNG)*<br>– *Section 4: Pinouts and pin description*<br>– *Figure 8: UFBGA64 ballout*<br>– *Table 9: STM32F410x8/B pin definitions*<br>– *Section 6.2: Absolute maximum ratings*<br>– *Table 12: Voltage characteristics*<br>– *Table 20: Embedded reset and power control block characteristics*<br>– *Section : I/O system current consumption*<br>– *Figure 23: $ACC_{HSI}$ versus temperature*<br>– Note 1 of *Table 42: HSI oscillator characteristics*<br>– *Table 51: EMI characteristics for fHSE = 8 MHz and fHCLK = 64 MHz*<br>– *Table 55: I/O static characteristics*<br>– *Table 56: Output voltage characteristics*<br>– *Table 57: I/O AC characteristics*<br>– *Figure 28: I/O AC characteristics definition*<br>– *Figure 32: SPI timing diagram - slave mode and CPHA = 0*, *Figure 33: SPI timing diagram - slave mode and CPHA = 1*, and *Figure 34: SPI timing diagram - master mode*<br>– *Figure 37: ADC accuracy characteristics* and *Figure 38: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function*<br>– *Section 7: Package information*<br>Added *Section 9: Important security notice* |

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