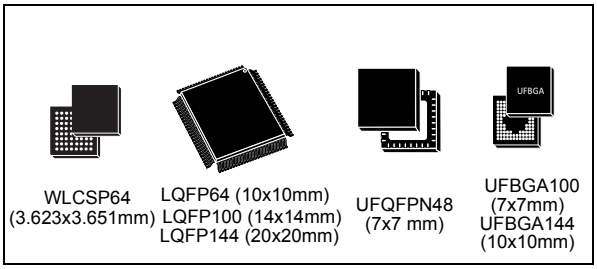
STM32F412xE STM32F412xG

Arm®-Cortex®-M4 32b MCU+FPU, 125 DMIPS, 1MB Flash, 256KB RAM, USB OTG FS, 17 TIMs, 1 ADC, 17 comm. interfaces

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Dynamic efficiency line with BAM (Batch acquisition mode)
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 1 Mbyte of flash memory
  - 256 Kbytes of SRAM
  - Flexible external static memory controller with up to 16-bit data bus: SRAM, PSRAM, NOR flash memory
  - Dual mode Quad-SPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 112 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 50 µA typical at 25 °C; 75 µA max at 25 °C
  - Stop (flash memory in Deep power down mode, slow wakeup time): down to 18 µA at 25 °C; 40 µA max at 25 °C
  - Standby: 2.4 µA at 25 °C / 1.7 V without RTC; 12 µA at 85 °C at 1.7 V
  - V_{BAT} supply for RTC: 1 µA at 25 °C 1×12-bit, 2.4 MSPS ADC: up to 16 channels



WLCSP64 (3.623x3.651mm) | LQFP64 (10x10mm) LQFP100 (14x14mm) LQFP144 (20x20mm) | UFQFPN48 (7x7 mm) | UFBGA100 (7x7mm) UFBGA144 (10x10mm)

- 2x digital filters for sigma delta modulator, 4x PDM interfaces, stereo microphone support
- General-purpose DMA: 16-stream DMA
- Up to 17 timers: up to twelve 16-bit timers, two 32-bit timers up to 100 MHz each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window), one SysTick timer
- Debug mode
  - Serial wire debug (SWD) and JTAG
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 114 I/O ports with interrupt capability
  - Up to 109 fast I/Os up to 100 MHz
  - Up to 114 five V-tolerant I/Os
- Up to 17 communication interfaces
  - Up to 4x I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs (2 x 12.5 Mbit/s, 2 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPI/I2Ss (up to 50 Mbit/s, SPI or I2S audio protocol), out of which 2 muxed full-duplex I2S interfaces
  - SDIO interface (SD/MMC/eMMC)
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with PHY
  - 2x CAN (2.0B Active)
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages are ECOPACK2 compliant

This is information on a product in full production. www.st.com

Table 1. Device summary

Reference	Part number
STM32F412xE	STM32F412CE, STM32F412RE, STM32F412VE, STM32F412ZE
STM32F412xG	STM32F412CG, STM32F412RG, STM32F412VG, STM32F412ZG

Applications

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

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1 Introduction

This datasheet provides the description of the STM32F412xE/G microcontrollers.

This document should be read in conjunction with the reference manual RM0402 “STM32F412 advanced Arm®-based 32-bit MCUs. The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, refer to the Cortex®-M4 technical reference manual, available from the www.arm.com website.

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2 Description

STM32F412xE/G devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all Arm single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

STM32F412xE/G devices belong to the STM32 Dynamic Efficiency™ product line (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing even more power consumption saving during data batching.

STM32F412xE/G devices incorporate high-speed embedded memories (up to 1 Mbyte of flash memory, 256 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, twelve general-purpose 16-bit timers, two PWM timers for motor control and two general-purpose 32-bit timers.

They also feature standard and advanced communication interfaces:

- Up to four I^2Cs, including one I^2C supporting Fast-Mode Plus

- Five SPIs

- Five I^2Ss of which two are full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL, or via an external clock to allow synchronization.

- Four USARTs

- An SDIO/MMC interface

- A USB 2.0 OTG full-speed interface

- Two CANs.

In addition, STM32F412xE/G devices embed advanced peripherals:

- A flexible static memory controller interface (FSMC)

- A Quad-SPI memory interface

- A digital filter for sigma modulator (DFSDM), two filters, up to four inputs, and support of microphone MEMs.

STM32F412xE/G devices are offered in 7 packages ranging from 48 to 144 pins. The set of available peripherals depends on the selected package.

The STM32F412xE/G operates in the -40 to +125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Table 2. STM32F412xE/G features and peripheral counts

Peripherals		STM32F412xE				STM32F412xG			
Flash memory (Kbyte)		512				1024			
SRAM (Kbyte)	System	256							
FSMC memory controller(1)		-		1		-		1	
Quad-SPI memory interface		-	1			-	1		
Timers	General-purpose	10							
	Advanced-control	2							
	Basic	2							
Random number generator		1							
Comm. interfaces	SPI/ I^2S	5/5 (2 full duplex)							
	I^2C	3							
	I^2CFMP	1							
	USART	4(2)	4			4(2)	4		
	SDIO/MMC	1							
	USB/OTG FS Dual power rail	1 No			1 Yes	1 No			1 Yes
	CAN	2							
Number of digital Filters for Sigma-delta modulator Number of channels		2 3	2 4			2 3	2 4		
LCD parallel interface Data bus size		-	8	16		-	8	16	
GPIOs		36	50	81	114	36	50	81	114
12-bit ADC Number of channels		1							
		10	16			10	16		
Maximum CPU frequency		100 MHz							
Operating voltage		1.7 to 3.6 V							
Operating temperatures		Ambient temperatures: -40 to +85 °C / -40 to +105 °C/ -40 to +125 °C							
		Junction temperature: -40 to +130 °C							
Package		UFQFPN48	LQFP64 WLCSP64	UFBGA 100 LQFP100	UFBGA 144 LQFP144	UFQFPN48	LQFP64 WLCSP 64	UFBGA 100 LQFP100	UFBGA 144 LQFP144

1. The FSMC can also be used to interface most graphic LCD controllers.
2. Limited application for the USART3 since RX is not available for the UFQFPN48.

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

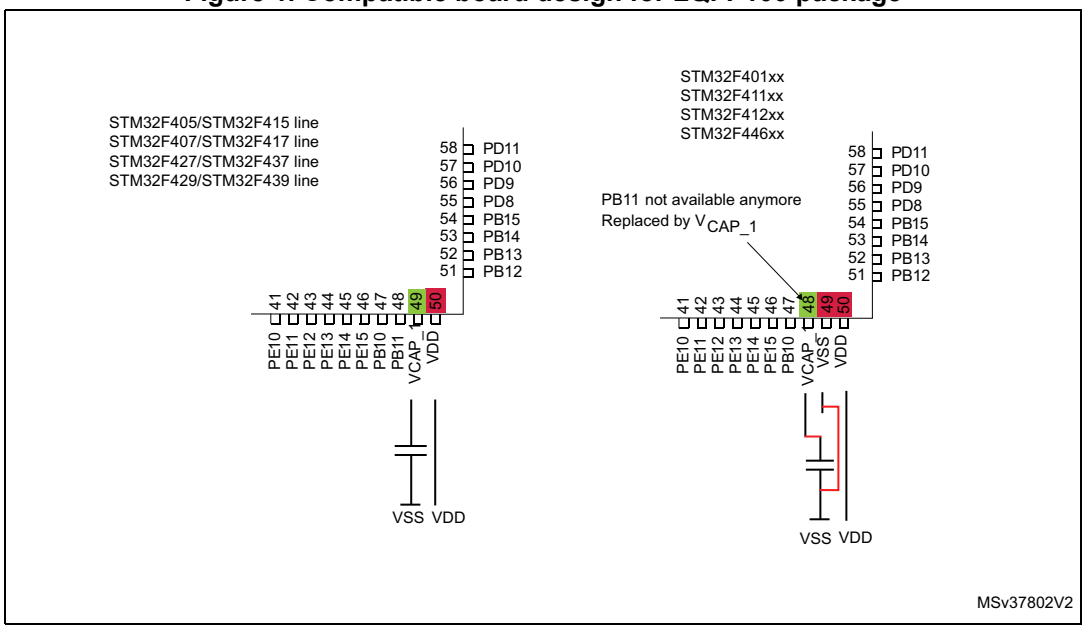


Figure 2. Compatible board design for LQFP64 package

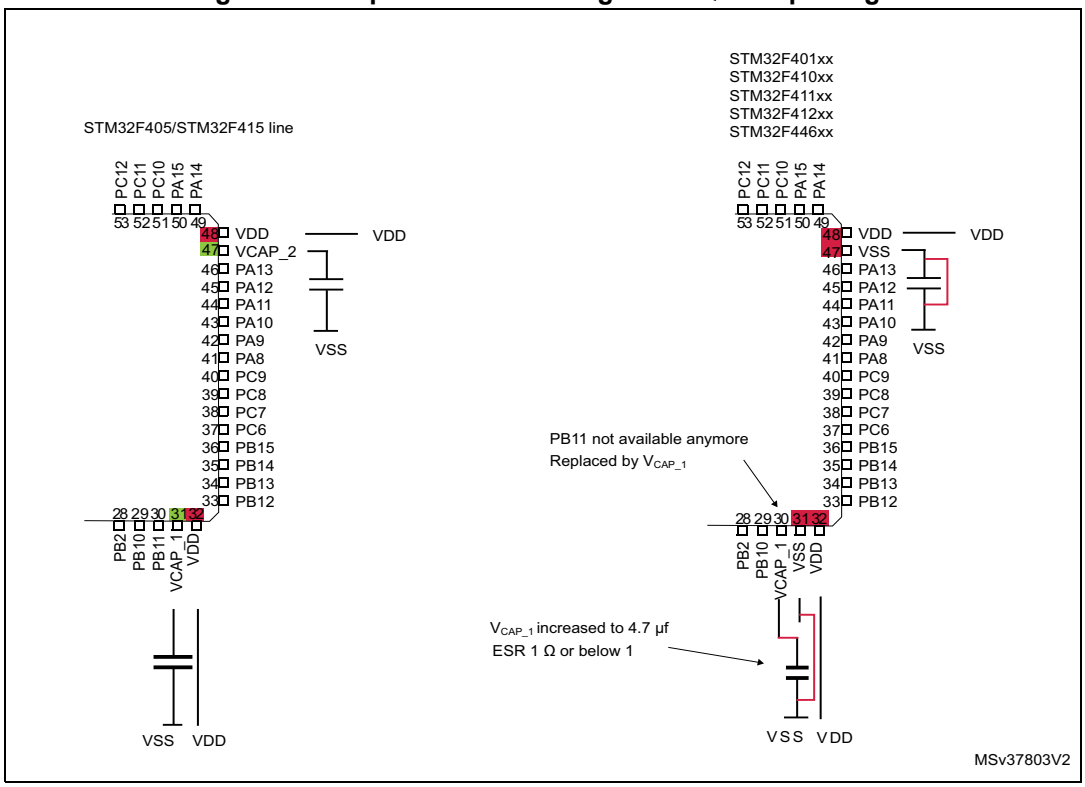


Figure 3. Compatible board design for LQFP144 package

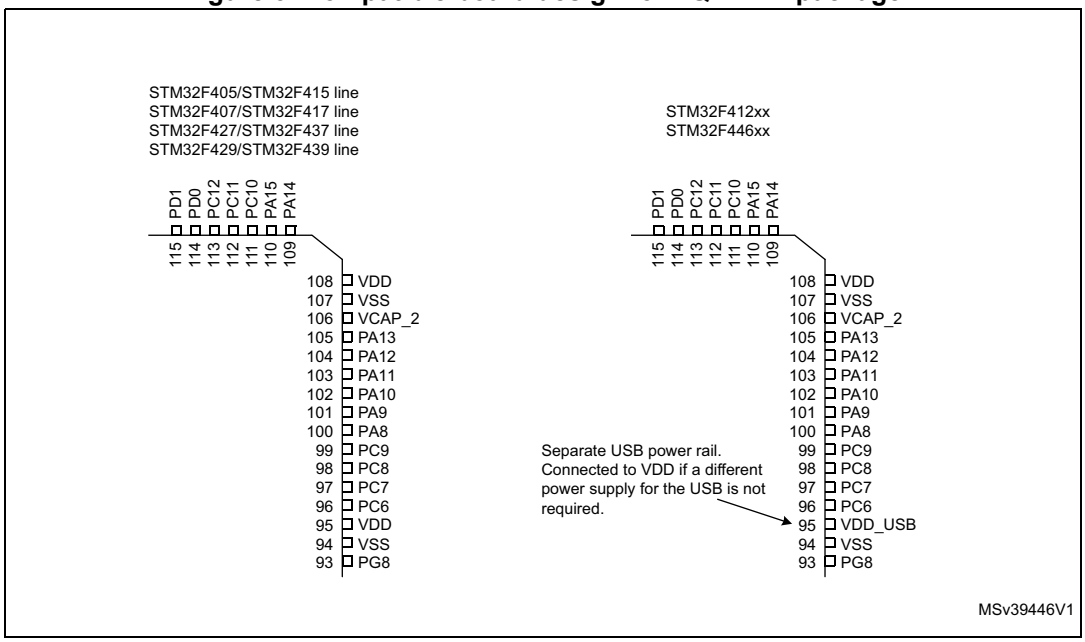
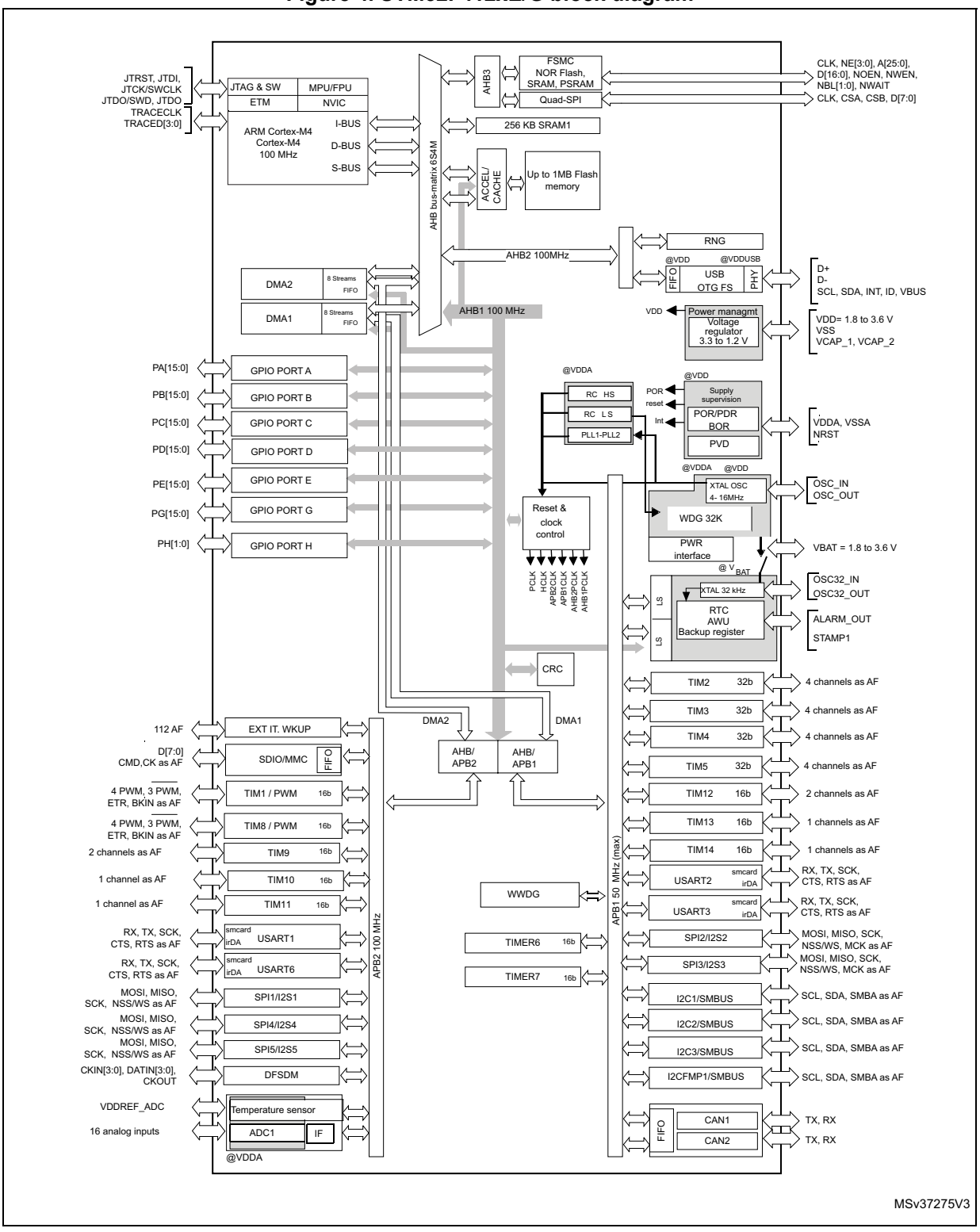


Figure 4. STM32F412xE/G block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

3 Functional overview

3.1 Arm® Cortex®-M4 with FPU core with embedded flash memory and SRAM

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F412xE/G devices are compatible with all Arm tools and software.

Figure 4 shows the general block diagram of the STM32F412xE/G.

Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 with FPU over flash memory technologies, which normally requires the processor to wait for the flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 100 MHz.

3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F412xE/G BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded flash memory

The devices embed up to 1 Mbyte of flash memory available for storing programs and data.

The flash memory user area can be protected against reading by an entrusted code (Read Protection, RDP) with different protection levels.

The flash user sectors can also be individually protected against write operation.

Furthermore the proprietary readout protection (PCROP) can also individually protect the flash user sectors against D-bus read accesses.

(Additional information can be found in the product reference manual).

To optimize the power consumption the flash memory can also be switched off in Run or in Sleep mode (see *Section 3.21: Low-power modes*).

Two modes are available: flash memory in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the flash memory, the code must be executed from the internal RAM.

3.6 One-time programmable bytes

A one-time programmable area is available with16 OTP blocks of 32 bytes. Each block can be individually locked

(Additional information can be found in the product reference manual)

3.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

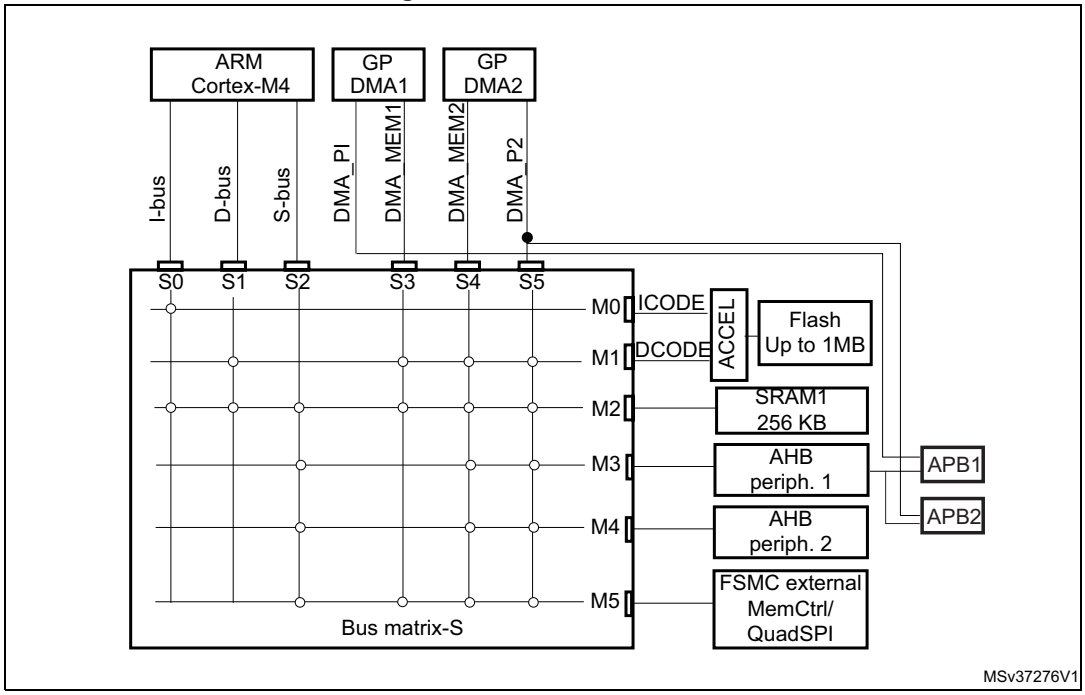
3.8 Embedded SRAM

All devices embed 256 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

3.9 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



3.10 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C and I^2CFMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter.

3.11 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.12 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI flash memories. It can work in direct mode through registers, external flash memory status register polling mode and memory mapped mode. Up to 256 Mbyte of external flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.16 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the flash memory by using one of the interface listed in the *Table 3* or the USB OTG FS in device mode through DFU (device firmware upgrade).

Table 3. Embedded bootloader interfaces

Package	USART1 PA9/ PA10	USART2 PD6/ PD5	USART3 PB11/ PB10	I2C1 PB6/ PB7	I2C2 PF0/ PF1	I2C3 PA8/ PB4	I2C FMP1 PB14/ PB15	SPI1 PA4/ PA5/ PA6/ PA7	SPI3 PA15/ PC10/ PC11/ PC12	SPI4 PE11/ PE12/ PE13/ PE14	CAN2 PB5/ PB13	USB PA11 /P12
UFQFPN48	Y	-	-	Y	-	Y	Y	Y	-	-	Y	Y
WLCSP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP100	Y	Y	-	Y	-	Y	Y	Y	Y	Y	Y	Y
LQFP144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
UFBGA100	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
UFBGA144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.17 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and NRST pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.18.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.

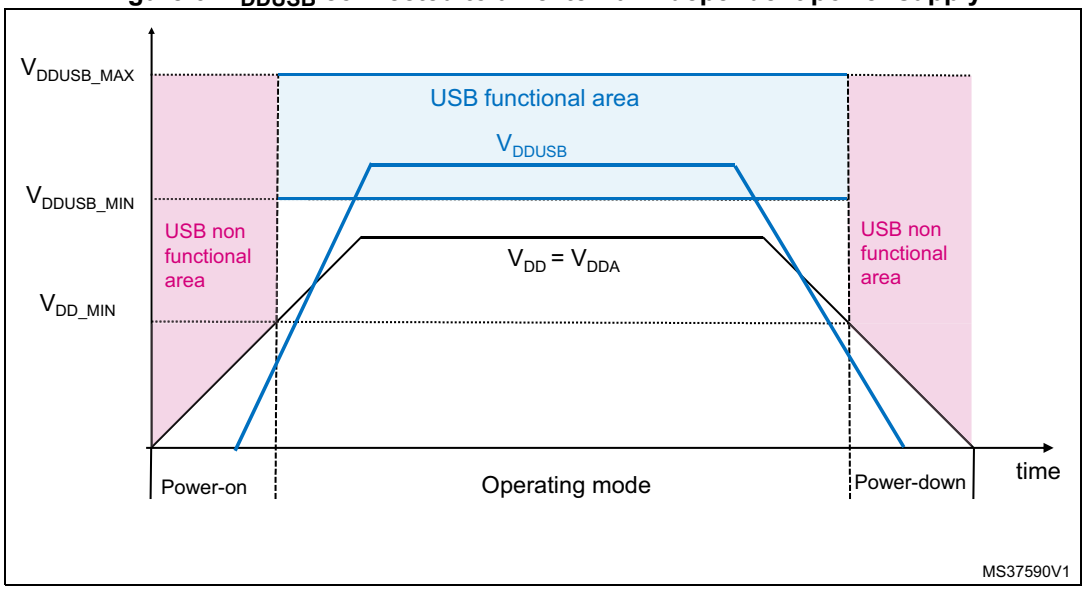
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.
  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply,

it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - If USB is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 6. V_{DDUSB} connected to an external independent power supply



3.18 Power supply supervisor

3.18.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

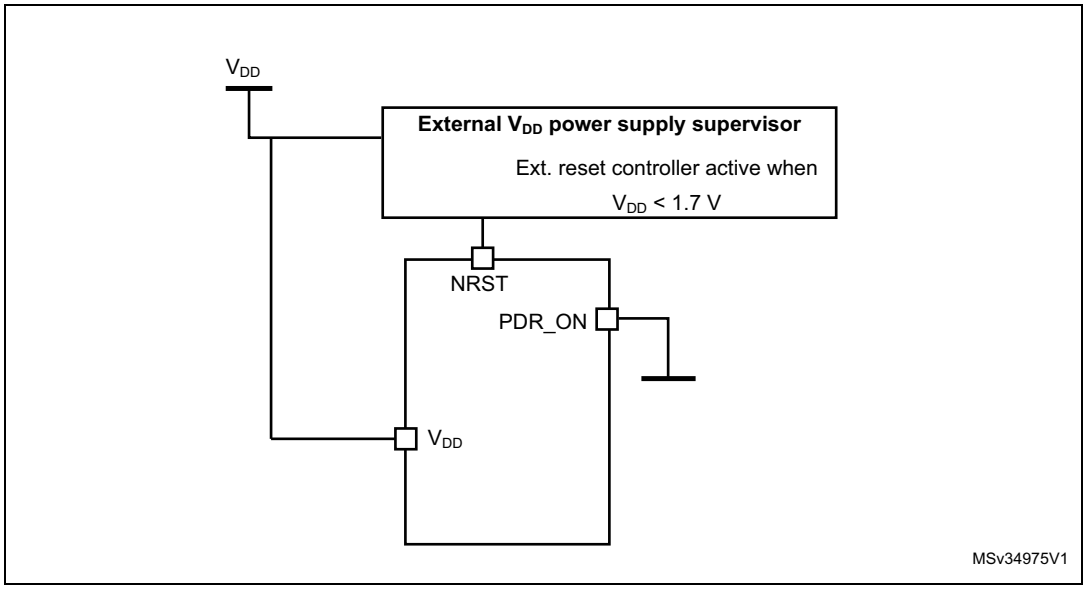
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available only on WLCSP64, UFBGA100, UFBGA144 and LQFP144 packages.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.19 Voltage regulator

The regulator has three operating modes:

– Main regulator mode (MR)
– Low power regulator (LPR)
– Power-down

3.19.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. The WLCSP64 is available in two versions, one with the regulator internally enabled and one with the regulator internally disabled. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run mode)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop mode

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the V_{CAP_1} and V_{CAP_2} pins. The V_{CAP_2} pin is only available for the 100 pins and 144 pins packages.

All packages have the regulator ON feature.

3.19.2 Regulator OFF

The regulator is disabled by holding BYPASS_REG pin high.

This feature is available only on UFBGA100 and UFBGA144 packages, which feature the BYPASS_REG pin. The WLCSP64 is available in two versions, one with a fixed enabled regulator and one with a fixed disabled regulator (see *Table 4: Regulator ON/OFF and internal power supply supervisor availability* and *Section 8: Ordering information*). The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

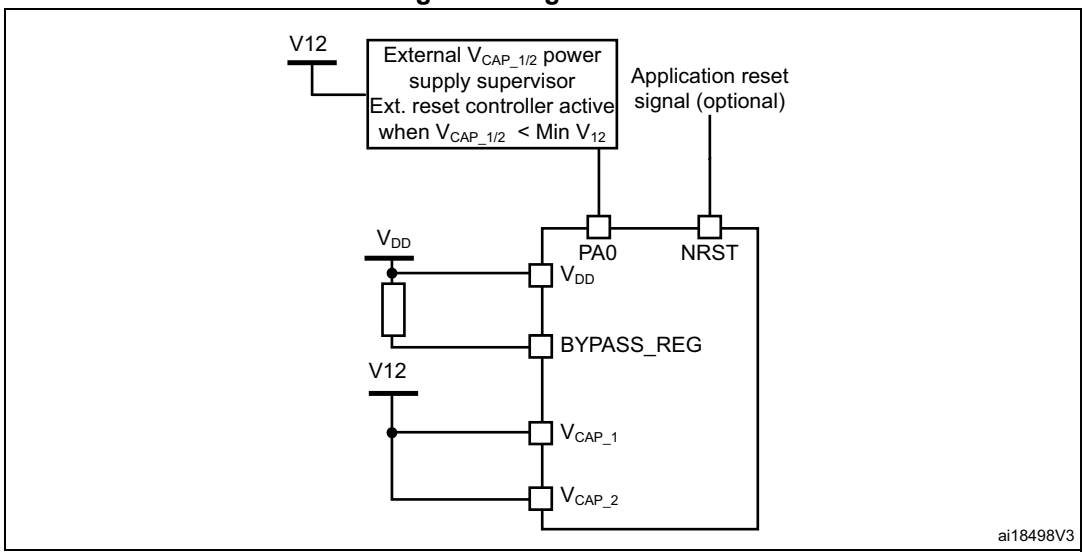
The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

Figure 8. Regulator OFF

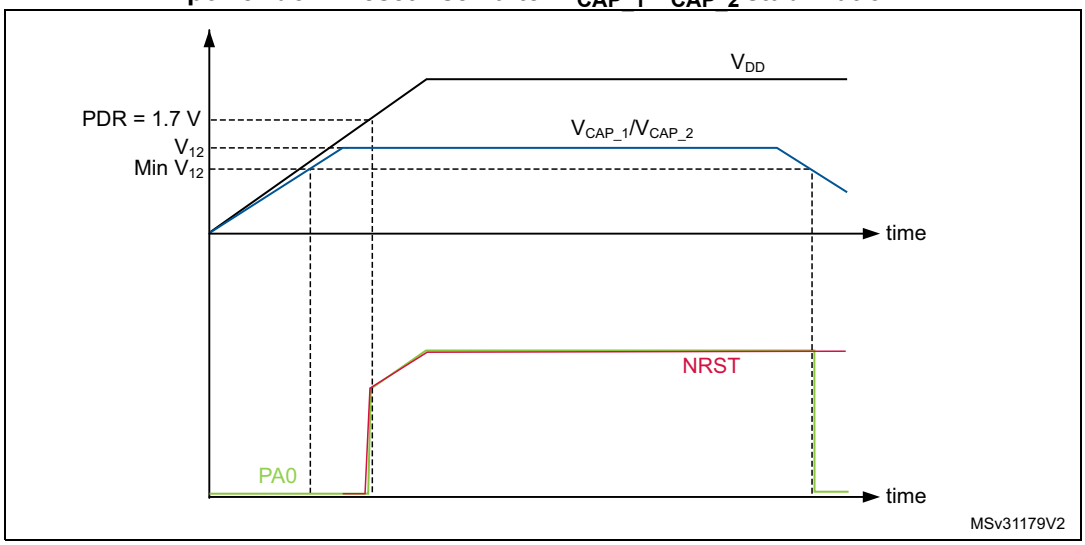


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

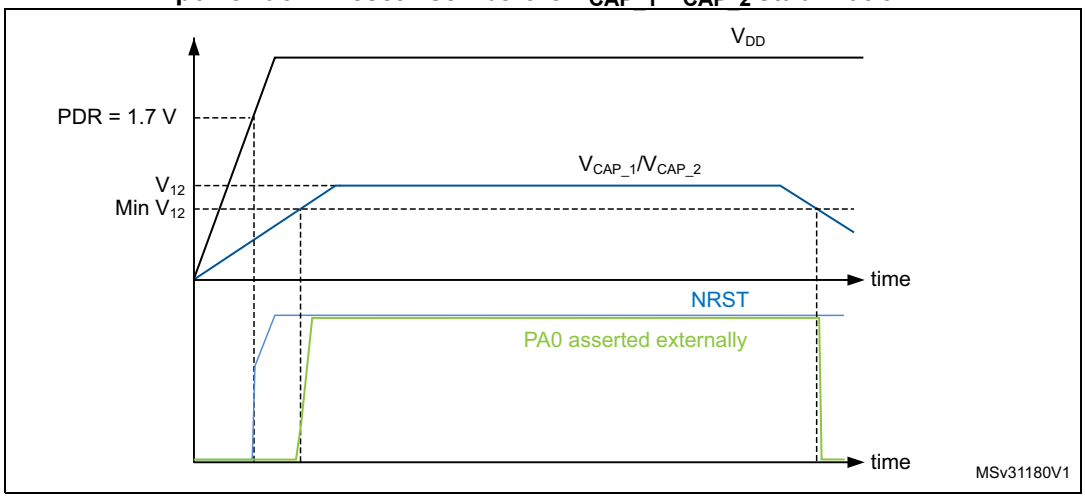
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

Figure 9. Startup in regulator OFF: slow V_{DD} slope power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

3.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP64	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
WLCSP64 option P(1)	No	Yes	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		
UFBGA144	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		

1. Refer to *Section 8: Ordering information*.

3.20 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset,

or when the device wakes up from the Standby mode (see *Section 3.21: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.22 V_{BAT} operation

The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal

Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.23 Timers and watchdogs

The devices embed two advanced-control timer, ten general-purpose timers, two basic timers, two watchdog timers and one SysTick timer.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control and general-purpose timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	50	100
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	50	100
Basic timers	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	50	100

3.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F412xE/G (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F412xE/G devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 15 input capture/output compare/PWMs

  TIM2. TIM3, TIM4 and TIM5 general-purpose timers can operate together or in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM output.

  TIM2. TIM3, TIM4 and TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13 and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13 and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM2. TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

3.23.3 Basic timer (TIM6, TIM7)

TIM6 and TIM7 timers are basic 16-bit timers. They support independent DMA request generation.

3.23.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.23.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.23.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.24 Inter-integrated circuit interface (I^2C)

The devices feature up to four I^2C bus interfaces which can operate in multimaster and slave modes:

- One I^2C interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Three I^2C interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All I^2C interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.25 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6).

These four interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. USART1 and USART6 interfaces are able to communicate at speeds of up to 12.5 Mbit/s. USART2 and USART3 interfaces communicate at up to 6.25 bit/s.

All USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 7. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)
USART2	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
USART3 (1)	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
USART6	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)

1. The RX is not available for the UFQFPN48 package.

3.26 Serial peripheral interface (SPI)

The devices feature five SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4 and SPI5 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interfaces can be configured to operate in TI mode for communications in master mode and slave mode.

3.27 Inter-integrated sound (I^2S)

Five standard I^2S interfaces (multiplexed with SPI1 to SPI5) are available. They can be operated in master or slave mode, in simplex communication mode, and full duplex mode for I2S2 and I2S3. All I^2S interfaces can be configured to operate with a 16-/32-bit resolution as an input or output channel. I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx interfaces can be served by the DMA controller.

3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

Different sources can be selected for the I2S master clock of the APB1 and the I2S master clock of the APB2. This gives the flexibility to work with two different audio sampling frequencies. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or Codec output)

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

3.29 Digital filter for sigma-delta modulators (DFSDM)

The device embeds one DFSDM with 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 2 internal parallel inputs support.

The amount of filters defines the number of conversions which can be performed simultaneously.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 4 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0...20 MHz
- alternative inputs from 4 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 2 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1...5), oversampling ratio (up to 1...1024)
  - integrator: oversampling ratio (1...256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM1FLT0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable $Sinc^x$ digital filter (order = 1...3, oversampling ratio = 1...32
  - input from digital output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1...256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit input serial channel clock absence
- "regulator" or injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority.

3.30 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.31 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 byte of SRAM are allocated for each CAN.

3.32 Universal serial bus on-the-go full-speed (USB_OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The Battery Charging Detection (BCD) can detect and identify the type of port, it is connected to (standard USB or charger). The type of charging is also detected: Dedicated Charging Port (DCP), Charging Downstream Port (CDP) and Standard Downstream Port (SDP). Some packages provide a dedicated USB power rail allowing a different supply for the USB and for the rest of the chip. For instance the chip can be powered with the minimum specified supply and the USB running at the level defined by the standard. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Link power management (LPM)
- Battery charging detection (BCD) supporting DCP, CDP, and SDP (battery charging specification revision 1.2)

3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.38 Embedded Trace Macrocell™

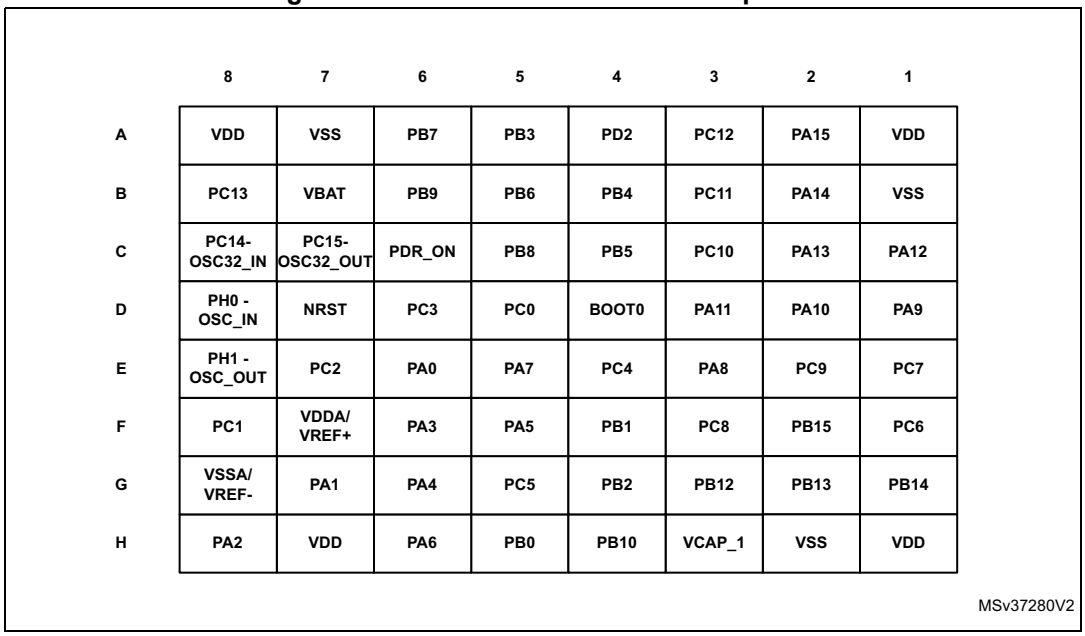
The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F412xE/G through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

4.1 WLSCP64 pinout description

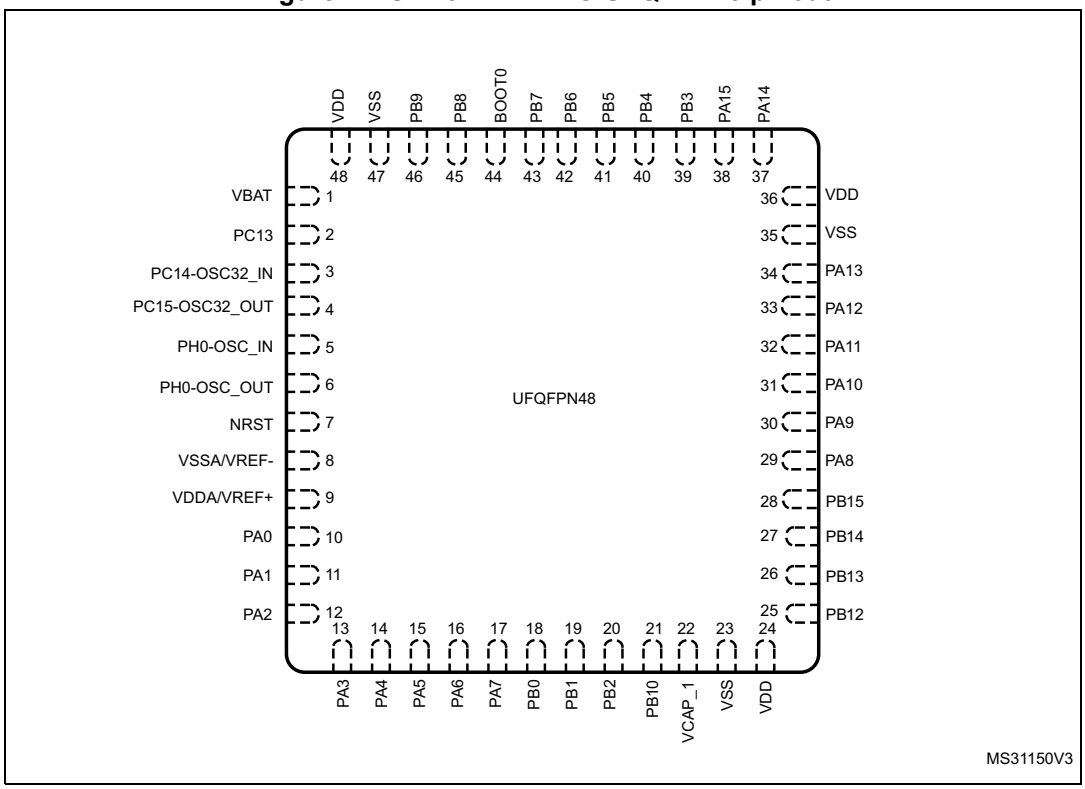
Figure 11. STM32F412xE/G WLCSP64 pinout



1. The above figure shows the package bump side.

4.2 UFQFPN48 pinout description

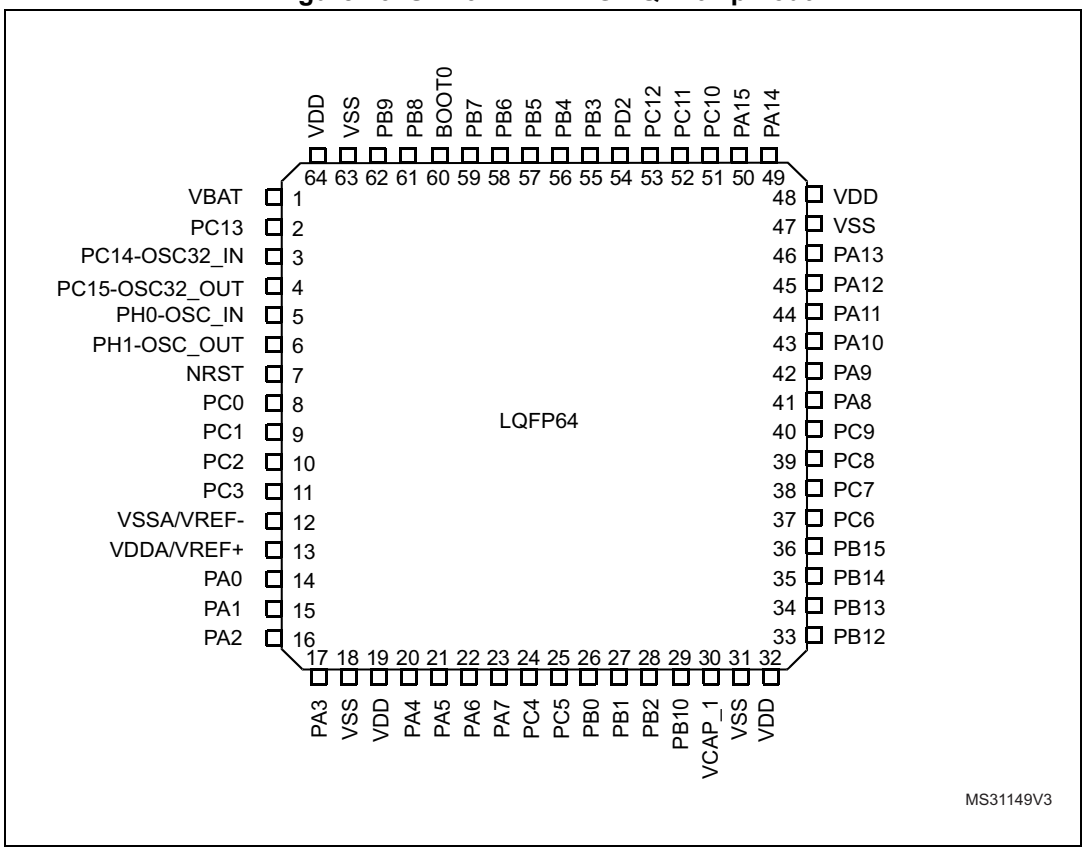
Figure 12. STM32F412xE/G UFQFPN48 pinout



1. The above figure shows the package top view.

4.3 LQFP64 pinout description

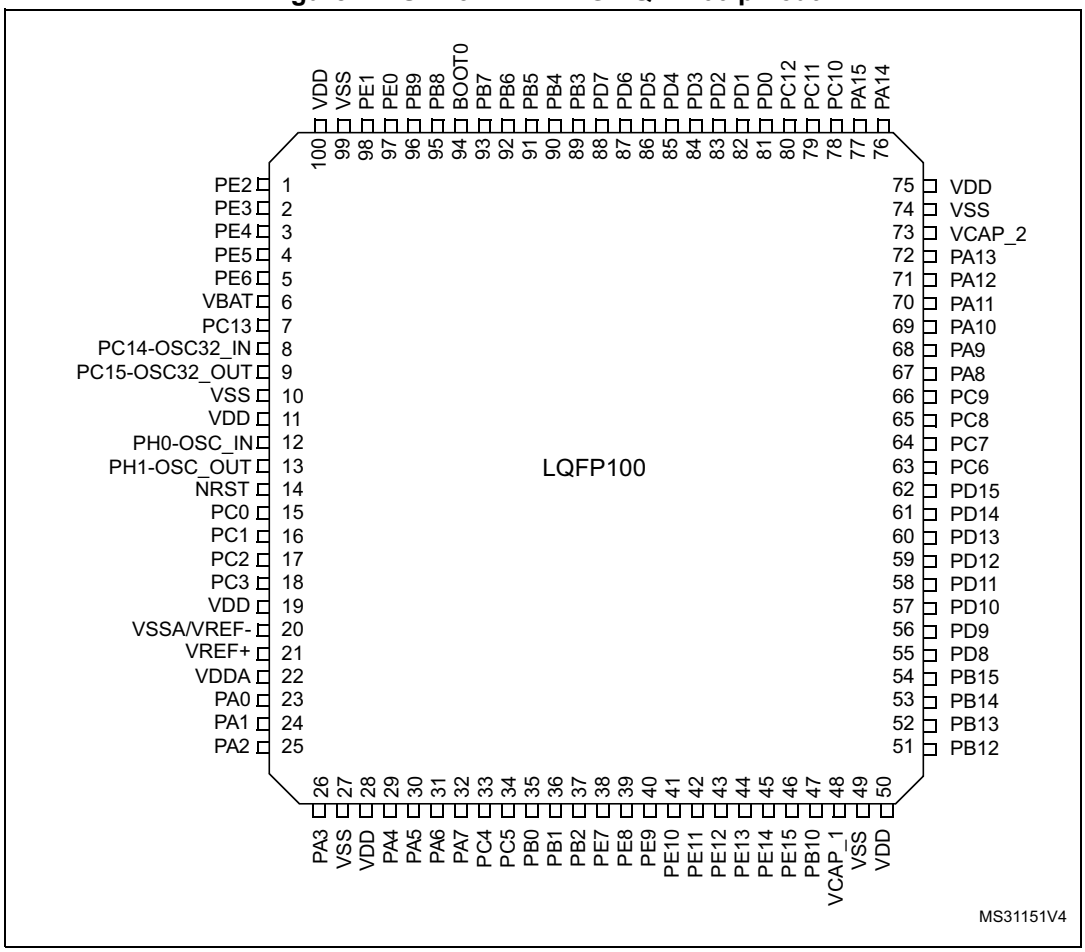
Figure 13. STM32F412xE/G LQFP64 pinout



1. The above figure shows the package top view.

4.4 LQFP100 pinout description

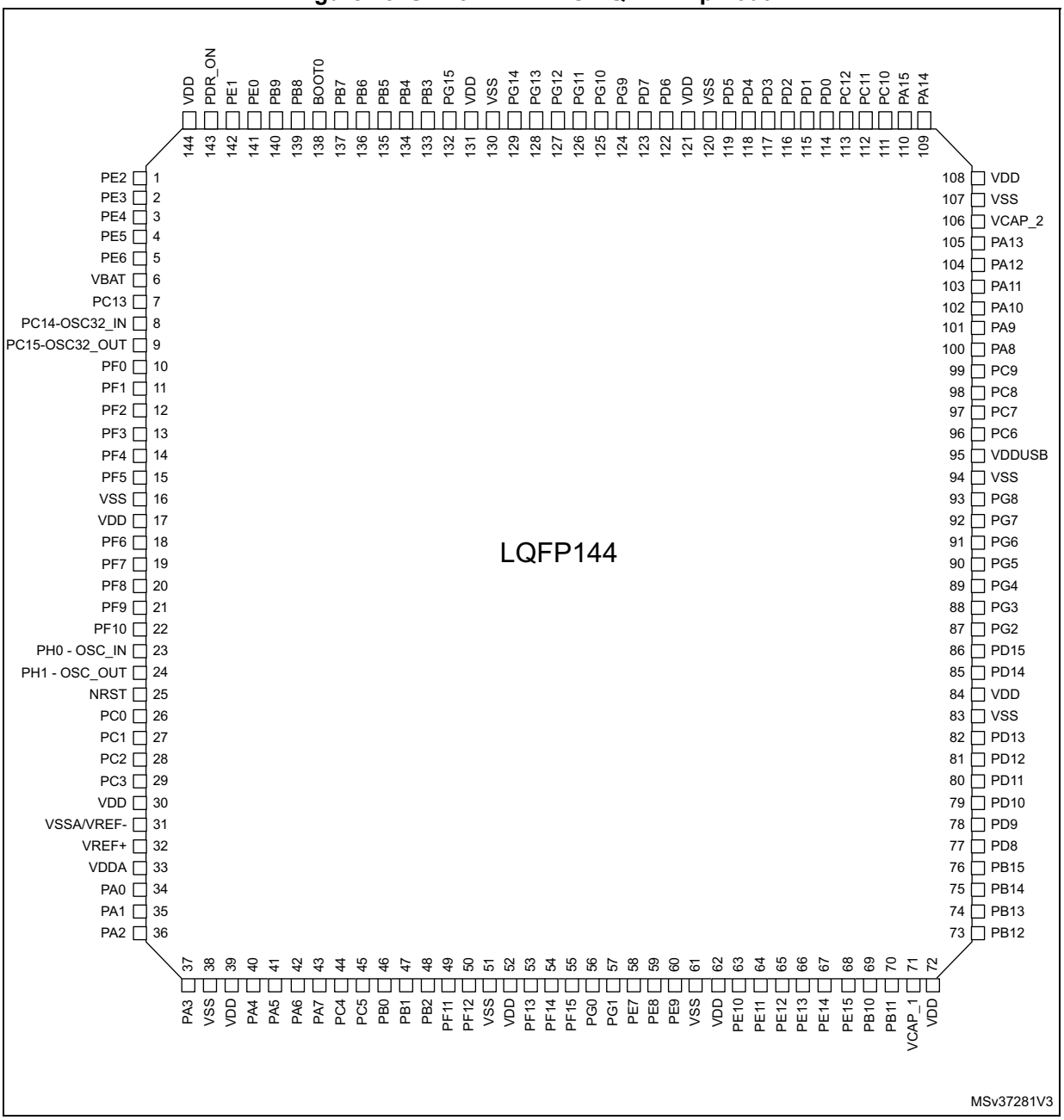
Figure 14. STM32F412xE/G LQFP100 pinout



1. The above figure shows the package top view.

4.5 LQFP144 pinout description

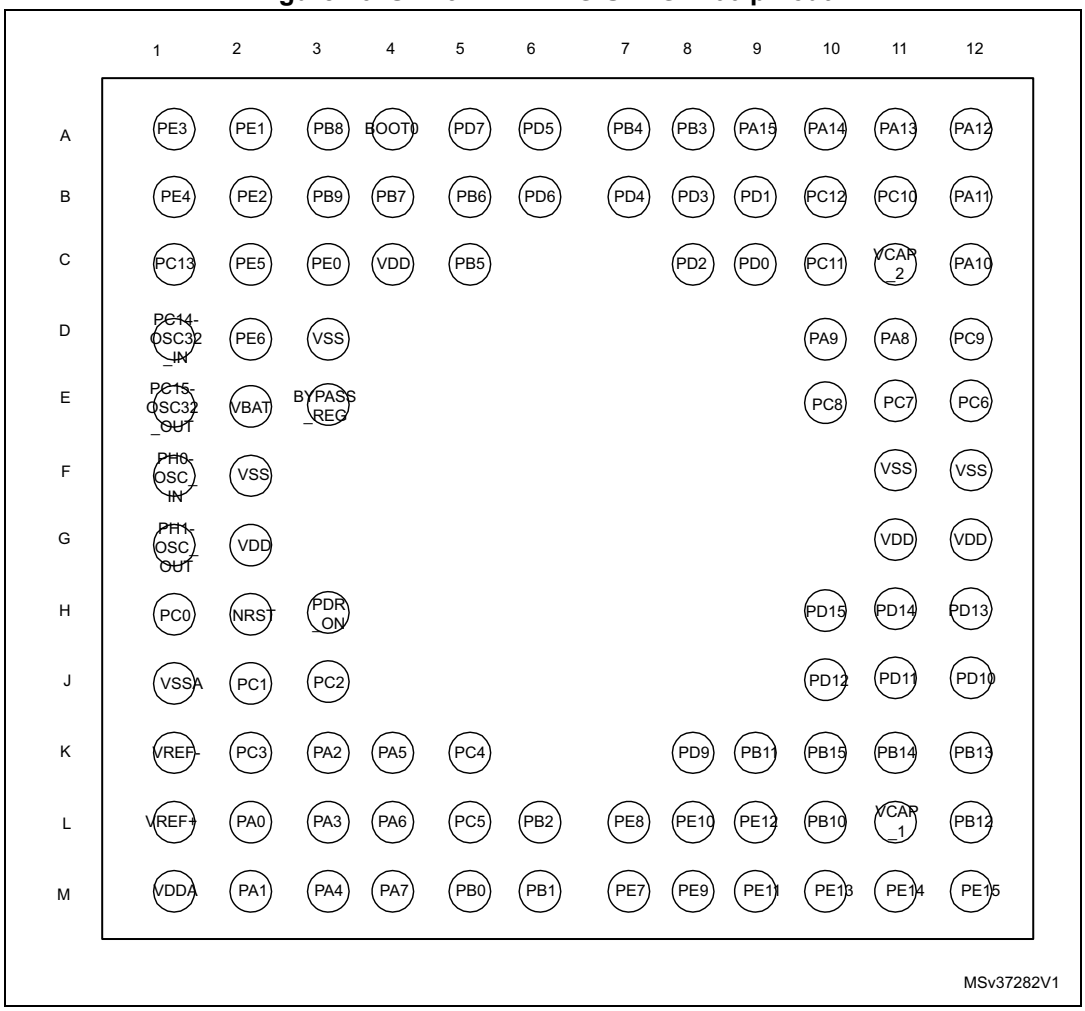
Figure 15. STM32F412xE/G LQFP144 pinout



1. The above figure shows the package top view.

4.6 UFBGA100 pinout description

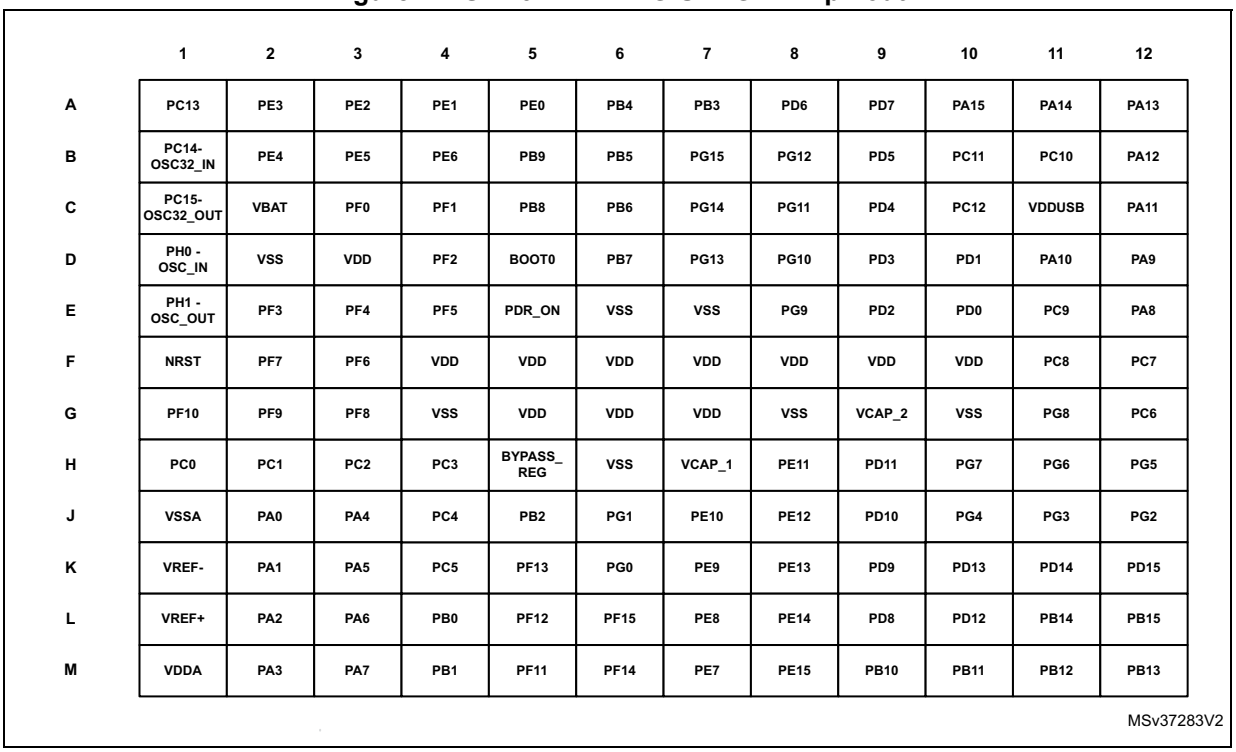
Figure 16. STM32F412xE/G UFBGA100 pinout



1. The above figure shows the package top view.

4.7 UFBGA144 pinout description

Figure 17. STM32F412xE/G UFBGA144 pinout



	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	PG7	PG6	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv37283V2

1. The above figure shows the package top view.

4.8 Pin definition

Table 8. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	

Table 8. Legend/abbreviations used in the pinout table (continued)

Name	Abbreviation	Definition
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32F412xE/G pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	1	B2	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, QUADSPI_BK1_IO2, FSMC_A23, EVENTOUT	-
-	-	-	2	A1	A2	2	PE3	I/O	FT	-	TRACED0, FSMC_A19, EVENTOUT	-
-	-	-	3	B1	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	-	4	C2	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	-	5	D2	B4	5	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_A22, EVENTOUT	-
1	1	B7	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	B8	7	C1	A1	7	PC13	I/O	FT	(2)(3)	EVENTOUT	TAMP_1
3	3	C8	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(2)(3)(4)	EVENTOUT	OSC32_IN

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
4	4	C7	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(2)(4)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-
-	-	-	-	-	E4	15	PF5	I/O	FT	-	TIM5_CH3, FSMC_A5, EVENTOUT	-
-	-	-	10	F2	D2	16	VSS	S	-	-	-	-
-	-	-	11	G2	D3	17	VDD	S	-	-	-	-
-	-	-	-	-	F3	18	PF6	I/O	FT	-	TRACED0, TIM10_CH1, QUADSPI_BK1_IO3, EVENTOUT	-
-	-	-	-	-	F2	19	PF7	I/O	FT	-	TRACED1, TIM11_CH1, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	G3	20	PF8	I/O	FT	-	TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	G2	21	PF9	I/O	FT	-	TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	G1	22	PF10	I/O	FT	-	TIM1_ETR, TIM5_CH4, EVENTOUT	-
5	5	D8	12	F1	D1	23	PH0 - OSC_IN	I/O	FT	(4)	EVENTOUT	OSC_IN
6	6	E8	13	G1	E1	24	PH1 - OSC_OUT	I/O	FT	(4)	EVENTOUT	OSC_OUT
7	7	D7	14	H2	F1	25	NRST	I/O	RST	-	-	NRST

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	8	D5	15	H1	H1	26	PC0	I/O	FT	-	EVENTOUT	ADC1_10, WKUP2
-	9	F8	16	J2	H2	27	PC1	I/O	FT	-	EVENTOUT	ADC1_11, WKUP3
-	10	E7	17	J3	H3	28	PC2	I/O	FT	-	SPI2_MISO, I2S2ext_SD, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT	ADC1_12
-	11	D6	18	K2	H4	29	PC3	I/O	FT	-	SPI2_MOSI/I2S2_SD, FSMC_A0, EVENTOUT	ADC1_13
-	-	-	19	-	-	30	VDD	S	-	-	-	-
8	12	G8	20	-	-	31	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	J1	J1	-	VSSA	S	-	-	-	-
-	-	-	-	K1	K1	-	VREF-	S	-	-	-	-
9	13	F7	-	-	-	-	VDDA/ VREF+	S	-	-	-	-
-	-	-	21	L1	L1	32	VREF+	S	-	-	-	-
-	-	-	22	M1	M1	33	VDDA	S	-	-	-	-
10	14	E6	23	L2	J2	34	PA0	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, EVENTOUT	ADC1_0, WKUP1
11	15	G7	24	M2	K2	35	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, QUADSPI_BK1_IO3, EVENTOUT	ADC1_1
12	16	H8	25	K3	L2	36	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4/FSMC_DA4, EVENTOUT	ADC1_2

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
13	17	F6	26	L3	M2	37	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, FSMC_D5/FSMC_DA5, EVENTOUT	ADC1_3
-	18	-	27	-	G4	38	VSS	S	-	-	-	-
-	-	-	-	E3	H5	-	BYPASS_REG	I	FT	-	-	-
-	19	H7	28	-	F4	39	VDD	S	-	-	-	-
14	20	G6	29	M3	J3	40	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6/FSMC_DA6, EVENTOUT	ADC1_4
15	21	F5	30	K4	K3	41	PA5	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7/FSMC_DA7, EVENTOUT	ADC1_5
16	22	H6	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_6
17	23	E5	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_7
-	24	E4	33	K5	J4	44	PC4	I/O	FT	-	I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_14

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	25	G5	34	L5	K4	45	PC5	I/O	FT	-	I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_15
18	26	H5	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
19	27	F4	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_9
20	28	G4	37	L6	J5	48	PB2	I/O	FT	-	DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-
-	-	-	-	-	M6	54	PF14	I/O	FT	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FT	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, FSMC_A11, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	38	M7	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-
-	-	-	39	L7	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, QUADSPI_BK2_IO1, FSMC_D5/FSMC_DA5, EVENTOUT	-
-	-	-	40	M8	K7	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, QUADSPI_BK2_IO2, FSMC_D6/FSMC_DA6, EVENTOUT	-
-	-	-	-	-	-	61	VSS	S	-	-	-	-
-	-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FSMC_D7/FSMC_DA7, EVENTOUT	-
-	-	-	42	M9	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, FSMC_D8/FSMC_DA8, EVENTOUT	-
-	-	-	43	L9	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, FSMC_D9/FSMC_DA9, EVENTOUT	-
-	-	-	44	M10	K8	66	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SPI5_MISO, FSMC_D10/FSMC_DA10, EVENTOUT	-
-	-	-	45	M11	L8	67	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_D11/FSMC_DA11, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	46	M12	M8	68	PE15	I/O	FT	-	TIM1_BKIN, FSMC_D12/FSMC_DA12, EVENTOUT	-
21	29	H4	47	L10	M9	69	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, USART3_TX, I2CFMP1_SCL, SDIO_D7, EVENTOUT	-
-	-	-	-	K9	M10	70	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, I2S2_CKIN, USART3_RX, EVENTOUT	-
22	30	H3	48	L11	H7	71	VCAP_1	S	-	-	-	-
23	31	H2	49	F12	H6	-	VSS	S	-	-	-	-
24	32	H1	50	G12	G7	72	VDD	S	-	-	-	-
25	33	G3	51	L12	M11	73	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, USART3_CK, CAN2_RX, DFSDM1_DATIN1, FSMC_D13/FSMC_DA13, EVENTOUT	-
26	34	G2	52	K12	M12	74	PB13	I/O	FT	-	TIM1_CH1N, I2CFMP1_SMBA, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, USART3_CTS, CAN2_TX, DFSDM1_CKIN1, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
27	35	G1	53	K11	L11	75	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0/FSMC_DA0, SDIO_D6, EVENTOUT	-
28	36	F2	54	K10	L12	76	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	-	55	-	L9	77	PD8	I/O	FT	-	USART3_TX, FSMC_D13/ FSMC_DA13, EVENTOUT	-
-	-	-	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	-	57	J12	J9	79	PD10	I/O	FT	-	USART3_CK, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	-	58	J11	H9	80	PD11	I/O	FT	-	I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	-	59	J10	L10	81	PD12	I/O	FT	-	TIM4_CH1, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	60	H12	K10	82	PD13	I/O	FT	-	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	-	61	H11	K11	85	PD14	I/O	FT	-	TIM4_CH3, I2CFMP1_SCL, FSMC_D0/FSMC_DA0, EVENTOUT	-
-	-	-	62	H10	K12	86	PD15	I/O	FT	-	TIM4_CH4, I2CFMP1_SDA, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-			
-	-	-	-	-	C11	95	VDDUSB	S	-	-	-	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	37	F1	63	E12	G12	96	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT	-
-	38	E1	64	E11	F12	97	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-
-	39	F3	65	E10	F11	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT	-
-	40	E2	66	D12	E11	99	PC9	I/O	FT	-	MCO_2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S2_CKIN, QUADSPI_BK1_IO0, SDIO_D1, EVENTOUT	-
29	41	E3	67	D11	E12	100	PA8	I/O	FT	-	MCO_1, TIM1_CH1, I2C3_SCL, USART1_CK, USB_FS_SOF, SDIO_D1, EVENTOUT	-
30	42	D1	68	D10	D12	101	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	-
31	43	D2	69	C12	D11	102	PA10	I/O	FT	-	TIM1_CH3, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
32	44	D3	70	B12	C12	103	PA11	I/O	FT	-	TIM1_CH4, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, EVENTOUT	-
33	45	C1	71	A12	B12	104	PA12	I/O	FT	-	TIM1_ETR, SPI5_MISO, USART1_RTS, USART6_RX, CAN1_TX, USB_FS_DP, EVENTOUT	-
34	46	C2	72	A11	A12	105	PA13	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	-	-	73	C11	G9	106	VCAP_2	S	-	-	-	-
35	47	B1	74	F11	G10	107	VSS	S	-	-	-	-
36	48	-	75	G11	-	-	VDD	S	-	-	-	-
-	-	A1	-	-	F9	108	VDD	S	-	-	-	-
37	49	B2	76	A10	A11	109	PA14	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
38	50	A2	77	A9	A10	110	PA15	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, EVENTOUT	-
-	51	C3	78	B11	B11	111	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT	-
-	52	B3	79	C10	B10	112	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, QUADSPI_BK2_NCS, FSMC_D2/FSMC_DA2, SDIO_D3, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	53	A3	80	B10	C10	113	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, FSMC_D3/FSMC_DA3, SDIO_CK, EVENTOUT	-
-	-	-	81	C9	E10	114	PD0	I/O	FT	-	CAN1_RX, FSMC_D2/FSMC_DA2, EVENTOUT	-
-	-	-	82	B9	D10	115	PD1	I/O	FT	-	CAN1_TX, FSMC_D3/FSMC_DA3, EVENTOUT	-
-	54	A4	83	C8	E9	116	PD2	I/O	FT	-	TIM3_ETR, FSMC_NWE, SDIO_CMD, EVENTOUT	-
-	-	-	84	B8	D9	117	PD3	I/O	FT	-	TRACED1, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, QUADSPI_CLK, FSMC_CLK, EVENTOUT	-
-	-	-	85	B7	C9	118	PD4	I/O	FT	-	DFSDM1_CKIN0, USART2_RTS, FSMC_NOE, EVENTOUT	-
-	-	-	86	A6	B9	119	PD5	I/O	FT	-	USART2_TX, FSMC_NWE, EVENTOUT	-
-	-	-	-	-	E7	120	VSS	S	-	-	-	-
-	-	-	-	-	F7	121	VDD	S	-	-	-	-
-	-	-	87	B6	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, DFSDM1_DATIN1, USART2_RX, FSMC_NWAIT, EVENTOUT	-
-	-	-	88	A5	A9	123	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, FSMC_NE1, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	E8	124	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FSMC_NE2, EVENTOUT	-
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FT	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-
40	56	B4	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
41	57	C4	91	C5	B6	135	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SDIO_D3, EVENTOUT	-
42	58	B5	92	B5	C6	136	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D0, EVENTOUT	-
43	59	A6	93	B4	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	D4	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C5	95	A3	C5	139	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, CAN1_RX, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	B6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	A5	141	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, EVENTOUT	-
-	-	-	98	A2	A4	142	PE1	I/O	FT	-	FSMC_NBL1, EVENTOUT	-
47	63	A7	99	D3	E6	-	VSS	S	-	-	-	-
-	-	C6	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A8	100	C4	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.

2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).

3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F412xE/Greference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 10. FSMC pin definition

Pins	FSMC		64 pins	100 pins	144 pins
	LCD/NOR/PSRAM/SRAM	NOR/PSRAM Mux			
PE2	A23	A23	-	Yes	Yes
PE3	A19	A19	-	Yes	Yes
PE4	A20	A20	-	Yes	Yes
PE5	A21	A21	-	Yes	Yes
PE6	A22	A22	-	Yes	Yes
PF0	A0	-	-	-	Yes
PF1	A1	-	-	-	Yes
PF2	A2	-	-	-	Yes
PF3	A3	-	-	-	Yes
PF4	A4	-	-	-	Yes
PF5	A5	-	-	-	Yes
PC2	NWE	NWE	Yes	Yes	Yes
PC3	A0	-	Yes	Yes	Yes
PA2	D4	DA4	Yes	Yes	Yes
PA3	D5	DA5	Yes	Yes	Yes
PA4	D6	DA6	Yes	Yes	Yes
PA5	D7	DA7	Yes	Yes	Yes
PC4	NE4	NE4	Yes	Yes	Yes
PC5	NOE	NOE	Yes	Yes	Yes
PF12	A6	-	-	-	Yes
PF13	A7	-	-	-	Yes
PF14	A8	-	-	-	Yes
PF15	A9	-	-	-	Yes
PG0	A10	-	-	-	Yes
PG1	A11	-	-	-	Yes
PE7	D4	DA4	-	Yes	Yes
PE8	D5	DA5	-	Yes	Yes
PE9	D6	DA6	-	Yes	Yes

Table 10. FSMC pin definition

Pins	FSMC		64 pins	100 pins	144 pins
	LCD/NOR/PSRAM/SRAM	NOR/PSRAM Mux			
PE10	D7	DA7	-	Yes	Yes
PE11	D8	DA8	-	Yes	Yes
PE12	D9	DA9	-	Yes	Yes
PE13	D10	DA10	-	Yes	Yes
PE14	D11	DA11	-	Yes	Yes
PE15	D12	DA12	-	Yes	Yes
PB12	D13	DA13	Yes	Yes	Yes
PB14	D0	DA0	Yes	Yes	Yes
PD8	D13	DA13	-	-	Yes
PD9	D14	DA14	-	Yes	Yes
PD10	D15	DA15	-	Yes	Yes
PD11	A16	A16	-	Yes	Yes
PD12	A17	A17	-	Yes	Yes
PD13	A18	A18	-	Yes	Yes
PD14	D0	DA0	-	Yes	Yes
PD15	D1	DA1	-	Yes	Yes
PG2	A12	-	-	-	Yes
PG3	A13	-	-	-	Yes
PG4	A14	-	-	-	Yes
PG5	A15	-	-	-	Yes
PC6	D1	DA1	Yes	Yes	Yes
PC11	D2	DA2	Yes	Yes	Yes
PC12	D3	DA3	Yes	Yes	Yes
PD0	D2	DA2	-	Yes	Yes
PD1	D3	DA3	-	Yes	Yes
PD2	NWE	NWE	Yes	Yes	Yes
PD3	CLK	CLK	-	Yes	Yes
PD4	NOE	NOE	-	Yes	Yes
PD5	NWE	NEW	-	Yes	Yes
PD6	NWAIT	NWAIT	-	Yes	Yes
PD7	NE1	NE1	-	Yes	Yes
PG9	NE2	NE2	-	-	Yes
PG10	NE3	NE3	-	-	Yes

Table 10. FSMC pin definition

Pins	FSMC		64 pins	100 pins	144 pins
	LCD/NOR/PSRAM/SRAM	NOR/PSRAM Mux			
PG12	A24	A24	-	-	Yes
PG14	A25	A25	-	-	Yes
PB7	NL	NL	Yes	Yes	Yes
PE0	NBL0	NBL0	-	Yes	Yes
PE1	NBL1	NBL1	-	Yes	Yes

Table 11. STM32F412xE/G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI/I 2S4_SD	-	USART2_RTS	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_TX	-	-	-	FSMC_D4	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_RX	-	-	-	FSMC_D5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2 S1_WS	SPI3_NSS/ I2S3_WS	USART2_CK	DFSDM1_ DATIN1	-	-	FSMC_D6	EVENTOUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/ I2S1_CK	-	-	DFSDM1_ CKIN1	-	-	FSMC_D7	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	I2S2_MCK	-	-	TIM13_ CH1	QUADSPI_ BK2_IO0	SDIO_CMD	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I 2S1_SD	-	-	-	TIM14_ CH1	QUADSPI_ BK2_IO1	-	EVENTOUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	USB_FS_ SOF	SDIO_D1	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_TX	-	-	USB_FS_ VBUS	SDIO_D2	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	SPI5_MOSI/ I2S5_SD	USART1_RX	-	-	USB_FS_ID	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	SPI4_MISO	USART1_CTS	USART6_ TX	CAN1_RX	USB_FS_DM	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	SPI5_MISO	USART1_RTS	USART6_ RX	CAN1_TX	USB_FS_DP	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART1_TX	-	-	-	-	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	SPI5_SCK/ I2S5_CK	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	SPI5_NSS/ I2S5_WS	-	DFSDM1_ DATIN0	QUADSPI_ CLK	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	DFSDM1_ CKIN0	-	-	QUADSPI_ CLK	-	-	EVENTOUT
	PB3	JTDO-SWO	TIM2_CH2			I2CFMP1_ SDA	SPI1_SCK/I2 S1_CK	SPI3_SCK/ I2S3_CK	USART1_RX	-	I2C2_SDA	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_ SD	-	I2C3_SDA	-	SDIO_D0	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I 2S1_SD	SPI3_MOSI/ I2S3_SD	-	-	CAN2_RX	-	SDIO_D3	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QUADSPI_ BK1_NCS	SDIO_D0	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	FSMC_NL	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	SPI5_MOSI/I2S 5_SD	-	CAN1_RX	I2C3_SDA	-	SDIO_D4	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-	CAN1_TX	I2C2_SDA	-	SDIO_D5	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/ I2S2_CK	I2S3_MCK	USART3_TX	-	I2CFMP1_ SCL	-	SDIO_D7	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_CKIN	-	USART3_RX	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/ I2S2_WS	SPI4_NSS/ I2S4_WS	SPI3_SCK/ I2S3_CK	USART3_ CK	CAN2_RX	DFSDM1_ DATIN1	FSMC_D13/F SMC_DA13	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2CFMP1_ SMBA	SPI2_SCK/ I2S2_CK	SPI4_SCK/ I2S4_CK	-	USART3_ CTS	CAN2_TX	DFSDM1_ CKIN1	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2CFMP1_ SDA	SPI2_MISO	I2S2ext_SD	USART3_ RTS	DFSDM1_ DATIN2	TIM12_CH1	FSMC_D0	SDIO_D6	EVENTOUT
	PB15	RTC_ 50Hz	TIM1_CH3N	-	TIM8_CH3N	I2CFMP1_ SCL	SPI2_MOSI/I 2S2_SD	-	-	DFSDM1_ CKIN2	TIM12_CH2	-	SDIO_CK	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	DFSDM1_ CKOUT	-	-	FSMC_NWE	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I 2S2_SD	-	-	-	-	-	FSMC_A0	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	-	-	QUADSPI_ BK2_IO2	FSMC_NE4	EVENTOUT
	PC5	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_RX	-	-	QUADSPI_ BK2_IO3	FSMC_NOE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_ SCL	I2S2_MCK	DFSDM1_ CKIN3	-	USART6_ TX	-	FSMC_D1	SDIO_D6	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_ SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	-	USART6_ RX	-	DFSDM1_ DATIN3	SDIO_D7	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_ CK	QUADSPI_ BK1_IO2	-	SDIO_D0	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	-	-	QUADSPI_ BK1_IO0	-	SDIO_D1	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_ BK1_IO1	-	SDIO_D2	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	-	QUADSPI_ BK2_NCS	FSMC_D2	SDIO_D3	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	-	-	FSMC_D3	SDIO_CK	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FSMC_D2/FSMC_DA2	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	FSMC_D3/FSMC_DA3	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	FSMC_NWE	SDIO_CMD	EVENTOUT
	PD3	TRACED1	-	-	-	-	SPI2_SCK/ I2S2_CK	DFSDM1_ DATIN0	USART2_ CTS	-	QUADSPI_ CLK	-	FSMC_CLK	EVENTOUT
	PD4	-	-	-	-	-	-	DFSDM1_ CKIN0	USART2_ RTS	-	-	-	FSMC_NOE	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	FSMC_NWE	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I 2S3_SD	DFSDM1_ DATIN1	USART2_RX	-	-	-	FSMC_ NWAIT	EVENTOUT
	PD7	-	-	-	-	-	-	DFSDM1_ CKIN1	USART2_CK	-	-	-	FSMC_NE1	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	FSMC_D13/ FSMC_DA13	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	FSMC_D14/ FSMC_DA14	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	FSMC_D15/ FSMC_DA15	EVENTOUT
	PD11	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_ CTS	-	QUADSPI_ BK1_IO0	-	FSMC_A16	EVENTOUT
	PD12	-	-	TIM4_CH1	-	I2CFMP1_ SCL			USART3_ RTS	-	QUADSPI_ BK1_IO1	-	FSMC_A17	EVENTOUT
	PD13	-	-	TIM4_CH2	-	I2CFMP1_ SDA	-	-	-	-	QUADSPI_ BK1_IO3	-	FSMC_A18	EVENTOUT
	PD14	-	-	TIM4_CH3	-	I2CFMP1_ SCL	-	-	-	-	-	-	FSMC_D0/ FSMC_DA0	EVENTOUT
	PD15	-	-	TIM4_CH4	-	I2CFMP1_ SDA	-	-	-	-	-	-	FSMC_D1/ FSMC_DA1	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	FSMC_NBL0	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	QUADSPI_ BK1_IO2	-	FSMC_A23	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	FSMC_A19	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	DFSDM1_ DATIN3	-	-	FSMC_A20	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SPI5_MISO	-	DFSDM1_ CKIN3	-	-	FSMC_A21	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_A22	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-	-	-	QUADSPI_ BK2_IO0	FSMC_D4/ FSMC_DA4	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_ CKIN2	-	-	-	QUADSPI_ BK2_IO1	FSMC_D5/ FSMC_DA5	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-	-	-	QUADSPI_ BK2_IO2	FSMC_D6/ FSMC_DA6	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	QUADSPI_ BK2_IO3	FSMC_D7/ FSMC_DA7	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	-	-		FSMC_D8/ FSMC_DA8	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	-	-	FSMC_D9/ FSMC_DA9	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	SPI5_MISO	-	-	-	-	FSMC_D10/ FSMC_DA10	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_D11/ FSMC_DA11	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	FSMC_D12/ FSMC_DA12	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	FSMC_A0	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	FSMC_A1	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	FSMC_A2	EVENTOUT
	PF3	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	FSMC_A3	EVENTOUT
	PF4	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	FSMC_A4	EVENTOUT
	PF5	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	FSMC_A5	EVENTOUT
	PF6	TRACED0	-	-	TIM10_CH1	-	-	-	-	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PF7	TRACED1	-	-	TIM11_CH1	-	-	-	-	-	QUADSPI_ BK1_IO2	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	QUADSPI_ BK1_IO0	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	QUADSPI_ BK1_IO1	-	EVENTOUT
	PF10	-	TIM1_ETR	TIM5_CH4	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF11	-	-	-	TIM8_ETR	-	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	FSMC_A6	EVENTOUT
	PF13	-	-	-	-	I2CFMP1_ SMBA	-	-	-	-	-	-	FSMC_A7	EVENTOUT
	PF14	-	-	-	-	I2CFMP1_ SCL	-	-	-	-	-	-	FSMC_A8	EVENTOUT
	PF15	-	-	-	-	I2CFMP1_ SDA	-	-	-	-	-	-	FSMC_A9	EVENTOUT

Table 11. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port G	PG0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FSMC_A10	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	FSMC_A11	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	QUADSPI_ BK1_NCS	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_ CK	-	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_ RX	QUADSPI_ BK2_IO2	-	FSMC_NE2	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE3	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	CAN2_RX	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_ RTS	CAN2_TX	-	FSMC_NE4	EVENTOUT
	PG13	TRACED2	-	-	-	-	-	-	-	USART6_ CTS	-	-	FSMC_A24	EVENTOUT
	PG14	TRACED3	-	-	-	-	-	-	-	USART6_ TX	QUADSPI_ BK2_IO3	-	FSMC_A25	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

5 Memory mapping

The memory map is shown in *Figure 18*.

Figure 18. Memory map

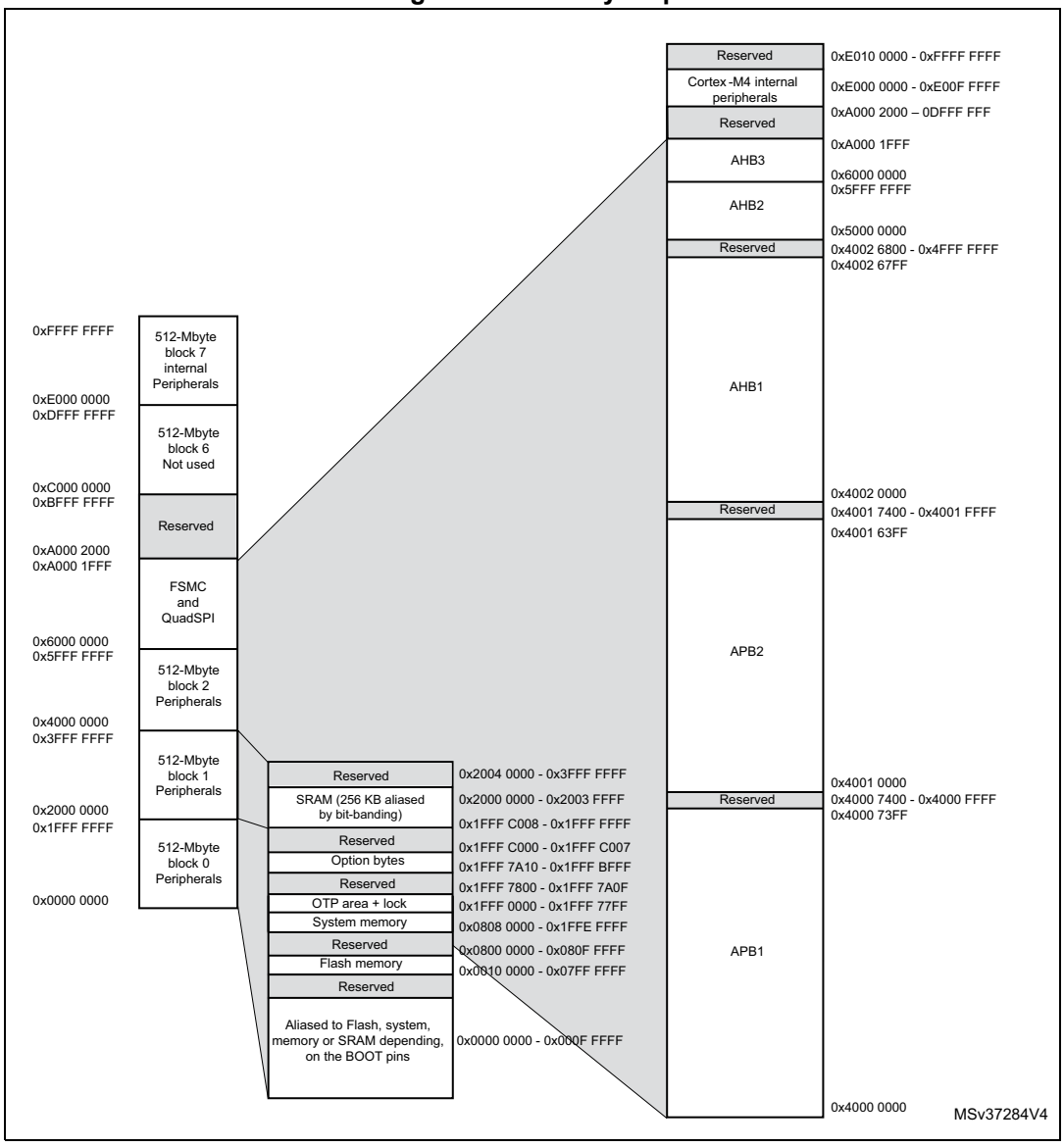


Table 12. STM32F412xE/G register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 0x5006 0BFF	RNG
	0x5004 000- 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 12. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6400- 0x4001 FFFF	Reserved
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5400 - 0x4001 5FFF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

Table 12. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB1	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800- 0x4000 6BFF	CAN2
	0x4000 6400- 0x4000 67FF	CAN1
	0x4000 6000- 0x4000 63FF	I2CFMP1
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 4C00 - 0x4000 53FF	Reserved
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC and BKP registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

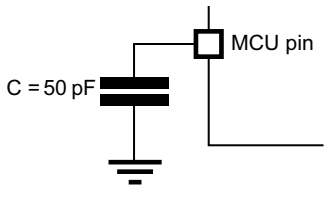
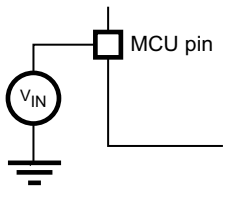
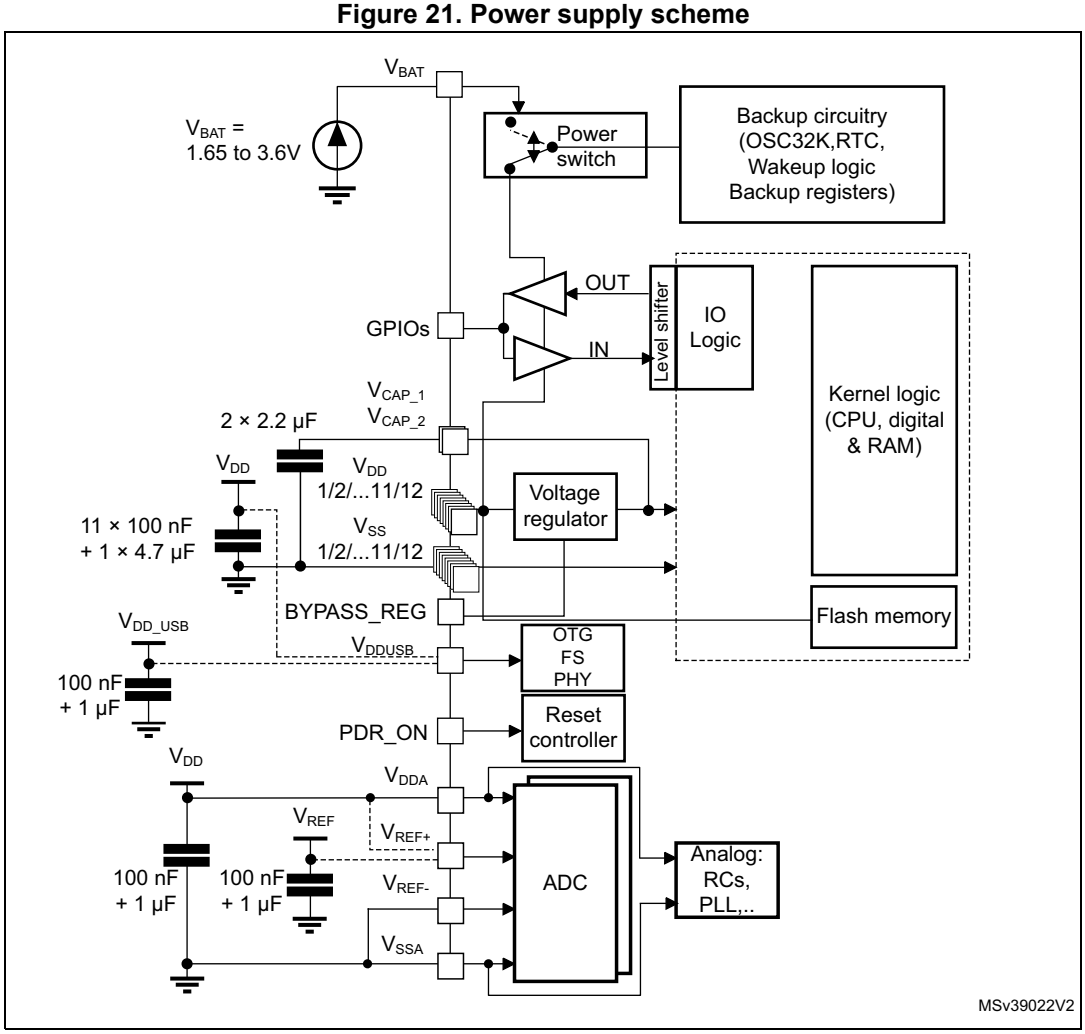


Figure 20. Input voltage measurement



6.1.6 Power supply scheme

Figure 21. Power supply scheme

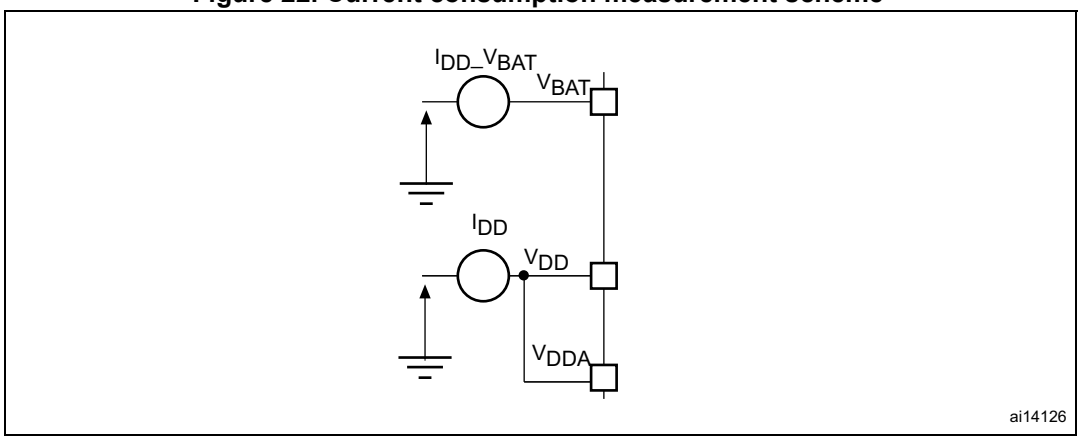


1. To connect PDR_ON pin, refer to Section: Power supply supervisor.
2. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
3. VCAP_2 pad is only available on 100-pin and 144-pin packages.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.
5. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. V_{DDUSB} value does not depend on the V_{DD} and V_{DDA} values, but it must be the last supply to be provided and the first to disappear.

Caution: Each power supply pair (for example V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{DDUSB} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT and TC pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 14* for the values of the maximum allowed injected current.

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	-160	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power lines (source)	25	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins(2)	-120	
$I_{INJ(PIN)}$ (3)	Injected current on FT and TC pins (4)	–5/+0	
	Injected current on NRST and B pins (4)		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP64, LQFP64/100/144, UFQFPN48, UFBGA100/144)	see note (1)	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

6.3 Operating conditions

6.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	-0.3	-	5.5	V
		$V_{DD} \le 2\ V$	-0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_D	Power dissipation at T_A = 85°C for range 6 or T_A = 105°C for range 7(8)	UFQFPN48	-	-	625	mW
		WLCSP64	-	-	392	
		LQFP64	-	-	425	
		LQFP100	-	-	465	
		LQFP144	-	-	571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	416	
P_D	Power dissipation at T_A = 125 °C for range 3(8)	UFQFPN48	-	-	156	
		WLCSP64	-	-	98	
		LQFP64	-	-	106	
		LQFP100	-	-	116	
		LQFP144	-	-	142	
		UFBGA100	-	-	88	
		UFBGA144	-	-	104	
T_A	Ambient temperature for range 6	Maximum power dissipation	-40	-	85	°C
		Low power dissipation(9)	-40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	-40	-	105	
		Low power dissipation(9)	-40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	-40	-	110	
		Low power dissipation(9)	-40	-	130	
T_J	Junction temperature range	Range 6	-40	-	105	
		Range 7	-40	-	125	
		Range 3	-40	-	130	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 72: ADC characteristics*.
3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF}+ < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB}. For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required.

   (some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 17. Features depending on the operating power supply range

Operating power supply range	ADC operation	Maximum flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum flash memory access frequency with wait states (1)(2)	I/O operation	Clock output frequency on I/O pins(3)	Possible flash memory operations
V_{DD} =1.7 to 2.1 V(4)	Conversion time up to 1.2 Msps	16 MHz(5)	100 MHz with 6 wait states	– No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	18 MHz	100 MHz with 5 wait states	– No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	100 MHz with 4 wait states	– I/O compensation works	up to 50 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(6)	Conversion time up to 2.4 Msps	30 MHz	100 MHz with 3 wait states	– I/O compensation works	– up to 100 MHz when V_{DD} = 3.0 to 3.6 V – up to 50 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

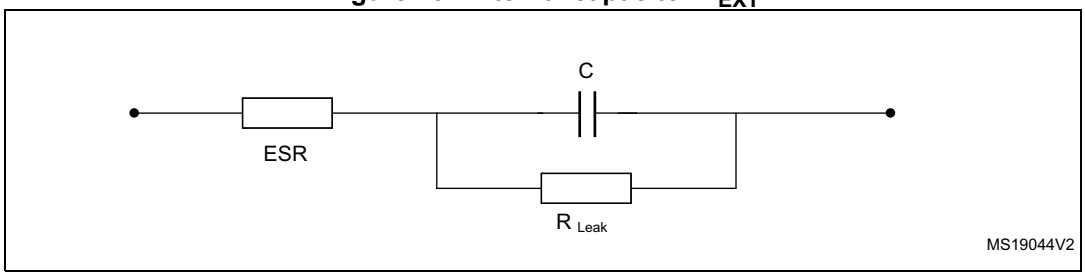
1. Applicable only when the code is executed from flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit flash memory, the number of wait states given here does not impact the execution speed from flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to *Table 59: I/O AC characteristics* for frequencies vs. external load.
4. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
5. Prefetch available over the complete VDD supply range.
6. The voltage range for the USB full speed embedded PHY can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

6.3.2 VCAP_1/VCAP_2 external capacitors

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 and VCAP_2 pins. For packages supporting only 1 VCAP pin, the 2 CEXT capacitors are replaced by a single capacitor.

C_{EXT} is specified in *Table 18*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 18. VCAP_1/VCAP_2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor with the pins VCAP_1 and VCAP_2 available	2.2 µF
ESR	ESR of external capacitor with the pins VCAP_1 and VCAP_2 available	< 2 Ω
CEXT	Capacitance of external capacitor with a single VCAP pin available	4.7 µF
ESR	ESR of external capacitor with a single VCAP pin available	< 1 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Note: This feature is only available for UFBGA100 and UFBGA144 packages.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage at 3.3V.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60(1)	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	

Table 21. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(2)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(2)(3)	POR reset timing	-	0.5	1.5	3.0	ms
I_{RUSH}(2)	In-Rush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(2)	In-Rush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 125 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 17: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	28.1	30.24	31.27	32.21	34.21	mA
			84	22.7	24.05	24.54	25.11	26.74	
			64	15.7	16.99	17.47	18.03	19.71	
			50	12.3	13.36	13.82	14.36	15.51	
			25	6.5	7.44	7.82	8.30	8.96	
			20	5.6	6.16	6.66	7.20	7.77	
		HSI, PLL off, all peripherals enabled(2)(3)	16	3.9	4.70	5.31	6.08	6.57	
			1	0.6	0.78	1.33	1.98	2.14	
		External clock, PLL ON, all peripherals disabled(3)	100	14.0	15.48	16.08	16.83	18.51	
			84	11.3	12.23	12.75	13.41	16.09	
			64	7.9	8.84	9.31	10.01	11.61	
			50	6.2	7.06	7.53	8.19	9.50	
			25	3.4	4.18	4.61	5.13	5.95	
			20	2.9	3.44	3.98	4.65	5.39	
		HSI, PLL off, all peripherals disabled(3)	16	2.0	2.51	3.13	3.89	4.51	
			1	0.5	0.64	1.21	1.90	2.21	

1. Based on characterization, not tested in production unless otherwise specified
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	28.4	28.80(3)	30.84	32.39	34.40(3)	mA
			84	23.0	24.09(3)	25.20	26.57	28.30(3)	
			64	16.0	16.83(3)	17.77	19.12	20.90(3)	
			50	12.6	13.46	13.98	14.68	15.85	
			25	6.8	7.63	8.14	8.61	9.30	
			20	5.8	6.31	6.74	7.43	8.03	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	3.9	4.65	5.33	6.11	6.60	
			1	0.6	0.78	1.34	2.00	2.16	
		External clock, PLL ON, all peripherals disabled(2)	100	14.3	15.09(3)	16.22	17.90	19.72(3)	
			84	11.6	12.28(3)	13.36	14.99	16.80(3)	
			64	8.2	8.75(3)	9.68	11.21	13.00(3)	
			50	6.5	7.21	7.69	8.47	9.74	
			25	3.6	4.22	4.68	5.29	6.08	
			20	3.2	3.65	4.18	4.94	5.68	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.0	2.48	3.12	3.94	4.54	
			1	0.5	0.65	1.26	1.94	2.24	

1. Based on characterization, not tested in production unless otherwise specified
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	26.9	28.78	29.86	31.30	33.08	mA
			84	21.6	23.14	23.93	24.89	26.31	
			64	15.0	16.08	16.70	17.46	18.45	
			50	11.8	12.74	13.33	14.07	14.87	
			25	6.3	7.13	7.69	8.30	8.77	
			20	5.5	6.09	6.64	7.30	7.72	
		HSI, PLL OFF, all peripherals enabled(2)	16	3.9	4.20	4.78	5.49	5.81	
			1	0.9	0.98	1.50	2.20	2.33	
		External clock, PLL ON(4) all peripherals disabled(2)	100	12.7	13.82	14.71	15.76	17.53	
			84	10.3	11.20	11.97	12.96	14.41	
			64	7.2	7.87	8.57	9.41	10.47	
			50	5.7	6.33	7.02	7.87	8.75	
			25	3.2	3.77	4.38	5.13	5.71	
			20	2.9	3.31	3.93	4.69	5.22	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.1	2.25	2.83	3.56	3.96	
			1	0.7	0.83	1.42	2.12	2.36	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 45* and RM0402 for the possible PLL VCO setting

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	27.2	28.70(4)	30.14	31.98	33.80	mA
			84	21.9	23.60	24.31	25.37	26.82	
			64	15.2	16.45	17.03	17.87	18.89	
			50	12.1	13.12	13.67	14.46	15.29	
			25	6.6	7.59	8.12	8.77	9.27	
			20	5.7	6.51	7.07	7.77	8.21	
		HSI, PLL OFF, all peripherals enabled(3)	16	4.0	4.32	4.88	5.69	6.01	
			1	0.8	1.14	1.67	2.38	2.51	
		External clock, PLL ON(2) all peripherals disabled(3)	100	13.0	14.06(4)	15.34	17.27	19.20	
			84	10.5	11.21	12.16	13.47	14.98	
			64	7.5	8.29	9.01	9.88	10.99	
			50	6.0	6.73	7.32	8.27	9.20	
			25	3.5	4.18	4.73	5.57	6.19	
			20	3.1	3.72	4.25	5.10	5.67	
		HSI, PLL OFF, all peripherals disabled(3)	16	2.1	2.41	2.94	3.75	4.17	
			1	0.7	0.99	1.51	2.30	2.56	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 45* and RM0402 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. Tested in production.

Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	36.3	38.95	41.19	42.95	45.40	mA
			84	31.1	33.22	34.81	36.10	38.16	
			64	22.3	23.97	25.10	26.23	27.73	
			50	18.3	19.77	20.65	21.73	22.97	
			25	10.1	11.39	12.16	13.11	13.86	
			20	8.6	9.60	10.25	11.06	11.69	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.3	6.85	7.51	8.38	8.85	
			1	1.1	1.39	1.82	2.61	2.76	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.1	23.95	25.80	27.50	30.58	
			84	19.7	20.79	22.52	24.12	26.82	
			64	14.5	15.88	17.21	18.54	20.62	
			50	12.2	13.38	14.59	15.79	17.56	
			25	7.0	8.05	8.89	10.16	11.29	
			20	6.0	6.84	7.51	8.52	9.47	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.4	4.91	5.56	6.54	7.28	
			1	0.9	1.25	1.79	2.59	2.88	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 45* and RM0402 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	35.9	38.55	40.77	42.52	44.95	mA
			84	29.4	31.59	33.12	34.42	36.38	
			64	22.4	24.02	25.15	26.28	27.78	
			50	18.6	20.07	21.08	22.05	23.30	
			25	10.3	11.62	12.39	13.34	14.10	
			20	8.9	9.85	10.59	11.32	11.96	
		HSI, PLL OFF, all peripherals enabled(2)(3)	16	6.7	7.26	8.04	8.80	9.30	
			1	1.1	1.44	1.99	2.66	2.81	
		External clock, PLL ON(3) all peripherals disabled	100	21.7	23.55	25.48	27.07	30.10	
			84	18.0	19.16	20.93	22.39	24.89	
			64	14.6	15.93	17.32	18.59	20.68	
			50	12.5	13.63	14.90	16.07	17.87	
			25	7.2	8.25	9.26	10.26	11.41	
			20	6.3	7.15	7.99	8.84	9.83	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.9	5.37	6.20	7.03	7.82	
			1	1.0	1.30	1.91	2.65	2.95	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 28. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	38.9	41.10	42.85	44.28	46.80	mA
			84	32.8	34.61	35.77	36.72	38.81	
			64	23.6	24.96	25.84	26.64	28.16	
			50	18.7	19.90	20.67	21.45	22.67	
			25	10.1	11.11	11.70	12.40	13.10	
			20	8.6	9.46	10.07	10.81	11.43	
		HSI, PLL OFF, all peripherals enabled	16	6.3	6.77	7.42	8.21	8.68	
			1	1.1	1.35	1.84	2.59	2.74	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.11	27.59	28.84	32.07	
			84	21.4	22.22	23.53	24.66	27.42	
			64	15.8	16.80	17.90	18.99	21.12	
			50	12.6	13.51	14.52	15.54	17.28	
			25	7.0	7.85	8.57	9.39	10.44	
			20	6.0	6.67	7.37	8.26	9.19	
		HSI, PLL OFF, all peripherals disabled	16	4.5	4.80	5.47	6.33	7.04	
			1	0.9	1.25	1.81	2.58	2.87	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(2), External clock, PLL ON, Flash deep power down	100	17.7	18.48(3)	19.83	21.70	24.00	mA
			84	14.3	15.39	16.31	17.48	19.34	
			64	10.0	10.71	11.35	12.13	13.41	
			50	7.9	8.53	9.13	9.89	10.94	
			25	4.4	4.99	5.46	6.11	6.75	
			20	4.0	4.42	4.95	5.64	6.23	
		All peripherals enabled(2), HSI, PLL OFF, Flash deep power down	16	2.7	2.83	3.47	4.21	4.66	
			1	0.5	0.68	1.25	1.92	2.12	
		All peripherals enabled(2), External clock, PLL ON Flash ON	100	18.1	19.39	20.70	22.24	24.59	
			84	14.7	15.80	16.71	17.92	19.82	
			64	10.3	11.02	11.66	12.45	13.77	
			50	8.2	8.88	9.53	10.26	11.35	
			25	4.7	5.30	5.82	6.53	7.23	
			20	4.2	4.67	5.18	5.90	6.53	
		All peripherals enabled(2), HSI, PLL OFF, Flash ON	16	2.7	3.10	3.72	4.50	4.98	
			1	0.8	0.93	1.50	2.18	2.41	
		All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	3.2	3.42	4.98	6.88	9.70	
			84	2.6	3.09	3.63	4.44	6.26	
			64	2.0	2.33	2.81	3.46	4.87	
			50	1.7	2.02	2.54	3.12	4.39	
			25	1.2	1.63	2.21	2.89	4.08	
			20	1.3	1.62	2.09	2.78	3.92	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.5	0.63	1.24	1.92	2.71	
			1	0.4	0.53	1.14	1.82	2.57	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	3.6	4.17	4.84	5.63	7.93	
			84	3.0	3.49	4.13	4.88	6.88	
			64	2.3	2.69	3.23	3.85	5.42	
			50	2.0	2.33	2.83	3.45	4.86	
			25	1.4	1.88	2.39	3.06	4.31	
			20	1.5	1.88	2.43	3.06	4.31	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.8	0.91	1.50	2.22	3.13	
			1	0.7	0.78	1.37	2.09	2.95	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. Tested in production.

Table 30. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	External clock, PLL ON, Flash deep power down, all peripherals enabled(2)	100	17.3	18.62	19.90	21.40	23.67	mA
			84	14.0	15.08	16.04	17.16	18.97	
			64	9.7	10.41	11.02	11.80	13.06	
			50	7.6	8.27	8.89	9.62	10.64	
			25	4.2	4.79	5.35	6.00	6.63	
			20	3.7	4.11	4.67	5.31	5.88	
		HSI, PLL OFF(2), Flash deep power down, all peripherals enabled	16	2.4	2.81	3.45	4.20	4.64	
			1	0.5	0.67	1.27	1.91	2.11	
		External clock, PLL ON(2) all peripherals enabled, Flash ON	100	17.8	19.08	20.35	21.90	24.22	
			84	14.4	15.49	16.42	17.59	19.46	
			64	10.0	10.76	11.43	12.18	13.47	
			50	7.9	8.58	9.19	9.94	10.99	
			25	4.4	4.99	5.54	6.21	6.87	
			20	4.0	4.42	4.95	5.64	6.23	
		HSI, PLL OFF(2), all peripherals enabled, Flash ON	16	2.7	3.09	3.75	4.49	4.97	
			1	0.8	0.93	1.52	2.18	2.41	
I_{DD}	Supply current in **Sleep mode**	All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	2.9	3.51	4.14	4.90	5.59	mA
			84	2.4	2.83	3.46	4.16	4.74	
			64	1.7	2.08	2.59	3.18	3.63	
			50	1.4	1.77	2.23	2.84	3.24	
			25	1.0	1.37	1.88	2.50	2.85	
			20	1.3	1.37	1.88	2.50	2.85	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.5	0.63	1.23	1.91	2.18	
			1	0.4	0.52	1.13	1.81	2.07	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	3.3	3.22	3.98	4.90	5.59	
			84	2.8	2.62	3.30	4.16	4.74	
			64	2.1	1.89	2.50	3.18	3.63	
			50	1.7	1.58	2.16	2.84	3.24	
			25	1.2	1.28	1.82	2.50	2.85	
			20	1.3	1.28	1.82	2.50	2.85	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.8	0.88	1.36	1.91	2.18	
			1	0.7	0.77	1.26	1.81	2.07	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 31. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions	Parameter	Typ(1)	Max(1)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	121.1	168.0	648.7	1213.0	2970.0	µA
		Low power regulator usage	50.8	74.8	651.3	1328.0	2730.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	79.1	122.0	609.1	1181.0	2540.0	
		Low power regulator usage	22.4	74.7	631.9	1286.0	2680.0	
		Low power low voltage regulator usage	18.5	40.0	548.3	1145.0	2480.0	

1. Based on characterization, not tested in production.

Table 32. Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V

Symbol	Conditions	Parameter	Typ	Max(1)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	124.0	179.0(2)	907.2	1762.0	3000.0(2)	µA
		Low power regulator usage	52.8	75.0(2)	757.6	1559.0	2750.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	87.6	123.0	698.5	1374.0	2550.0	
		Low power regulator usage	26.2	74.7	737.2	1515.0	2700.0	
		Low power low voltage regulator usage	20.1	40.0(2)	619.1	1299.0	2500.0(2)	

1. Based on characterization, not tested in production.
2. Tested in production.

Table 33. Typical and maximum current consumption in Standby mode - V_{DD}= 1.7 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	1.8	3.7	12.9	23.7	50.7	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	2.6	4.5	13.7	24.5	51.6	
		RTC and LSE OFF	1.1	3.0	12.2	23	50.0	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Based on characterization, not tested in production unless otherwise specified.

Table 34. Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	3.7	5.4	17.2	31.2	62.3	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	4.5	6.2	18.0	32.0	63.2	
		RTC and LSE OFF	2.6	4.0	16.0	30.0	61.0(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, not tested in production unless otherwise specified.
3. Tested in production.

Table 35. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions(1)	Typ				Max(2)			Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V			
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.87	1.04	1.11	3.0	5.0	10.0	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.52	1.70	1.97	2.09	3.8	5.8	11.6	
		RTC and LSE OFF	0.04	0.04	0.05	0.05	2.0	4.0	8.0	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization, not tested in production.

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)

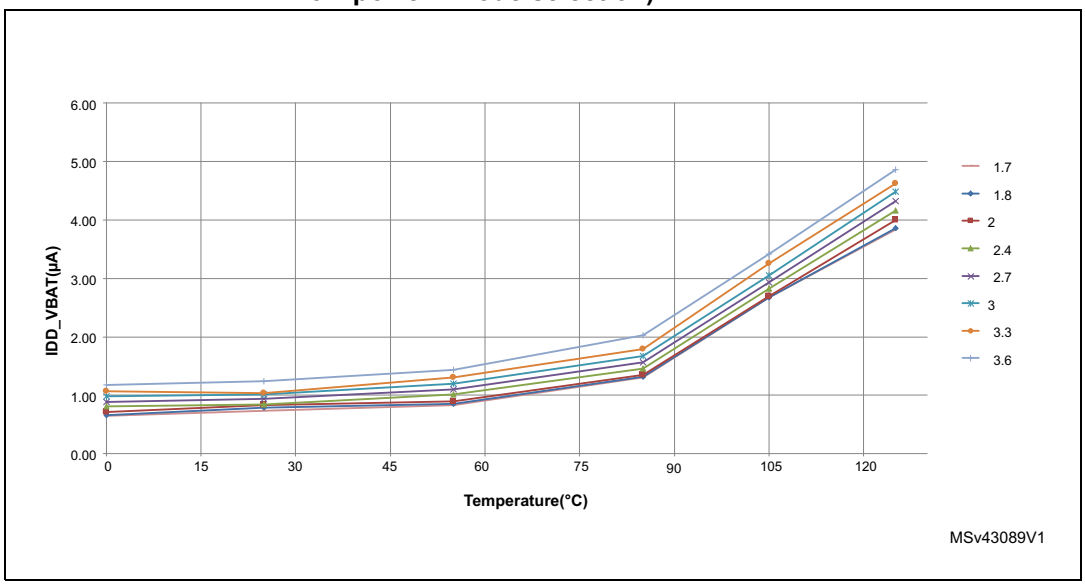
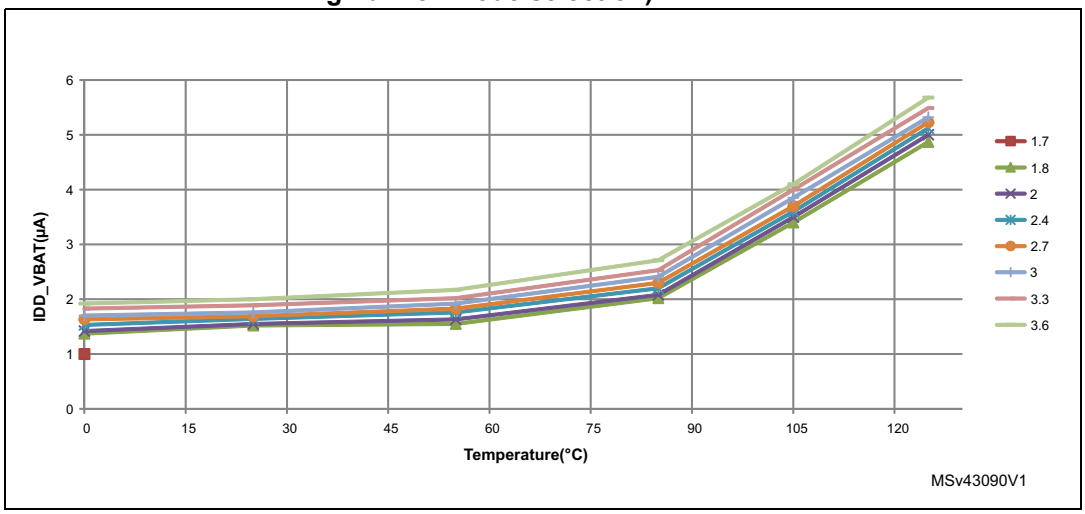


Figure 25. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 57: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 37: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 36. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 37. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.84	1.75	1.55	µA/MHz
	GPIOB	1.90	1.80	1.61	
	GPIOC	1.77	1.67	1.50	
	GPIOD	1.67	1.58	1.42	
	GPIOE	1.75	1.67	1.48	
	GPIOF	1.65	1.56	1.39	
	GPIOG	1.65	1.56	1.39	
	GPIOH	0.62	0.57	0.53	
	CRC	0.26	0.25	0.22	
	DMA1(1)	1,71N+2,98	1,62N+2,87	1,45N+2,58	
	DMA2(1)	1,78N+2,62	1,70N+2.53	1,52N+2.26	
AHB2	RNG	0.77	0.74	0.66	
	USB_OTG_FS	19.68	18.73	16.78	
AHB3	FSMC	5.36	5.11	4.56	
	QSPI	9.99	9.51	8.53	

Table 37. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB1	AHB-APB1 bridge	1.10	1.00	0.94	µA/MHz
	TIM2	13.62	12.95	11.59	
	TIM3	10.56	10.05	8.97	
	TIM4	10.72	10.21	9.12	
	TIM5	13.46	12.83	11.47	
	TIM6	2.92	2.79	2.47	
	TIM7	2.72	2.60	2.31	
	TIM12	6.22	5.93	5.28	
	TIM13	4.70	4.48	3.97	
	TIM14	4.60	4.38	3.91	
	WWDG	1.76	1.67	1.47	
	SPI2/I2S2	4.04	3.83	3.41	
	SPI3/I2S3	4.26	4.05	3.62	
	USART2	4.42	4.19	3.75	
	USART3	4.44	4.21	3.75	
	I2C1	4.32	4.10	3.66	
	I2C2	4.36	4.17	3.69	
	I2C3	4.36	4.14	3.69	
	I2CFMP1	5.96	5.69	5.06	
	CAN1	6.18	5.90	5.25	
	CAN2	5.86	5.52	4.97	
	PWR	1.82	1.69	1.56	

Table 37. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB2	AHB-APB2 bridge	0.09	0.07	0.08	µA/MHz
	TIM1	6.83	6.46	5.81	
	TIM8	6.63	6.29	5.63	
	USART1	3.31	3.11	2.80	
	USART6	3.21	3.02	2.73	
	ADC1	3.51	3.31	2.98	
	SDIO	3.74	3.51	3.17	
	SPI1	1.47	1.36	1.23	
	SPI4	1.56	1.45	1.31	
	SYSCFG	0.54	0.49	0.45	
	TIM9	3.09	2.92	2.63	
	TIM10	1.91	1.79	1.61	
	TIM11	1.93	1.81	1.64	
	SPI5	1.54	1.44	1.30	
	DFSDM1	4.25	4.02	3.61	
Bus Matrix		3.23	3.06	2.73	

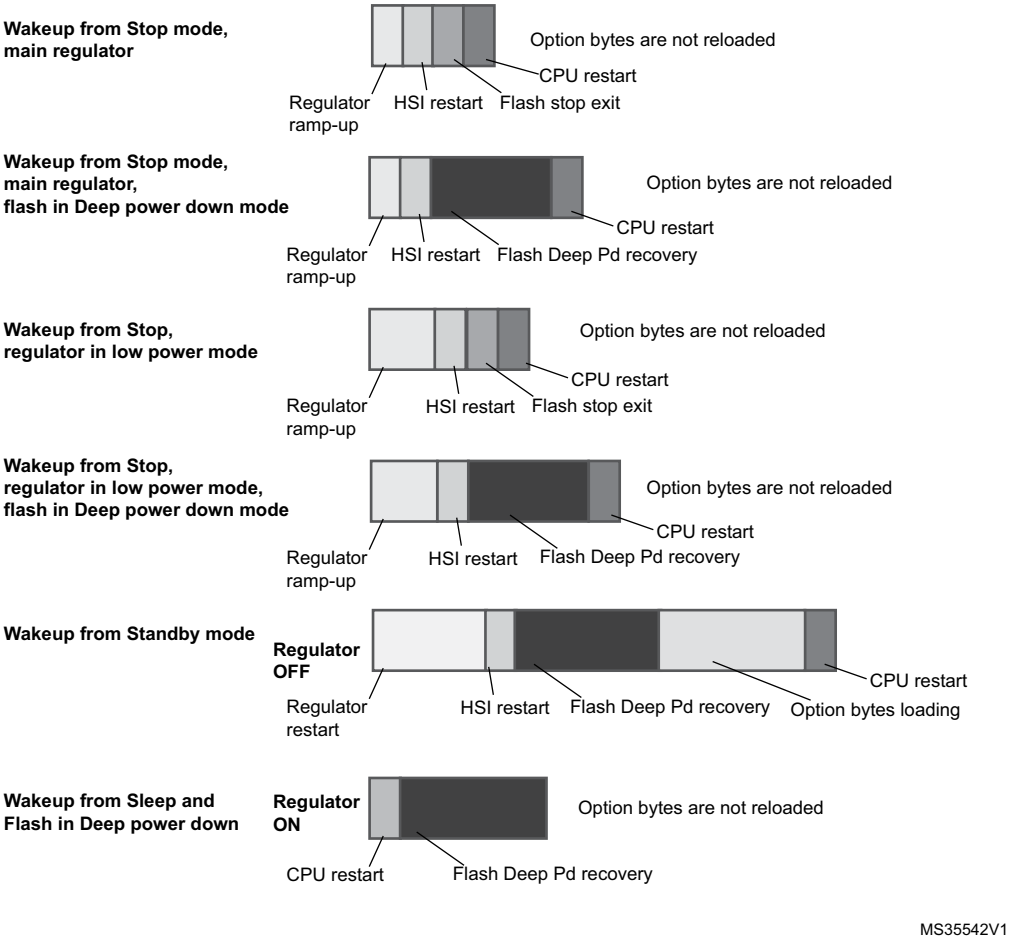
1. N is the number of stream enable (1...8).

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 38* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

Figure 26. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 38. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	-	4	6	clk cycles
$t_{WUSLEEPFDSM}$		Flash memory in Deep power down mode	-	-	50.0	µs
t_{WUSTOP}	Wakeup from STOP mode Code execution on flash memory	Main regulator	-	12.9	15.0	µs
		Main regulator, flash memory in Deep power down mode	-	104.9	120.0	
		Wakeup from Stop mode, regulator in low power mode(2)	-	20.8	28.0	
		Regulator in low power mode, flash memory in Deep power down mode(2)	-	112.9	130.0	
t_{WUSTOP}	Wakeup from STOP mode code execution on RAM(3)	Main regulator with flash memory in Stop mode or Deep power down	-	4.9	7.0	
		Wakeup from Stop mode, regulator in low power mode and the flash memory in Stop mode or Deep power down(2)	-	12.8	20.0	
$t_{WUSTDBY}$	Wakeup from Standby mode	-	-	316.8	400.0	
$t_{WUFLASH}$	Wakeup of flash memory	From Flash_Stop mode	-		11.0	
		From Flash Deep power down mode	-		50.0	

1. Guaranteed by characterization, not tested in production.
2. The specification is valid for wakeup from regulator in low power mode or low power low voltage mode, since the timing difference is negligible.
3. For the faster wakeup time for code execution on RAM, the flash memory must be in STOP or DeepPower Down mode (see reference manual RM0402).

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 57*. However, the recommended clock input waveform is shown in *Figure 27*.

The characteristics given in *Table 39* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 39. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 57*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 40* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 40. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 27. High-speed external clock source AC timing diagram

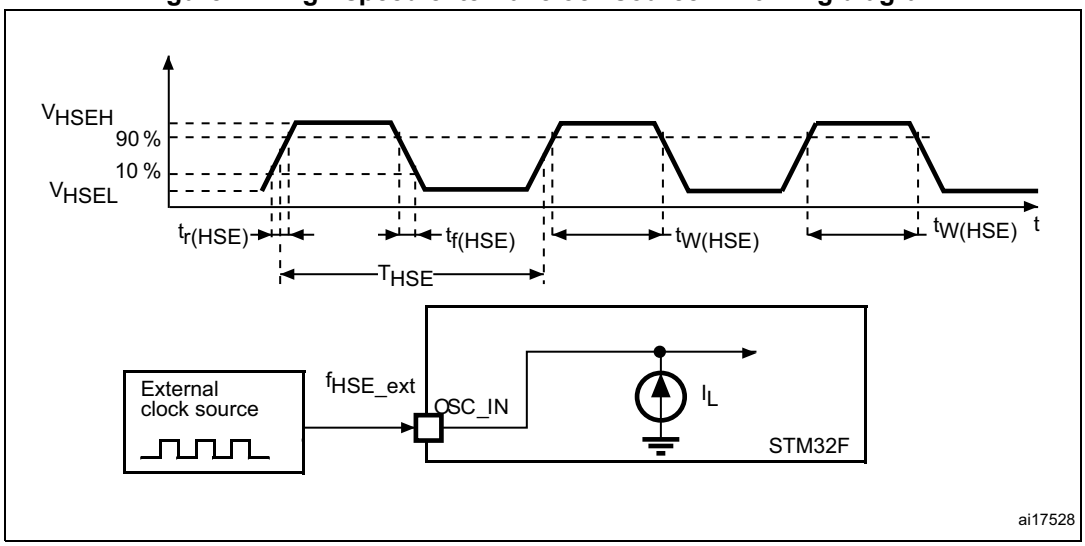
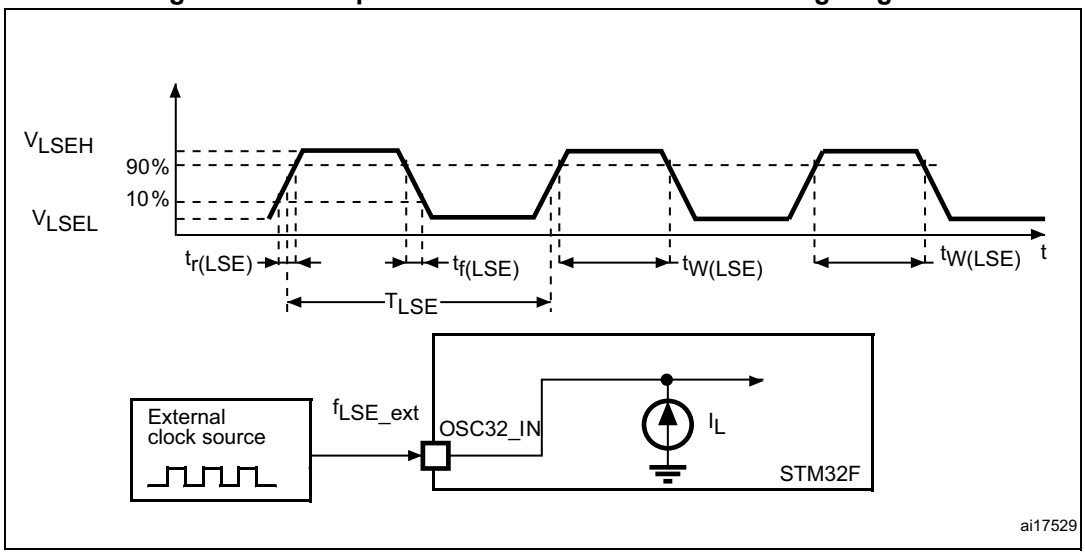


Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. HSE 4-26 MHz oscillator characteristics(1)

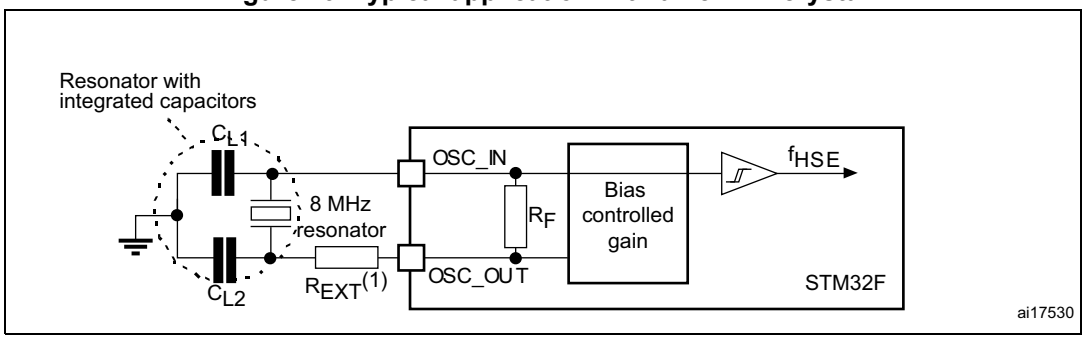
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF at 25 MHz	-	450	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF at 25 MHz	-	530	-	
ACC_{HSE}(2)	HSE accuracy	-	-500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 29*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
ACC_{LSE} (2)	LSE accuracy	-	-500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (3)	startup time	V_{DD} is stabilized	-	2	-	s

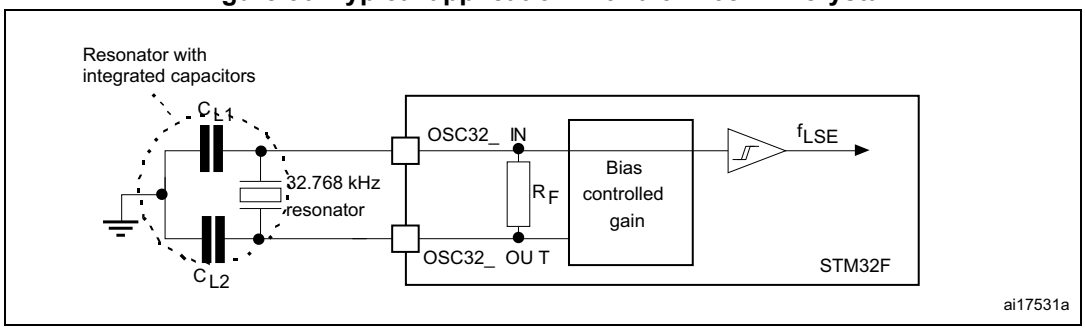
1. Guaranteed by design, not tested in production.

2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0402.

Figure 30. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

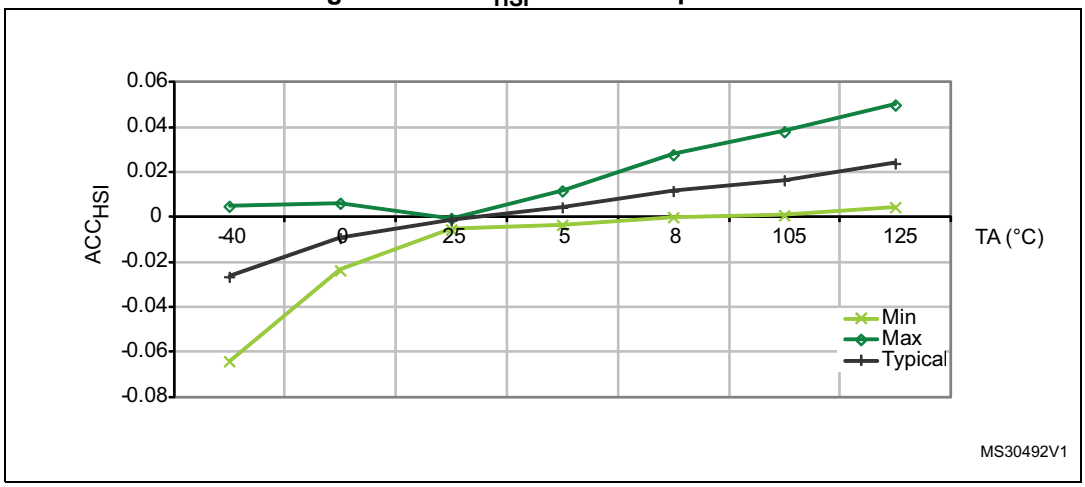
High-speed internal (HSI) RC oscillator

Table 43. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	HSI user trimming step(2)		-	-	1	%
		Factory-calibrated	T_A = -40 to 125 °C(3)	-8	-	5.5	%
			T_A = -40 to 105 °C(3)	-8	-	4.5	%
			T_A = -10 to 85 °C(3)	-4	-	4	%
			T_A = 25 °C(4)	-1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-		-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-		-	60	80	µA

1. V_{DD} = 3.3 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design, not tested in production
3. Based on characterization, not tested in production
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization, not tested in production.

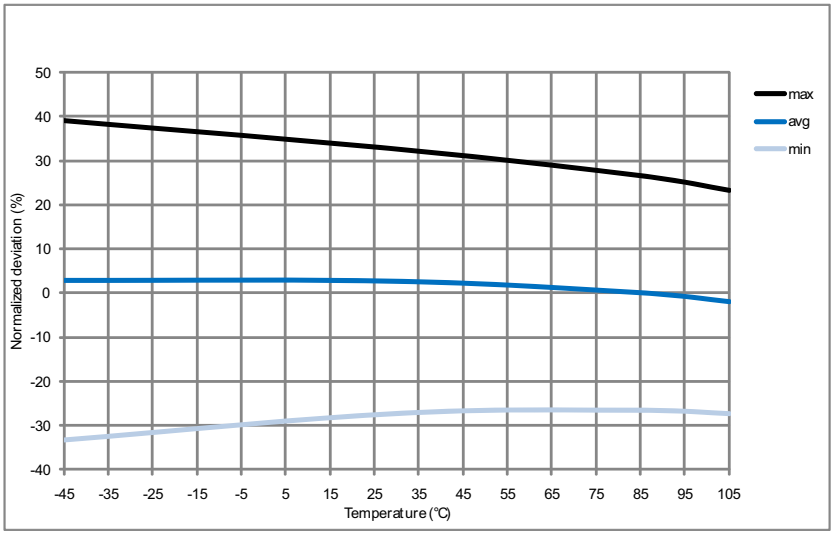
Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Figure 32. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 45. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-		24	-	100	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-		-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-		100	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples.		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization, not tested in production.

Table 46. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization, not tested in production.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 53: EMI characteristics for LQFP144*). It is available only on the main PLL.

Table 47. SSCG parameter constraints

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	(Modulation period) * (Increment Step)	-	-	2^{15}-1	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

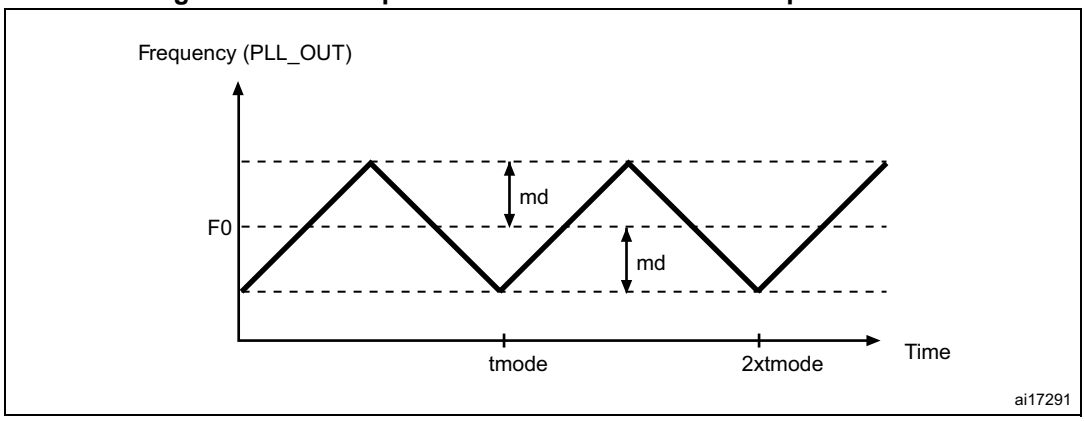
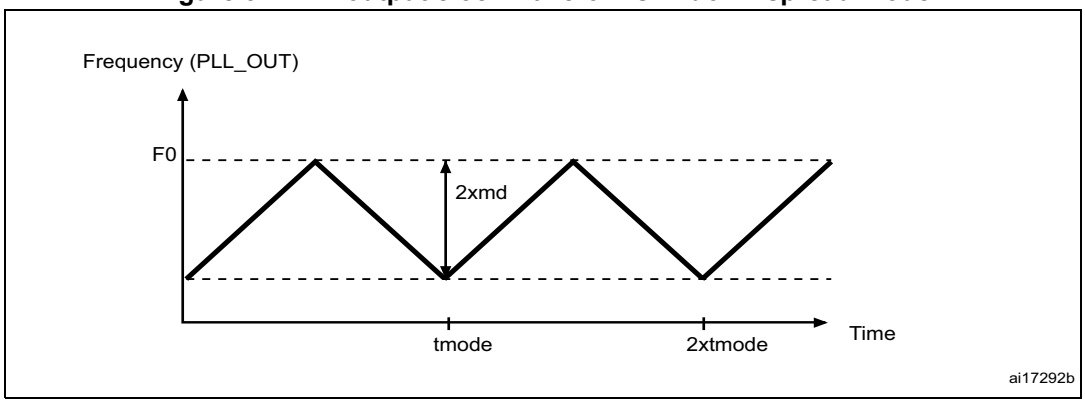


Figure 34. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 48. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 49. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Table 49. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Table 50. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 51. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = -40 to +85 °C (temp. range 6) T_A = -40 to +105 °C (temp. range 7) T_A = -40 to +125 °C (temp. range 3)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		1 kcycle(2) at T_A = 125 °C	3	
		10 kcycle(2) at T_A = 55 °C	20	

1. Guaranteed by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

Table 52. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 53. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	20	dBµV
			30 to 130 MHz	28	
			130 MHz to 1 GHz	21	
			EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 54. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP100, LQFP64, UFQFPN48	4	500	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, WLCSP64	3	400	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, LQFP144	3	250	

1. Guaranteed by characterization, not tested in production.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 55. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 56*.

Table 56. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	–0	NA	mA
	Injected current on NRST pin	–0	NA	
	Injected current on PB3, PB4, PB5, PB6, PB7, PB8, PB9, PC13, PC14, PC15, PH1, PDR_ON, PC0, PC1,PC2, PC3, PD1, PD5, PD6, PD7, PE0, PE2, PE3, PE4, PE5, PE6	–0	NA	
	Injected current on any other FT pin	–5	NA	
	Injected current on any other pins	–5	+5	

1. NA = not applicable.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Table 57. I/O static characteristics

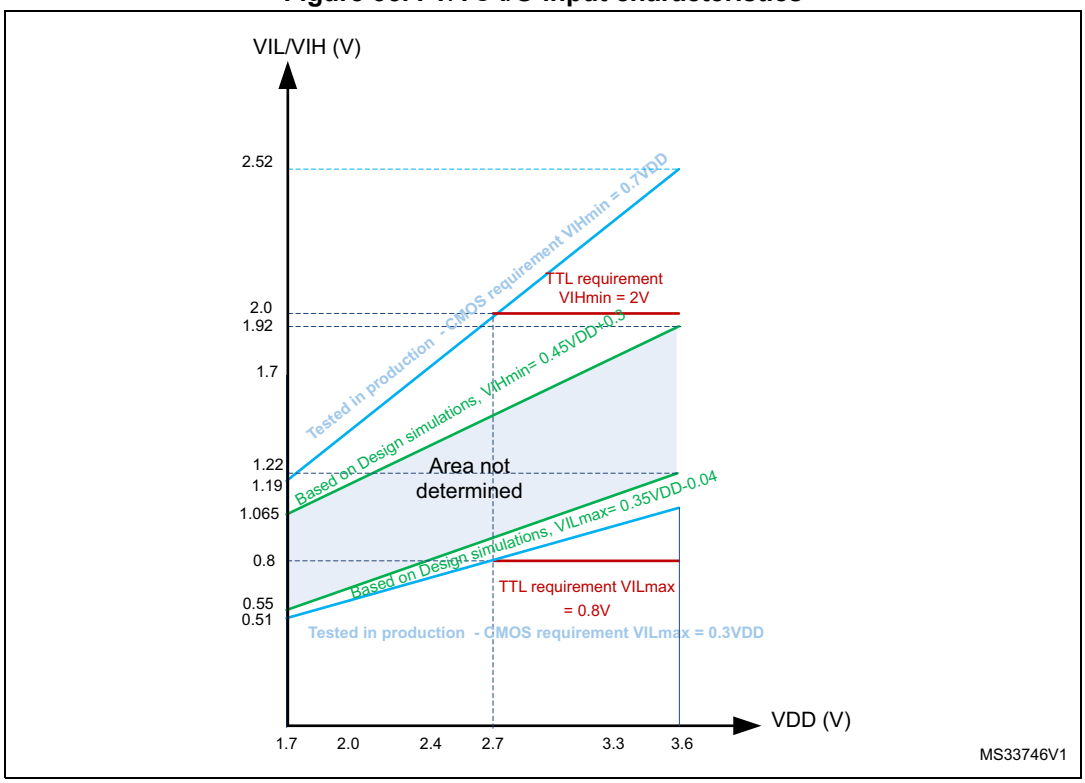
Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TC and NRST I/O input low level voltage		1.7 V ≤ V_{DD} ≤ 3.6 V	-	-	$0.3V_{DD}$(1)	V
	BOOT0 I/O input low level voltage		1.75 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C	-	-	$0.1V_{DD}+0.1$(2)	
			1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 125 °C	-	-		
V_{IH}	FT, TC and NRST I/O input high level voltage(5)		1.7 V ≤ V_{DD} ≤ 3.6 V	$0.7V_{DD}$(1)	-	-	V
	BOOT0 I/O input high level voltage		1.75 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C	$0.17V_{DD}+0.7$(2)	-	-	
			1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 125 °C				
V_{HYS}	FT, TC and NRST I/O input hysteresis		1.7 V ≤ V_{DD} ≤ 3.6 V	10% V_{DD}(2)(3)	-	-	V
	BOOT0 I/O input hysteresis		1.75 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C	0.1	-	-	
			1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 125 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤ V_{IN} ≤ V_{DD}	-	-	±1	µA
	I/O FT/TC input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 (OTG_FS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design, not tested in production.

3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 56: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 56: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 35*.

Figure 35. FT/TC I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Table 58. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 14*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.
5. Guaranteed by design, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 59*, respectively.

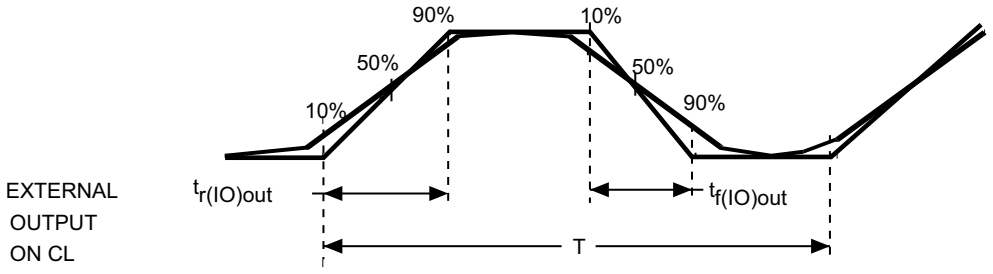
Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 59. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	12.5	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD}≥ 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	6	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	6	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by characterization, not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 36*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 36. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 57*).

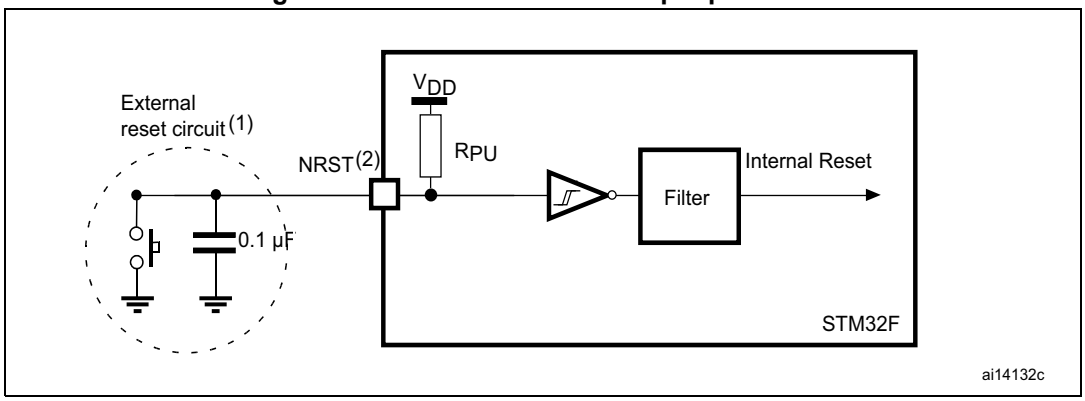
Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*. Refer to *Table 57: I/O static characteristics* for the values of VIH and VIL for NRST pin.

Table 60. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design, not tested in production.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 60*. Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in *Table 61* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 61. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 100 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	50	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 100 MHz	0.0119	780	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 62*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

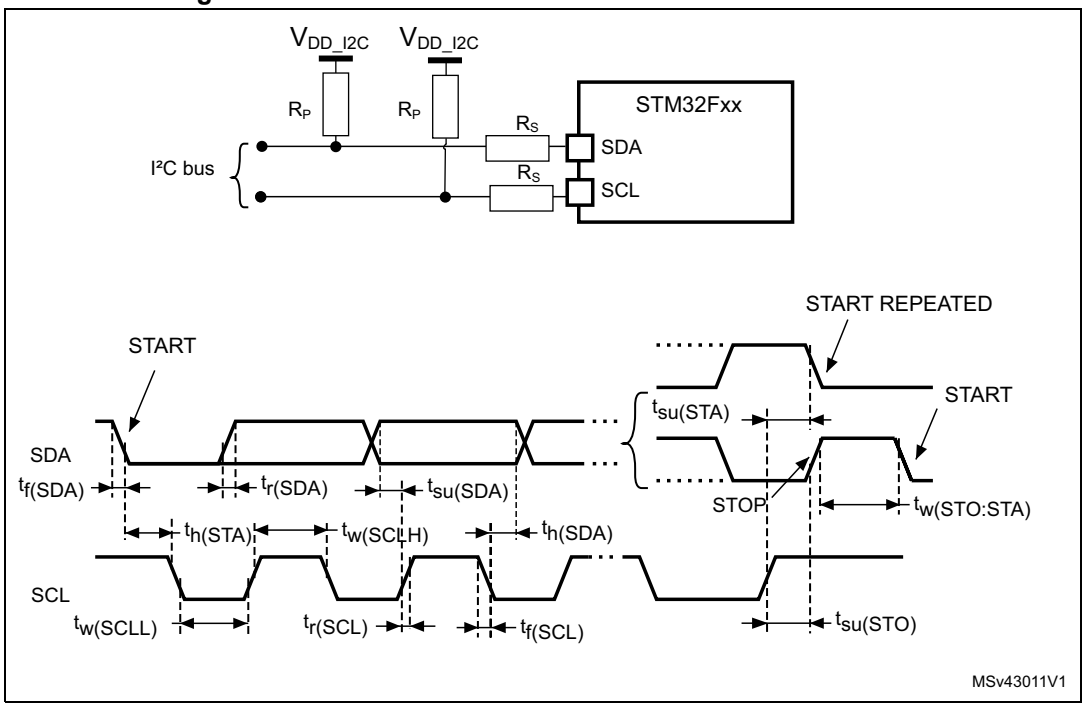
Table 62. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450(3)	0	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	-	-	50	120(5)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max)

Figure 38. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 63. SCL frequency (f_{PCLK1}= 50 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

FMPI^{2}C characteristics

The following table presents FMPI^{2}C characteristics.

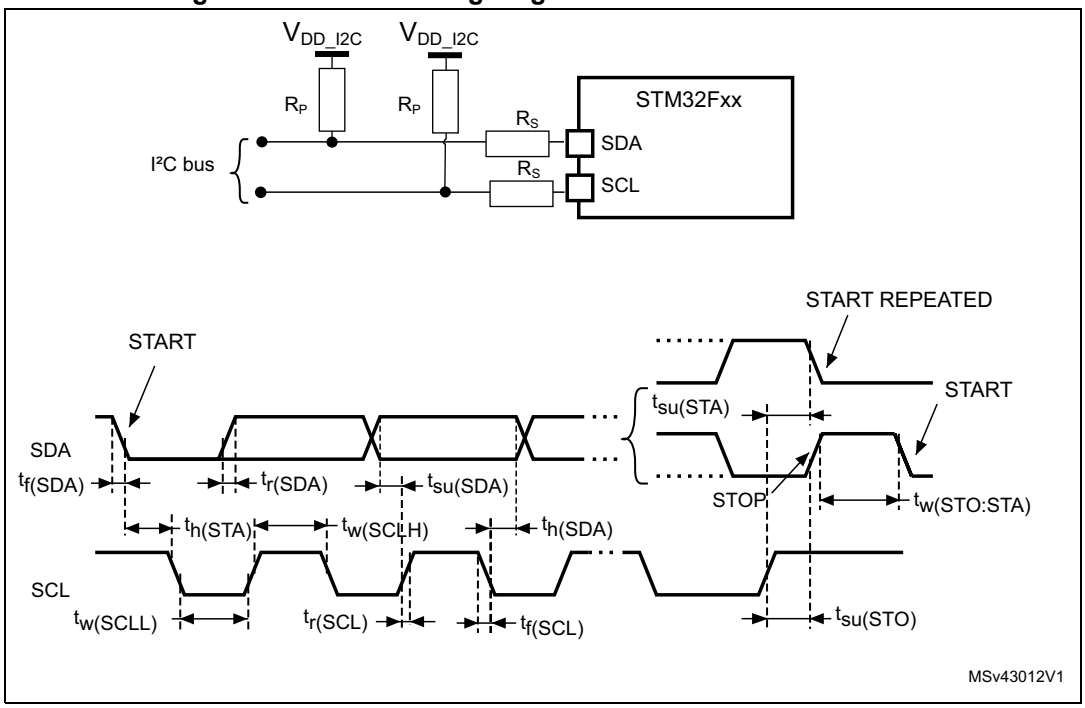
Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

Table 64. FMPI^{2}C characteristics(1)

	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	18	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(2)	pF

1. Based on characterization results, not tested in production.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Figure 39. FMPI^{2}C timing diagram and measurement circuit



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 65. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	MHz
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1//4/5	-	-	50	
		Slave transmitter/full duplex mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	35(2)	
		Slave receiver mode, 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.7 V < V_{DD} < 3.6 V SPI2/3	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK}-1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	0.5	-	-	ns

Table 65. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7.5	9	ns
		Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	-	7.5	14	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	5.5	-	-	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	3	8	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	2	-	-	ns

1. Guaranteed by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0

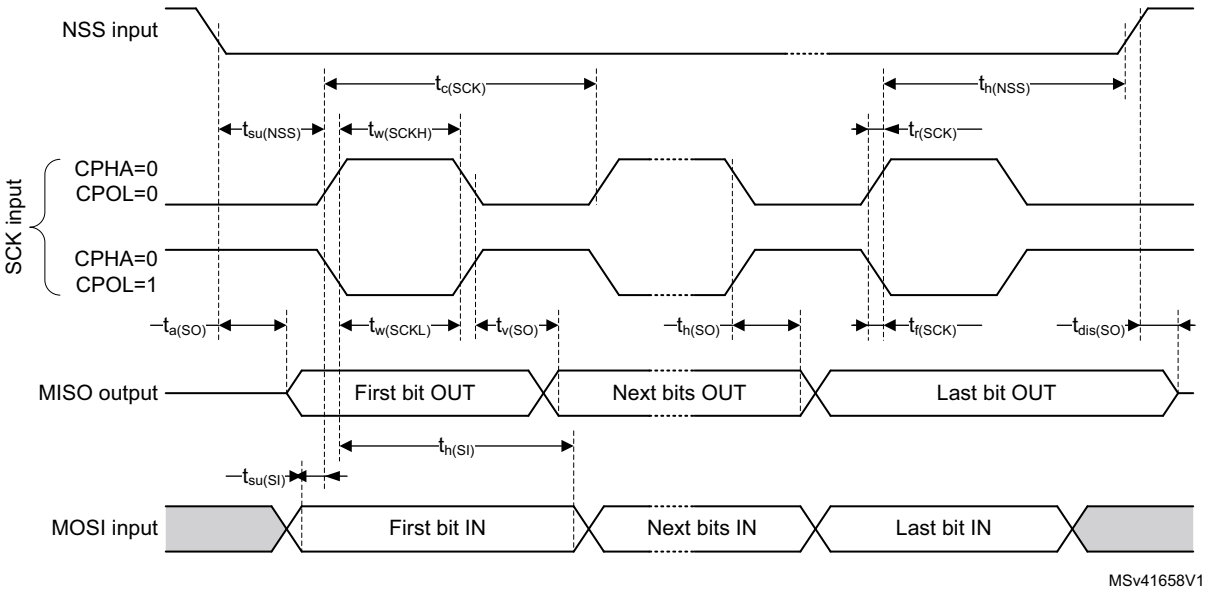


Figure 41. SPI timing diagram - slave mode and CPHA = 1(1)

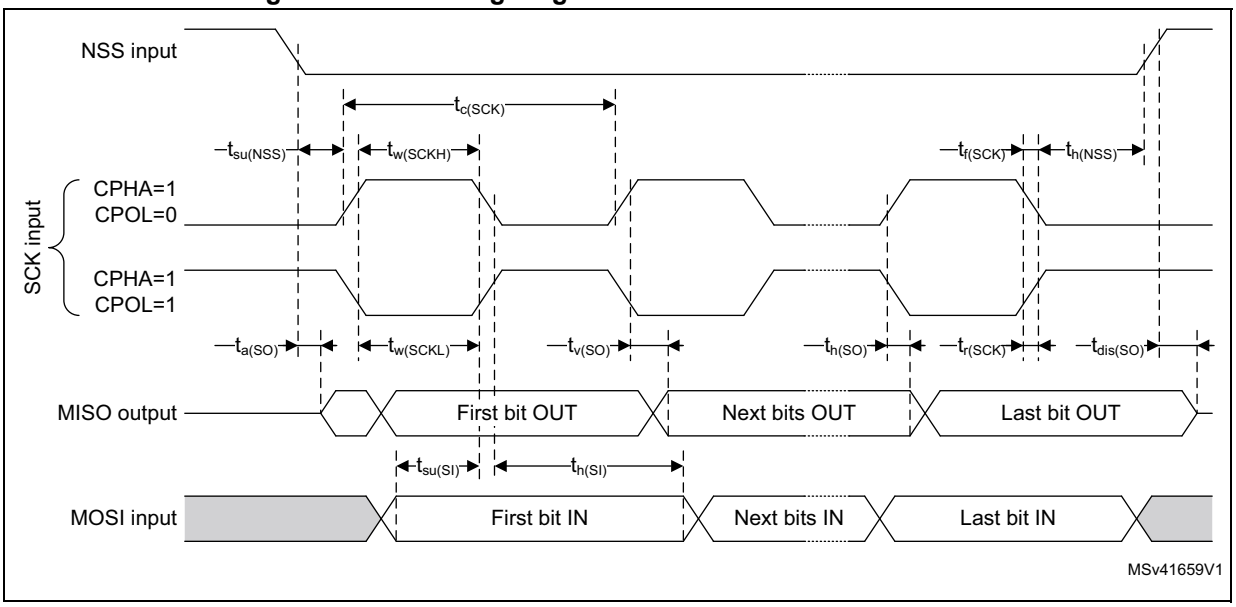
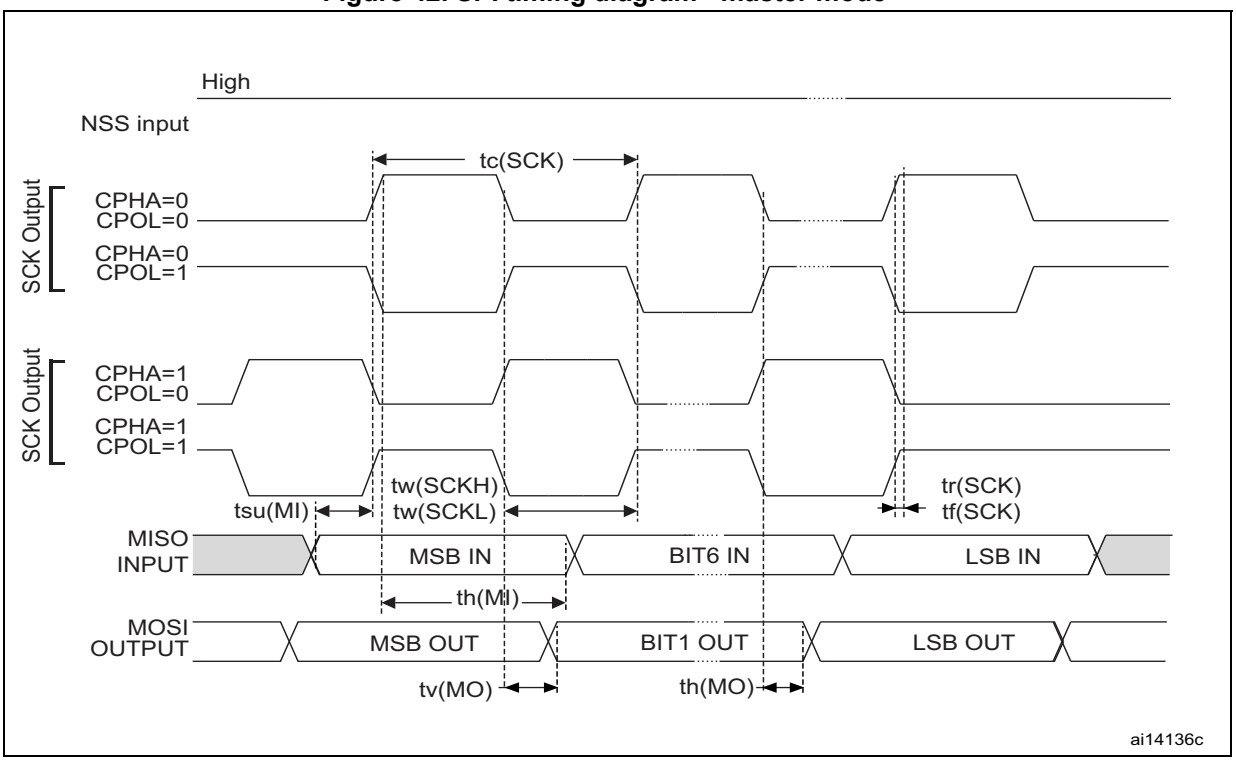


Figure 42. SPI timing diagram - master mode(1)



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 66* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 66. I²S dynamic characteristics(1)

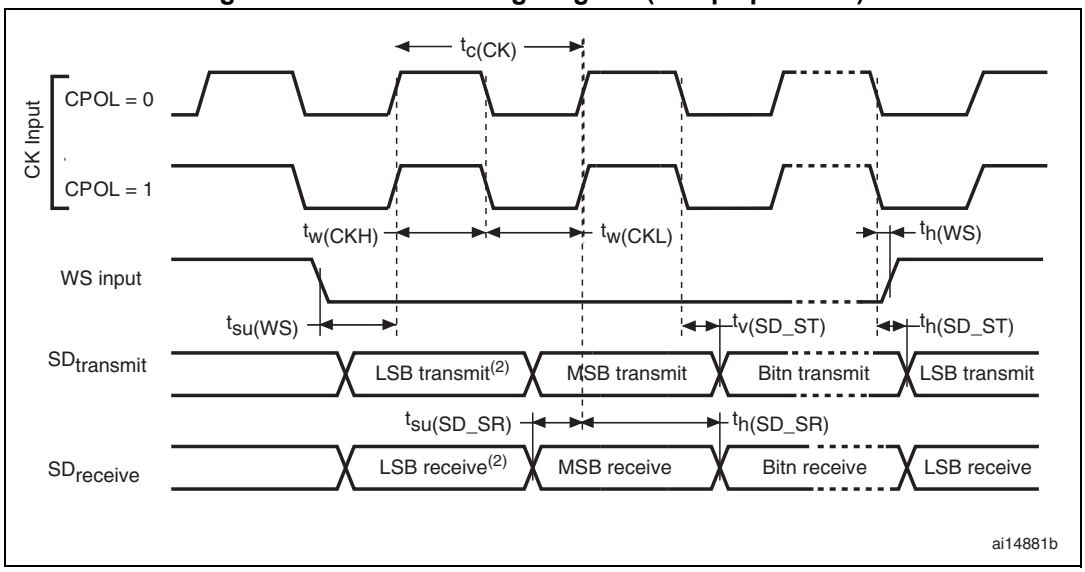
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD_SR)}$		Slave receiver	2.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	2.5	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0402 reference manual for more details on the sampling frequency (F_S).

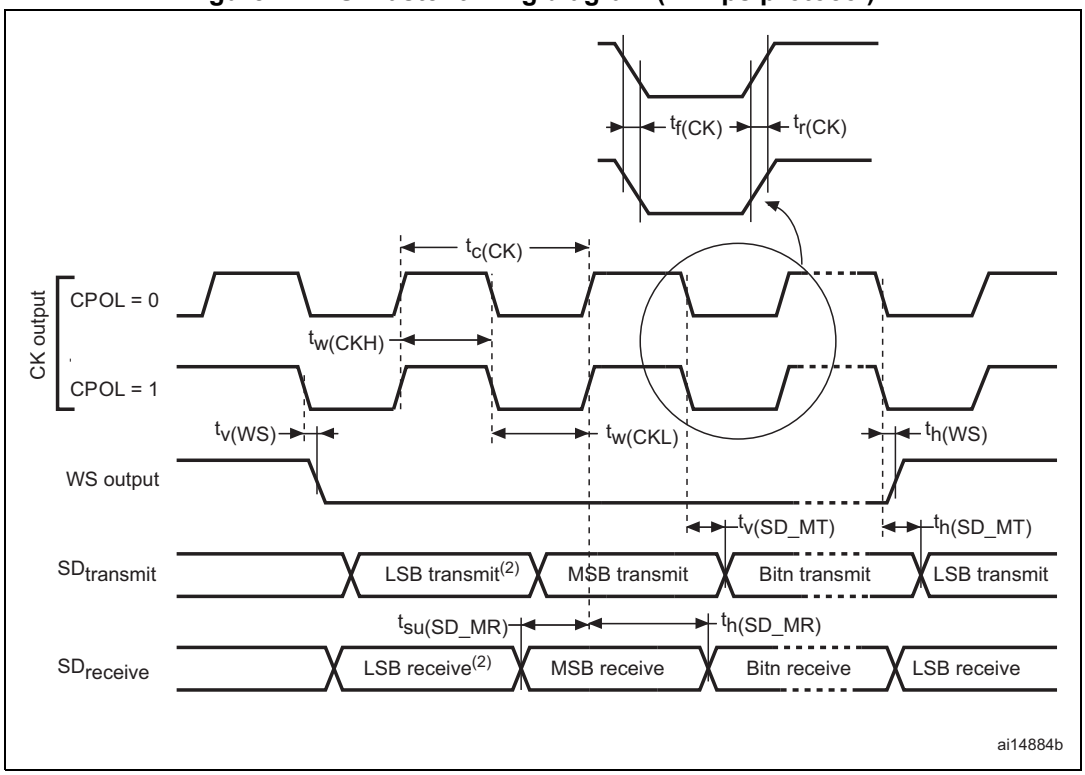
*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 43. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 44. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

QSPI interface characteristics

Unless otherwise specified, the parameters given in the following tables for QSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=20pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 67. QSPI dynamic characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	QSPI clock frequency	Write mode 1.71 V≤V_{DD}≤3.6 V C_{load} = 15 pF	-	-	80	MHz
		Read mode 2.7 V<V_{DD}<3.6 V C_{load} = 15 pF	-	-	100	
		1.71 V≤V_{DD}≤3.6 V	-	-	50	
$t_{w(CKH)}$	QSPI clock high and low	-	($T_{(CK)}$ / 2)-1	-	$T_{(CK)}$ / 2	ns
$t_{w(CKL)}$			$T_{(CK)}$ / 2)	-	($T_{(CK)}$ / 2)+1	
$t_{s(IN)}$	Data input setup time	-	0.5	-	-	
$t_{h(IN)}$	Data input hold time	-	3.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.

Table 68. QSPI dynamic characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	QSPI clock frequency	Write mode 1.71 V≤V_{DD}≤3.6 V C_{load} = 15 pF	-	-	80	MHz
		Read mode 2.7 V<V_{DD}<3.6 V C_{load} = 15 pF	-	-	80	
		1.71 V≤V_{DD}≤3.6 V	-	-	50	

Table 68. QSPI dynamic characteristics in DDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low	-	$(T_{(CK)} / 2)-1$	-	$T_{(CK)} / 2$	ns
$t_{w(CKL)}$			$T_{(CK)} / 2)$	-	$(T_{(CK)} / 2)+1$	
$t_{s(IN)}$	Data input setup time	-	0	-	-	
$t_{h(IN)}$	Data input hold time	-	4	-	-	
$t_{v(OUT)}$	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8	10.5	
		1.71 V<V_{DD}<3.6 V	-	8	13	
$t_{h(OUT)}$	Data output hold time	-	7.5	-	-	

1. Guaranteed by characterization results, not tested in production.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 69. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 70. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 45. USB OTG FS timings: definition of data signal rise and fall time

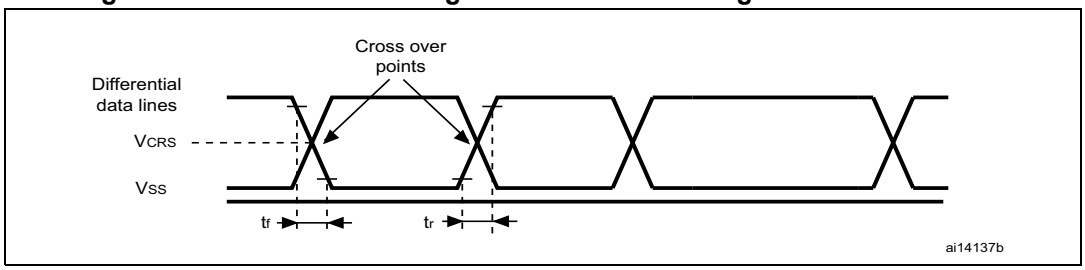


Table 71. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 72* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 16*.

Table 72. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	V_{DDA} –V_{REF+} < 1.2 V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 72. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. Guaranteed by characterization, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 72*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 73. ADC accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 74. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, V_{DDA} –V_{REF} < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 75. ADC accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 76. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization, not tested in production.

Table 77. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

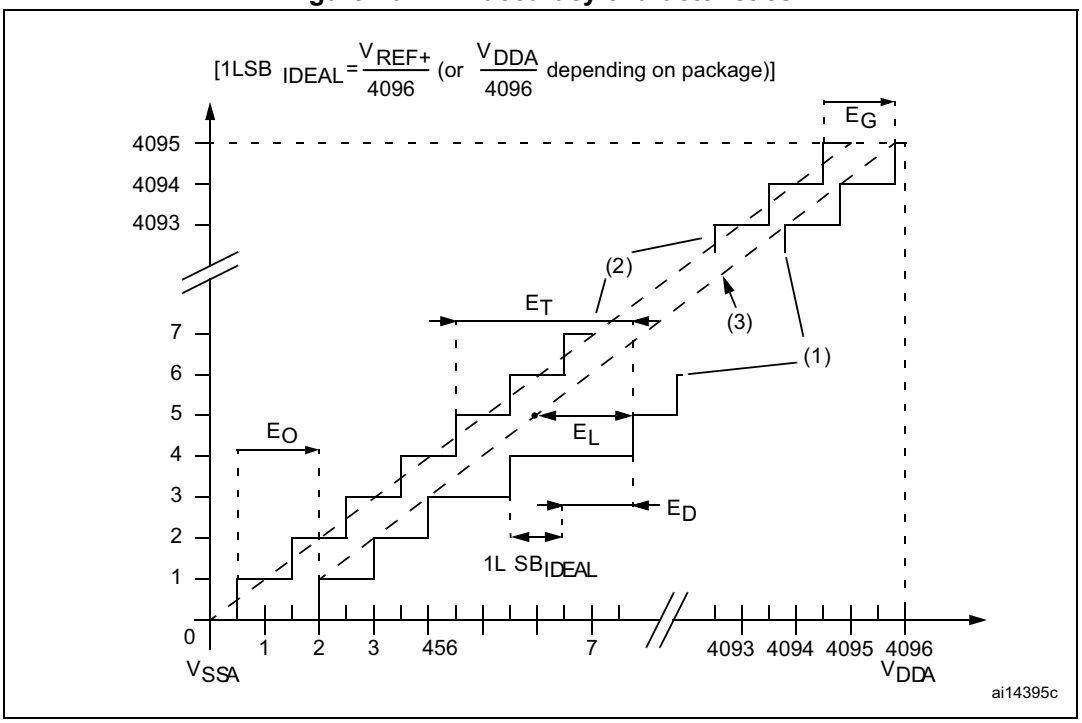
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization, not tested in production.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

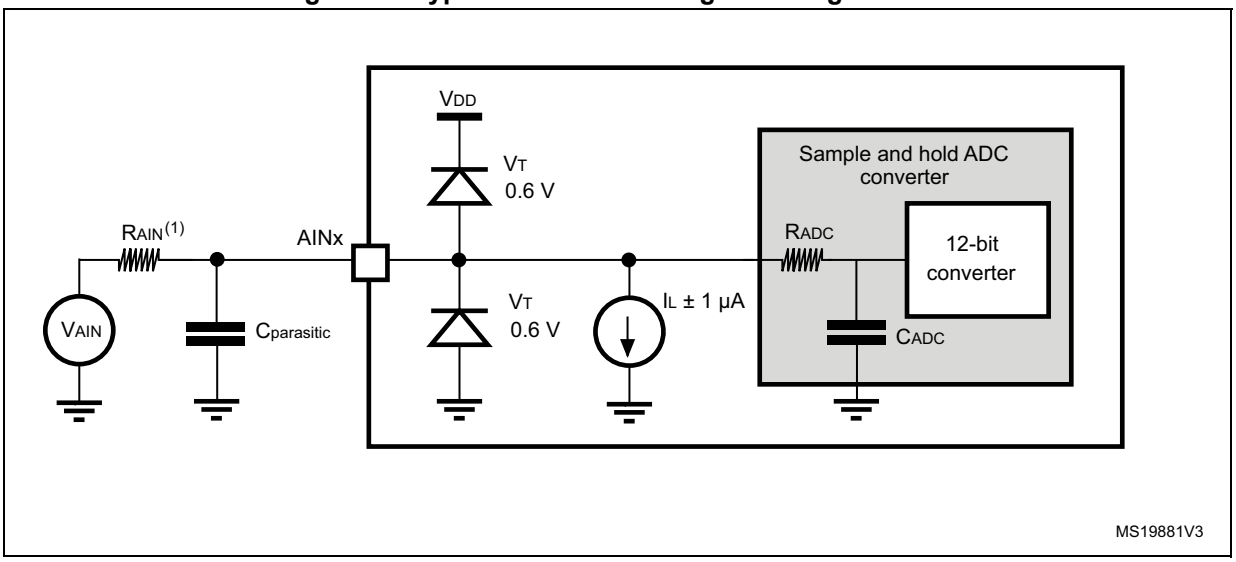
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 46. ADC accuracy characteristics



1. See also *Table 74*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 47. Typical connection diagram using the ADC

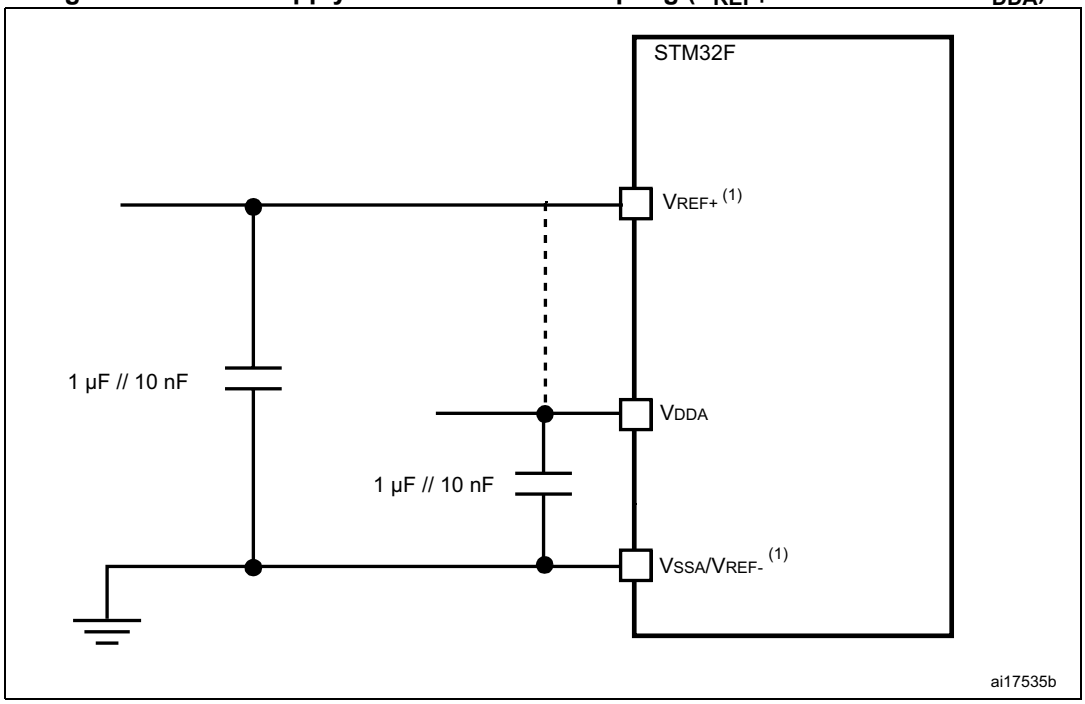


1. Refer to *Table 72* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

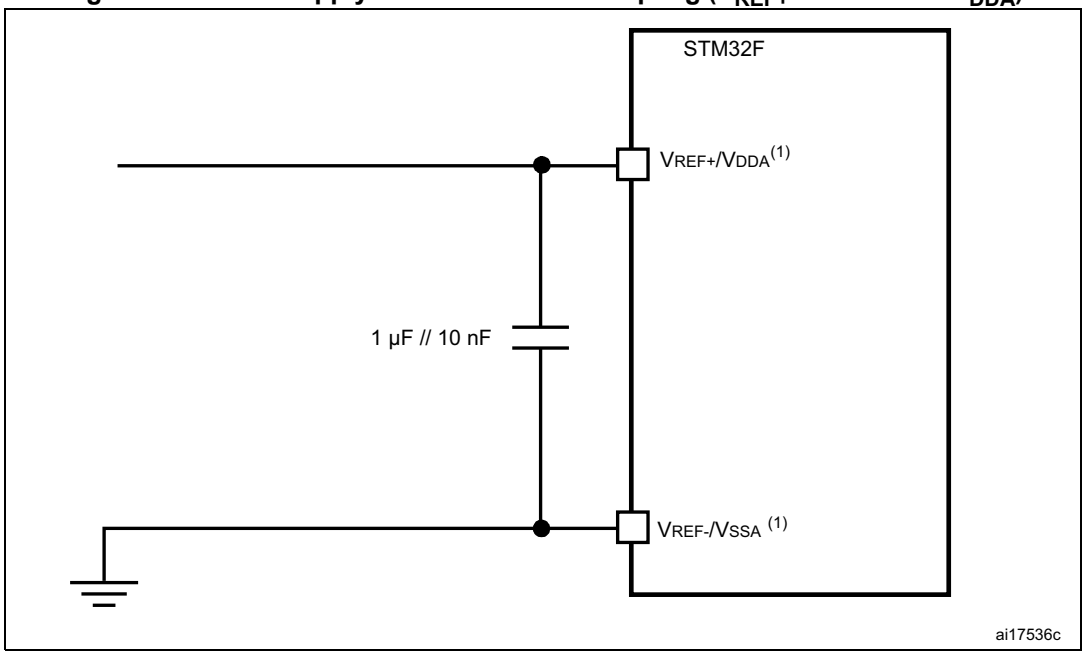
Power supply decoupling should be performed as shown in *Figure 48* or *Figure 49*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 48. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 49. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 Temperature sensor characteristics

Table 78. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 79. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

6.3.22 V_{BAT} monitoring characteristics

Table 80. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 81* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 81. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	- 40 °C < T_A < +125 °C	1.18	1.21	1.24	V
$T_{S_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

Table 82. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

6.3.24 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 83* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

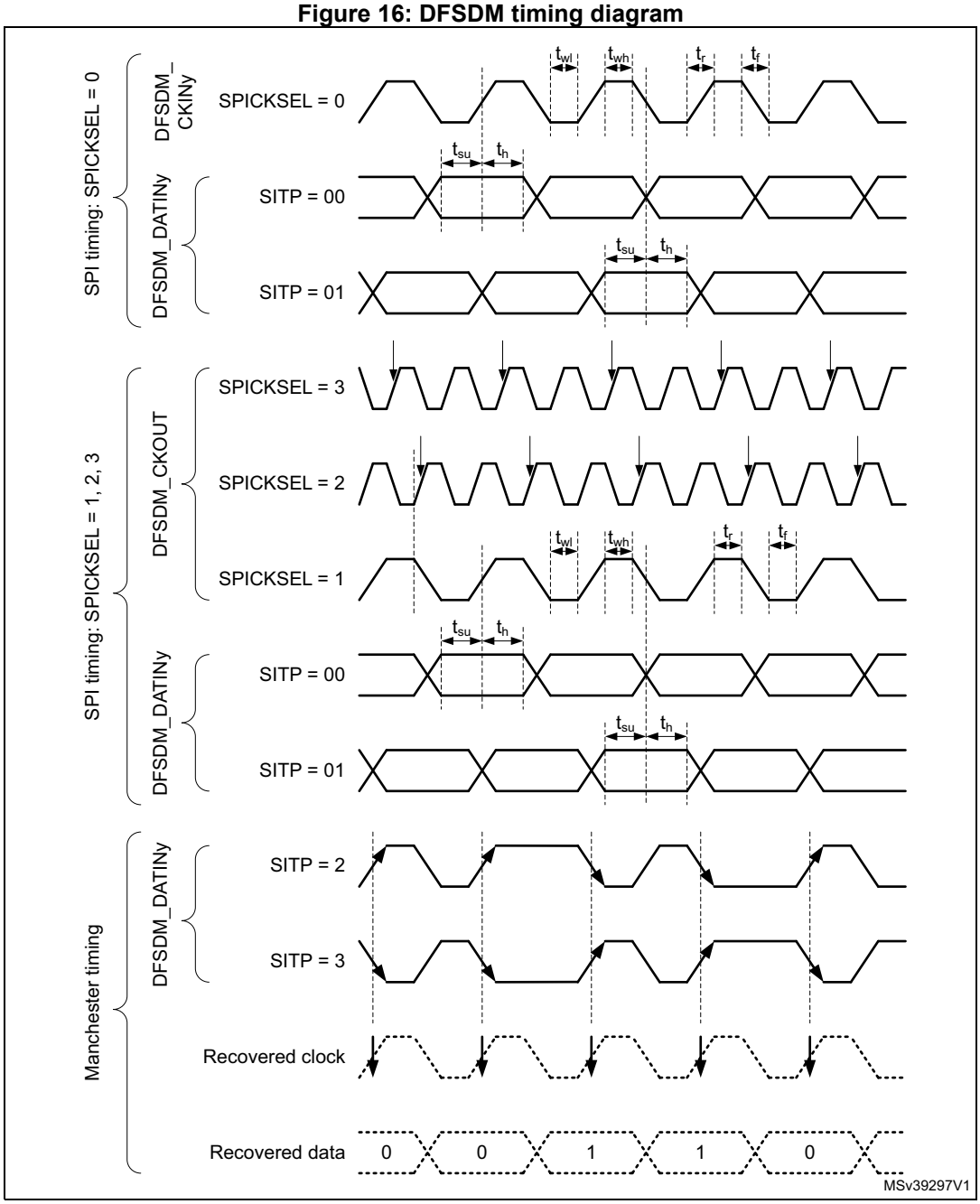
Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 83. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20 ($f_{DFSDMCLK}/4$)	
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2-0.5$	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 16: DFSDM timing diagram



6.3.25 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 84* to *Table 91* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitance load C = 30 pF
- Measurement points are done at CMOS levels: $0.5.V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

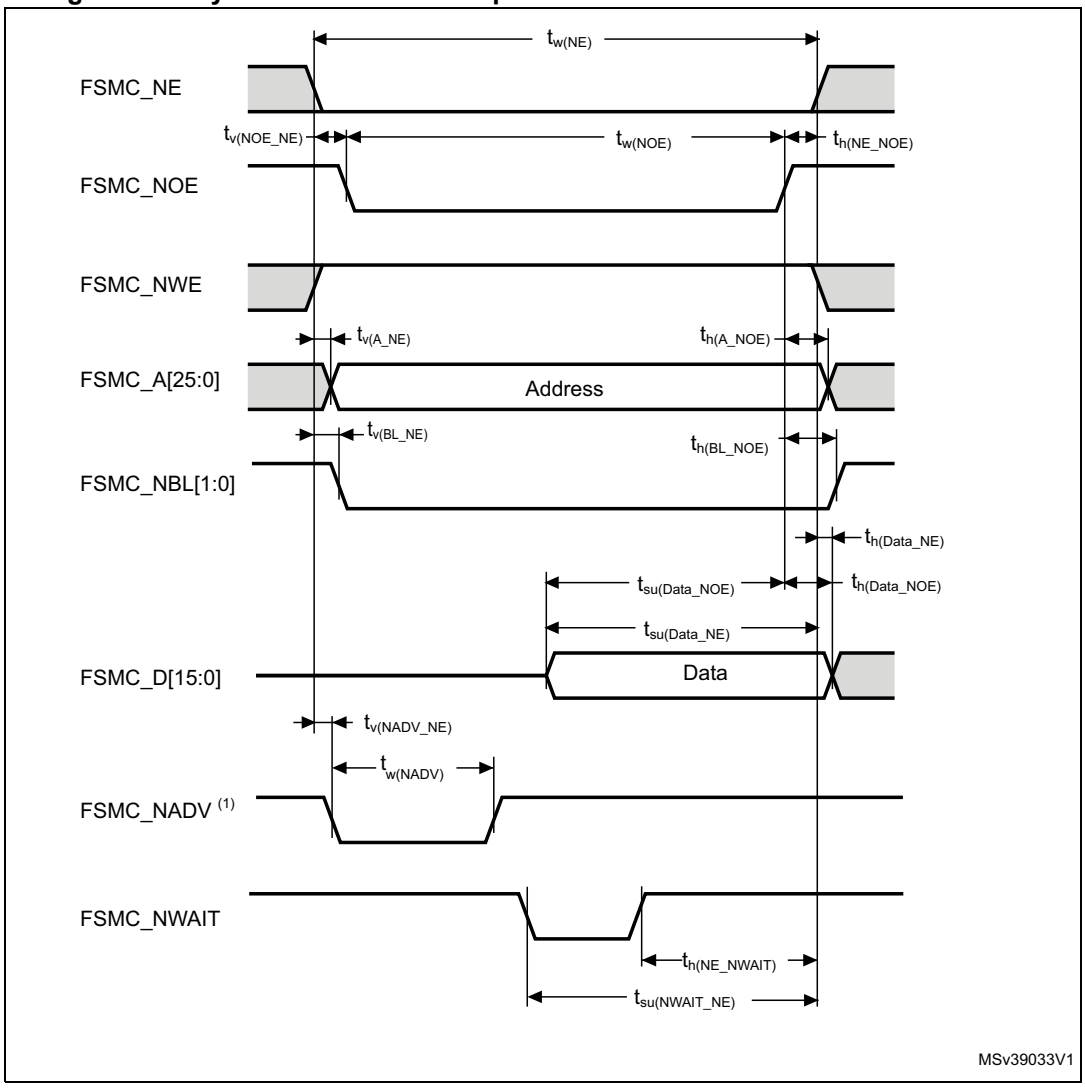
Asynchronous waveforms and timings

Figure 50 through *Figure 53* represent asynchronous waveforms and *Table 84* through *Table 91* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 84. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK} – 1$	$2\ T_{HCLK} + 0.5$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	0	1	
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK}$ - 1.5	$2T_{HCLK}$	
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	1.5	
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	0	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK} - 1	-	
$t_{su(Data_NOE)}$	Data to FSMC_NOEx high setup time	T_{HCLK} - 1	-	
$t_{h(Data_NOE)}$	Data hold time after FSMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} + 0.5$	

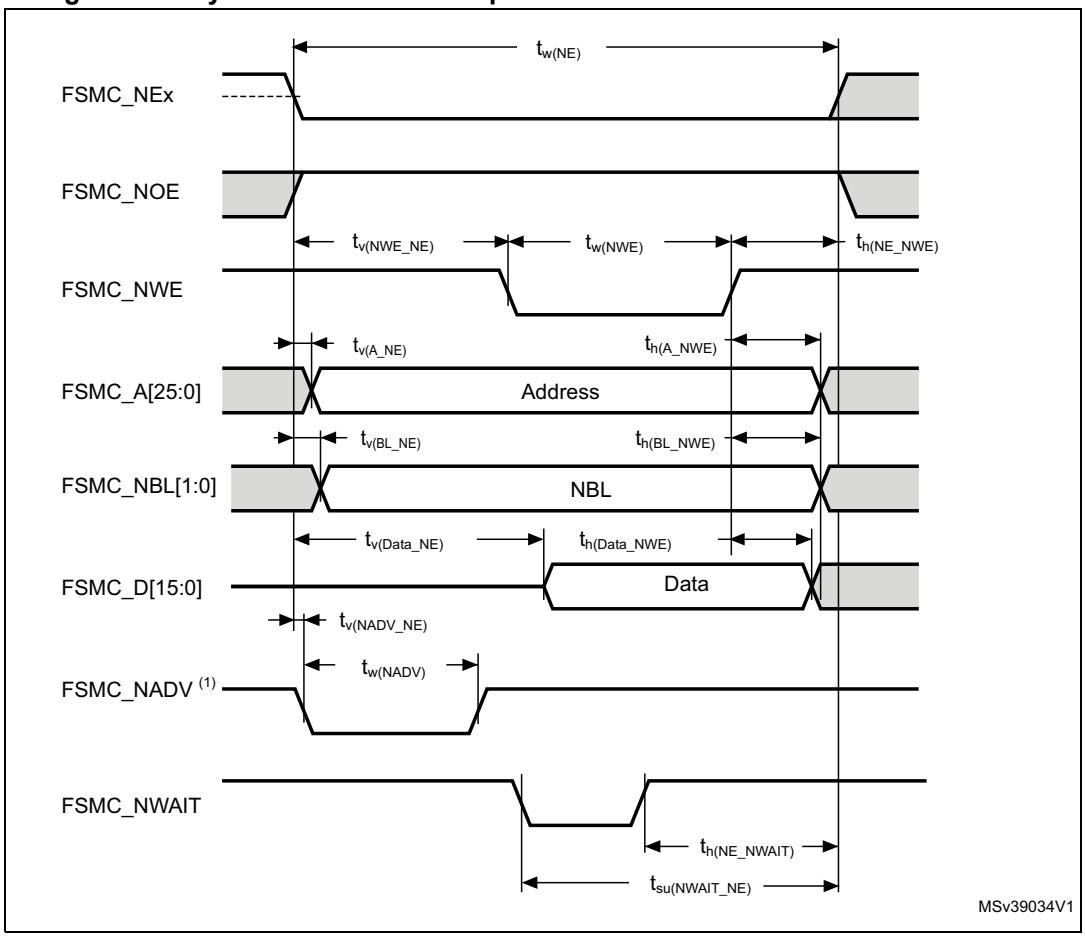
1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 85. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK}$ - 1	$7T_{HCLK} + 0.5$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK}$	
$t_{w(NWAIT)}$	FSMC_NWAIT low time	$T_{HCLK} – 0.5$	-	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5T_{HCLK}$ -1	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	3 T_{HCLK} - 1	3 T_{HCLK} +0.5	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK} + 0.5	T_{HCLK} + 0.5	
$t_{w(NWE)}$	FSMC_NWE low time	T_{HCLK} – 1.5	T_{HCLK}+ 1	
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 1	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK} - 0.5	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK} - 1	-	
$t_{v(Data_NE)}$	Data to FSMC_NEx low to Data valid	-	T_{HCLK} + 2	
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	-	1	
$t_{w(NADV)}$	FSMC_NADV low time	-	T_{HCLK}+ 0.5	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 87. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8T_{HCLK}$ - 1	$8T_{HCLK}$ + 0.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$6T_{HCLK}$ + 0.5	$6T_{HCLK}$ + 1	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6T_{HCLK}$ + 0.5	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK}$ + 1	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms

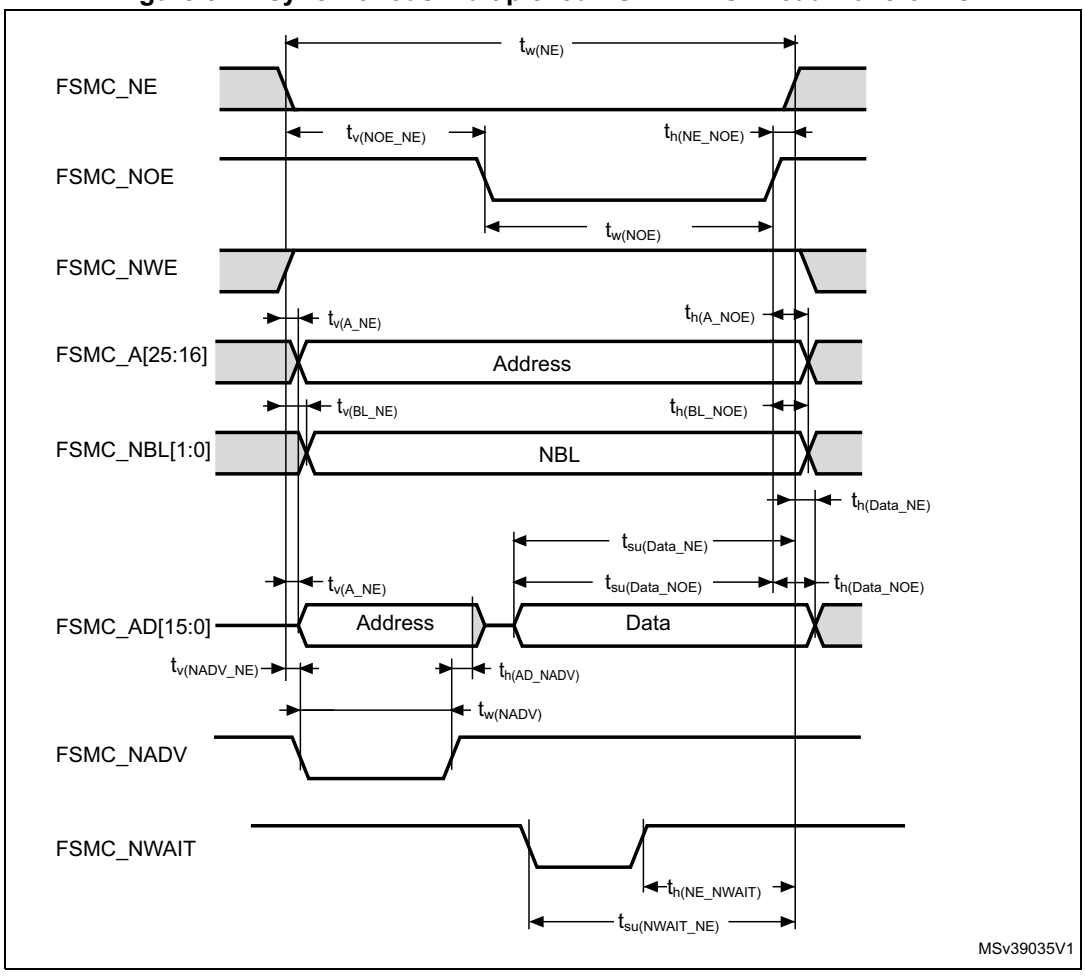


Table 88. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK} – 1$	$3T_{HCLK} + 0.5$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}$	$2T_{HCLK} + 1$	
$t_{tw(NOE)}$	FSMC_NOE low time	$T_{HCLK} – 1.5$	T_{HCLK}	
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} – 0.5$	$T_{HCLK} + 0.5$	
$t_{h(AD_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high)	0	-	
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	$T_{HCLK} – 0.5$	-	
$t_{h(BL_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK} - 2	-	
$t_{su(Data_NOE)}$	Data to FSMC_NOE high setup time	T_{HCLK} - 2	-	
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FSMC_NOE high	0	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 89. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8T_{HCLK}$ - 1	$8T_{HCLK} + 0.5$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5T_{HCLK}$	$5T_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5T_{HCLK}$ - 1	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms

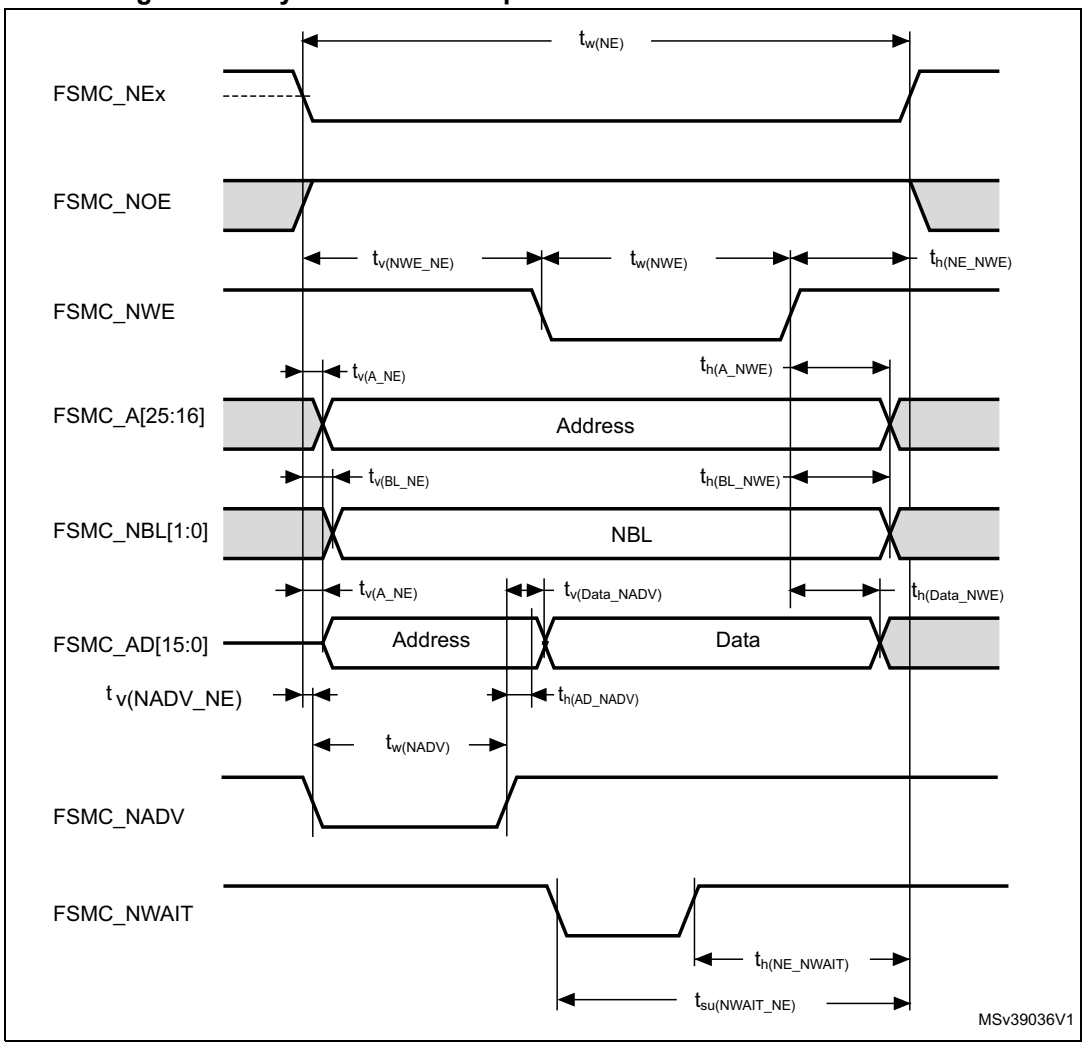


Table 90. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$ - 1	$4T_{HCLK}$+0.5	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}	T_{HCLK} + 1	
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK}$ - 1	$2T_{HCLK}$ + 0.5	
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 1.5	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK} – 0.5	T_{HCLK}+ 0.5	
$t_{h(AD_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}- 1.5	-	
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	
$t_{v(Data_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK} + 2	
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} + 0.5	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 91. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$9T_{HCLK}$ - 1	$9T_{HCLK}$ + 0.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$7T_{HCLK}$ - 1	$7T_{HCLK}$ + 0.5	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6T_{HCLK}$ -1	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK}$ + 1	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 54 through *Figure 57* represent synchronous waveforms and *Table 92* through *Table 95* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0402)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FSMC_CLK = 90 MHz).

Figure 54. Synchronous multiplexed NOR/PSRAM read timings

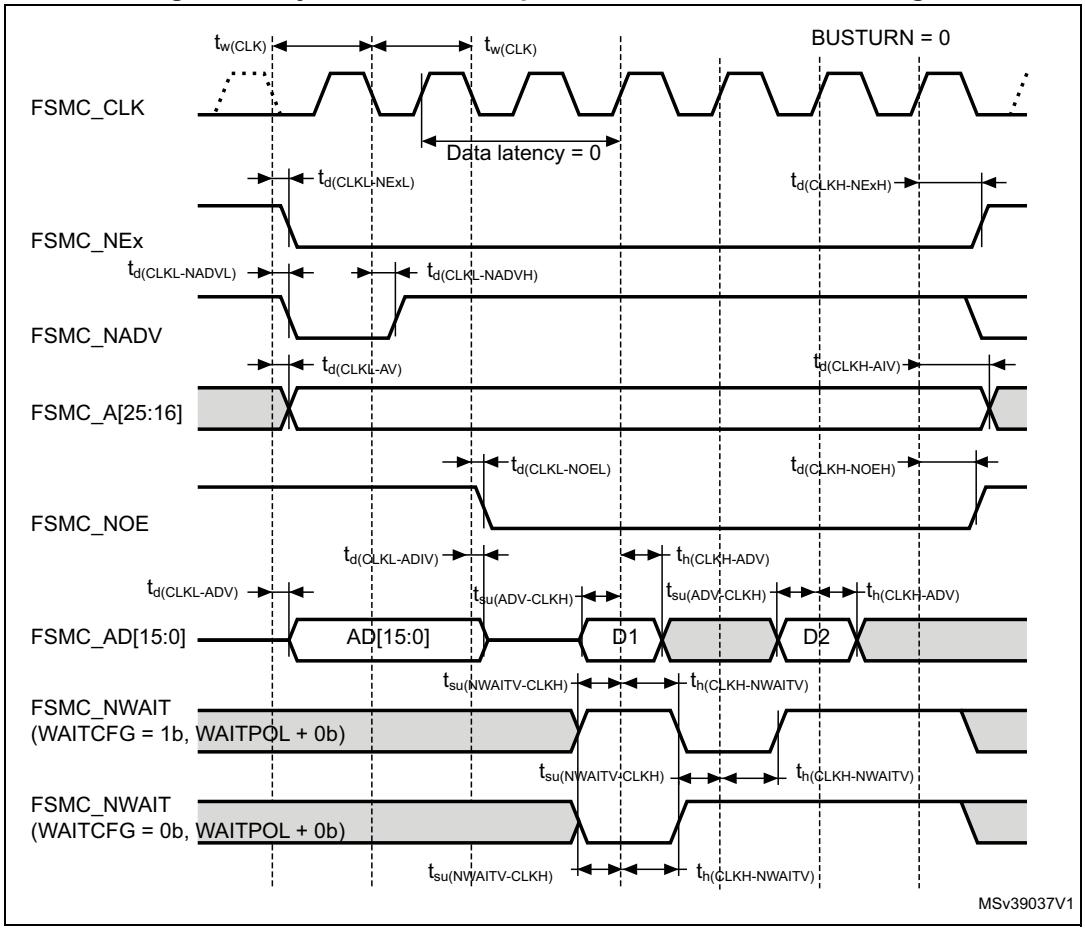


Table 92. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH_NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 55. Synchronous multiplexed PSRAM write timings

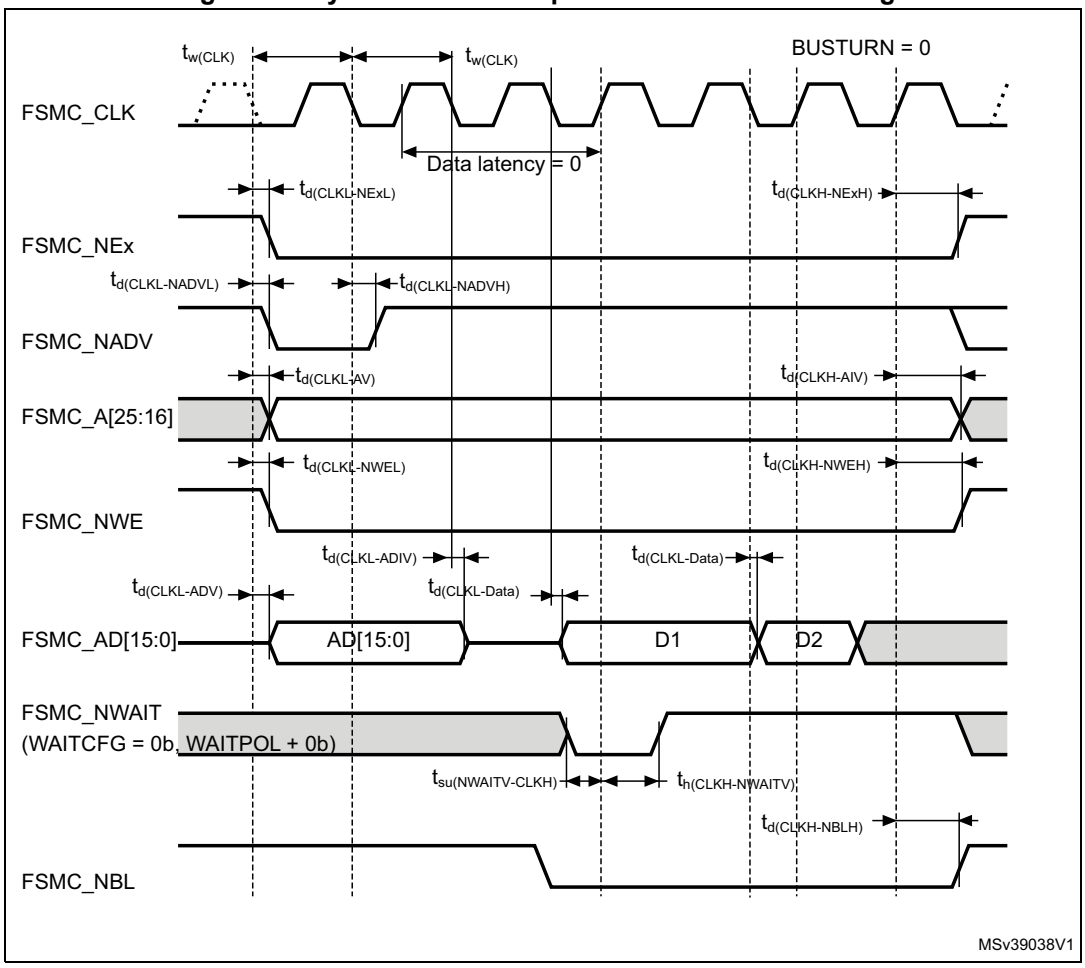


Table 93. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period, V_{DD} range= 2.7 to 3.6 V	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x= 0...2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	-	3	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK}	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

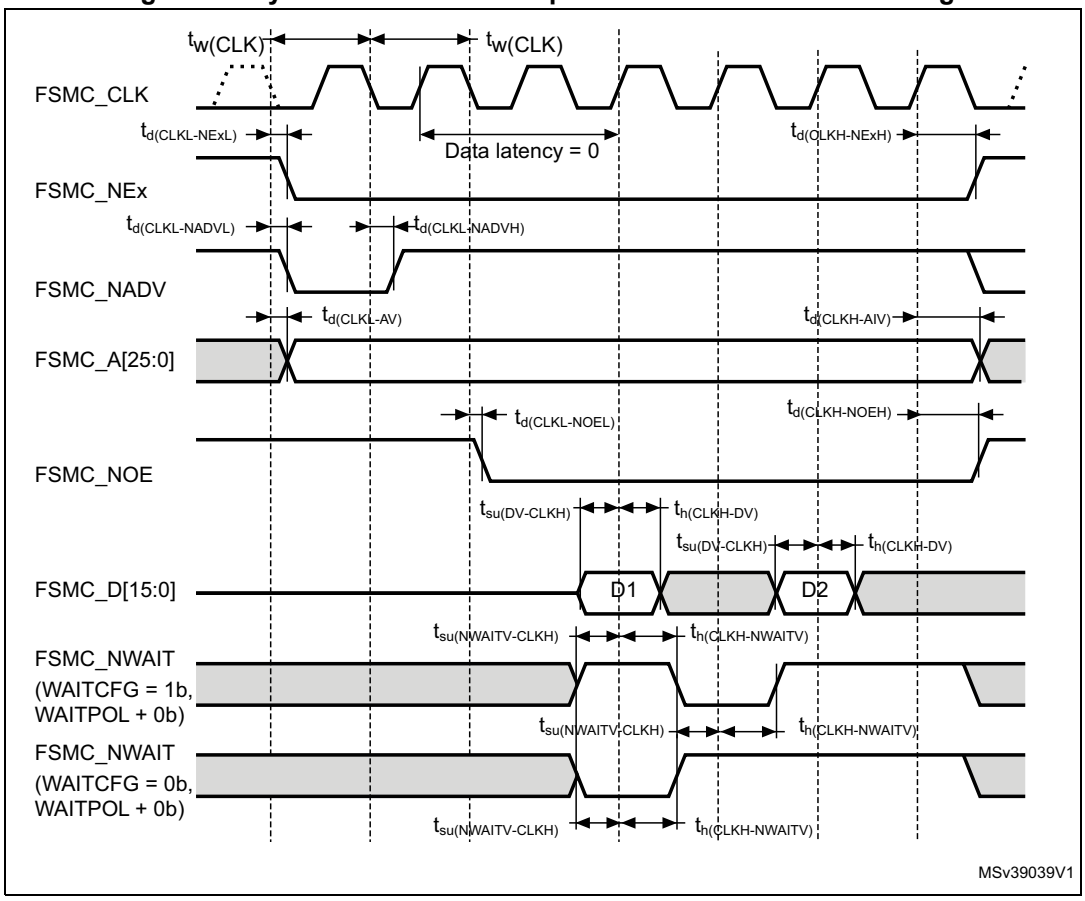


Table 94. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK} – 0.5$	-	ns
$t_{(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} +0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 57. Synchronous non-multiplexed PSRAM write timings

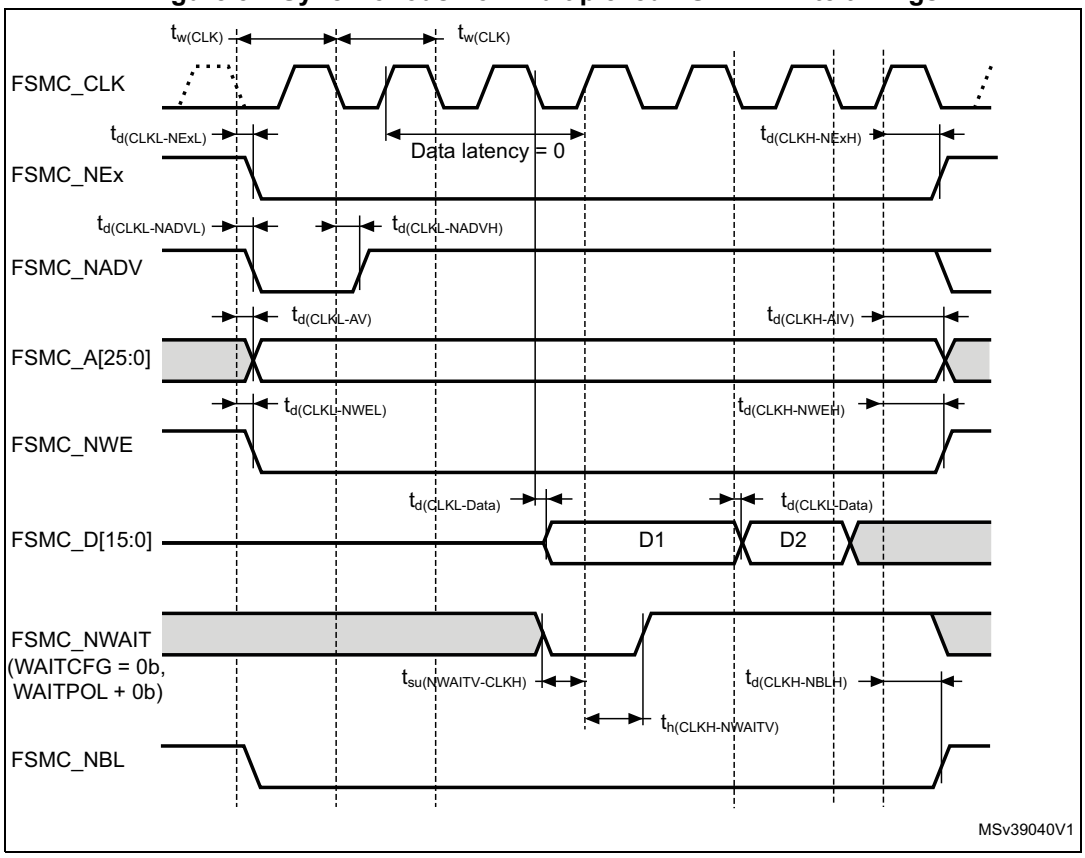


Table 95. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	-	3	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK}	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

6.3.26 SD/SDIO MMC/eMMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 96* for the SDIO are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

Figure 58. SDIO high-speed mode

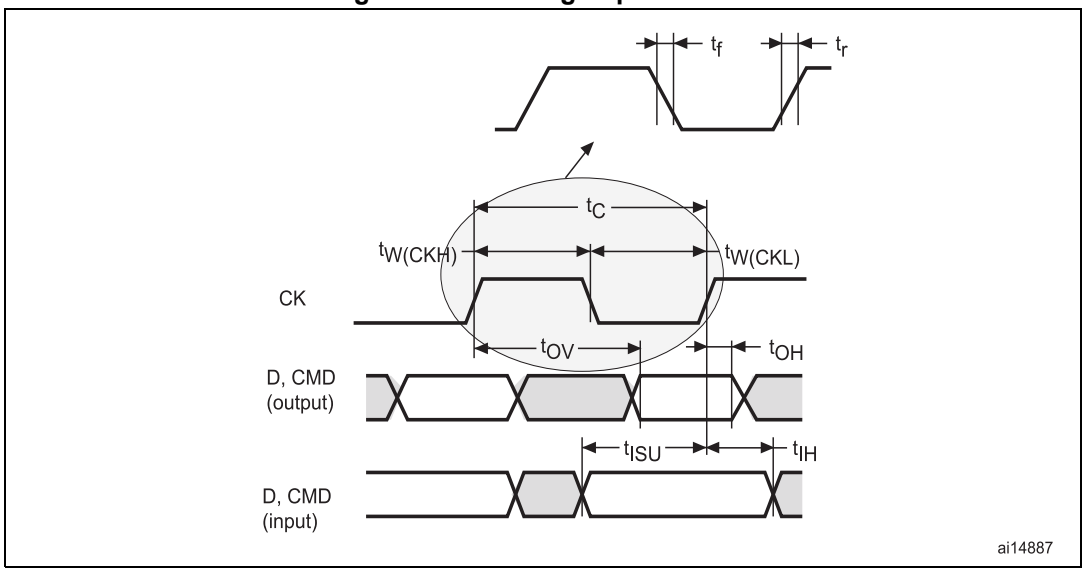


Figure 59. SD default mode

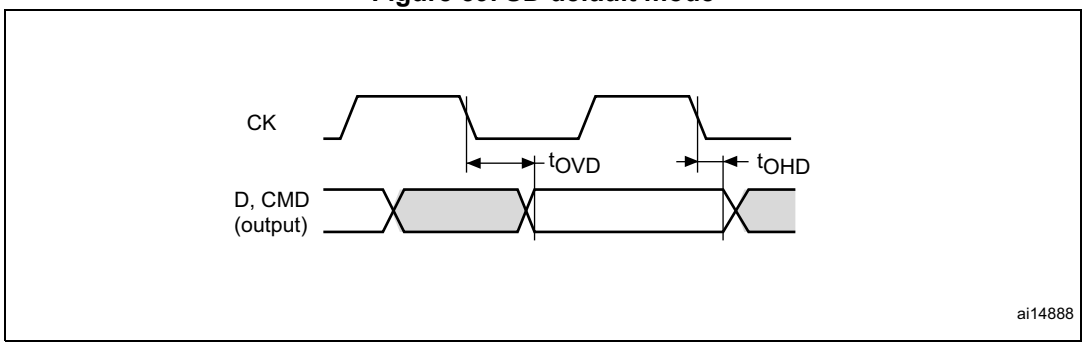


Table 96. Dynamic characteristics: SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	4	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	

Table 96. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	2.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	1.5	2	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.
2. V_{DD} = 2.7 to 3.6 V.

Table 97. Dynamic characteristics: eMMC characteristics V_{DD} = 1.7 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	fpp =50MHz	12	-	-	

1. Guaranteed by characterization results, not tested in production.
2. C_{LOAD} = 20 pF.

6.3.27 RTC characteristics

Table 98. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK is an ST trademark.

7.1 Device marking

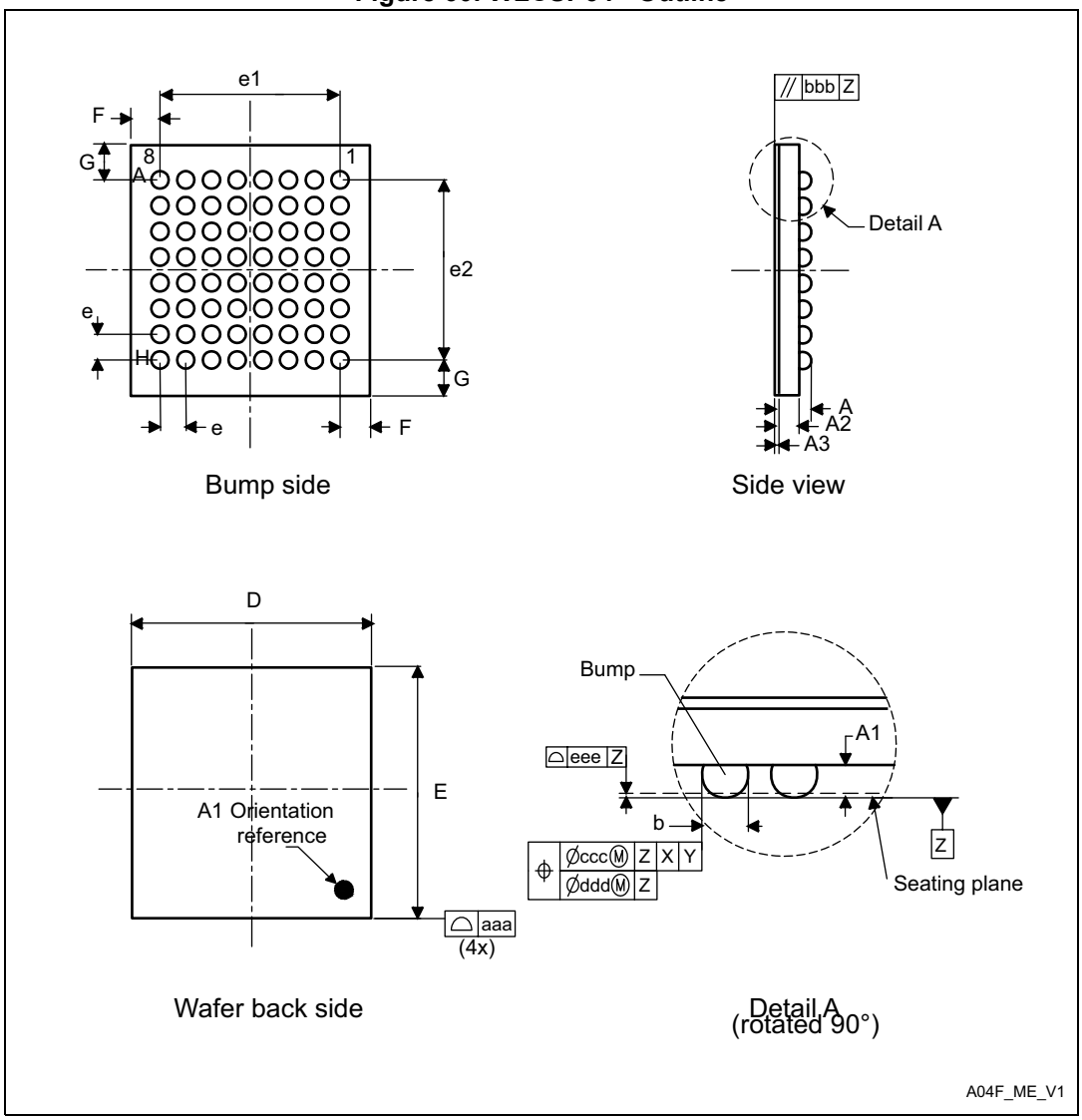
Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 WLCSP64 package information (A04F)

This WLCSP is a 64-ball, 3.658 x 3.658 mm, 0.4 mm pitch wafer level chip scale.

Figure 60. WLCSP64 - Outline



1. Drawing is not to scale.

Table 99. WLCSP64 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0067	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-

Table 99. WLCSP64 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.588	3.623	3.658	0.1413	0.1426	0.1440
E	3.616	3.651	3.686	0.1424	0.1437	0.1451
e	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
e2	-	2.800	-	-	0.1102	-
F	-	0.4115	-	-	0.0162	-
G	-	0.4255	-	-	0.0168	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP64 - Footprint example

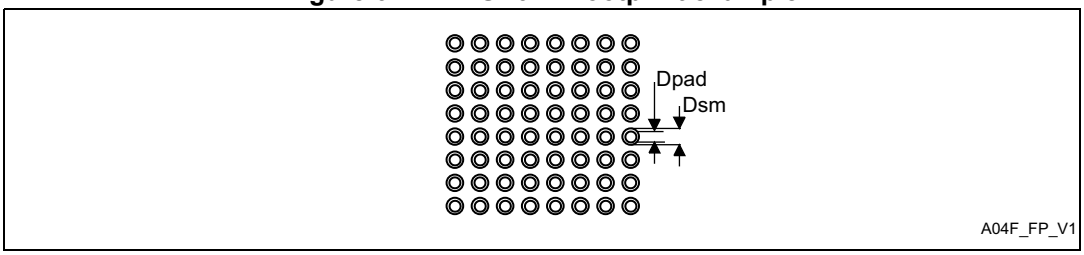


Table 100. WLCSP64 - Example of PCB design rules (0.4 mm pitch)

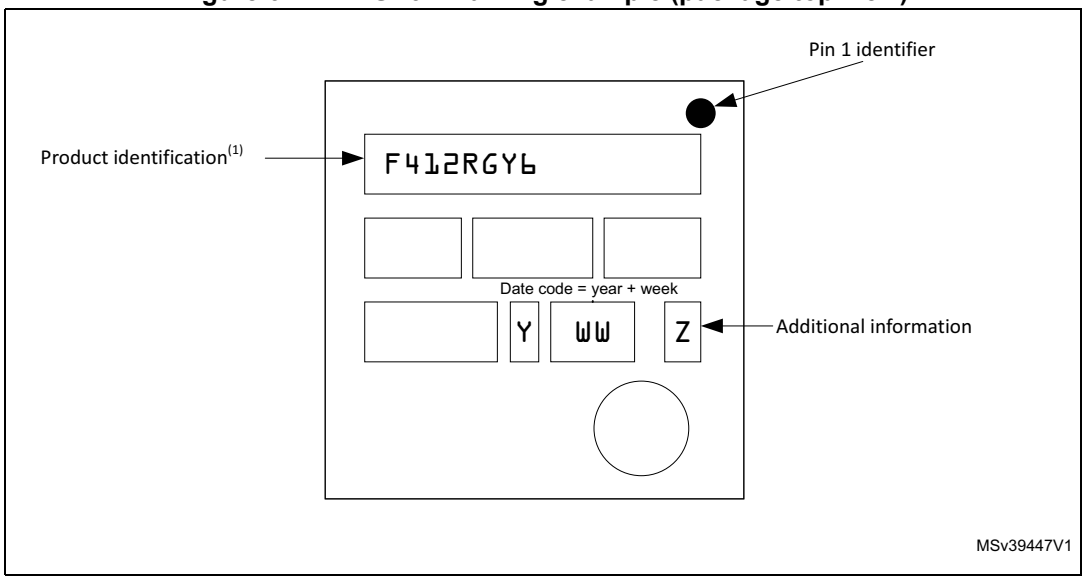
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 62. WLCSP64 marking example (package top view)

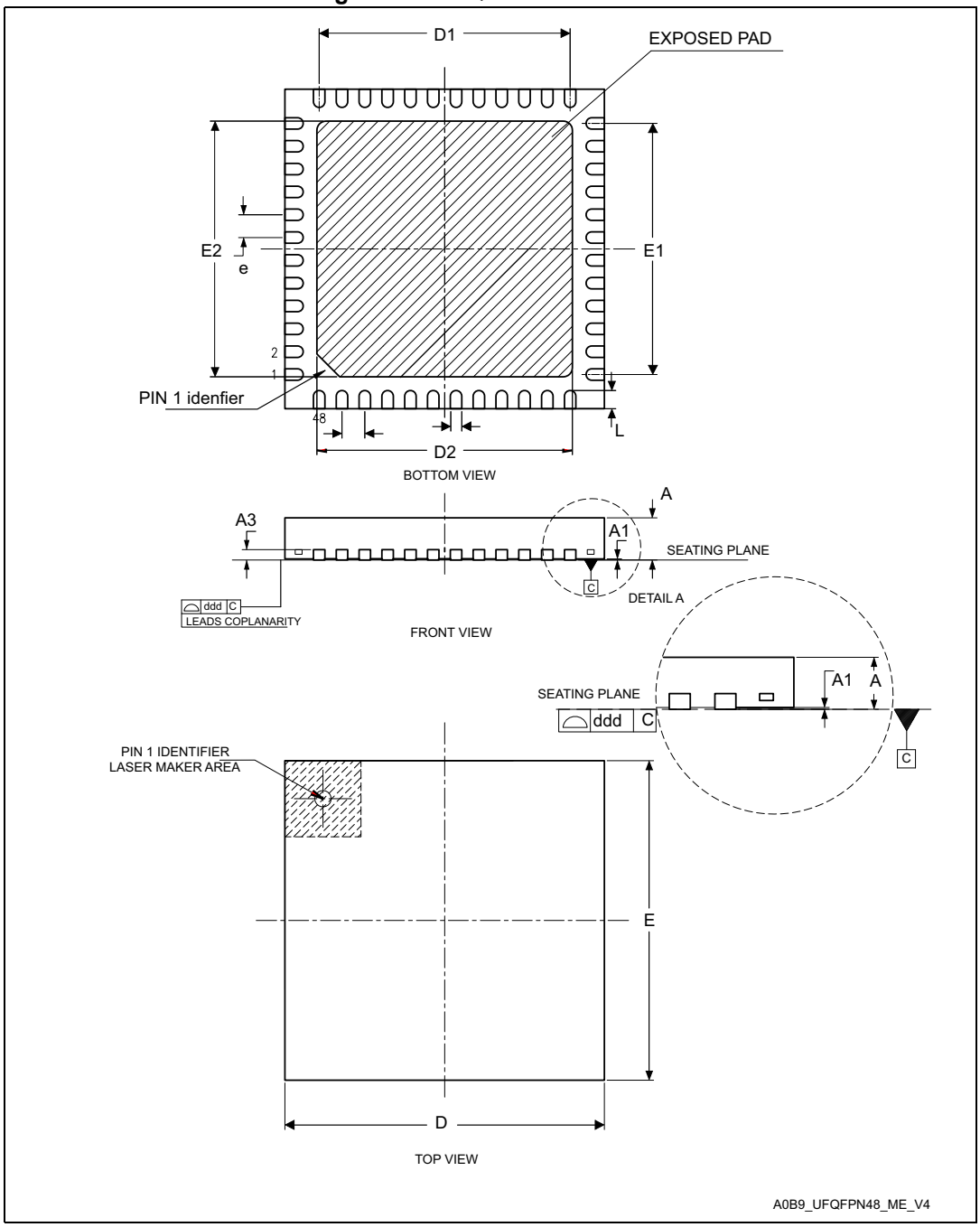


1. Parts marked as “ES” or “E” or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 63. UFQFPN48 – Outline



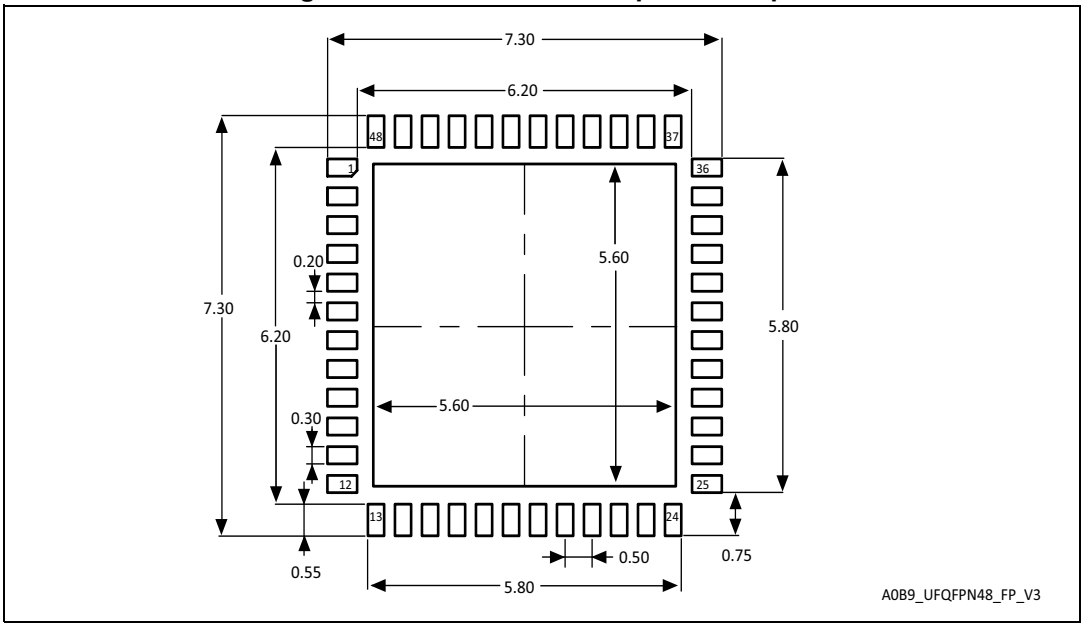
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 101. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
E[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 64. UFQFPN48 – Footprint example



1. Dimensions are expressed in millimeters.

7.4 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 65. LQFP64 - Outline(15)

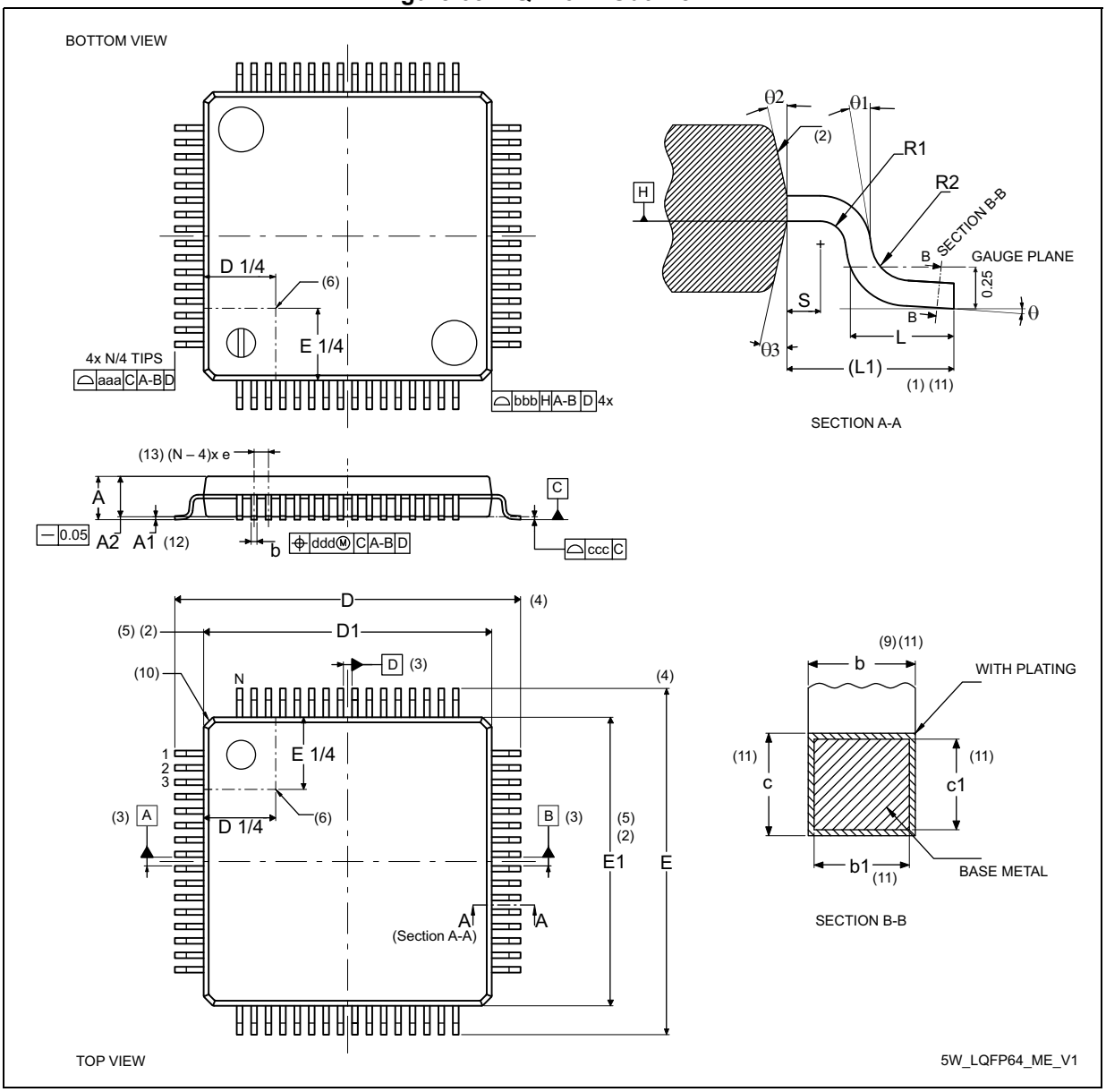


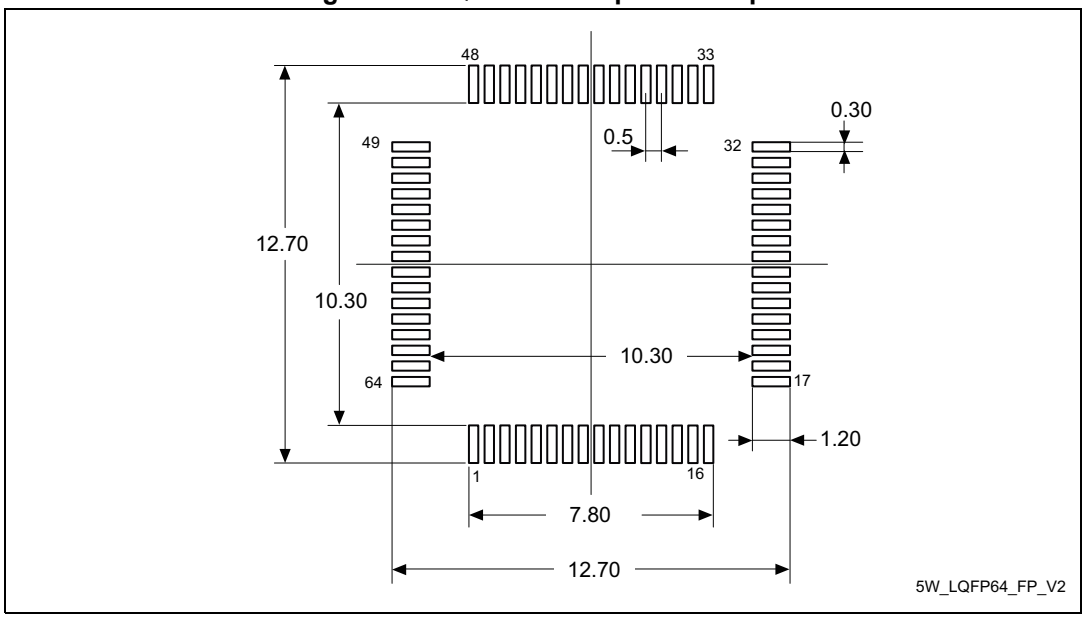
Table 102. LQFP64 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 66. LQFP64 - Footprint example



1. Dimensions are expressed in millimeters.

7.5 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 67. LQFP100 - Outline(15)

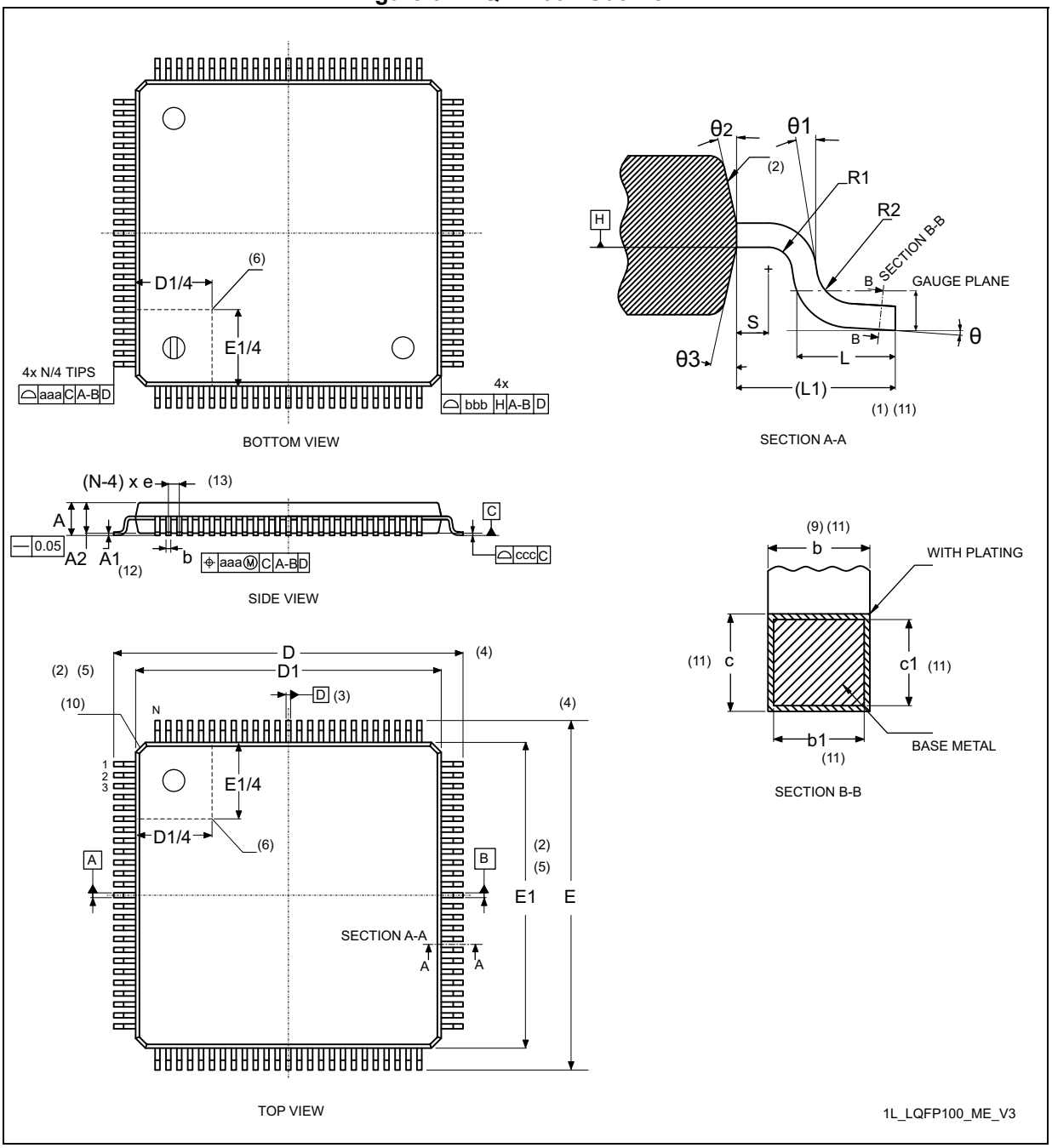


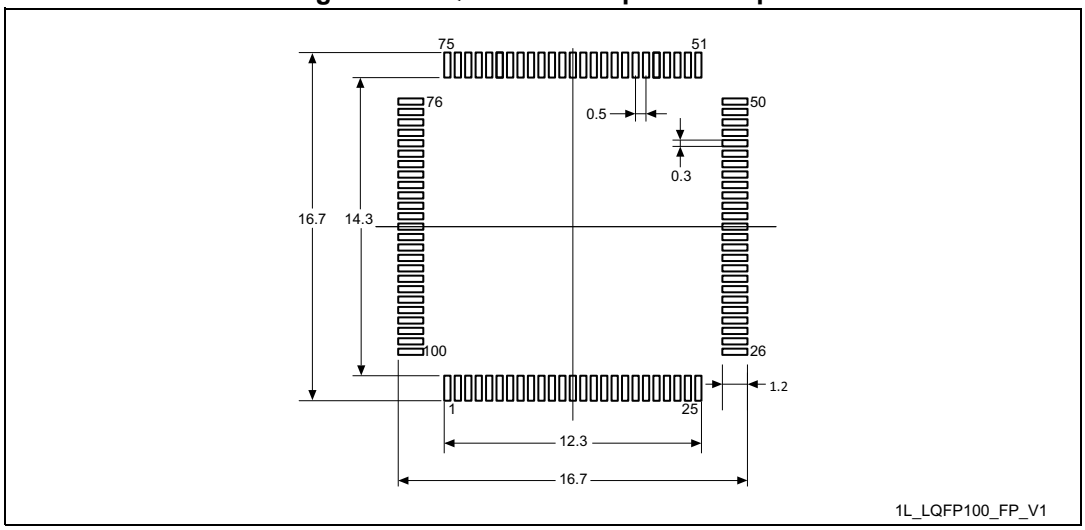
Table 103. LQFP100 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12]	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	16.00 BSC			0.6299 BSC		
D1[2][5]	14.00 BSC			0.5512 BSC		
E[4]	16.00 BSC			0.6299 BSC		
E1[2][5]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1[1][11]	1.00			-	0.0394	-
N[13]	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 68. LQFP100 - Footprint example



1. Dimensions are expressed in millimeters.

7.6 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 69. LQFP144 - Outline(15)

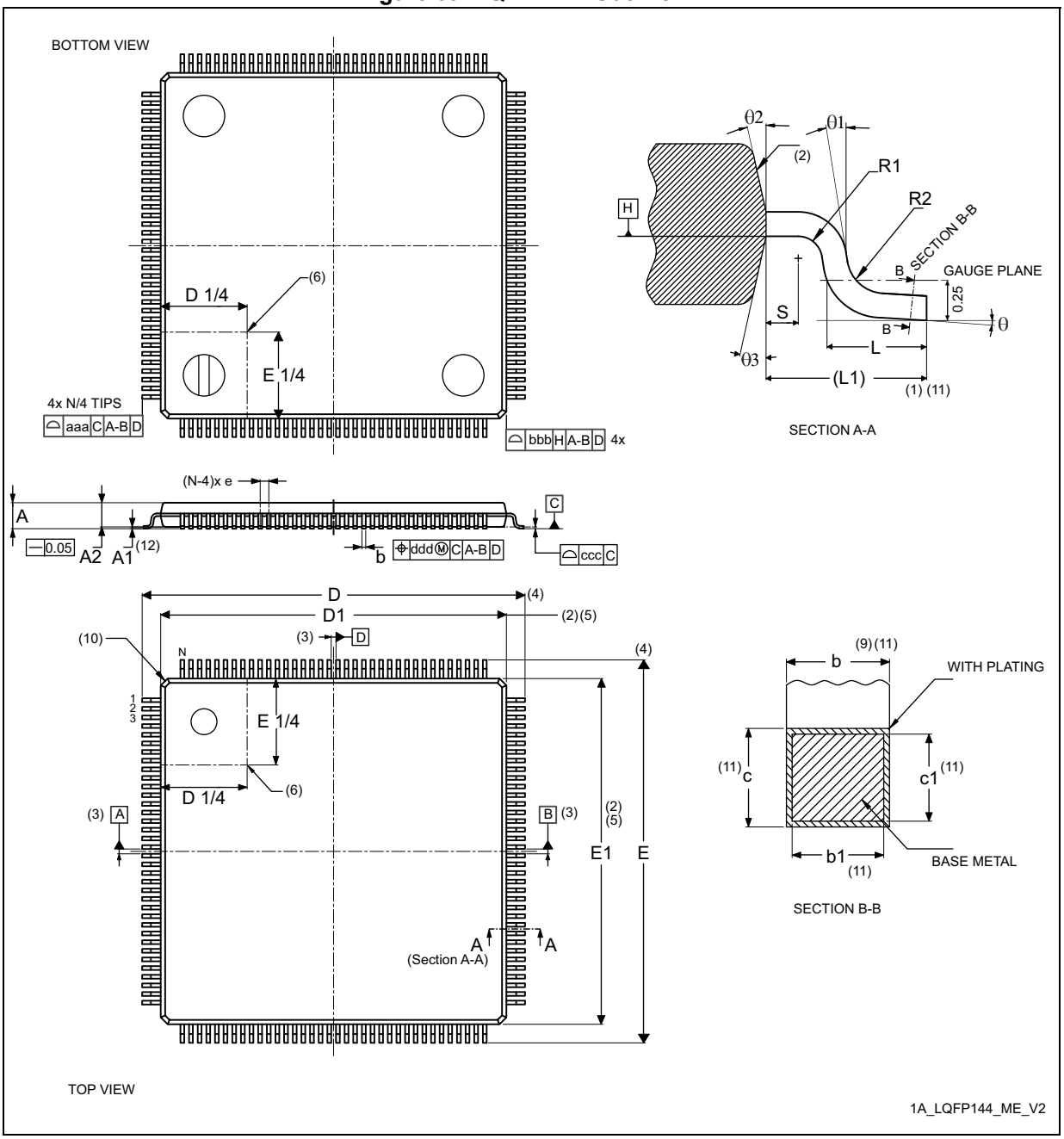


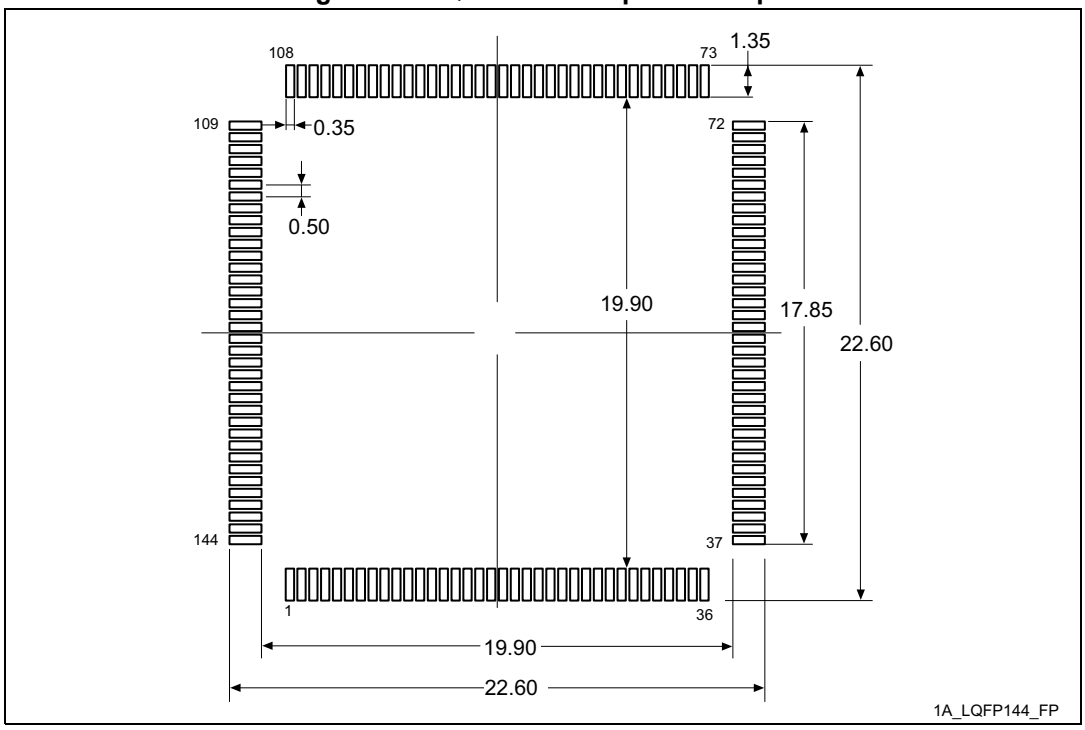
Table 104. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 70. LQFP144 - Footprint example



1. Dimensions are expressed in millimeters.

7.7 UFBGA100 package information (A0C2)

This UFBGA is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 71. UFBGA100 - Outline(13)

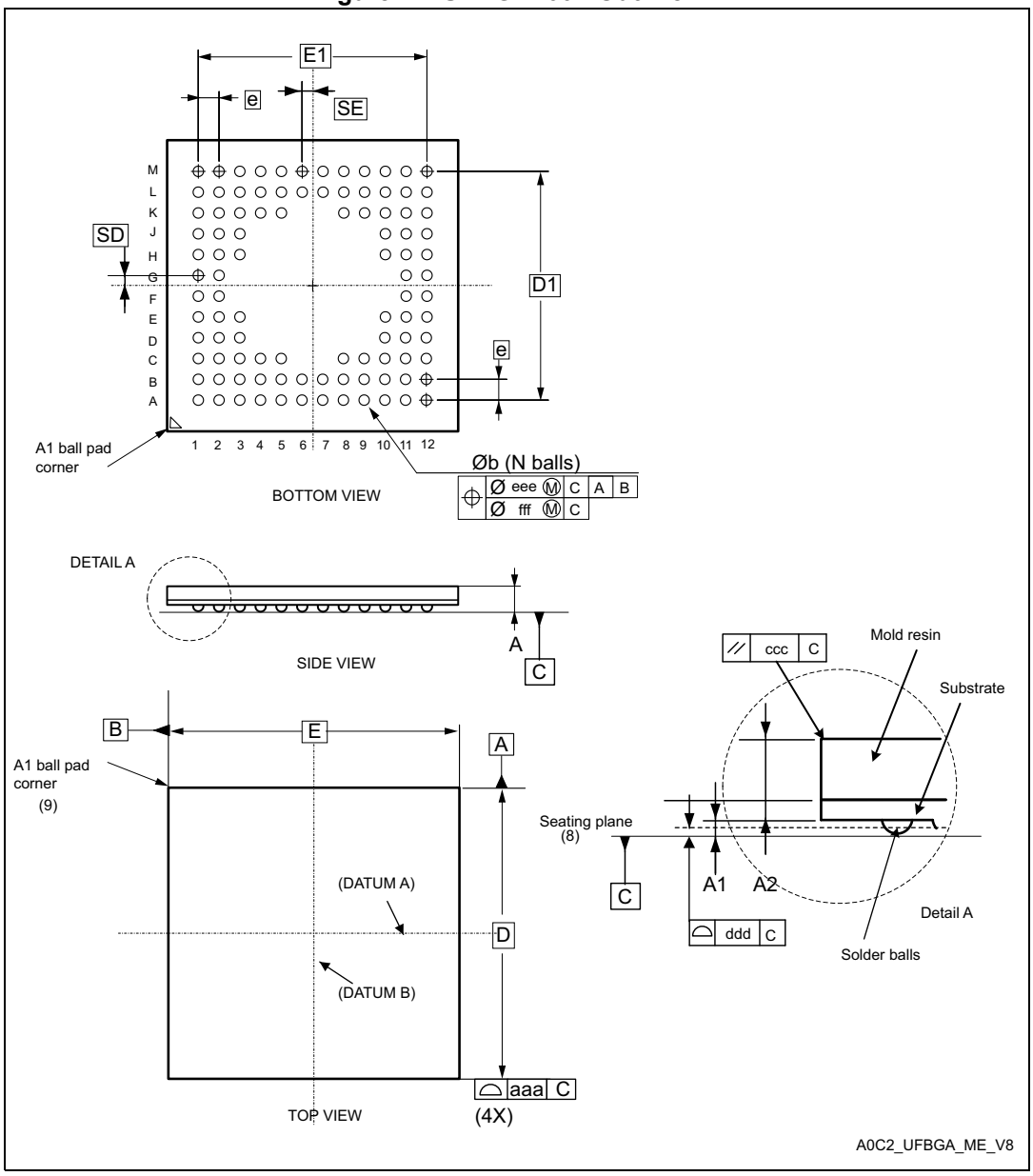


Table 105. UFBGA100 - Mechanical data

Symbol	millimeters(1)			inches(12)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(2)(3)	-	-	0.60	-	-	0.0236
A1(4)	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b(5)	0.23	0.28	0.33	0.0090	0.0110	0.0130
D(6)	7.00 BSC			0.2756 BSC		
D1	5.50 BSC			0.2165 BSC		
E	7.00 BSC			0.2756 BSC		
E1	5.50 BSC			0.2165 BSC		
e(9)	0.50 BSC			0.0197 BSC		
N(11)	100					
SD(12)	0.25 BSC			0.0098 BSC		
SE(12)	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ulta profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 72. UFBGA100 - Footprint example

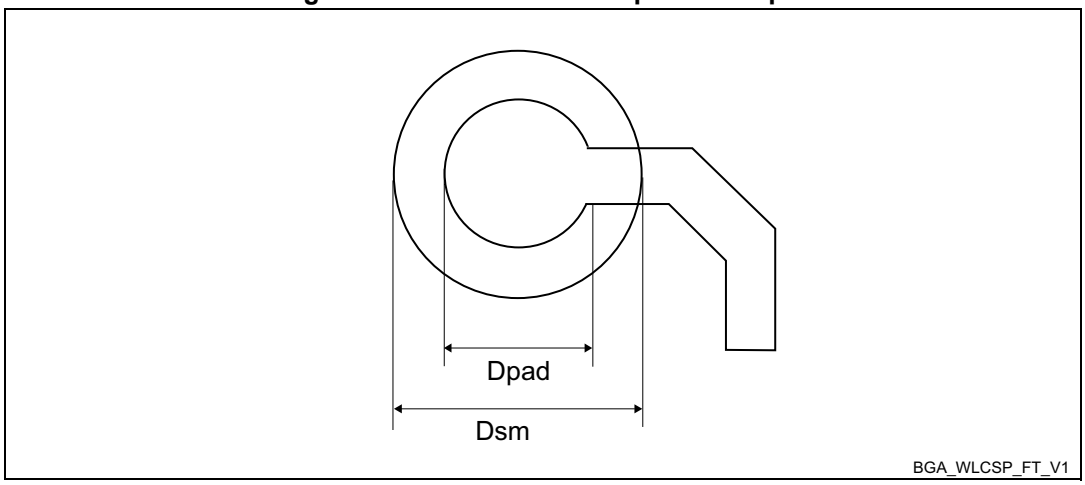


Table 106. UFBGA100 - Example of PCB design rules (0.5 mm pitch BGA)

Dimension	Values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

7.8 UFBGA144 package information (A0Y2)

This UFBGA is a 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 73. UFBGA144 - Outline(13)

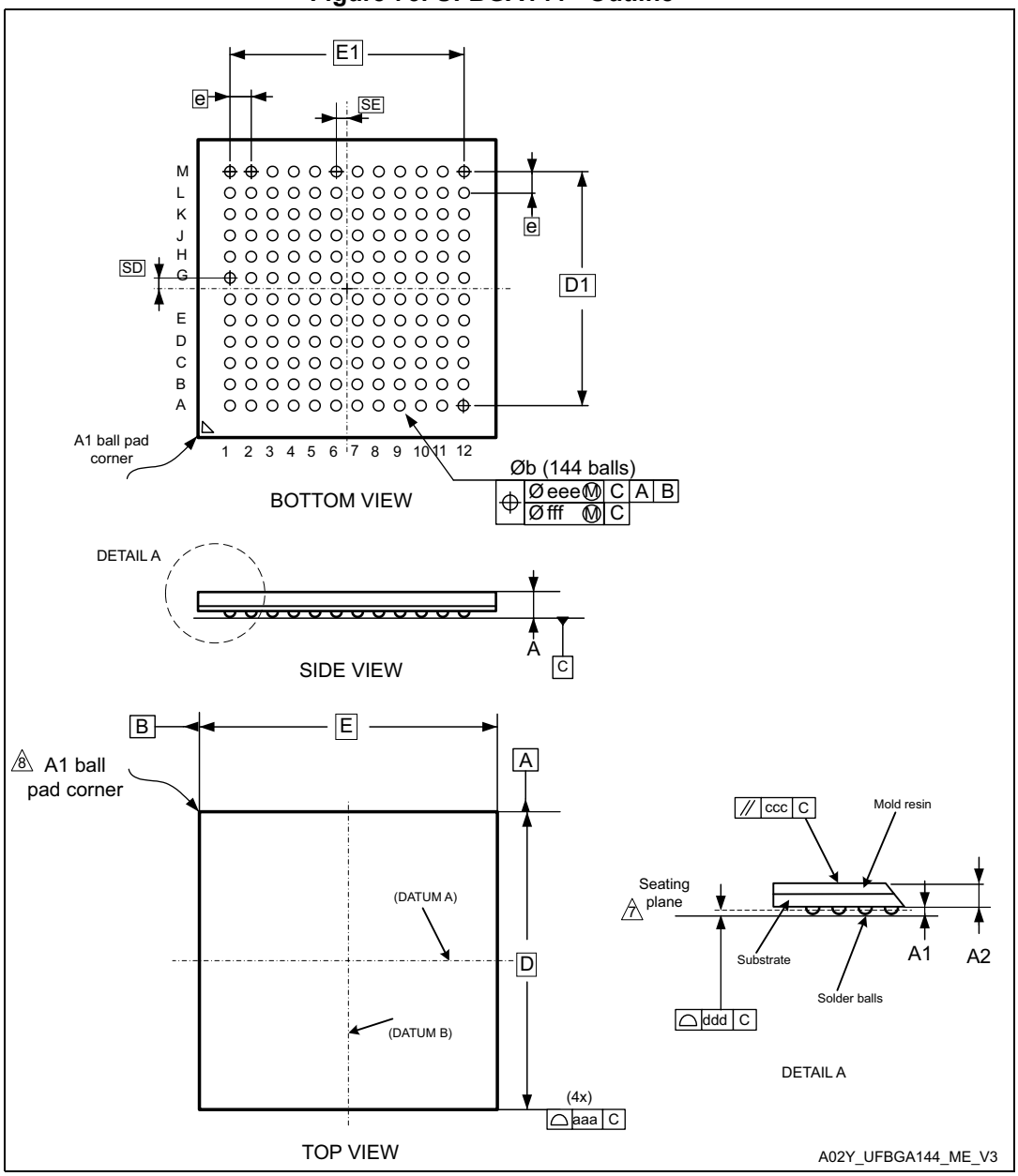


Table 107. UFBGA144 - Mechanical data

Symbol	millimeters(1)			inches(12)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(2)(3)	-	-	0.60	-	-	0.0236
A1(4)	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b(5)	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	10.00 BSC(6)			0.3937 BSC		
D1	8.80 BSC			0.3465 BSC		
E	10.00 BSC			0.3937 BSC		
E1	8.80 BSC			0.3465 BSC		
e(9)	0.80 BSC			0.0315 BSC		
N(11)	144					
SD(12)	0.40 BSC			0.0157 BSC		
SE(12)	0.40 BSC			0.0157 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ulta profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 74. UFBGA144 - Footprint example

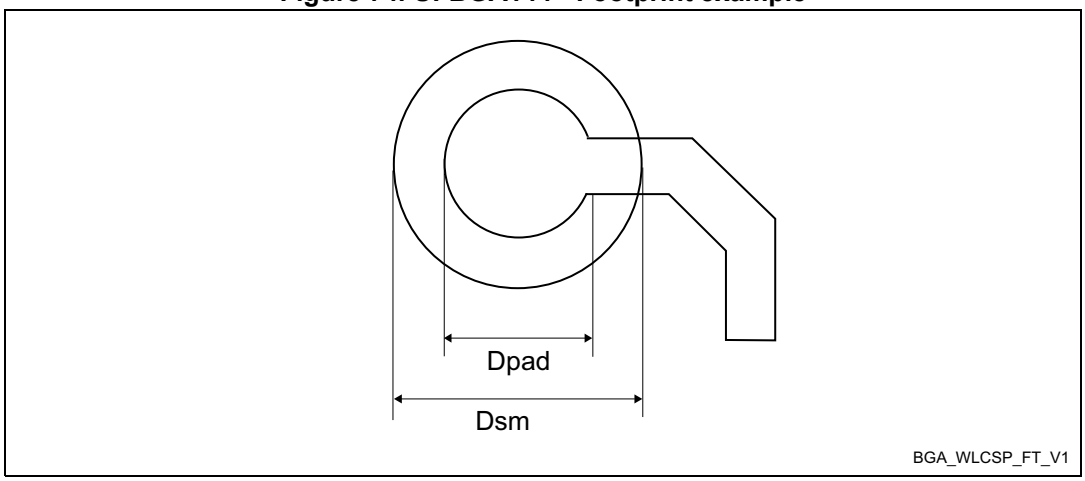


Table 108. UFBGA144 - Example of PCB design rules (0.80 mm pitch BGA)

Dimension	Values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7.9 Package term definition

Table 109. Term definition

Acronym	Definition
BSC	BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
REF	Reference dimension is the numerical value provided for information only, and it is not used in the fabrication and measurement of the part.

7.10 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 16: General operating conditions on page 81*.

The maximum chip-junction temperature, T_J max., in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (PD max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- PD max is the sum of P_{INT} max and $P_{I/O}$ max (PD max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 110. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm	35	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm	47	
	Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	48	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm	57	
	Thermal resistance junction-ambient WLCSP64 - 3.623 x 3.651 mm	51	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm	32	

7.10.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 111. Ordering information scheme

Example: STM32 F 412 C E T 6 P TR

Device family

STM32 = Arm®-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

412 = 412 line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

E = 512 Kbytes of flash memory

G = 1024 Kbytes of flash memory

Package

H = UFBGA 7 x 7 mm

J = UFBGA 10 x 10 mm

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C

7 = Industrial temperature range, -40 to 105 °C

3 = Industrial temperature range, -40 to 125°C

Option

Blank = Standard production

P = Internal regulator disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

Appendix A Recommendations when using the internal reset OFF

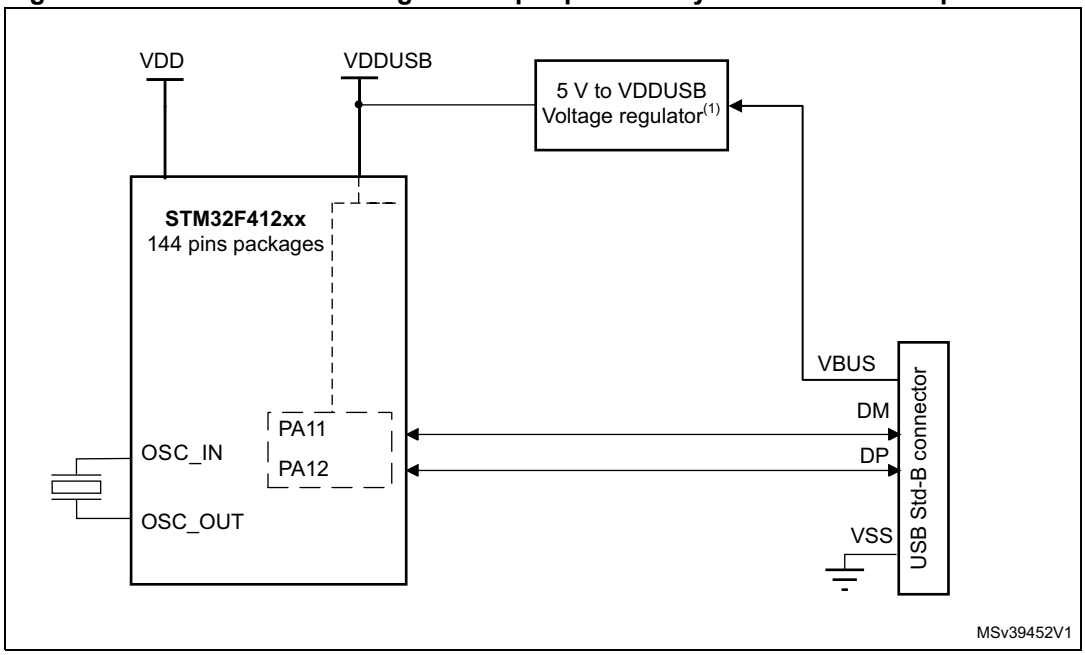
When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Appendix B Application block diagrams

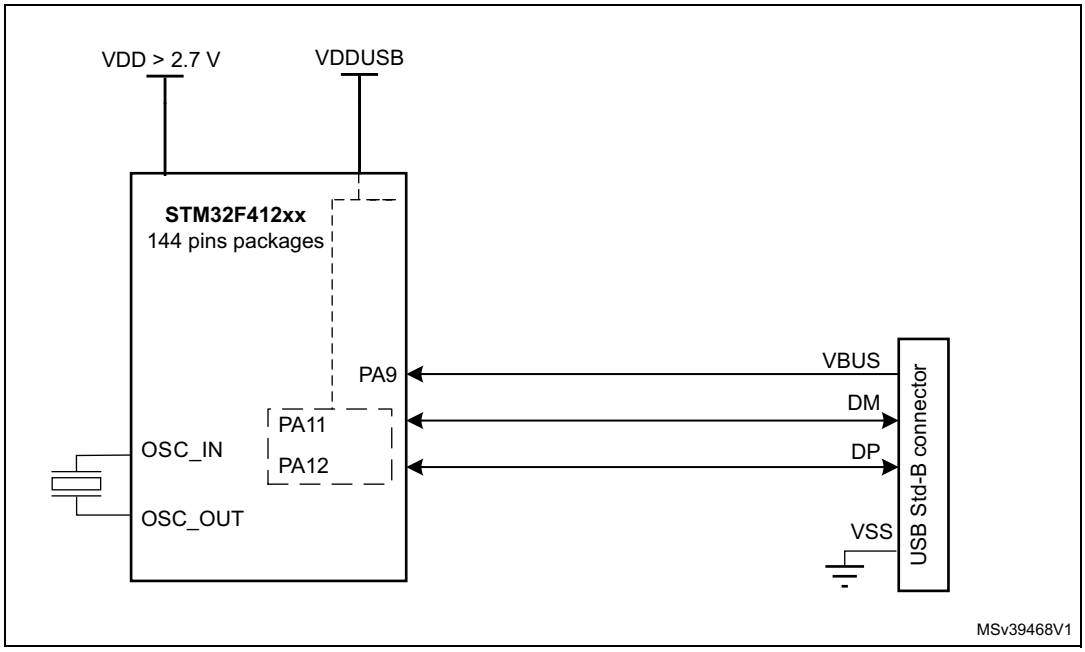
B.1 USB OTG full speed (FS) interface solutions

Figure 75. USB controller configured as peripheral-only and used in Full speed mode



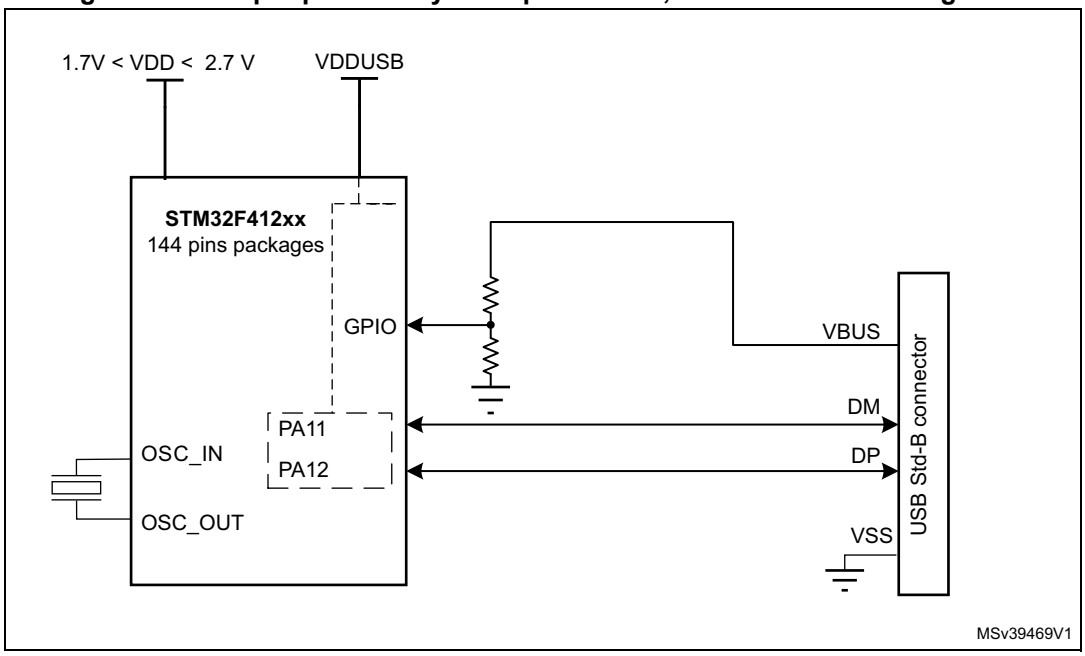
1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 76. USB peripheral-only Full speed mode with direct connection for VBUS sense



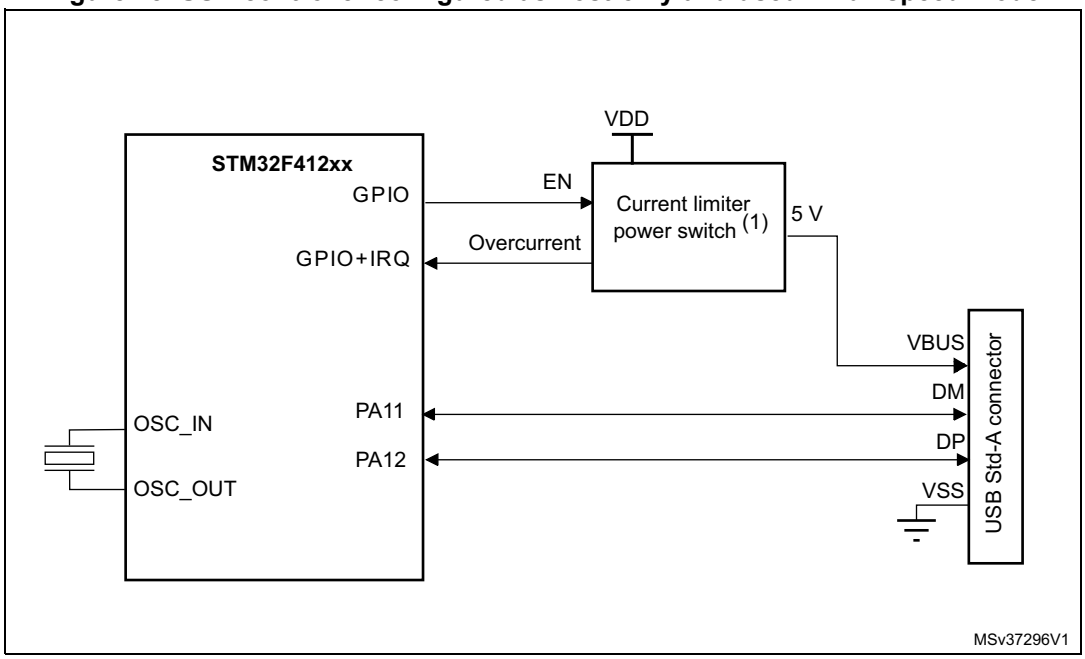
1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 77. USB peripheral-only Full speed mode, VBUS detection using GPIO



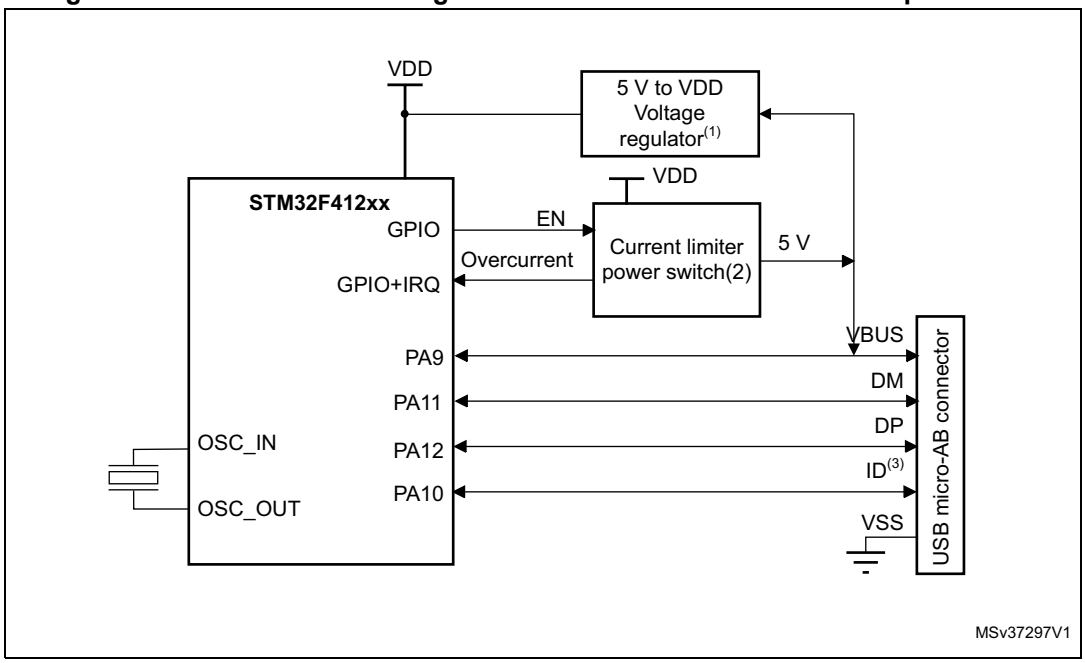
1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 78. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

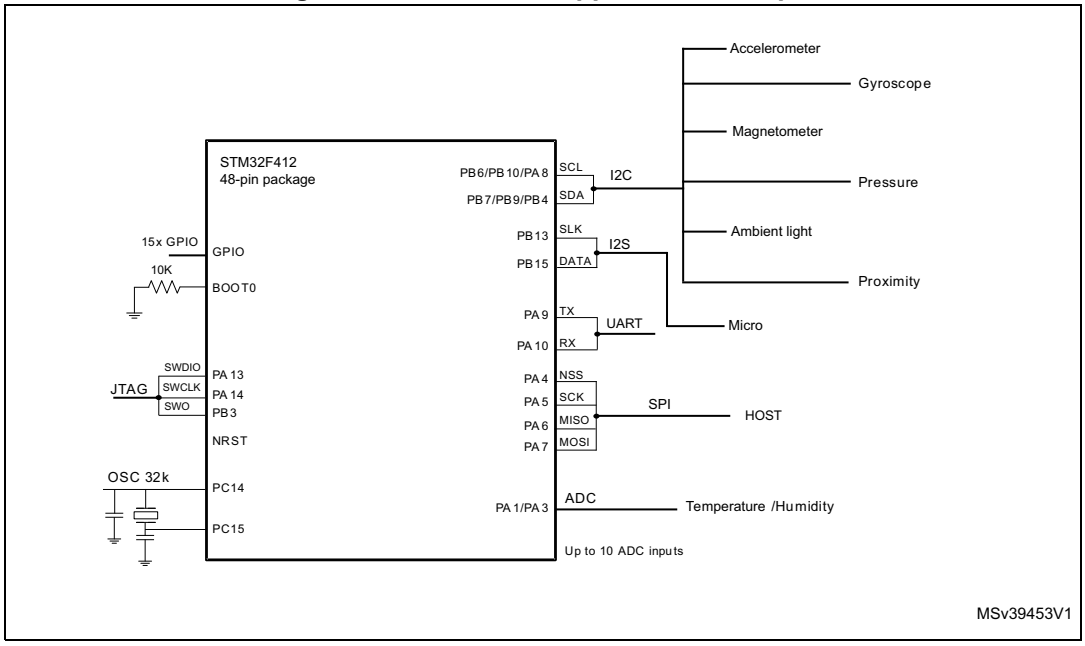
Figure 79. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.

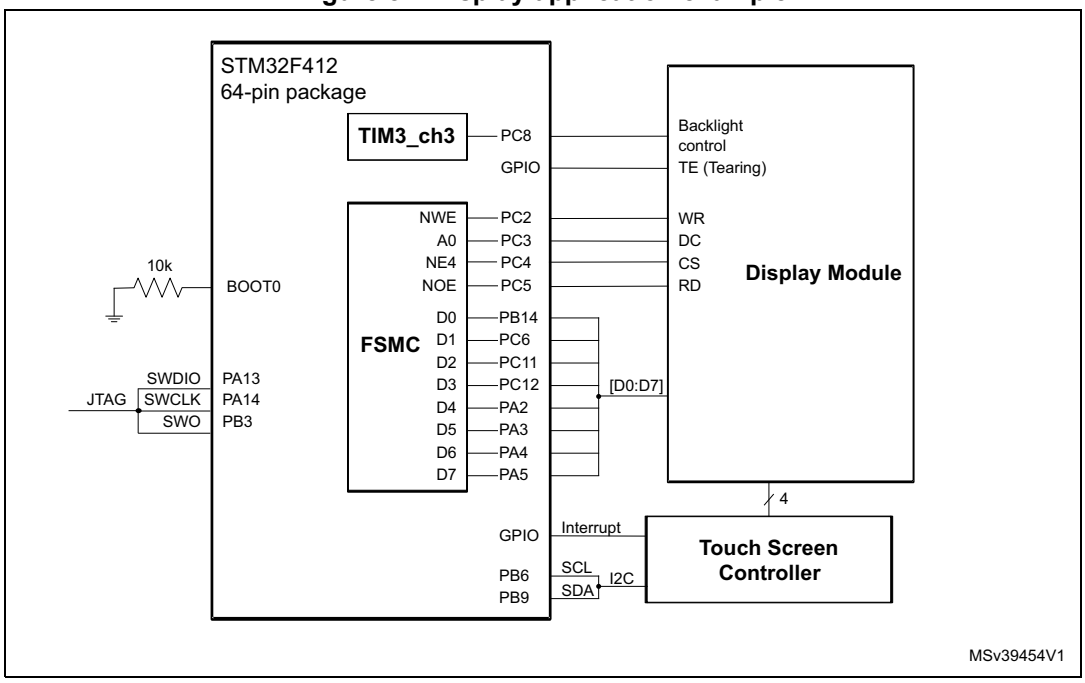
B.2 Sensor Hub application example

Figure 80. Sensor Hub application example



B.3 Display application example

Figure 81. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

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Revision history

Table 112. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
01-Feb-2016	2	Added: – *Table 3: Embedded bootloader interfaces* – *Figure 3: Compatible board design for LQFP144 package* – *Figure 62: WLCSP64 marking example (package top view)* – *Figure 77: UFBGA100 marking example (package top view)* Updated: – *Section 3.17: Power supply schemes* – *Section 3.23: Timers and watchdogs* – *Section 3.32: Universal serial bus on-the-go full-speed (USB_OTG_FS)* – *Figure 1: Compatible board design for LQFP100 package* – *Figure 2: Compatible board design for LQFP64 package* – *Figure 14: STM32F412xE/G LQFP100 pinout* – *Figure 16: STM32F412xE/G UFBGA100 pinout* – *Figure 17: STM32F412xE/G UFBGA144 pinout* – *Figure 20: Input voltage measurement* – *Figure 73: UFBGA144 marking example (package top view)* – *Table 2: STM32F412xE/G features and peripheral counts* – *Table 9: STM32F412xE/G pin definition* – *Table 13: Voltage characteristics* – *Table 14: Current characteristics* – *Table 16: General operating conditions* – *Table 37: Peripheral current consumption* – *Table 52: EMS characteristics for LQFP144 package* – *Table 64: FMPI^{2}C characteristics*
25-Mar-2016	3	Added: – *Figure 76: USB peripheral-only Full speed mode with direct connection for VBUS sense* – *Figure 77: USB peripheral-only Full speed mode, VBUS detection using GPIO* Updated: – *Figure 15: STM32F412xE/G LQFP144 pinout* – *Section 6.3.6: Supply current characteristics* – *Table 9: STM32F412xE/G pin definition* – *Table 11: STM32F412xE/G alternate functions* – *Table 12: STM32F412xE/G register boundary addresses* – *Table 16: General operating conditions* – *Table 37: Peripheral current consumption* – *Table 97: Dynamic characteristics: eMMC characteristics VDD = 1.7 V to 1.9 V*

Table 112. Document revision history

Date	Revision	Changes
27-May-2016	4	Updated: – *Section 3.23.2: General-purpose timers (TIMx)* – *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V* – *Table 23: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V* – *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from flash memory- V_{DD} = 1.7 V* – *Table 25: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from flash memory - V_{DD} = 3.6 V* – *Table 26: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from flash memory - V_{DD} = 3.6 V* – *Table 27: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from flash memory - V_{DD} = 1.7 V* – *Table 28: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from flash memory - V_{DD} = 3.6 V* – *Table 29: Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V* – *Table 30: Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V* – *Table 38: Low-power mode wakeup timings(1)* – *Figure 38: I^2C bus AC waveforms and measurement circuit* – *Figure 39: FMPI^2C timing diagram and measurement circuit*

Table 112. Document revision history

Date	Revision	Changes
23-May-2017	5	Updated: – *Section 2: Description* – *Table 2: STM32F412xE/G features and peripheral counts* – *Section 3.19.1: Regulator ON* – *Section 3.19.2: Regulator OFF* – *Table 4: Regulator ON/OFF and internal power supply supervisor availability* – *Table 15: Thermal characteristics* – *Table 16: General operating conditions* – *Table 21: Embedded reset and power control block characteristics* – Table from: *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V* to *Table 35: Typical and maximum current consumptions in V_{BAT} mode* – *Figure 24: Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)* – *Figure 25: Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)* – *Table 43: HSI oscillator characteristics* – *Table 44: LSI oscillator characteristics* – *Table 51: Flash memory endurance and data retention* – *Table 55: Electrical sensitivities* – *Table 57: I/O static characteristics* – *Table 88: Asynchronous multiplexed PSRAM/NOR read timings* – Note *1.* in *Figure 62: WLCSP64 marking example (package top view)* – Note *1.* in *Figure 65: UFQFPN48 marking example (package top view)* – Note *1.* in *Figure 68: LQFP64 marking example (package top view)* – Note *1.* in *Figure 71: LQFP100 marking example (package top view)* – Note *1.* in *Figure 74: LQFP144 marking example (package top view)* – Note *1.* in *Figure 77: UFBGA100 marking example (package top view)* – Note *1.* in *Figure 73: UFBGA144 marking example (package top view)* – *Table 111: Ordering information scheme*

Table 112. Document revision history

Date	Revision	Changes
13-Jul-2017	6	Updated: – *Table 2: STM32F412xE/G features and peripheral counts* – *Table 7: USART feature comparison* – *Table 9: STM32F412xE/G pin definition* – *Section 3.29: Digital filter for sigma-delta modulators (DFSDM)* – *Table 108: UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data* Added: – *Section 4.1: WLSCP64 pinout description* – *Section 4.2: UFQFPN48 pinout description* – *Section 4.3: LQFP64 pinout description* – *Section 4.4: LQFP100 pinout description* – *Section 4.5: LQFP144 pinout description* – *Section 4.6: UFBGA100 pinout description* – *Section 4.7: UFBGA144 pinout description* – *Section 4.8: Pin definition* – *Table 10: FSMC pin definition*
19-Dec-2017	7	Updated: – *Table 23: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V* – *Table 23: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V* – *Table 32: Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V* – *Table 34: Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V*

Table 112. Document revision history

Date	Revision	Changes
10-Mar-2023	8	Updated: – *Section 3.32: Universal serial bus on-the-go full-speed (USB_OTG_FS)* – *Table 9: STM32F412xE/G pin definition* – *Section :* – *Section 7.4: LQFP64 package information (5W)* – *Section 7.5: LQFP100 package information (1L)* – *Section 7.6: LQFP144 package information (1A)* – *Section 7.7: UFBGA100 package information (A0C2)* – *Section 7.8: UFBGA144 package information (A0Y2)* Added: – *Section 7.9: Package term definition* – *Section 9: Important security notice*
30-Jan-2024	9	Updated: – *Section 7.2: WLCSP64 package information (A04F)* – *Section 7.3: UFQFPN48 package information (A0B9)* – *Section 7.4: LQFP64 package information (5W)* – *Section 7.5: LQFP100 package information (1L)* – *Section 7.6: LQFP144 package information (1A)* – *Section 7.7: UFBGA100 package information (A0C2)* – *Section 7.8: UFBGA144 package information (A0Y2)* Added: – *Section 7.1: Device marking* Deleted all device marking except the one of WLCSP package

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