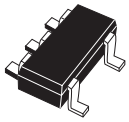
# STM6717/6718/6719/6720
# STM6777/6778/6779/6780

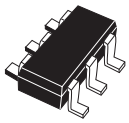
## Dual/triple ultra-low voltage supervisors with push-button reset (with delay option)

## Features

- Primary supply ($V_{CC1}$) monitor.
  Fixed (factory-programmed) reset thresholds: 4.63 V to 1.58 V
- Secondary supply ($V_{CC2}$) monitor (STM6717/18/19/20/77/78)
- Fixed (factory-programmed) reset thresholds: 3.08 V to 0.79 V
- Tertiary supply monitor (using externally adjustable RSTIN): 0.626 V internal reference
- $\overline{RST}$ outputs (push-pull or open drain); state guaranteed if $V_{CC1}$ or $V_{CC2} \geq 0.8$ V
- Reset delay time ($t_{rec}$) on power-up: 13.2 ms, 210 ms, 900 ms (typ)
- Manual reset input ($\overline{MR}$)
- Optional delayed manual reset input (MRC) with external capacitor (STM6777/78/79/80)
- Low supply current - 11 µA (typ), $V_{CC1} = V_{CC2} = 3.6$ V
- Operating temperature: –40 °C to 85 °C (industrial grade)



SOT23-5 (WY)



SOT23-6 (WB)

**Table 1. Device summary**

| Part number | Monitored voltages | | | Manual reset input ($\overline{MR}$) | Delayed $\overline{MR}$ pin (MRC) | Reset output ($\overline{RST}$) | | Package |
|---|---|---|---|---|---|---|---|---|
| | $V_{CC1}$ | $V_{CC2}$ | RSTIN | | | Active-low (push-pull) | Active-low (open drain) | |
| STM6717 | ✔ | ✔ | | ✔ | | | ✔ | WY |
| STM6718 | ✔ | ✔ | | ✔ | | ✔ | | WY |
| STM6719 | ✔ | ✔ | ✔ | ✔ | | | ✔ | WB |
| STM6720 | ✔ | ✔ | ✔ | ✔ | | ✔ | | WB |
| STM6777 | ✔ | ✔ | | ✔ | ✔ | | ✔ | WB |
| STM6778 | ✔ | ✔ | | ✔ | ✔ | ✔ | | WB |
| STM6779 | ✔ | | ✔ | ✔ | ✔ | | ✔ | WB |
| STM6780 | ✔ | | ✔ | ✔ | ✔ | ✔ | | WB |

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# 1 Description

The STM6717/18/19/20 and STM6777/78/79/80 supervisors are a family of low-voltage/low-supply current processor (micro or DSP) supervisors, designed to monitor two (or three) system power supply voltages. They are targeted at applications such as set-top boxes (STBs), portable, battery-powered systems, networking, and communication systems.

All device options have a push-button-type manual reset input ($\overline{MR}$). The STM6777/78/79/80 also includes an option which enables the user to delay the start of the manual reset process from 6 µs (MRC pin left open) or more with external capacitor. The delay is implemented by connecting the appropriately sized capacitor between the MRC pin and $V_{SS}$ (typical 4 s delay with a 3.3 µF capacitor, see *Table 7 on page 21*).

Two of the three supplies monitored ($V_{CC1}$ and $V_{CC2}$) have fixed (customer-selectable, factory-trimmed) thresholds ($V_{RST1}$ and $V_{RST2}$). The third voltage is monitored using an externally adjustable RSTIN threshold (0.626 V internal reference).

If any of the three monitored voltages drop below its factory-trimmed or adjustable thresholds, or if $\overline{MR}$ is asserted to logic low, a $\overline{RST}$ is asserted (driven low). Once asserted, $\overline{RST}$ is maintained at low for a minimum delay period ($t_{rec}$) after ALL supplies rise above their respective thresholds and $\overline{MR}$ returns to high. These devices are guaranteed to be in the correct reset output logic state when $V_{CC1}$ and/or $V_{CC2}$ is greater than 0.8 V.

These devices are available in standard 5-pin or 6-pin SOT23 packages (see *Table 1 on page 1*).

**Figure 1. Logic diagram (STM6717/18)**

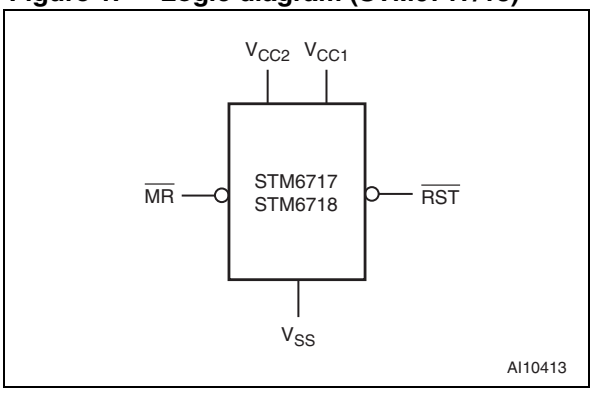



**Figure 2. Logic diagram (STM6777/78)**

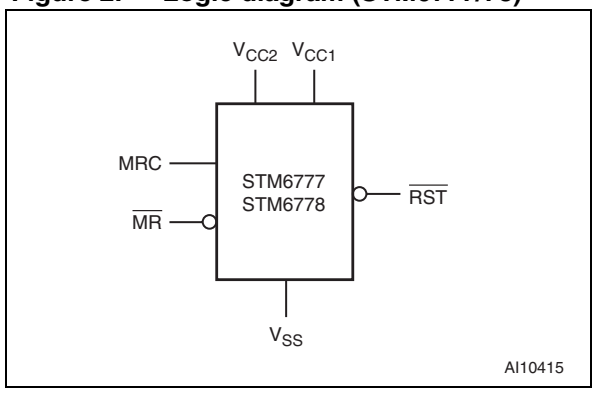



**Figure 3. Logic diagram (STM6719/20)**

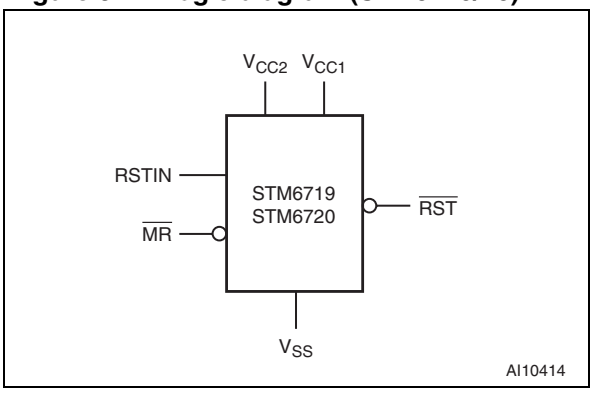



**Figure 4. Logic diagram (STM6779/80)**

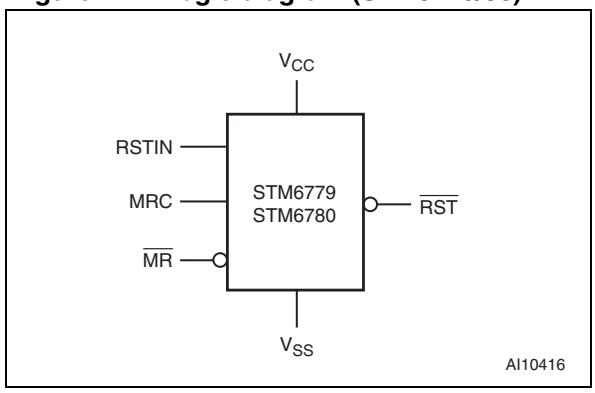



**Table 2. Signal names**

| | |
|---|---|
| $\overline{MR}$ | Push-button reset input |
| MRC | Manual reset delay input |
| $\overline{RST}$ | Active-low reset output |
| $V_{CC1}$ | Primary supply voltage input |
| $V_{CC2}$ | Secondary supply voltage input |
| RSTIN | Adjustable reset comparator input |
| $V_{SS}$ | Ground |

Figure 5. STM6717/18 SOT23-5 connections

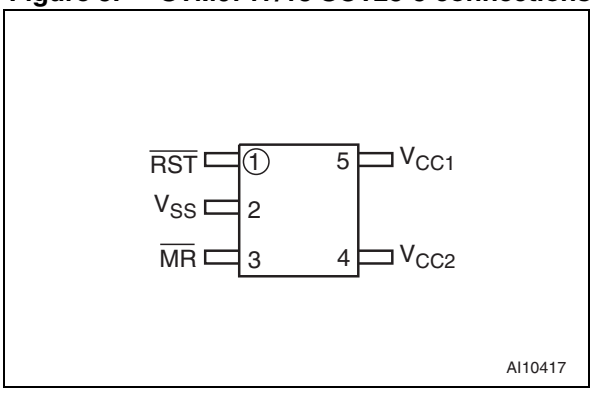



Figure 6. STM6777/78 SOT23-6 connections

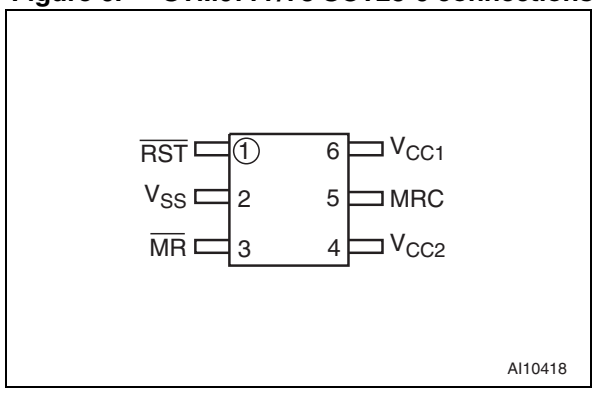



Figure 7. STM6719/20 SOT23-6 connections

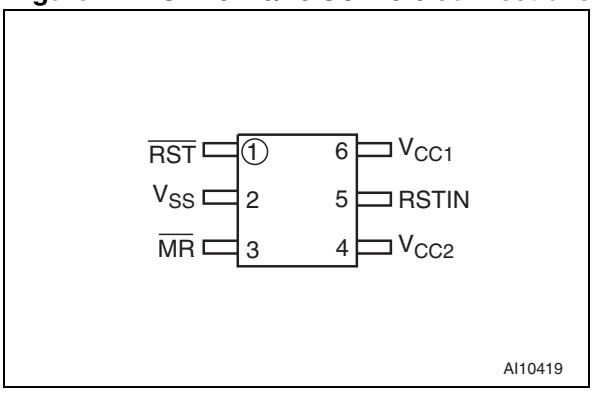
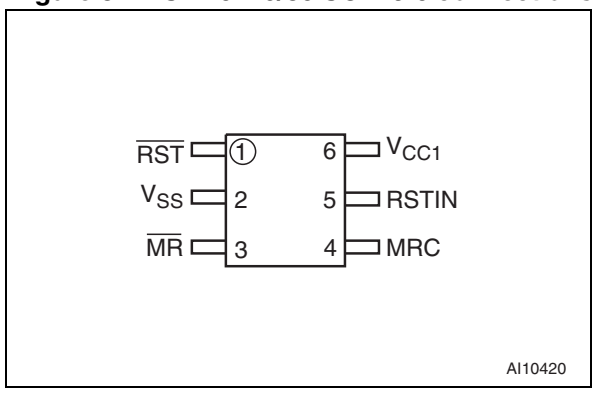



Figure 8. STM6779/80 SOT23-6 connections




## 1.1 Pin descriptions

### 1.1.1 Active-low, push-pull reset output ($\overline{RST}$) - STM6718/20/78/80

The $\overline{RST}$ pin is driven low and stays low whenever $V_{CC1}$ or $V_{CC2}$ or RSTIN falls below its factory-trimmed or adjustable reset threshold or when $\overline{MR}$ goes to logic low. It remains low for $t_{rec}$ after ALL supply voltages being monitored rise above their reset thresholds and $\overline{MR}$ goes from low to high. (Push-pull outputs are referenced to $V_{CC1}$.)

### 1.1.2 Active-low, open drain reset output ($\overline{RST}$) - STM6717/19/77/79

The $\overline{RST}$ pin is driven low and stays low whenever $V_{CC1}$ or $V_{CC2}$ or RSTIN falls below its factory-trimmed or adjustable reset threshold or when $\overline{MR}$ goes to logic low. It remains low for $t_{rec}$ after ALL supply voltages being monitored rise above their reset thresholds and $\overline{MR}$ goes from low to high. Connect an external pull-up resistor to $V_{CC1}$. A 10 kΩ pull-up resistor should be sufficient for most applications.

### 1.1.3 Push-button reset input ($\overline{MR}$)

When $\overline{MR}$ goes low the $\overline{RST}$ output is driven low. $\overline{RST}$ remains low as long as $\overline{MR}$ is low and for $t_{rec}$ after $\overline{MR}$ returns to high. This active-low input has an internal 50 kΩ pull-up resistor to

$V_{CC1}$. It can be driven from a TTL or CMOS logic line, or with open drain/collector outputs, or connected to $V_{SS}$ through a switch. If unused, leave this pin open or connect it to $V_{CC1}$.

Connect a normally open momentary switch from $\overline{MR}$ to $V_{SS}$; external debounce circuitry is not required. (If $\overline{MR}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1µF capacitor from $\overline{MR}$ to $V_{SS}$ provides additional noise immunity.

### 1.1.4 Manual reset delay input (MRC) - STM6777/78/79/80)

This pin is either left open or connected to $V_{SS}$ via a capacitor. By selecting the appropriate capacitor, the manual reset process, initiated by pressing the push-button manual reset input, can be delayed by any value from 6 µs or more (see *Table 7 on page 21*).

### 1.1.5 Primary supply voltage monitoring input ($V_{CC1}$)

It also is the input for the primary reset threshold monitor. Available fixed (customer-selectable, factory-programmed) reset thresholds include 4.63 V to 1.58 V.

### 1.1.6 Secondary supply voltage monitoring input ($V_{CC2}$)

This function is available on the STM6717/18/19/20/77/78. Fixed (customer-selectable, factory-programmed) reset thresholds include 3.08 V to 0.79 V.

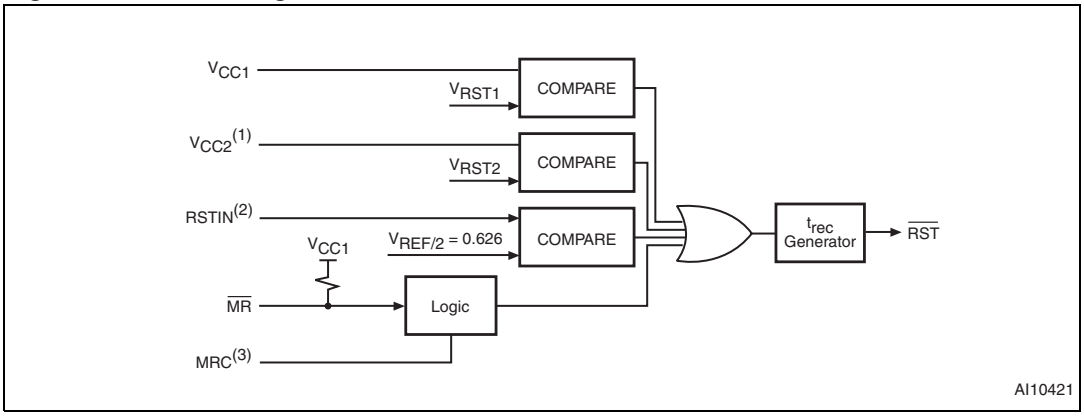
### 1.1.7 Adjustable reset comparator input (RSTIN; STM6719/20/79/80)

This is a high impedance input. $\overline{RST}$ is driven low when the voltage at the RSTIN pin falls below 0.626 V (internal reference voltage at this comparator). The monitored voltage reset threshold is set with an external resistor-divider network.

**Table 3. Pin functions**

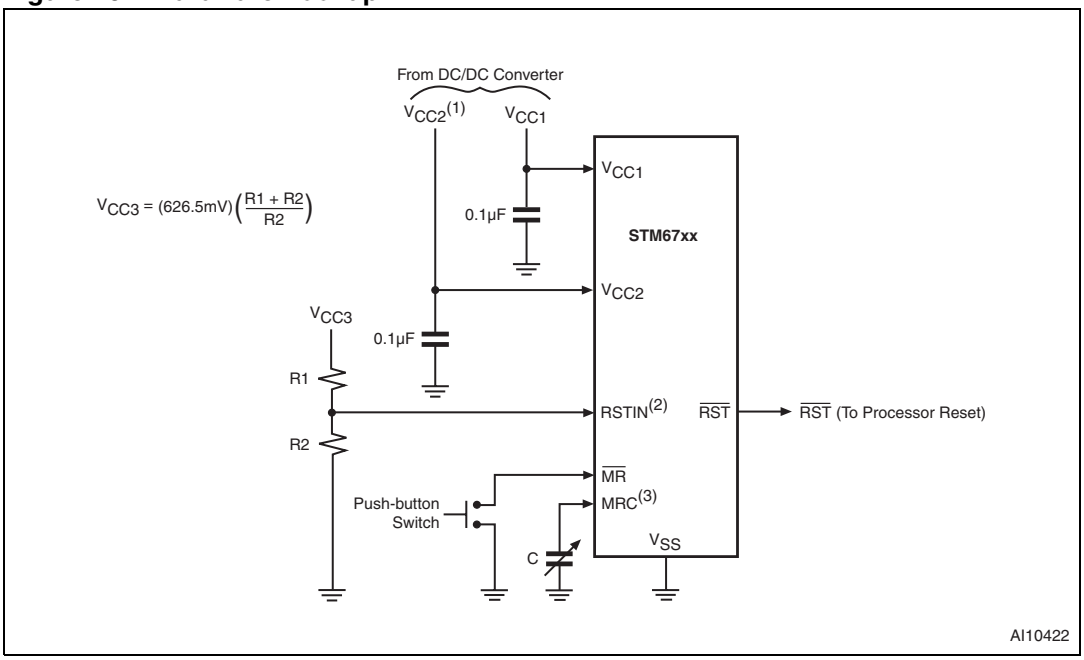
| Pin | | | | Name | Function |
|---|---|---|---|---|---|
| STM6717 STM6718 | STM6719 STM6720 | STM6777 STM6778 | STM6779 STM6780 | | |
| 1 | 1 | 1 | 1 | $\overline{RST}$ | Active-low reset output |
| 3 | 3 | 3 | 3 | $\overline{MR}$ | Push-button reset input |
| — | — | 5 | 4 | MRC | Manual reset delay input |
| 5 | 6 | 6 | 6 | $V_{CC1}$ | Primary supply voltage input |
| 4 | 4 | 4 | — | $V_{CC2}$ | Secondary supply voltage input |
| — | 5 | — | 5 | RSTIN | Adjustable reset comparator input |
| 2 | 2 | 2 | 2 | $V_{SS}$ | Ground |

**Figure 9. Block diagram**




1. $V_{CC2}$ input is available on STM6717/18/19/20/77/78.
2. RSTIN available only on STM6719/20/79/80.
3. MRC available only on STM6777/78/79/80.

**Figure 10. Hardware hookup**




1. $V_{CC2}$ is available only on STM6717/18/19/20/77/78.
2. RSTIN available only on STM6719/20/79/80.
3. MRC available only on STM6777/78/79/80.

# 2 Operation

## 2.1 Applications information

1. Interfacing to processors with bi-directional reset pins

   Most processors with bi-directional reset pins can interface directly to the open drain $\overline{RST}$ outputs (STM6717/19/77/79). Systems simultaneously requiring a push-pull $\overline{RST}$ output and a bi-directional reset interface can be in logic contention. To prevent this contention, connect a 4.7 kΩ resistor between $\overline{RST}$ and the processor's reset I/O as shown in *Figure 11*.

2. Ensuring a valid $\overline{RST}$ output down to $V_{CC}$ = 0 V

   The STM67xx supervisors are guaranteed to be in the correct $\overline{RST}$ output logic state when $V_{CC1}$ and/or $V_{CC2}$ is greater than 0.8 V. In applications which require valid reset levels down to $V_{CC}$ = 0, a pull-down resistor to active-low outputs (push-pull only, see *Figure 12*) will ensure that the reset line is valid while the reset output can no longer sink or source current. This scheme does NOT work with the open drain outputs of the STM6717/19/77/79.

   The resistor value used is not critical, but it must be large enough not to load the reset output when $V_{CC}$ is above the reset threshold. For most applications, 100 kΩ is adequate.

**Figure 11. STM67xx interface to processor with bi-directional reset pins**

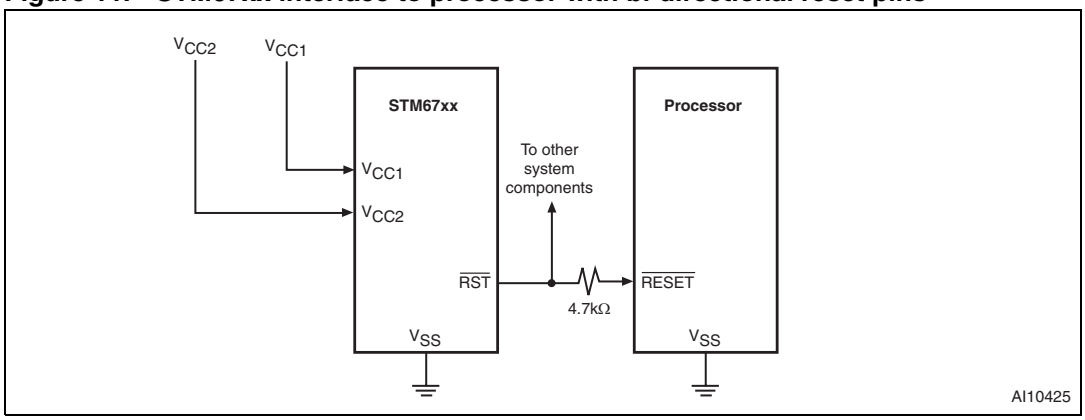
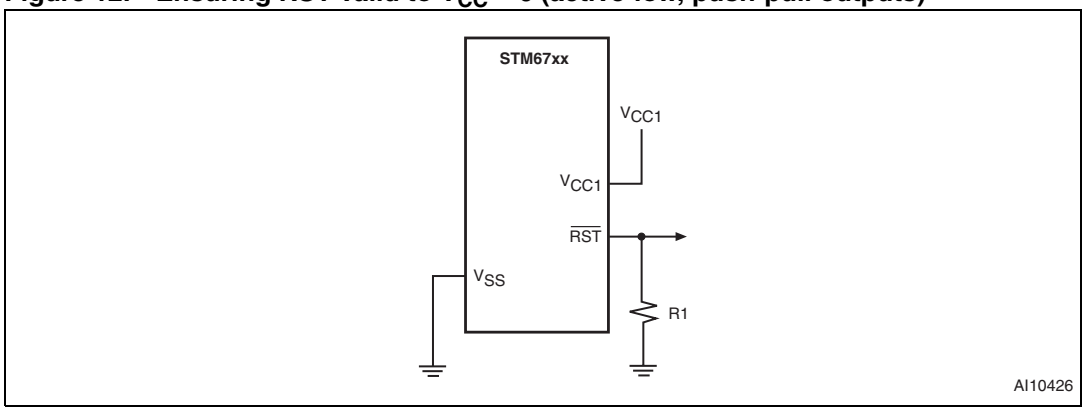



**Figure 12. Ensuring $\overline{RST}$ valid to $V_{CC}$ = 0 (active-low, push-pull outputs)**



# 3 Typical operating characteristics

*Note: Typical values are at $T_A$ = 25 °C unless otherwise noted.*

**Figure 13. Supply current vs. temperature ($V_{CC1}$ = 5.5 V; $V_{CC2}$ = 3.6 V)**

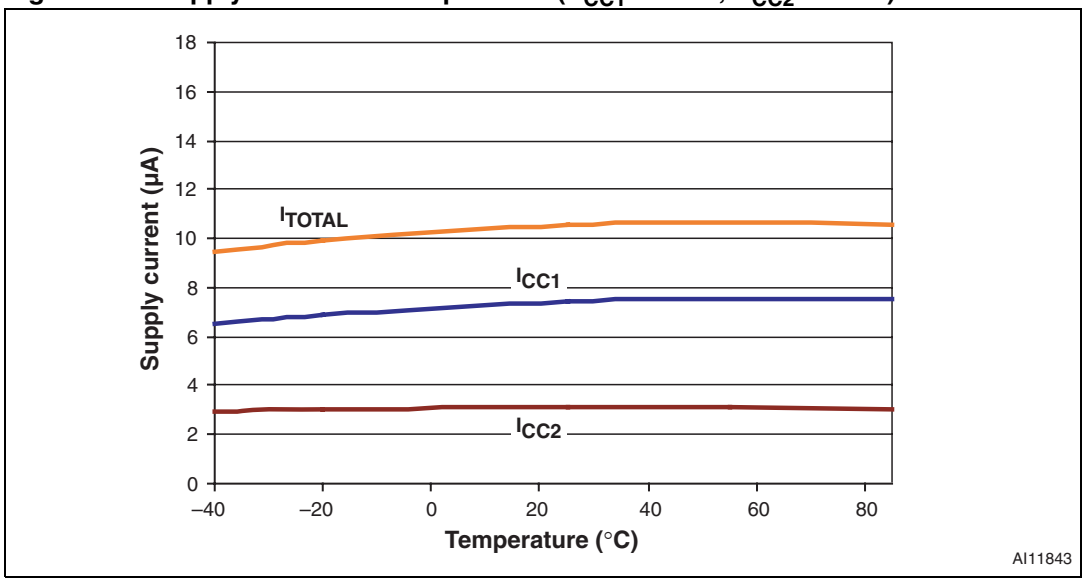



**Figure 14. Supply current vs. temperature ($V_{CC1}$ = 3.6 V; $V_{CC2}$ = 2.75 V)**

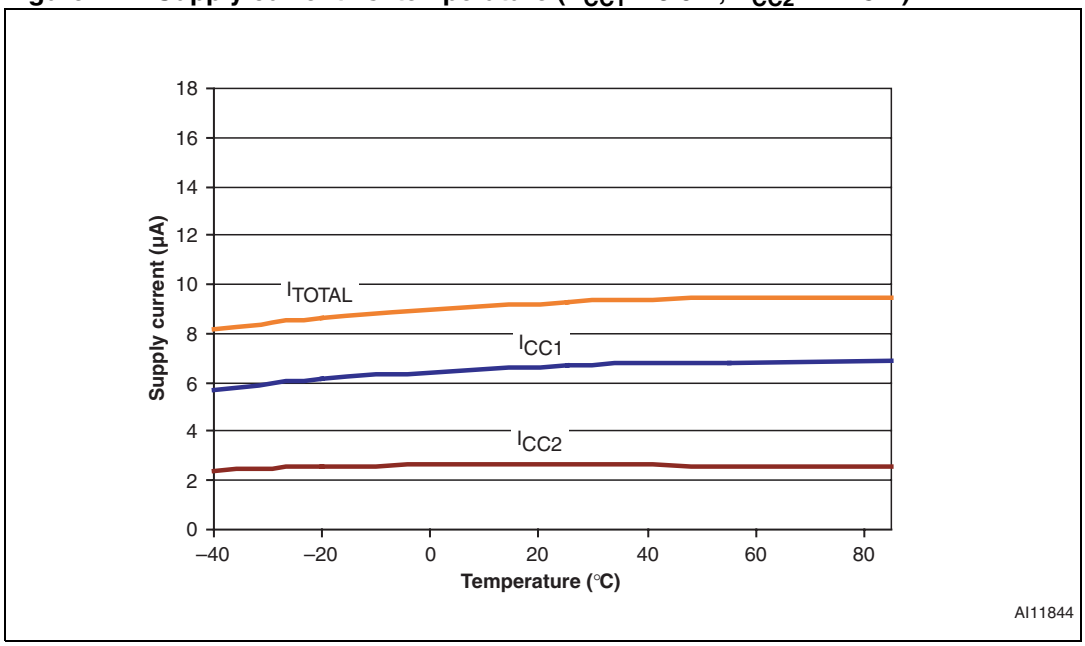


**Figure 15. Supply current vs. temperature ($V_{CC1}$ = 3.0 V; $V_{CC2}$ = 2.0 V)**

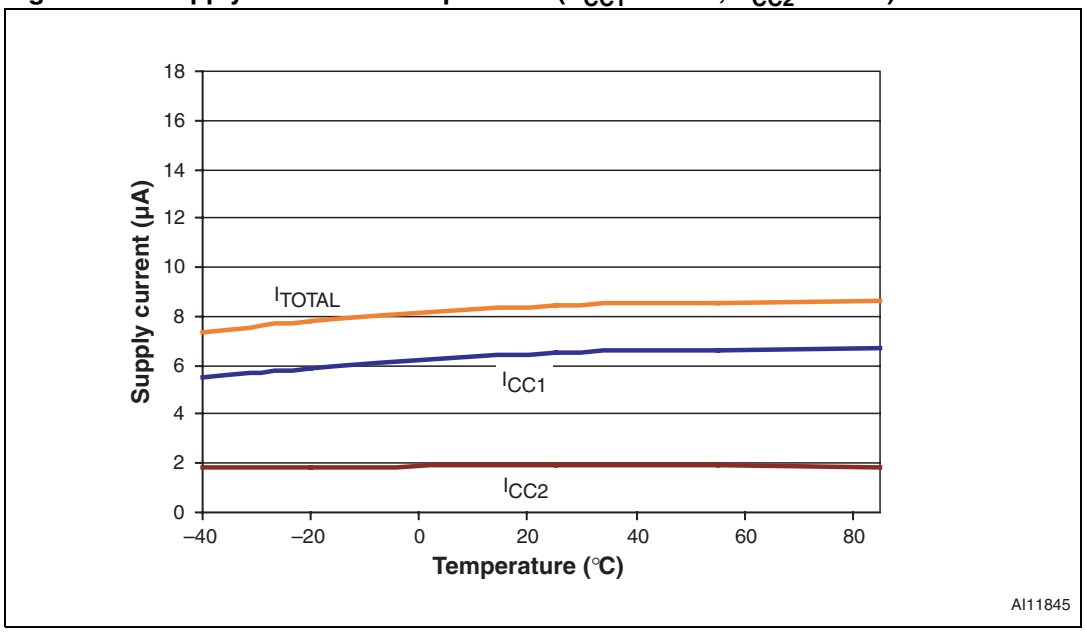



**Figure 16. Supply current vs. temperature ($V_{CC1}$ = 2.0 V; $V_{CC2}$ = 1.0 V)**

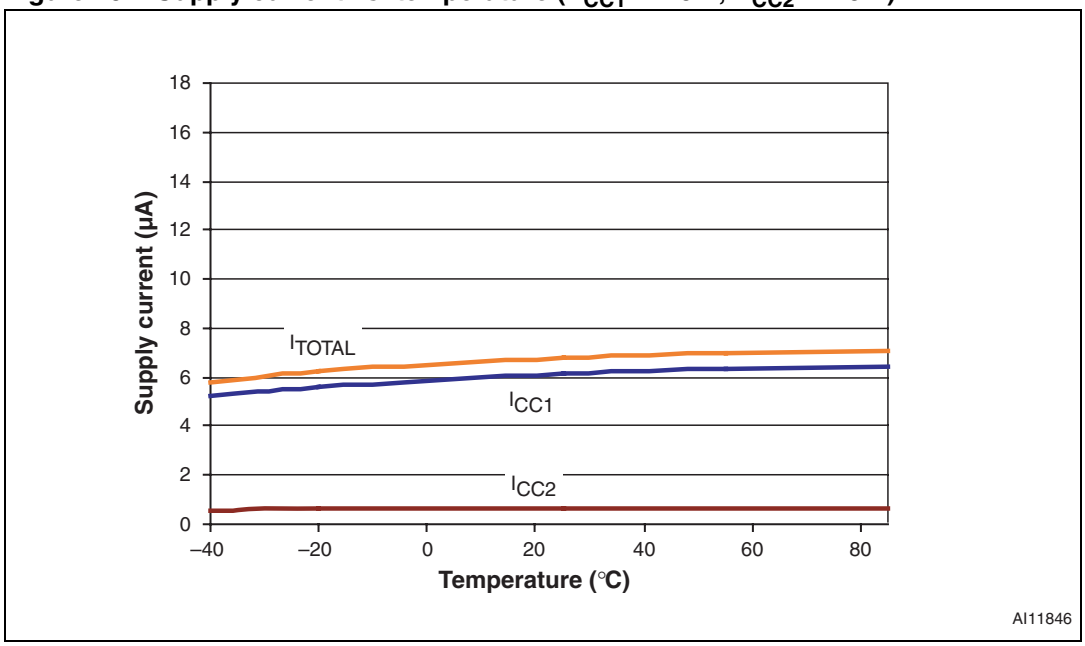


**Figure 17. Normalized $V_{CC}$ reset time-out period vs. temperature**

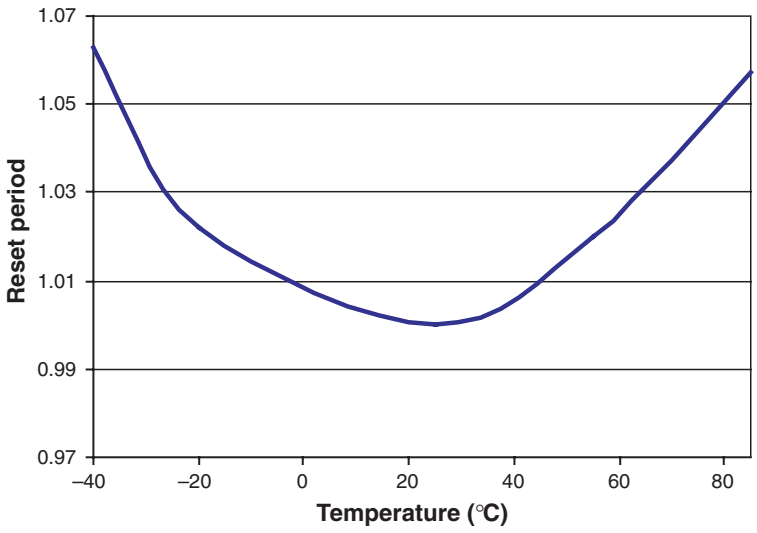



**Figure 18. Maximum $V_{CC}$ transient duration vs. reset threshold overdrive**

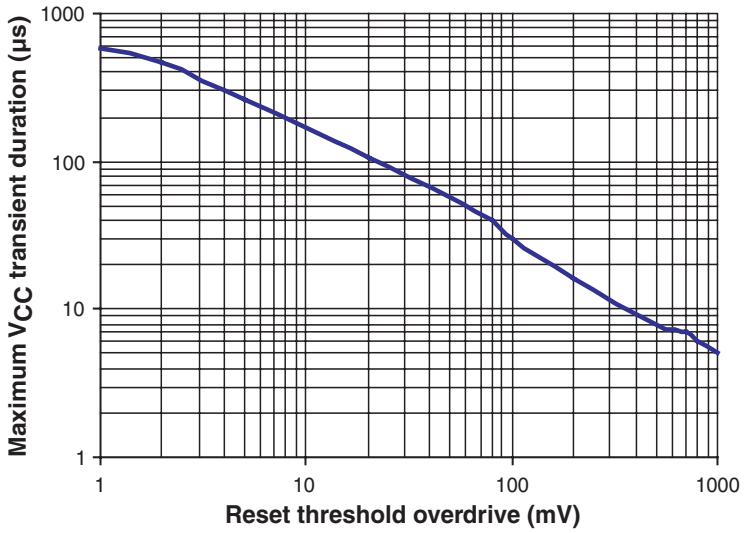


**Figure 19. Normalized $V_{RST1}$ threshold vs. temperature**

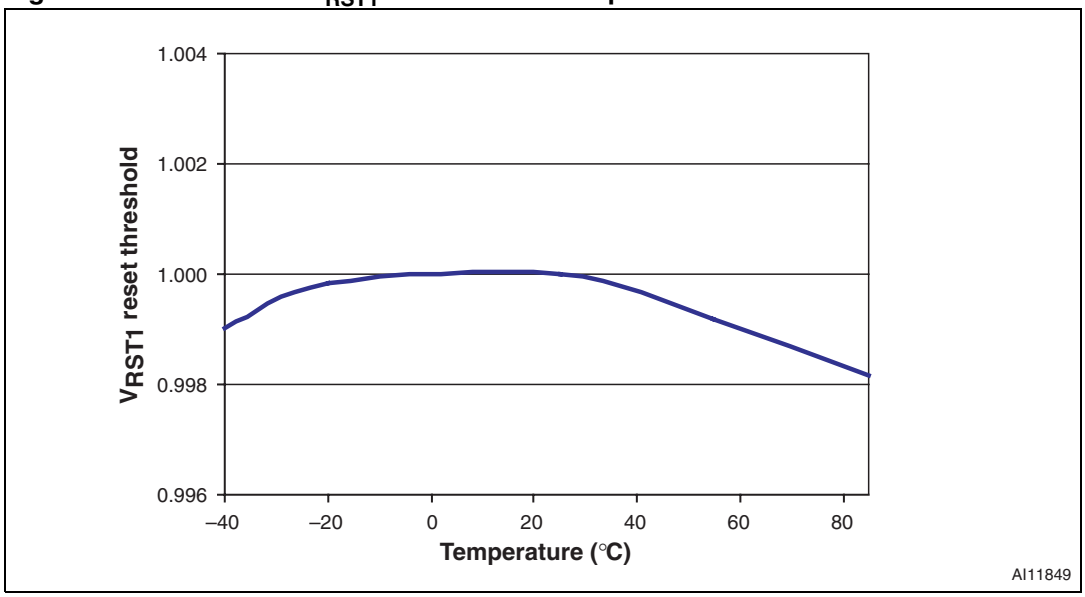



**Figure 20. Normalized $V_{RST2}$ threshold vs. temperature**

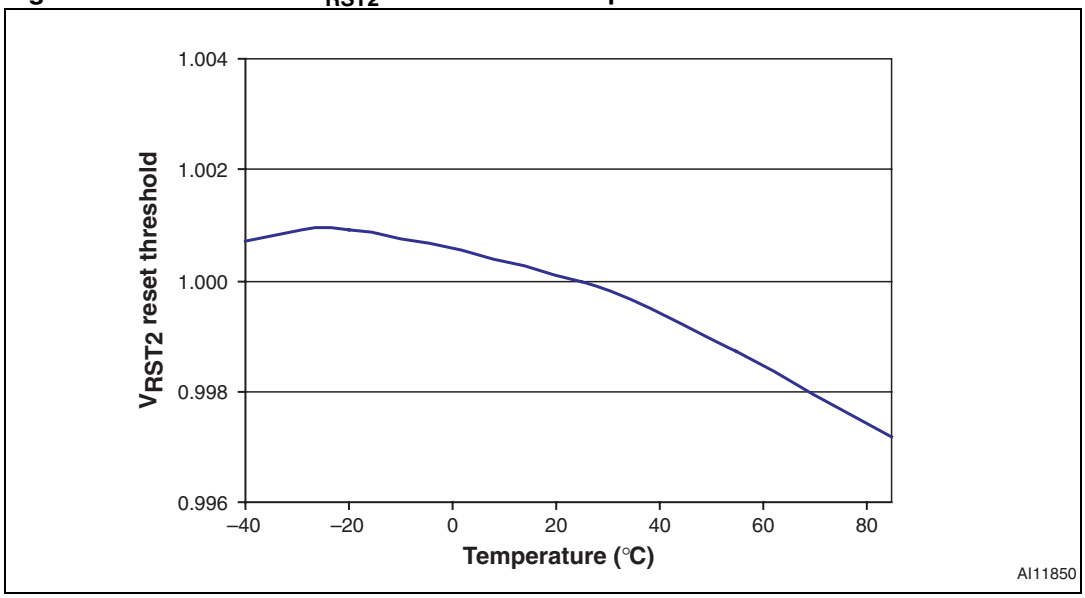


**Figure 21. Reset input threshold vs. temperature**

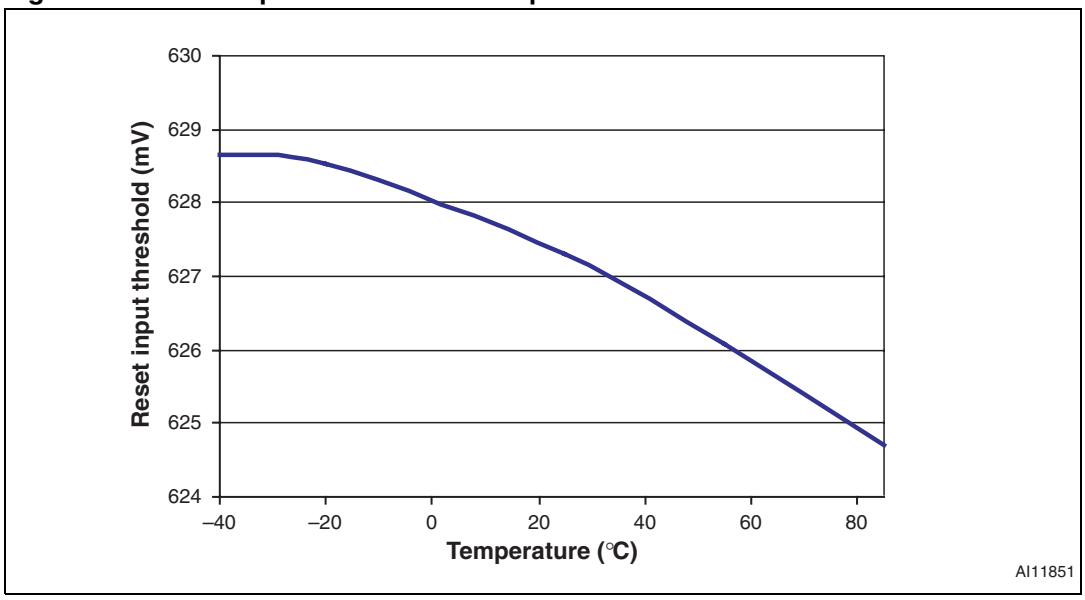



**Figure 22. $V_{CC1}$-to-reset delay vs. temperature**

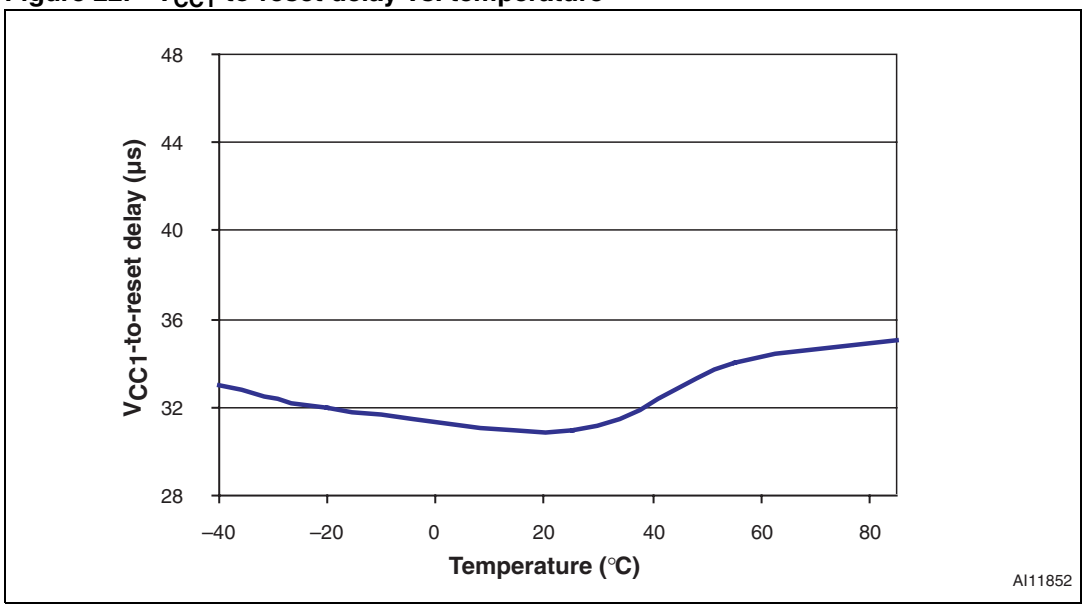


**Figure 23. Reset input-to-reset output delay vs. temperature**

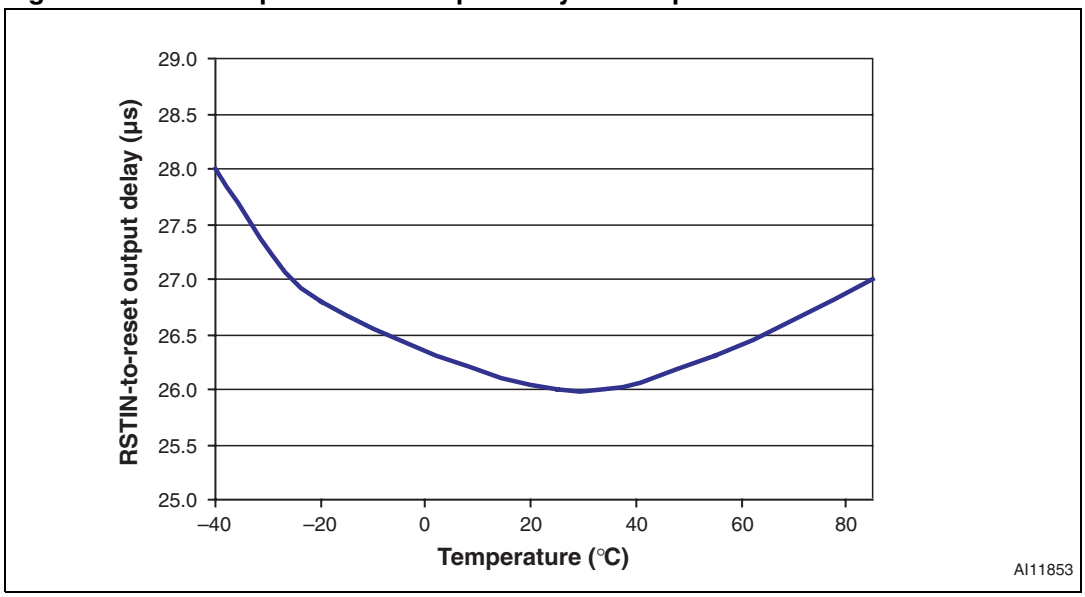
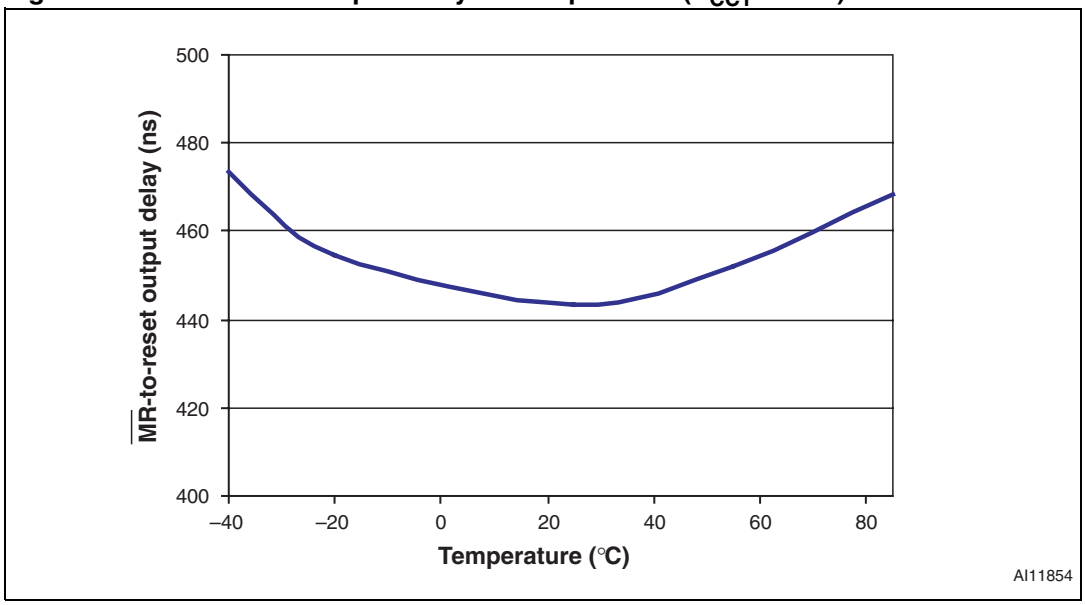



**Figure 24. $\overline{MR}$-to-reset output delay vs. temperature ($V_{CC1}$ = 3.6V)**



# 4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_{STG}$ | Storage temperature ($V_{CC}$ off) | | –55 to 150 | °C |
| $T_{SLD}$(1) | Lead solder temperature for 10 seconds | | 260 | °C |
| $V_{IO}$ | Input or output voltage | | –0.3 to $V_{CC1}$ + 0.3 | V |
| | | | –0.3 to $V_{CC2}$ + 0.3 | V |
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | | –0.3 to 7.0 | V |
| $I_{IO}$ | Input or output current (all pins) | | 20 | mA |
| $P_D$ | Power dissipation | SOT23-5 | 654 | mW |
| | | SOT23-6 | 675 | mW |

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

# 5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 5: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 5. Operating and AC measurement conditions**

| Parameter | STM67xx | Unit |
|---|---|---|
| $V_{CC}$ supply voltage | 0.8 to 5.5 | V |
| Ambient operating temperature ($T_A$) | –40 to 85 | °C |
| Input rise and fall times | ≤ 5 | ns |
| Input pulse voltages | 0.2 to 0.8$V_{CC}$ | V |
| Input and output timing ref. voltages | 0.3 to 0.7$V_{CC}$ | V |

**Figure 25. AC testing input/output waveforms**

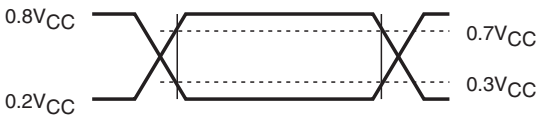



**Figure 26. $\overline{MR}$ timing waveform (STM6717/18/19/20)**

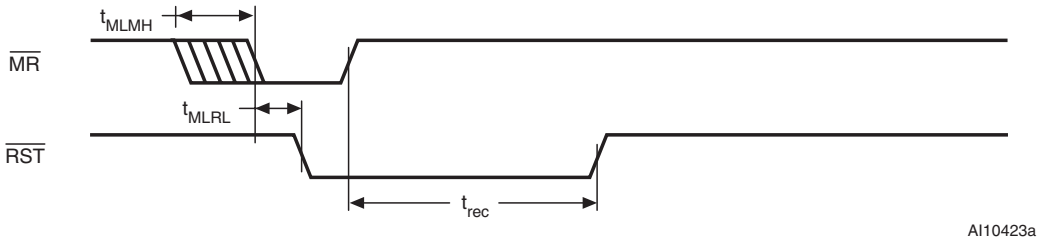
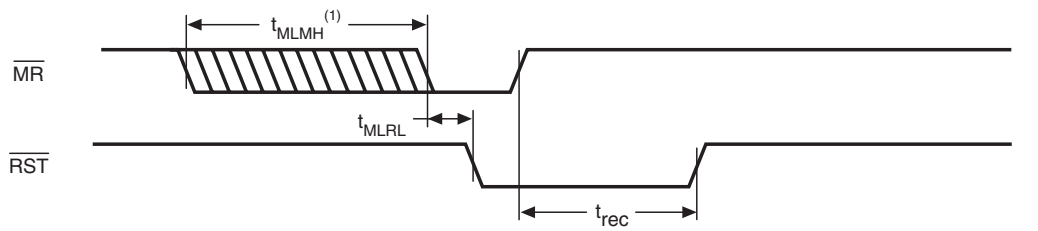



**Figure 27. $\overline{MR}$ timing waveform (STM6777/78/79/80)**




1. By connecting a certain capacitor between the MRC pin and $V_{SS}$, the $\overline{RST}$ can be delayed from 6 µs or more ($t_{MLMH}$, see *Table 7 on page 21*).

**Table 6. DC and AC characteristics**

| Sym | Alter-native | Description | Test condition(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | | Operating voltage | | 0.8 | | 5.5 | V |
| $I_{CC1}$ | | $V_{CC1}$ supply current | $V_{CC1}$ < 5.5 V, all I/O pins open | | 12 | 35 | µA |
| | | | $V_{CC1}$ < 3.6 V, all I/O pins open | | 8 | 23 | µA |
| $I_{CC2}$ | | $V_{CC2}$ supply current | $V_{CC2}$ < 3.6 V, all I/O pins open | | 3 | 9 | µA |
| | | | $V_{CC2}$ < 2.75 V, all I/O pins open | | 2.5 | 7 | µA |
| $I_{LI}$(2) | | Input leakage current | 0 V = $V_{IN}$ = $V_{CC}$ | –1 | | +1 | µA |
| $I_{LO}$ | | Open drain $\overline{RST}$ output leakage current | $V_{CC1}$ > $V_{RST1}$, $V_{CC2}$ > $V_{RST2}$; $\overline{RST}$ not asserted | | | 0.5 | µA |
| $V_{OL}$ | | Output low voltage ($\overline{RST}$; push-pull or open drain) | $V_{CC1}$ or $V_{CC2}$ ≥ 0.8 V, $I_{SINK}$ = 1 µA, $\overline{RST}$ asserted | | | 0.3 | V |
| | | | $V_{CC1}$ or $V_{CC2}$ ≥ 1.0 V, $I_{SINK}$ = 50 µA, $\overline{RST}$ asserted | | | 0.3 | V |
| | | | $V_{CC1}$ or $V_{CC2}$ ≥ 1.2 V, $I_{SINK}$ = 100 µA, $\overline{RST}$ asserted | | | 0.3 | V |
| | | | $V_{CC1}$ or $V_{CC2}$ ≥ 2.7 V, $I_{SINK}$ = 1.2 mA, $\overline{RST}$ asserted | | | 0.3 | V |
| | | | $V_{CC1}$ or $V_{CC2}$ ≥ 4.5 V, $I_{SINK}$ = 3.2 mA, $\overline{RST}$ asserted | | | 0.4 | V |
| $V_{OH}$ | | Output high voltage ($\overline{RST}$; push-pull only) | $V_{CC1}$ ≥ 1.8 V, $I_{SOURCE}$ = 200 µA, $\overline{RST}$ not asserted | 0.8$V_{CC1}$ | | | V |
| | | | $V_{CC1}$ ≥ 2.7 V, $I_{SOURCE}$ = 500 µA, $\overline{RST}$ not asserted | 0.8$V_{CC1}$ | | | V |
| | | | $V_{CC1}$ ≥ 4.5 V, $I_{SOURCE}$ = 800 µA, $\overline{RST}$ not asserted | 0.8$V_{CC1}$ | | | V |
| $t_R$(3) | | Push-pull $\overline{RST}$ rise time (STM6718/20/78/80) | Rise time measured from 10% to 90% of $V_{CC}$; $C_L$ = 5 pF, $V_{CC}$ = 3.3 V | | 5 | 25 | ns |
| **Reset thresholds** | | | | | | | |
| $V_{RST}$(4) | $V_{TH1}$ | $V_{CC1}$ reset threshold | L (falling) | 4.500 | 4.625 | 4.750 | V |
| | | | M (falling) | 4.250 | 4.375 | 4.500 | V |
| | | | T (falling) | 3.000 | 3.075 | 3.150 | V |
| | | | S (falling) | 2.850 | 2.925 | 3.000 | V |
| | | | R (falling) | 2.550 | 2.625 | 2.700 | V |
| | | | Z (falling) | 2.250 | 2.313 | 2.375 | V |
| | | | Y (falling) | 2.125 | 2.188 | 2.250 | V |
| | | | W (falling) | 1.620 | 1.665 | 1.710 | V |
| | | | V (falling) | 1.530 | 1.575 | 1.620 | V |

**Table 6. DC and AC characteristics (continued)**

| Sym | Alter-native | Description | Test condition(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{RST2}$(4) | $V_{TH2}$ | $V_{CC2}$ reset threshold | T (falling) | 3.000 | 3.075 | 3.150 | V |
| | | | S (falling) | 2.850 | 2.925 | 3.000 | V |
| | | | R (falling) | 2.550 | 2.625 | 2.700 | V |
| | | | Z (falling) | 2.250 | 2.313 | 2.375 | V |
| | | | Y (falling) | 2.125 | 2.188 | 2.250 | V |
| | | | W (falling) | 1.620 | 1.665 | 1.710 | V |
| | | | V (falling) | 1.530 | 1.575 | 1.620 | V |
| | | | I (falling) | 1.350 | 1.388 | 1.425 | V |
| | | | H (falling) | 1.275 | 1.313 | 1.350 | V |
| | | | G (falling) | 1.080 | 1.110 | 1.140 | V |
| | | | F (falling) | 1.020 | 1.050 | 1.080 | V |
| | | | K (falling) | 0.895 | 0.925 | 0.955 | V |
| | | | J (falling) | 0.845 | 0.875 | 0.905 | V |
| | | | E (falling) | 0.810 | 0.833 | 0.855 | V |
| | | | D (falling) | 0.765 | 0.788 | 0.810 | V |
| $V_{HYST}$ | | Reset threshold hysteresis | Referenced to $V_{RST}$ typical | | 0.5 | | % |
| $t_{RD}$ | | $V_{CC}$ to $\overline{RST}$ delay | $V_{CC1}$ = ($V_{RST1}$ + 100 mV) to ($V_{RST}$ – 100 mV) | | 20 | | µs |
| | | | $V_{CC2}$ = ($V_{RST2}$ + 75 mV) to ($V_{RST2}$ – 75 mV) | | 20 | | µs |
| $t_{rec}$ | $t_{RP}$ | $\overline{RST}$ pulse width | blank | 140 | 210 | 280 | ms |
| | | | B | 8.8 | 13.2 | 17.6 | |
| | | | G | 600 | 900 | 1200 | |
| **Adjustable reset comparator input (STM6719/20/79/80)** | | | | | | | |
| $V_{RSTIN}$ | | RSTIN input threshold | | 611 | 626.5 | 642 | mV |
| $I_{RSTIN}$ | | RSTIN input current | | –25 | | +25 | nA |
| | | RSTIN hysteresis | | | 3 | | mV |
| $t_{RSTIND}$ | | RSTIN to $\overline{RST}$ output delay | $V_{RSTIN}$ to ($V_{RSTIN}$ – 30 mV) | | 22 | | µs |

**Table 6. DC and AC characteristics (continued)**

| Sym | Alter-native | Description | Test condition(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Manual (push-button) reset input** | | | | | | | |
| $V_{IL}$ | | $\overline{MR}$ input voltage | | | | $0.3V_{CC1}$ | V |
| $V_{IH}$ | | | | $0.7V_{CC1}$ | | | V |
| $t_{MLMH}$ | $t_{MR}$ | $\overline{MR}$ minimum pulse width (STM6717/18/19/20) | | 1 | | | µs |
| | | $\overline{MR}$ minimum pulse width (STM6777/78/79/80) | MRC connected via capacitor to $V_{SS}$ | | 6 | | µs |
| $t_{MLRL}$ | $t_{MRD}$ | $\overline{MR}$ to $\overline{RST}$ output delay | | | 200 | | ns |
| | | $\overline{MR}$ glitch immunity (STM6717/18/19/20) | | | 100 | | ns |
| | | $\overline{MR}$ pull-up resistance | | 25 | 50 | 80 | kΩ |

1. Valid for ambient operating temperature: $T_A$ = –40 to 85 °C; $V_{CC1}$ = 0.8 to 5.5 V and $V_{CC2}$ = 0.8 to 3.6 V (except where noted).
2. Input leakage for the MRC pin is not tested.
3. Guaranteed by design.
4. The leakage current measured on the $\overline{RST}$ pin is tested with the reset de-asserted (output high impedance).

**Table 7. $t_{MLMH}$ minimum pulse width**

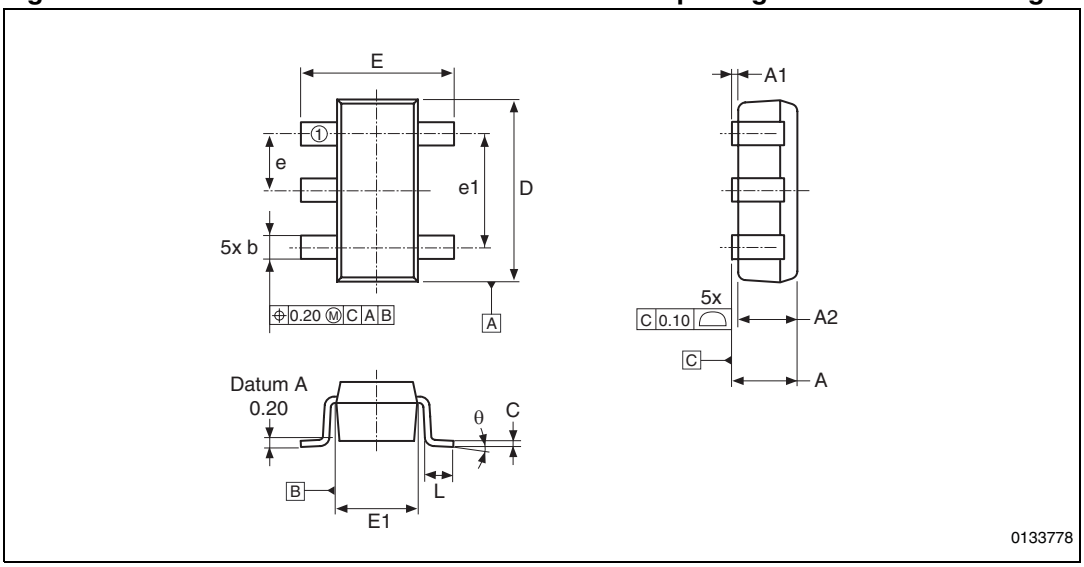
| $V_{CC1}$ | Capacitor value(1) | | | | | |
|---|---|---|---|---|---|---|
| | 100 pF | 0.1 µF | 2.2 µF | 3.3 µF | 4.7 µF | 6.8 µF |
| 1.6 V | 120 µs | 120 ms | 2.6 s | 4.0 s | 5.6 s | 8.2 s |
| 2.0 V | 122 µs | 122 ms | 2.7 s | 4.0 s | 5.8 s | 8.3 s |
| 3.0 V | 125 µs | 125 ms | 2.7 s | 4.1 s | 5.9 s | 8.5 s |
| 4.0 V | 128 µs | 129 ms | 2.8 s | 4.2 s | 6.0 s | 8.7 s |
| 5.0 V | 130 µs | 130 ms | 2.8 s | 4.3 s | 6.1 s | 8.8 s |

1. At 25 °C (typical)

# 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 28. SOT23-5 – 5-lead small outline transistor package mechanical drawing**



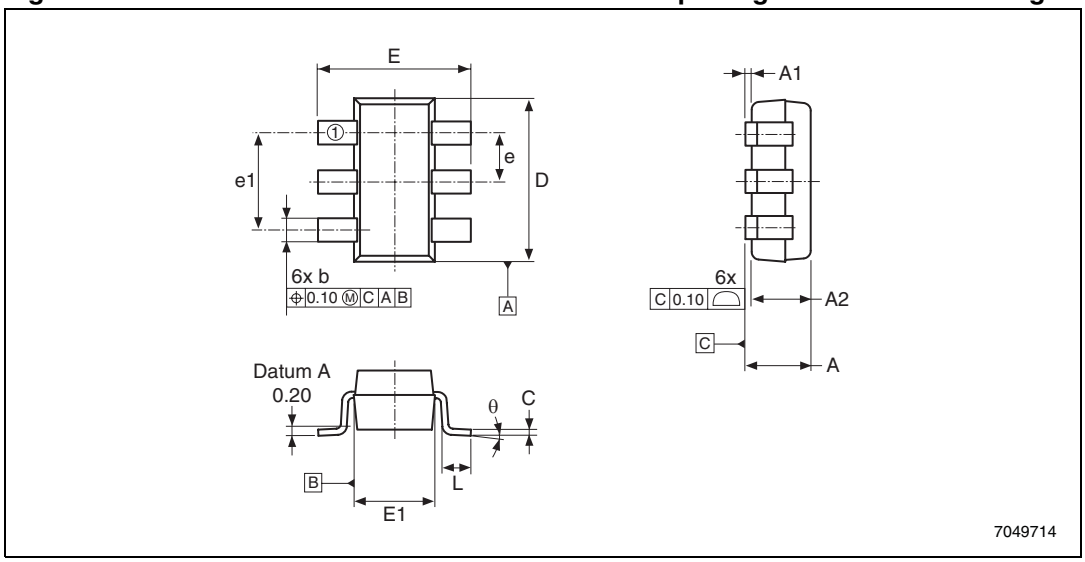

*Note: Drawing is not to scale.*

**Table 8. SOT23-5 – 5-lead small outline transistor package mechanical data**

| Symb | | mm | | | inches | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | — | — | 1.45 | — | — | 0.057 |
| A1 | — | — | 0.15 | — | — | 0.006 |
| A2 | 0.90 | 1.15 | 1.30 | 0.035 | 0.045 | 0.051 |
| b | 0.30 | — | 0.50 | 0.012 | — | 0.020 |
| C | 0.08 | — | 0.22 | 0.003 | — | 0.009 |
| D | — | 2.90 | — | — | 0.114 | — |
| E | — | 2.80 | — | — | 0.110 | — |
| E1 | — | 1.60 | — | — | 0.063 | — |
| e | — | 0.95 | — | — | 0.037 | — |
| e1 | — | 1.90 | — | — | 0.075 | — |
| L | 0.30 | 0.45 | 0.60 | 0.012 | 0.018 | 0.024 |
| Q | 0° | 4° | 8° | 0° | 4° | 8° |
| N | 5 | | | 5 | | |

*Note: Dimensions per JEDEC SOT/SOP product outline MO-178C, variation AA*

**Figure 29. SOT23-6 – 6-lead small outline transistor package mechanical drawing**



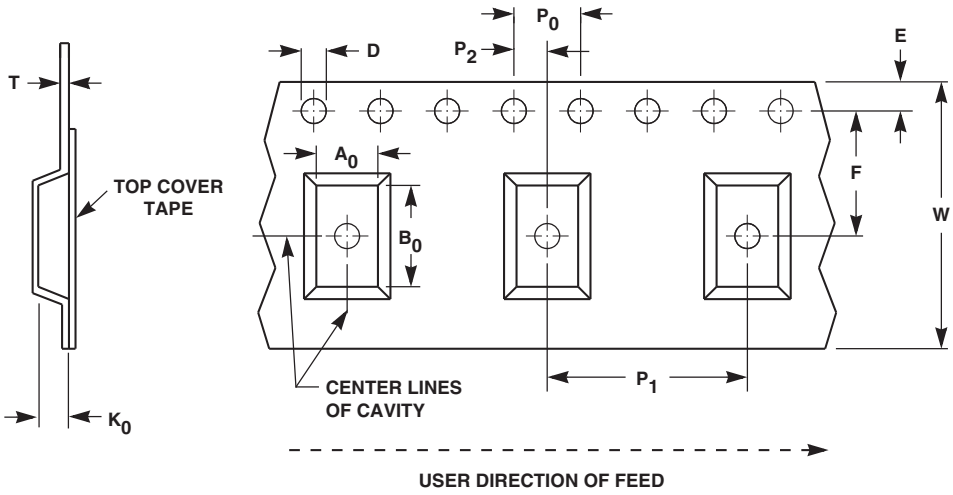

*Note: Drawing is not to scale.*

**Table 9. SOT23-6 – 6-lead small outline transistor package mechanical data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | — | — | 1.45 | — | — | 0.057 |
| A1 | — | — | 0.15 | — | — | 0.006 |
| A2 | 0.90 | 1.15 | 1.30 | 0.035 | 0.045 | 0.051 |
| b | 0.30 | — | 0.50 | 0.012 | — | 0.020 |
| C | 0.08 | — | 0.22 | 0.003 | — | 0.009 |
| D | — | 2.90 | — | — | 0.114 | — |
| E | — | 2.80 | — | — | 0.110 | — |
| E1 | — | 1.60 | — | — | 0.063 | — |
| e | — | 0.95 | — | — | 0.037 | — |
| e1 | — | 1.90 | — | — | 0.075 | — |
| L | 0.30 | 0.45 | 0.60 | 0.012 | 0.018 | 0.024 |
| Q | 0° | 4° | 8° | 0° | 4° | 8° |
| N | 6 | | | 6 | | |

*Note: Dimensions per JEDEC SOT/SOP product outline MO-178C variation AB*

**Figure 30. Carrier tape for SOT23-5L and SOT23-6L**




*Note: Part pin 1 indicator is on bottom left for shipping method "F" and is on top right for shipping method "R" see Section 7.*

**Table 10. Carrier tape dimensions for SOT23-5L and SOT23-6L**

| Package | W | D | E | $P_0$ | $P_2$ | F | $A_0$ | $B_0$ | $K_0$ | $P_1$ | T | Unit | Bulk Qty |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOT23-5<br>SOT23-6 | 8.00<br>+0.30/<br>–0.10 | 1.50<br>+0.10/<br>–0.00 | 1.75<br>±0.10 | 4.00<br>±0.10 | 2.00<br>±0.10 | 3.50<br>±0.05 | 3.23<br>±0.10 | 3.17<br>±0.10 | 1.37<br>±0.10 | 4.00<br>±0.10 | 0.254<br>±0.013 | mm | 3000 |

# 7 Part numbering

**Table 11. Ordering information scheme**

Example: STM67xx LT WY 6 F

**Device type**

STM67xx

**Reset thresholds ($V_{RST1}$ and $V_{RST2}$) for $V_{CC1}$ and $V_{CC2}$**

| STM6717/18/19/20/77/78 ($V_{RST1}$ and $V_{RST2}$) | | | STM6779/80 ($V_{RST1}$ only) | |
|---|---|---|---|---|
| Suffix | $V_{RST1}$ | $V_{RST2}$ | Suffix | $V_{RST1}$ |
| LT | 4.625 | 3.075 | L–(1) | 4.625 |
| MS | 4.375 | 2.925 | T–(1) | 3.075 |
| MR | 4.375 | 2.625 | S–(1) | 2.925 |
| TZ(1) | 3.075 | 2.313 | Y–(1) | 2.188 |
| TW(1) | 3.075 | 1.665 | V–(1) | 1.575 |
| TI | 3.075 | 1.388 | R– | 2.625 |
| TG(1) | 3.075 | 1.110 | Z– | 2.313 |
| TK | 3.075 | 0.925 | | |
| TE | 3.075 | 0.833 | | |
| SY(1) | 2.925 | 2.188 | | |
| SV(1) | 2.925 | 1.575 | | |
| SH(2) | 2.925 | 1.313 | | |
| SF(1) | 2.925 | 1.050 | | |
| SJ(3) | 2.925 | 0.875 | | |
| SD(3) | 2.925 | 0.788 | | |
| YV | 2.188 | 1.575 | | |
| YH | 2.188 | 1.313 | | |
| YF | 2.188 | 1.050 | | |
| YJ | 2.188 | 0.875 | | |
| YD | 2.188 | 0.788 | | |
| VH | 1.575 | 1.313 | | |
| VF | 1.575 | 1.050 | | |
| VJ | 1.575 | 0.875 | | |
| VD | 1.575 | 0.788 | | |

**Reset pulse width**

blank: $t_{rec}$ = 140 ms to 280 ms
B: $t_{rec}$ = 8.8 ms to 17.6 ms
G: $t_{rec}$ = 600 ms to 1200 ms

**Package**

WY = SOT23-5
WB = SOT23-6

**Temperature range**

6 = –40 to 85°C

**Shipping method**

E = ECOPACK® package, tubes
F = ECOPACK® package, tape and reel
R(4) = ECOPACK® package, tape and reel (pin 1 at top right).

1. These are standard versions and are typically held in stock. A non-standard version may require a higher minimum volumes, and/or longer delivery times. For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.
2. Available in STM6719 version only.
3. Available in STM6717 version only.
4. Available for STM6720SY, STM6719SF and STM6719SFB versions only.

**Table 12. Marking description**

| Part number | $V_{RST1}$ threshold (V) | $V_{RST2}$ threshold (V) | Topside marking | Bottomside marking |
|---|---|---|---|---|
| STM6717SD | 2.925 | 0.788 | 7SD1 | PYWW |
| STM6717SJ | 2.925 | 0.875 | 7SJ1 | PYWW |
| STM6717SF | 2.925 | 1.050 | 7SF1 | PYWW |
| STM6717TG | 3.075 | 1.110 | 7TG1 | PYWW |
| STM6717TGG | 3.075 | 1.110 | 7TG9 | PYWW |
| STM6717TW | 3.075 | 1.665 | 7TW1 | PYWW |
| STM6717SV | 2.925 | 1.575 | 7SV1 | PYWW |
| STM6717SY | 2.925 | 2.188 | 7SY1 | PYWW |
| STM6717TZ | 3.075 | 2.313 | 7TZ1 | PYWW |
| STM6718SF | 2.925 | 1.050 | 7SF2 | PYWW |
| STM6718TG | 3.075 | 1.110 | 7TG2 | PYWW |
| STM6718TW | 3.075 | 1.665 | 7TW2 | PYWW |
| STM6718SV | 2.925 | 1.575 | 7SV2 | PYWW |
| STM6718SY | 2.925 | 2.188 | 7SY2 | PYWW |
| STM6718TZ | 3.075 | 2.313 | 7TZ2 | PYWW |
| STM6719SF | 2.925 | 1.050 | 7SF3 | PYWW |
| STM6719SFB | 2.925 | 1.050 | 7SFB | PYWW |
| STM6719TG | 3.075 | 1.110 | 7TG3 | PYWW |
| STM6719SH | 2.925 | 1.313 | 7SH3 | PYWW |
| STM6719TW | 3.075 | 1.665 | 7TW3 | PYWW |
| STM6719SV | 2.925 | 1.575 | 7SV3 | PYWW |
| STM6719SY | 2.925 | 2.188 | 7SY3 | PYWW |
| STM6719TZ | 3.075 | 2.313 | 7TZ3 | PYWW |
| STM6720SF | 2.925 | 1.050 | 7SF4 | PYWW |
| STM6720TG | 3.075 | 1.110 | 7TG4 | PYWW |
| STM6720TW | 3.075 | 1.665 | 7TW4 | PYWW |
| STM6720SV | 2.925 | 1.575 | 7SV4 | PYWW |
| STM6720SY | 2.925 | 2.188 | 7SY4 | PYWW |
| STM6720TZ | 3.075 | 2.313 | 7TZ4 | PYWW |
| STM6777SF | 2.925 | 1.050 | 7SF5 | PYWW |
| STM6777TG | 3.075 | 1.110 | 7TG5 | PYWW |
| STM6777TW | 3.075 | 1.665 | 7TW5 | PYWW |
| STM6777SV | 2.925 | 1.575 | 7SV5 | PYWW |
| STM6777SY | 2.925 | 2.188 | 7SY5 | PYWW |
| STM6777TZ | 3.075 | 2.313 | 7TZ5 | PYWW |

**Table 12. Marking description (continued)**

| Part number | $V_{RST1}$ threshold (V) | $V_{RST2}$ threshold (V) | Topside marking | Bottomside marking |
|---|---|---|---|---|
| STM6778SF | 2.925 | 1.050 | 7SF6 | PYWW |
| STM6778TG | 3.075 | 1.110 | 7TG6 | PYWW |
| STM6778TW | 3.075 | 1.665 | 7TW6 | PYWW |
| STM6778SV | 2.925 | 1.575 | 7SV6 | PYWW |
| STM6778SY | 2.925 | 2.188 | 7SY6 | PYWW |
| STM6778TZ | 3.075 | 2.313 | 7TZ6 | PYWW |
| STM6779L | 4.625 | — | 7Lx7 | PYWW |
| STM6779T | 3.075 | — | 7Tx7 | PYWW |
| STM6779S | 2.925 | — | 7Sx7 | PYWW |
| STM6779Y | 2.188 | — | 7Yx7 | PYWW |
| STM6779V | 1.575 | — | 7Vx7 | PYWW |
| STM6780L | 4.625 | — | 7Lx8 | PYWW |
| STM6780T | 3.075 | — | 7Tx8 | PYWW |
| STM6780S | 2.925 | — | 7Sx8 | PYWW |
| STM6780Y | 2.188 | — | 7Yx8 | PYWW |
| STM6780V | 1.575 | — | 7Vx8 | PYWW |

*Note: For topside marking, "7" is the family number, followed by the $V_{RST1}$ threshold, $V_{RST2}$ threshold and device number (1,9 = STM6717, 2 = 6718, 3 = 6719, 4 = 6720, 5 = 6777, 6 = 6778, 7 = 6779, 8 = 6780).*

*For bottomside marking, "P" = assembly site, "Y" = 1-digit year, and "WW" = 2-digit work week.*

# 8 Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 18-Oct-2004 | 1 | First draft |
| 25-Oct-2004 | 1.1 | Descriptive text, sales types (*Table 11*) |
| 14-Jan-2005 | 1.2 | Update characteristics, pin functions (*Table 2*) |
| 09-Feb-2005 | 1.3 | Update characteristics (*Figure 9*; *Table 3*) |
| 08-Apr-2005 | 1.4 | Update characteristics and mechanical dimensions; add table (*Figure 9*, *10*, *27*, *28*, *29*; *Table 4*, *6*, *11*, *8*, *9*) |
| 28-Jul-2005 | 1.5 | Update characteristics, reset delay (*Figure 10*, *27*; *Table 4*, *6*, *7*, *11*) |
| 13-Sep-2005 | 2 | Add operating characteristics; update timings, document status, Lead-free text (Figure *Figure 13*, *14*, *15*, *16*, *17*, *18*, *19*, *20*, *21*, *22*, *23*, *24*, *26*, *27*; *Table 11*) |
| 07-Oct-2005 | 3 | Marked STM6779/6780 as availability request parts (*Table 1*, *11*) |
| 07-Feb-2007 | 4 | Updated STM6779/6780 availability (cover page, *Table 1*, *11*) |
| 12-Jun-2007 | 5 | Updated *Table 11*, added *Table 12: Marking description*. |
| 05-Dec-2007 | 6 | Updated cover page, *Table 6*, *11*, and *12*. |
| 22-Mar-2010 | 7 | Updated *Features*; *Table 6*, *8*, *9*, *11*, *12*; footnote *1* of *Table 4*; *Section 6: Package mechanical data*; added tape and reel specifications (*Figure 30*, *Table 10*, footnote *4* of *Table 11*); reformatted document. |
| 02-Aug-2011 | 8 | Removed footnote from *Table 6: DC and AC characteristics*. |

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