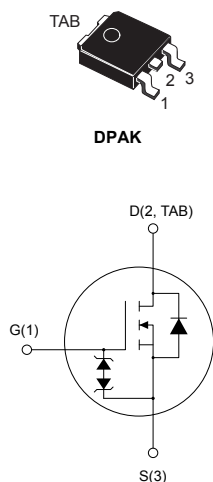


N-channel 600 V, 1.2 Ω typ., 5 A SuperMESH Power MOSFET in a DPAK package



AM01476v1_tab



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD5NK60ZT4	600 V	1.6 Ω	5 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STD5NK60ZT4](#)

Product summary

Order code	STD5NK60ZT4
Marking	D5NK60Z
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	5	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3.16	
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	W
ESD	Gate-source, human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	3	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.39	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	220	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			50	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		1.2	1.6	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	690		pF
C_{oss}	Output capacitance		-	90		pF
C_{rss}	Reverse transfer capacitance		-	20		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	40		pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	26	34 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	6		nC
Q_{gd}	Gate-drain charge		-	14		nC

1. $C_{oss\text{ eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
t_f	Fall time		-	25	-	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times and Figure 18. Switching time waveform)	-	12	-	ns
t_f	Fall time		-	10	-	ns
t_c	Cross-over time		-	24	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 30\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	485		ns
Q_{rr}	Reverse recovery charge		-	2.7		μC
I_{RRM}	Reverse recovery current		-	11		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.
2. Pulse width is limited by safe operating area.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

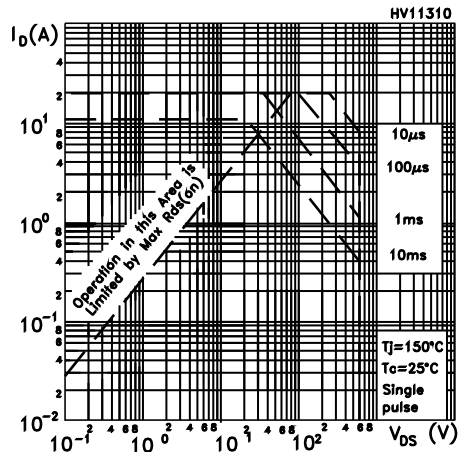


Figure 2. Normalized transient thermal impedance

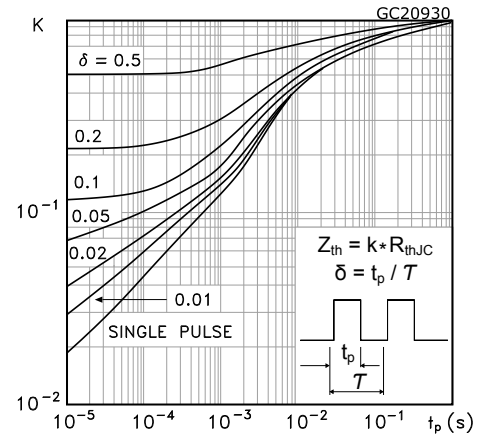


Figure 3. Typical output characteristics

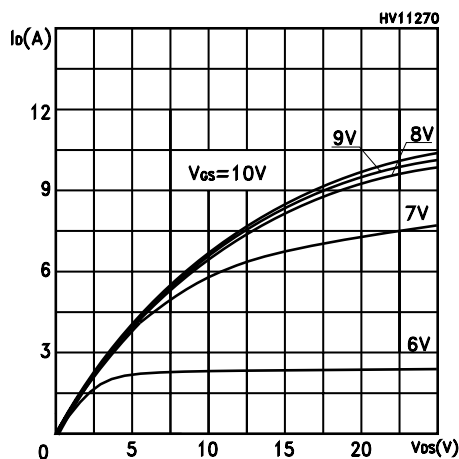


Figure 4. Typical transfer characteristics

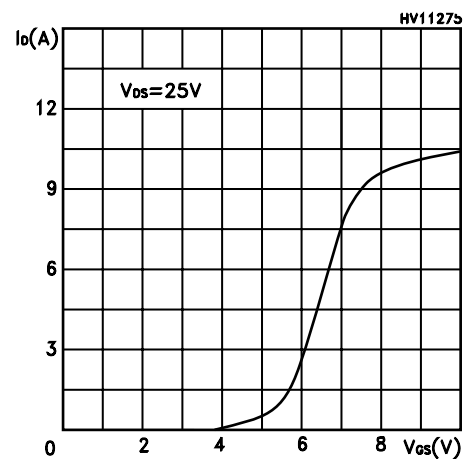


Figure 5. Typical drain-source on-resistance

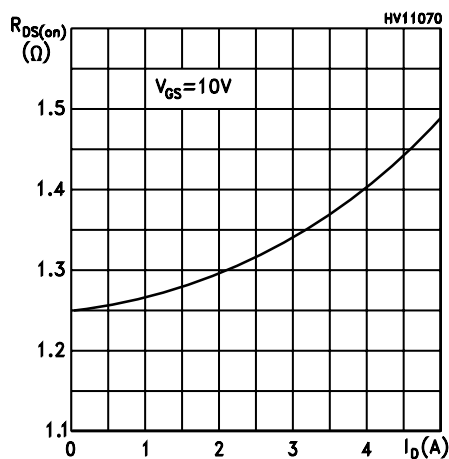


Figure 6. Typical gate charge characteristics

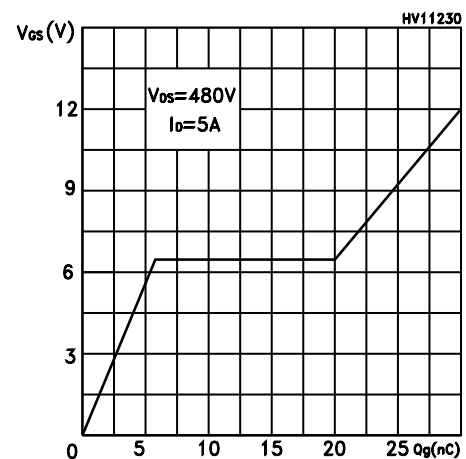


Figure 7. Typical capacitance characteristics

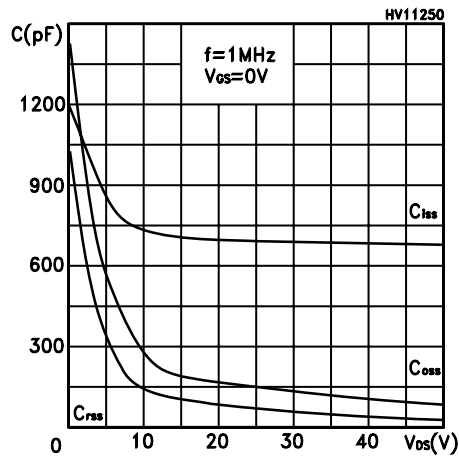


Figure 8. Normalized gate threshold vs temperature

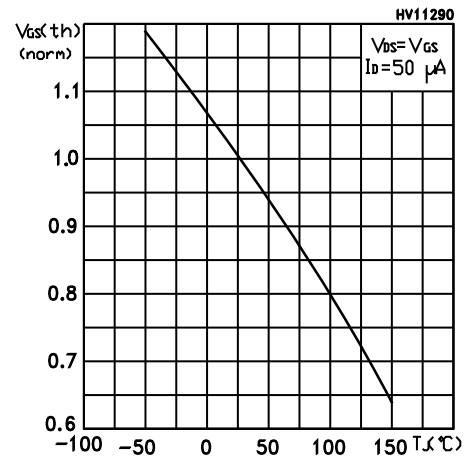


Figure 9. Normalized on-resistance vs temperature

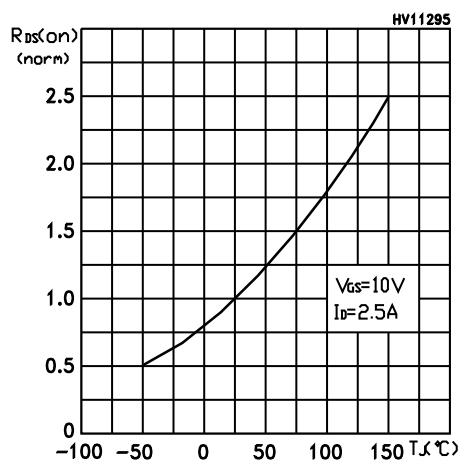


Figure 10. Typical drain-source on-resistance

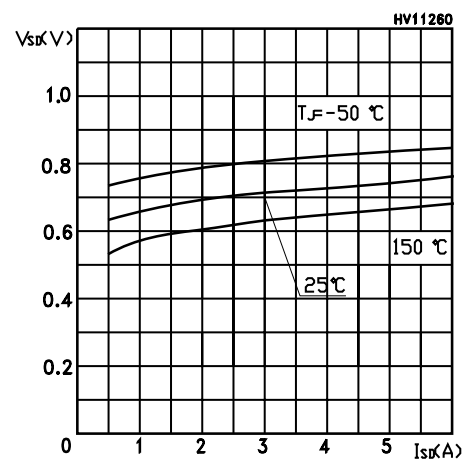


Figure 11. Normalized breakdown voltage vs temperature

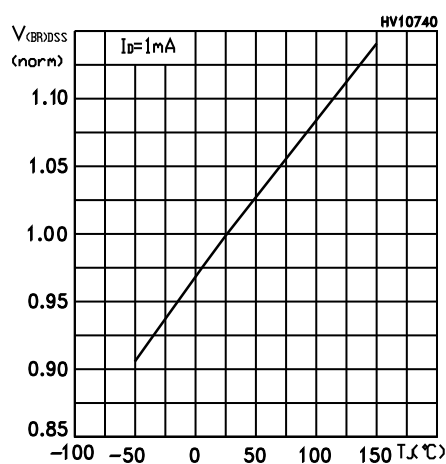
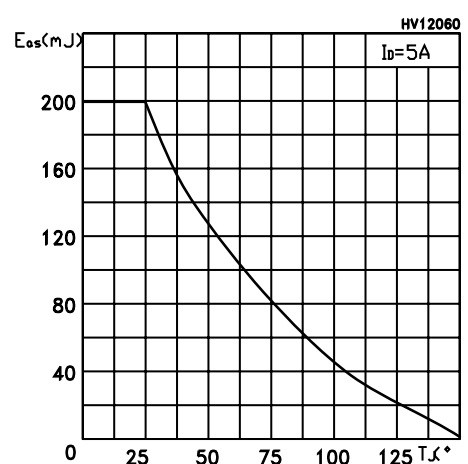
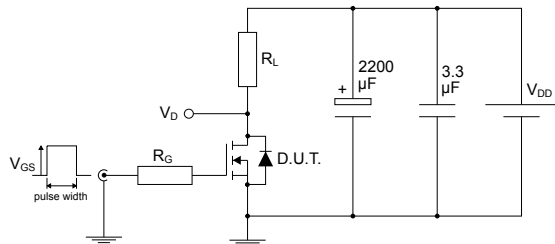


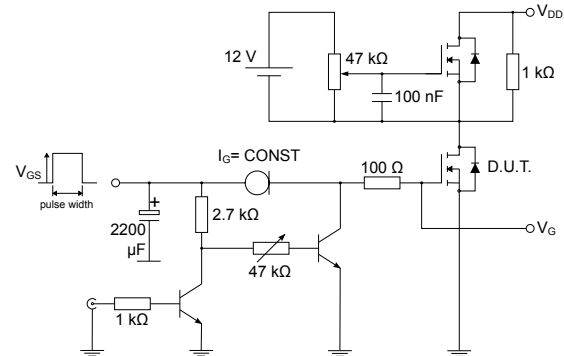
Figure 12. Maximum avalanche energy vs temperature



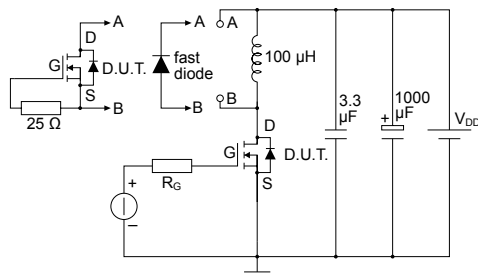
3 Test circuits

Figure 13. Test circuit for resistive load switching times


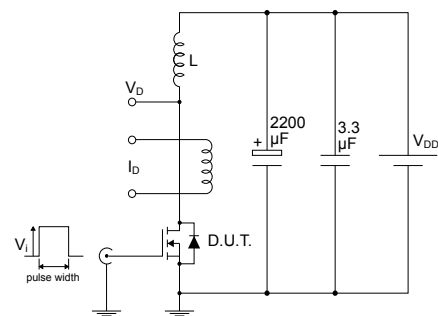
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Figure 14. Test circuit for gate charge behavior


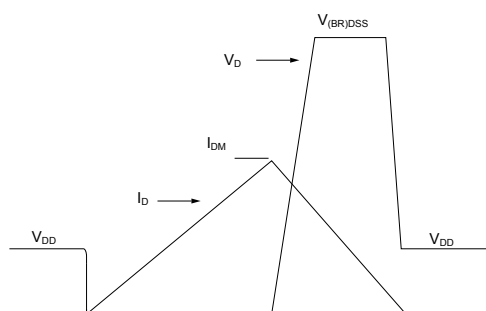
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Figure 15. Test circuit for inductive load switching and diode recovery times


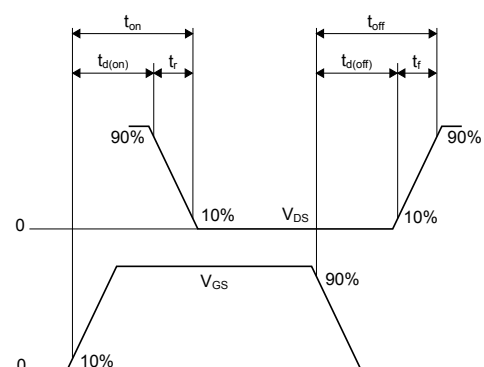
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


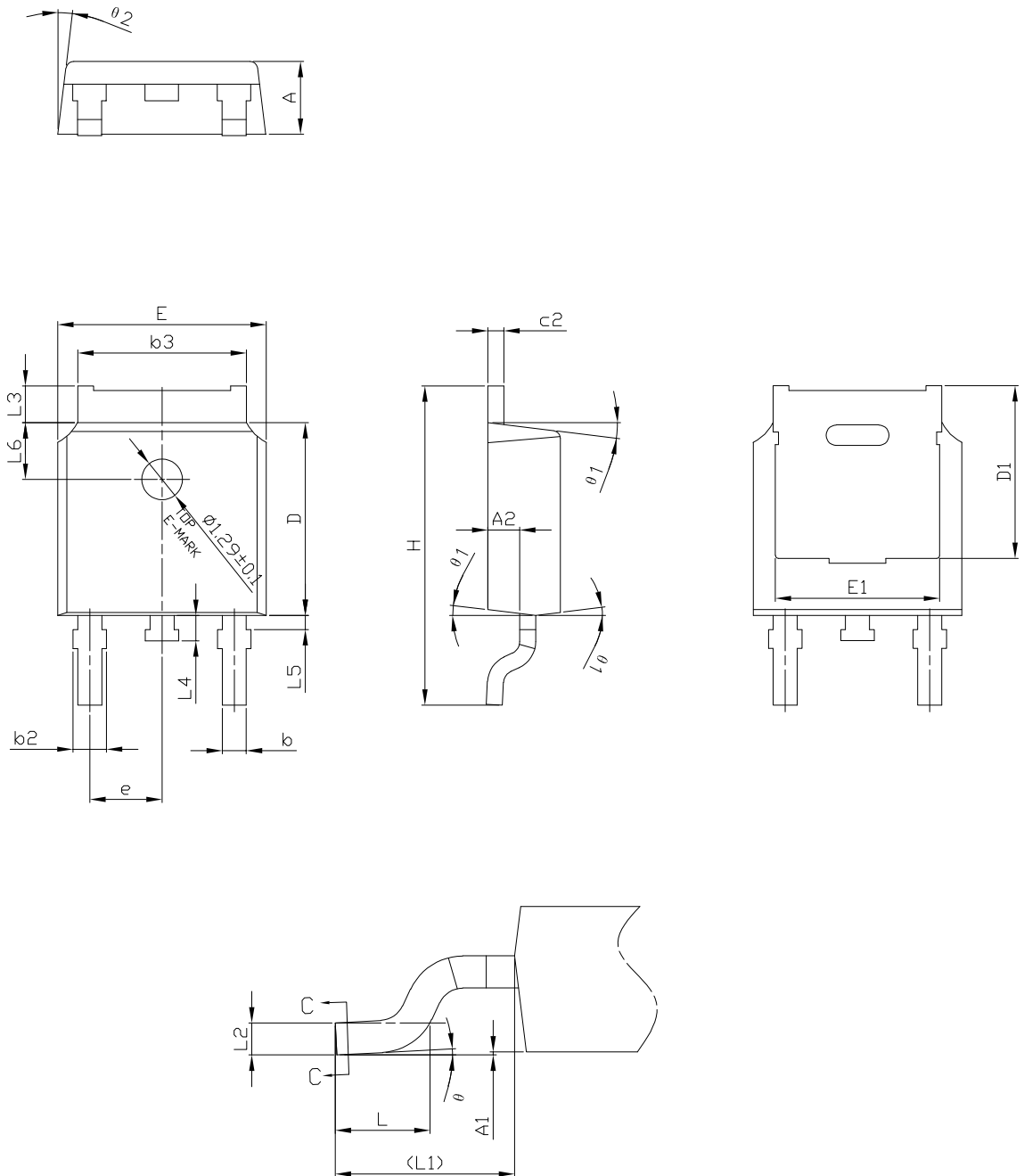
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type C3 package information

Figure 19. DPAK (TO-252) type C3 package outline

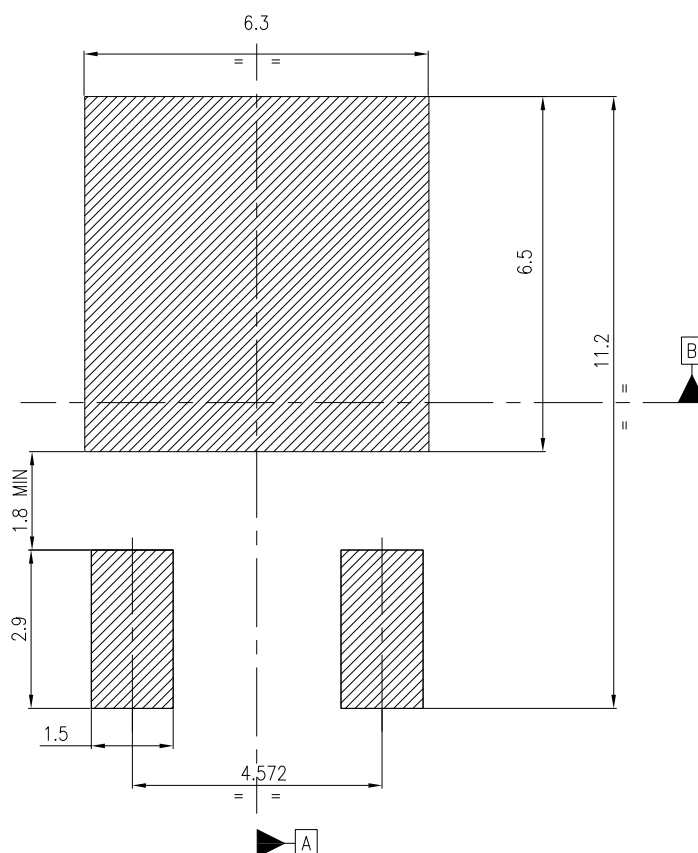


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Table 8. DPAK (TO-252) type C3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



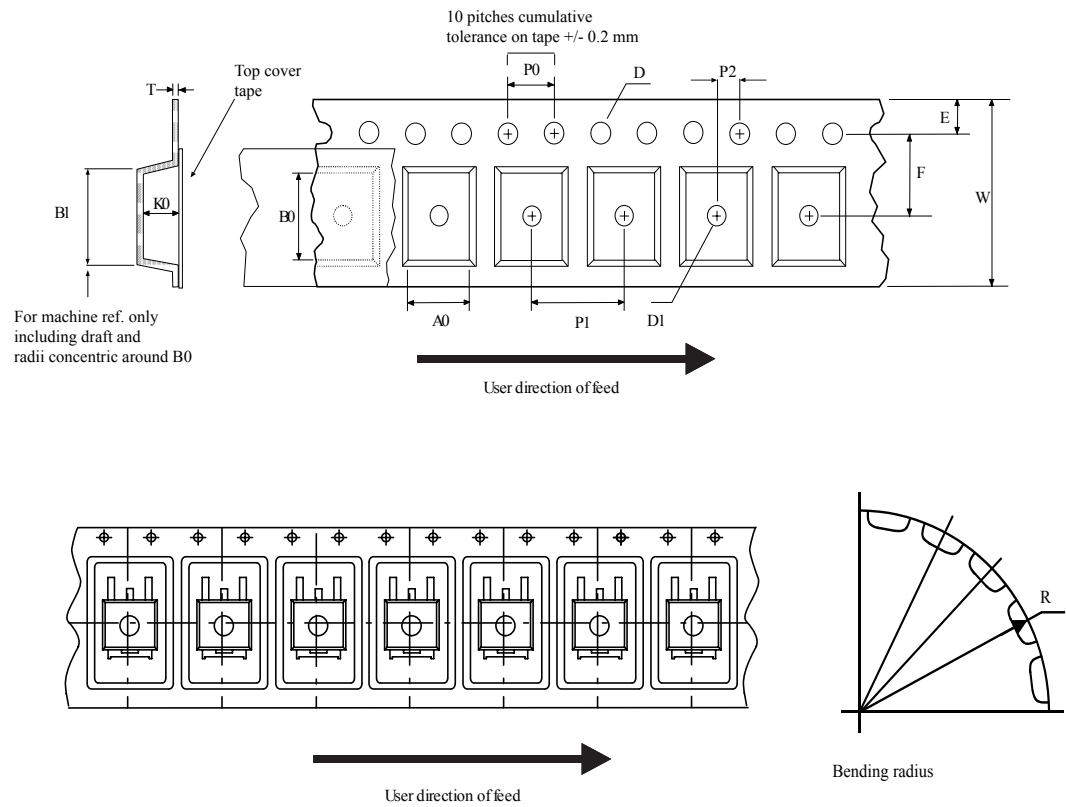
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\Phi 0.05$ A B

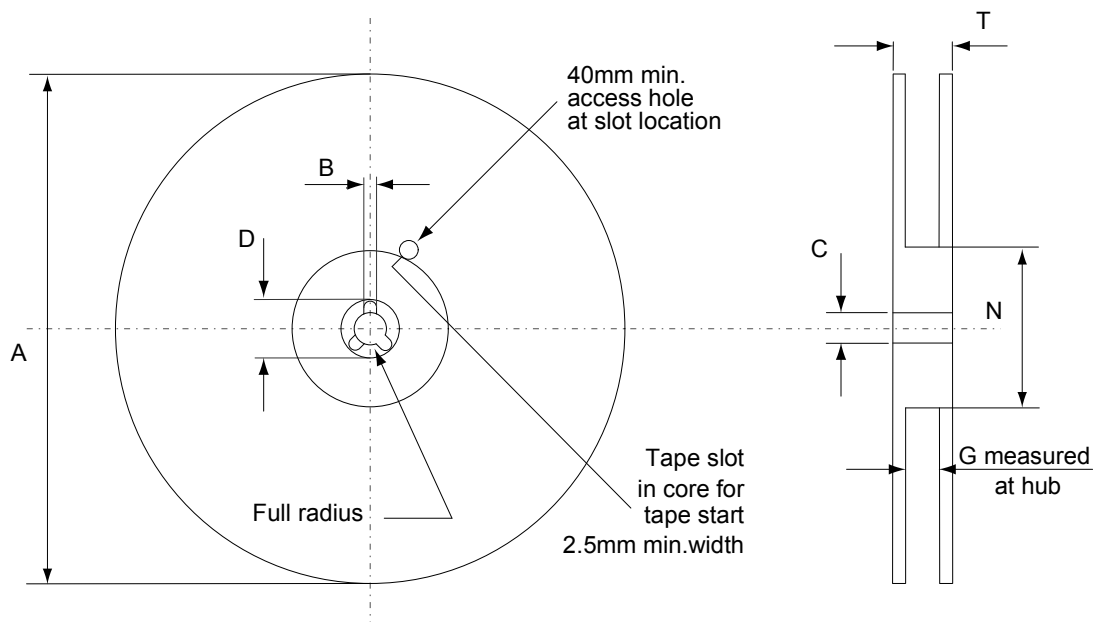
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4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline


AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
05-Apr-2005	1	First issue
29-Apr-2005	2	Modified value in Table 7.
06-Sep-2005	3	Inserted Ecopack indication
14-Oct-2005	4	Modified value on Table 1
28-Oct-2005	5	Tape & Reel info added
14-Nov-2005	6	Modified value on Table 6
15-Dec-2005	7	Various corrections
22-Aug-2018	8	Removed maturity status indication from cover page. The document status is production data. Updated <i>Section 4 Package information</i> . Minor text changes.
26-Sep-2023	9	The part numbers STP5NK60Z and STP5NK60ZFP have been moved to separate datasheets and the document has been updated accordingly. Removed gate-source Zener diode table. Updated <i>Section 4 Package information</i> . Minor text changes.

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