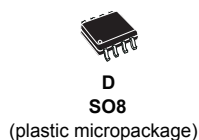


Micropower dual CMOS voltage comparators



Features

- Low supply current: 5 μ A typ. per comparator
- Wide single supply range 2.7 V to 16 V or dual supplies (± 1.35 V to ± 8 V)
- Extremely low input bias current: 1 pA typ.
- Input common-mode voltage range includes ground
- Open drain output
- High input impedance: $10^{12} \Omega$ typ.
- Fast response time: 2 μ s typ. for 5 mV overdrive
- ESD tolerance: 4 kV HBM, 200 V MM

Applications

- Automotive
- Industrial

Description

The **TSX393** is a micropower CMOS dual voltage comparator which exhibits a very low current consumption of 5 μ A typical per comparator. This device was designed as the improvement of the TS393: it shows a lower current consumption, a better input offset voltage, and an enhanced ESD tolerance. The **TSX393** is fully specified over a wide temperature range and is proposed in automotive grade for the SO8 package. It is fully compatible with the TS393 CMOS comparator and is available with similar packages. New tiny packages (MiniSO8 and DFN8 2x2 mm) are also proposed for the **TSX393** thus allowing even more integration on applications.

Maturity status link

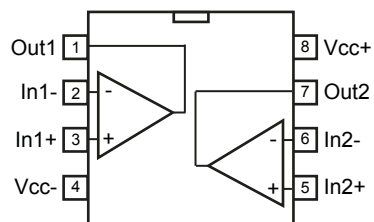
[TSX393](#)

Related products

TS393	Pin-to-pin and functionally compatible with the dual CMOS TS393 comparators
TSX3702	For push-pull output

1 Package pin connections

Figure 1. Pin connections top view



2 Absolute maximum ratings

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}^{+}	Supply voltage ⁽¹⁾		18	V
V_{id}	Differential input voltage ⁽²⁾		± 18	
V_{in}	Input voltage ⁽³⁾		-0.3 to 18	
V_o	Output voltage		18	
I_o	Output current		20	mA
I_F	Forward current in ESD protection diodes on inputs ⁽⁴⁾		50	
T_j	Maximum junction temperature		150	°C
R_{thja}	Thermal resistance junction to ambient ⁽⁵⁾	SO8	125	°C/W
		TSSOP8	120	
		MiniSO8	190	
		DFN8 2x2	115	
T_{stg}	Storage temperature range		-65 to 150	°C
ESD	HBM: human body model ⁽⁶⁾		4000	V
	MM: machine model ⁽⁷⁾		200	
	CDM: charged device model ⁽⁸⁾		1500	
	Latch-up immunity		200	mA

1. All voltage values, except the differential voltage, are with respect to network ground terminal
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3. Excursions of input voltages may exceed the power supply level. As long as the common mode voltage ($V_{icm} = (V_{in+}) + (V_{in-})/2$) remains within the specified range, the comparator provides a stable output state. However, the maximum current of the input stage, through the ESD diodes (I_F), must be strictly observed.
4. Guaranteed by design
5. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
6. According to JEDEC standard JESD22-A114F
7. According to JEDEC standard JESD22-A115A
8. According to ANSI/ESD STM5.3.1

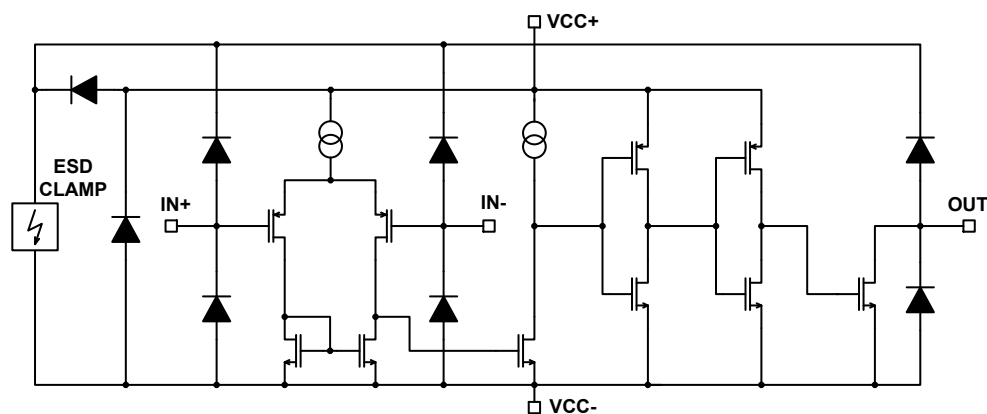
3 Operating conditions

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	0 to $(V_{CC}^{+}) - 1.5$	
	$T_{min} \leq T_{amb} \leq T_{max}$	0 to $(V_{CC}^{+}) - 2$	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

4 Schematic diagram

Figure 2. Schematic diagram (one operator)



5 Electrical characteristics

Table 3. $V_{CC}^+ = 3\text{ V}$, $V_{CC}^- = 0\text{ V}$, $T_{amb} = 25\text{ °C}$ (unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾	$V_{icm} = 0\text{ V}$	-5	0.1	5	mV
		$T_{min} \leq T_{amb} \leq T_{max}$	-6		6	
I_{io}	Input offset current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \leq T_{amb} \leq T_{max}$			600	
I_{ib}	Input bias current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \leq T_{amb} \leq T_{max}$			1200	
CMR	Common-mode rejection ratio	$V_{icm} = 0\text{ to } (V_{CC}^+) - 1.5\text{ V}$	58	73		dB
		$V_{icm} = 0\text{ to } (V_{CC}^+) - 2\text{ V}$, $T_{min} \leq T_{amb} \leq T_{max}$	55			
SVR	Supply voltage rejection ratio	$V_{CC}^+ = 3\text{ V to } 5\text{ V}$, $V_{icm} = V_{CC}/2$	69	88		
		$T_{min} \leq T_{amb} \leq T_{max}$	69			
I_{OH}	High-level output voltage	$V_{id} = 1\text{ V}$, $V_{OH} = 3\text{ V}$		1	40	nA
		$T_{min} \leq T_{amb} \leq T_{max}$			1000	
V_{OL}	Low-level output voltage	$V_{id} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$		300	400	mV
		$T_{min} \leq T_{amb} \leq T_{max}$			600	
I_{CC}	Supply current per comparator	No load, outputs low		5	6	μA
		$T_{min} \leq T_{amb} \leq T_{max}$			7	
		No load, outputs high		8	9	
		$T_{min} \leq T_{amb} \leq T_{max}$			11	
t_{PLH}	Response time low to high	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.5		μs
		Overdrive = 100 mV		0.53	0.65	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.7	
t_{PHL}	Response time high to low	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.0		
		Overdrive = 100 mV		0.4	0.6	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.65	
t_f	Fall time	$f = 10\text{ kHz}$, $C_L = 50\text{ pF}$, $R_L = 5.1\text{ k}\Omega$, overdrive 50 mV		39		ns

1. The specified offset voltage is the maximum value required to drive the output up to 2.5 V or down to 0.3 V

2. Guaranteed by design

Table 4. $V_{CC}^+ = 5\text{ V}$, $V_{CC}^- = 0\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾	$V_{icm} = V_{CC}/2$	-5	0.1	5	mV
		$T_{min} \leq T_{amb} \leq T_{max}$	-6		6	
I_{io}	Input offset current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \leq T_{amb} \leq T_{max}$			600	
I_{ib}	Input bias current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \leq T_{amb} \leq T_{max}$			1200	
CMR	Common-mode rejection ratio	$V_{icm} = 0\text{ to } (V_{CC}^+) - 1.5\text{ V}$	66	85		dB
		$V_{icm} = 0\text{ to } (V_{CC}^+) - 2\text{ V}$, $T_{min} \leq T_{amb} \leq T_{max}$	65			
SVR	Supply voltage rejection ratio	$V_{CC}^+ = 5\text{ V to } 10\text{ V}$, $V_{icm} = V_{CC}/2$	71	89		
		$T_{min} \leq T_{amb} \leq T_{max}$	70			
I_{OH}	High-level output voltage	$V_{id} = 1\text{ V}$, $V_{OH} = 5\text{ V}$		1	40	nA
		$T_{min} \leq T_{amb} \leq T_{max}$			1000	
V_{OL}	Low-level output voltage	$V_{id} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$		180	250	mV
		$T_{min} \leq T_{amb} \leq T_{max}$			400	
I_{CC}	Supply current per comparator	No load, outputs low		5	8	μA
		$T_{min} \leq T_{amb} \leq T_{max}$			9	
		No load, outputs high		9	10	
		$T_{min} \leq T_{amb} \leq T_{max}$			11	
t_{PLH}	Response time low to high	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.5		μs
		Overdrive = 10 mV		1.6		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.52	0.6	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.7	
		TTL input ⁽³⁾		0.55	0.7	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.75	
t_{PHL}	Response time high to low	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.8		
		Overdrive = 10 mV		1.8		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.46	0.6	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.7	
		TTL input ⁽³⁾		0.30	0.40	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.50	
t_f	Fall time	$f = 10\text{ kHz}$, $C_L = 50\text{ pF}$, $R_L = 5.1\text{ k}\Omega$, overdrive 50 mV		30		ns

1. The specified offset voltage is the maximum value required to drive the output up to 4.5 V or down to 0.3 V

2. Guaranteed by design

3. A step from 0 V to 3 V is applied on one input while the other is fixed at 1.4 V. Response time is the time interval between the application of the input voltage step and the moment the output voltage reaches 50 % of its final value.

Table 5. $V_{CC}^+ = 16\text{ V}$, $V_{CC}^- = 0\text{ V}$, $T_{amb} = 25\text{ °C}$ (unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾	$V_{icm} = V_{CC}/2$	-5	0.1	5	mV
		$T_{min} \leq T_{amb} \leq T_{max}$	-6		6	
I_{io}	Input offset current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \leq T_{amb} \leq T_{max}$			600	
I_{ib}	Input bias current ⁽²⁾	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \leq T_{amb} \leq T_{max}$			1200	
CMR	Common-mode rejection ratio	$V_{icm} = 0\text{ to } (V_{CC}^+) - 1.5\text{ V}$	72	90		dB
		$V_{icm} = 0\text{ to } (V_{CC}^+) - 2\text{ V}$, $T_{min} \leq T_{amb} \leq T_{max}$	70			
SVR	Supply voltage rejection ratio	$V_{CC}^+ = 5\text{ V to } 16\text{ V}$, $V_{icm} = V_{CC}/2$	73	90		
		$T_{min} \leq T_{amb} \leq T_{max}$	72			
I_{OH}	High-level output voltage	$V_{id} = 1\text{ V}$, $V_{OH} = 16\text{ V}$		1	40	nA
		$T_{min} \leq T_{amb} \leq T_{max}$			1000	
V_{OL}	Low-level output voltage	$V_{id} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$		90	150	mV
		$T_{min} \leq T_{amb} \leq T_{max}$			250	
I_{CC}	Supply current per comparator	No load, outputs low		7	9	μA
		$T_{min} \leq T_{amb} \leq T_{max}$			10	
		No load, outputs high		11	13	
		$T_{min} \leq T_{amb} \leq T_{max}$			14	
t_{PLH}	Response time low to high	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.3		μs
		Overdrive = 10 mV		1.5		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.55	0.65	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.70	
t_{PHL}	Response time high to low	$V_{icm} = 0\text{ V}$, $f = 10\text{ kHz}$, $R_L = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$, overdrive = 5 mV		2.4		
		Overdrive = 10 mV		1.6		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.55	0.70	
		$T_{min} \leq T_{amb} \leq T_{max}$			0.75	
t_f	Fall time	$f = 10\text{ kHz}$, $C_L = 50\text{ pF}$, $R_L = 5.1\text{ k}\Omega$, overdrive 50 mV		11		ns

1. The specified offset voltage is the maximum value required to drive the output up to 4.5 V or down to 0.3 V
2. Guaranteed by design

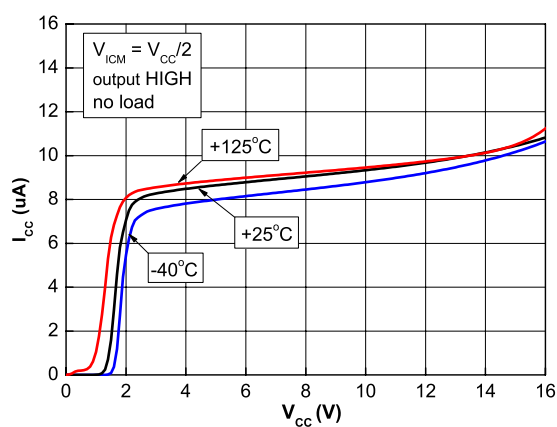
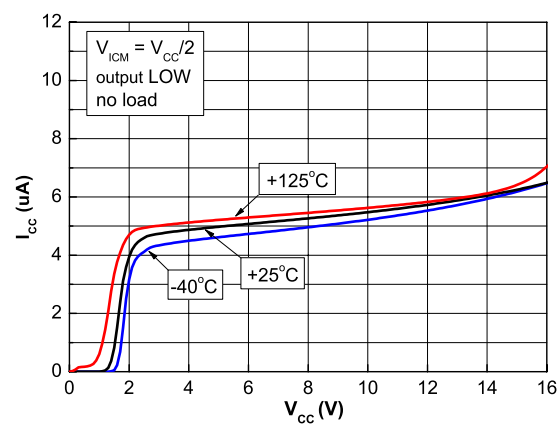
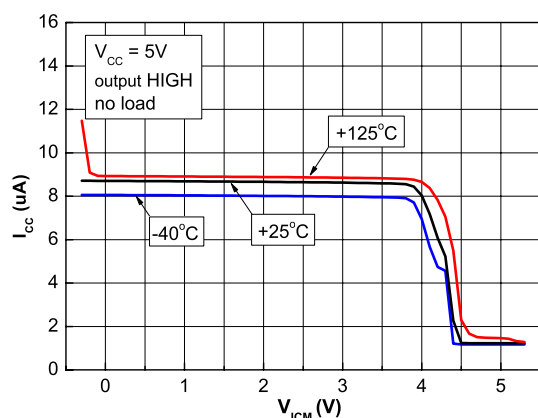
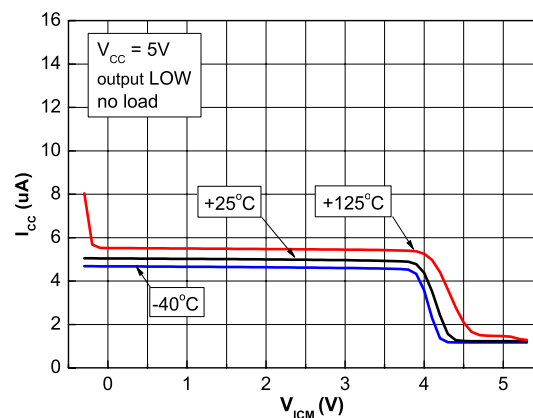
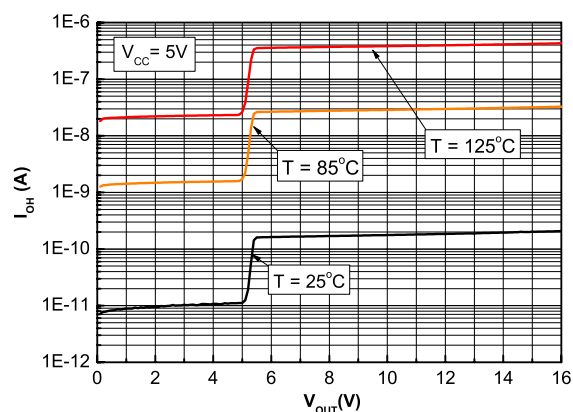
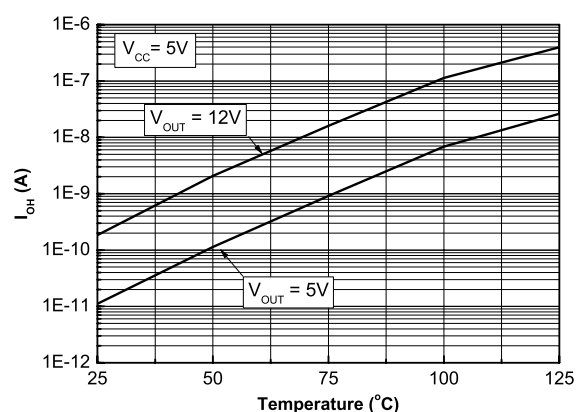
Figure 3. Current consumption vs. supply voltage, output high

Figure 4. Current consumption vs. supply voltage, output low

Figure 5. Current consumption vs. input common-mode voltage, output high

Figure 6. Current consumption vs. common-mode voltage, output low

Figure 7. Output leakage current vs. output voltage, $V_{CC} = 5V$

Figure 8. Output leakage current vs. supply voltage, $V_{CC} = 5V$


Figure 9. Output voltage drop vs. output sink current, $V_{CC} = 5\text{ V}$

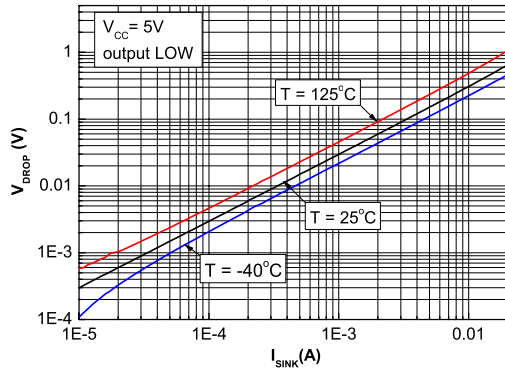


Figure 10. Output voltage drop vs. output sink current, $V_{CC} = 12\text{ V}$

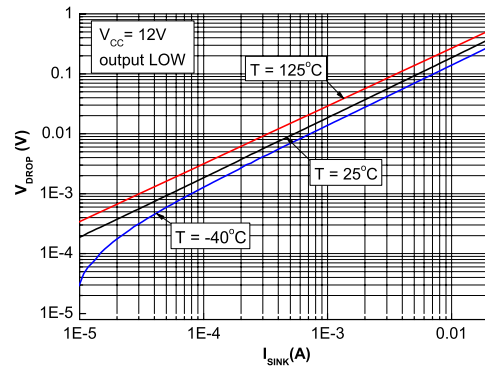


Figure 11. Input offset voltage distribution, $V_{CC} = 5\text{ V}$

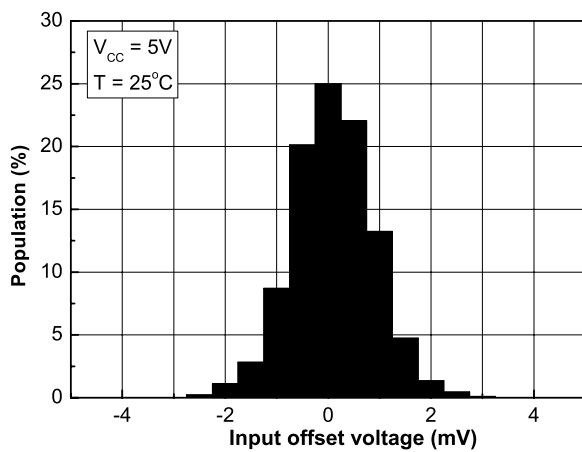


Figure 12. Input current vs input voltage, $V_{CC} = 5\text{ V}$

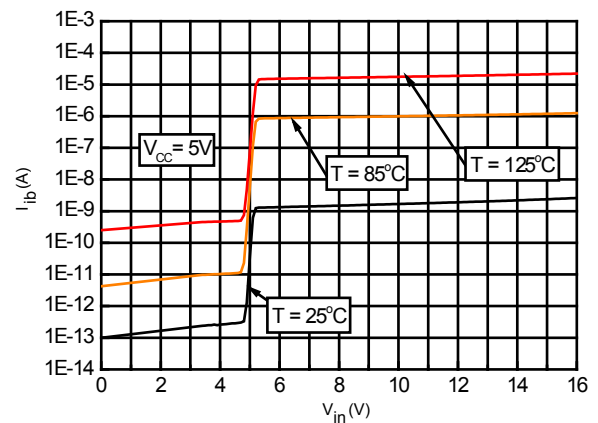


Figure 13. Propagation delay t_{PLH} vs. input signal overdrive, $V_{CC} = 5\text{ V}$

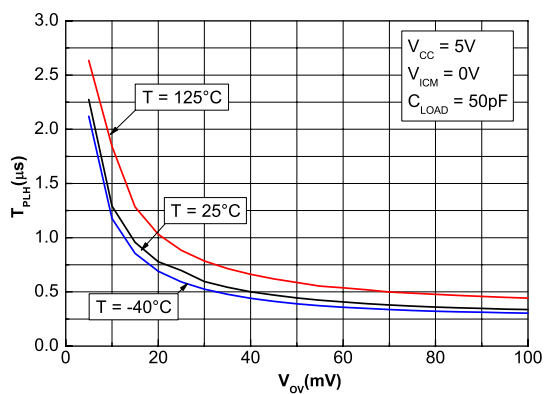


Figure 14. Propagation delay t_{PHL} vs. input signal overdrive, $V_{CC} = 5\text{ V}$

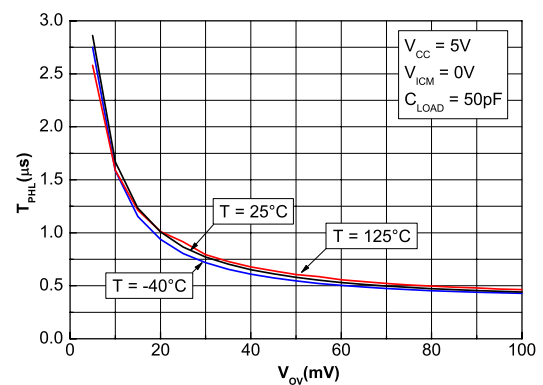


Figure 15. Propagation delay t_{PLH} vs. input signal overdrive, $V_{CC} = 5\text{ V}$

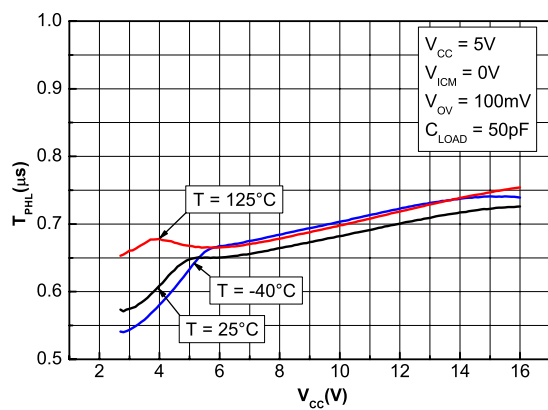
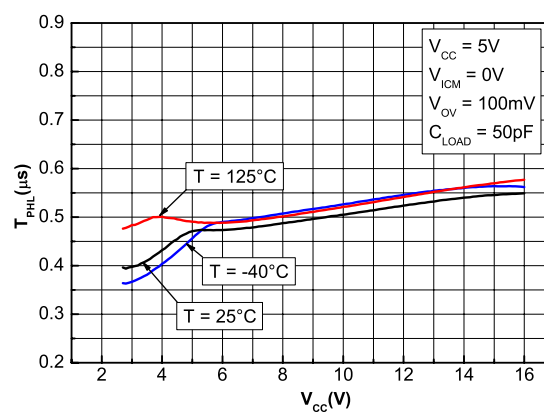


Figure 16. Propagation delay t_{PHL} vs. supply voltage, $V_{CC} = 5\text{ V}$



6 Application information (input voltages)

The ESD strategy used in the TSX393 (and shown in [Figure 2](#) allows input voltages from -0.3 V up to 16 V to be applied regardless of the V_{CC+} voltage. When $V_{IN} > V_{CC+}$ a leakage current goes from the input through the protection diode to the ESD clamp. This current is about 0.2 nA at 25 °C and about 250 nA at 125 °C. For a detailed input characteristic see [Section 5 Figure 12](#). The device is designed to prevent phase reversal.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO8 package information

Figure 17. SO8 package outline

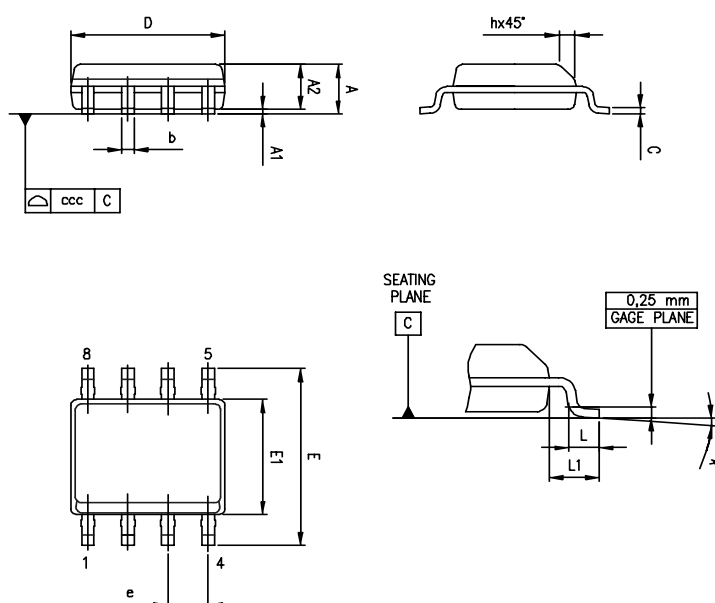


Table 6. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.2 TSSOP8 package information

Figure 18. TSSOP8 package outline

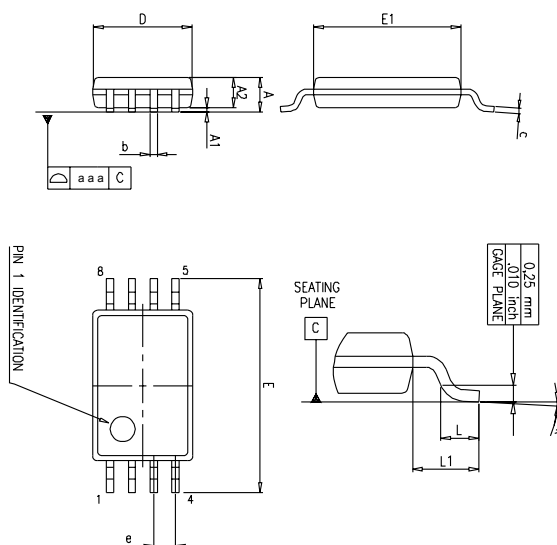


Table 7. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.10			0.004	

7.3 DFN8 2x2 package information

Figure 19. DFN8 2x2 package outline

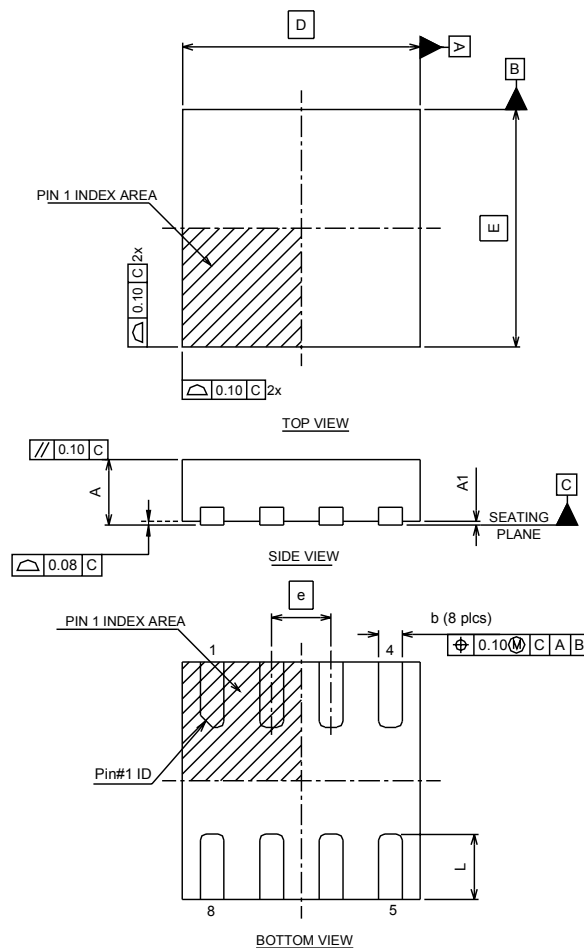
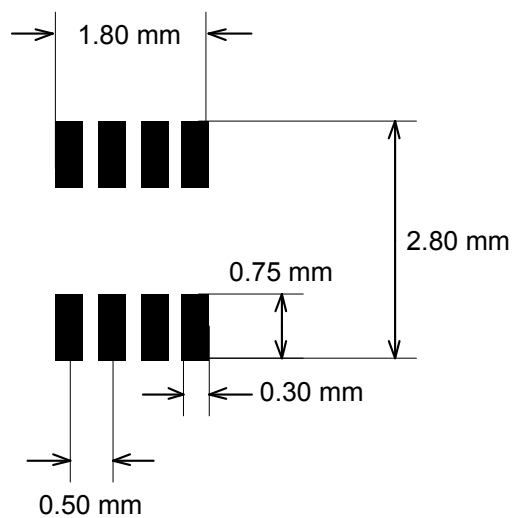


Table 8. DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8					

Figure 20. DFN8 2x2 recommended footprint



7.4 MiniSO8 package information

Figure 21. MiniSO8 package outline

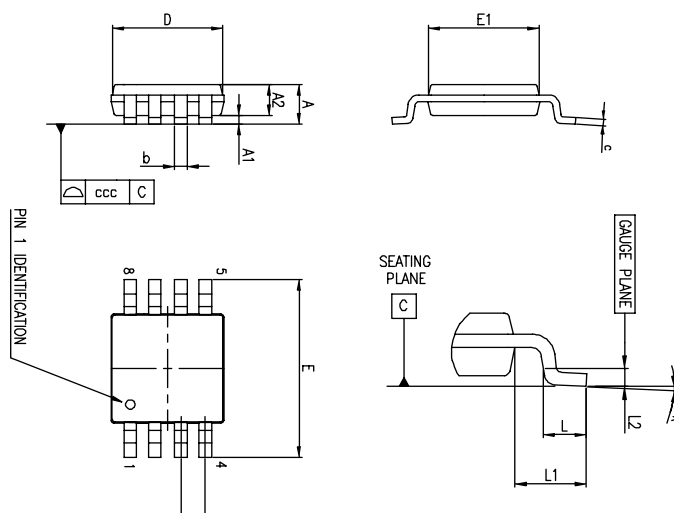


Table 9. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

8 Ordering information

Table 10. Order codes

Order code	Temperature range	Package	Packing	Marking
TSX393IDT	-40 °C, 125 °C	SO8	Tape and reel	SX393I
TSX393IPT		TSSOP8		SX393
TSX393IST		MiniSO8		K530
TSX393IQ2T		DFN8 2x2		K5K
TSX393IYDT ⁽¹⁾		SO8 (automotive grade)		SX393IY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Oct-2014	1	Initial release.
07-Sep-2015	2	Table 1: "Absoluet maximum ratings (AMR)": updated R_{thja} value for the DFN8 2x2 package. Section 7.3 "DFN8 2x2 package information": replaced pacakge outline, mechanical data, and recommended footprint by "non-exposed" pad information.
06-Jun-2016	3	Table 3, Table 4, and Table 5: updated I_{IO} and I_{IB} temperature max values, updated VOL condition. In Table 3 only, updated t_{PHL} max value. In Table 5 only, updated IOH condition. Table 10: updated automotive footnote.
06-Jul-2017	4	Table 10: updated automotive footnote.
20-Jan-2023	5	Updated figure on the cover page.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved