4-BIT D FLIP-FLOP

FEATURES

- 1100MHz min. toggle frequency
- Differential output
- Individual and common clocks
- Individual asynchronous reset
- Paired asynchronous sets
- ESD protection of 2000V
- Fully compatible with industry standard 10KH, 100K ECL levels
- Extended 100E V_{EE} range of –4.2V to –5.46V
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E131

DESCRIPTION

The SY10E131 and SY100E131 are high-speed quad master slave D-type flip-flops with differential outputs designed for use in new, high-performance ECL systems. The flip-flops may be individually clocked by holding Cc (Common Clock) at a logic LOW and then using the four individual $\overline{CE}$ (Clock Enable $\overline{CE}_0$–$\overline{CE}_3$) inputs to accomplish such clocking. Alternatively, all four flip-flops can be clocked in common by holding the $\overline{CE}$ inputs LOW and then using Cc to clock the data. In the common clock mode, the $\overline{CE}$ input acts as a control that passes the Cc signal to the flip-flop. Data is clocked into the flip-flop on the rising edge of the output of the logical OR operation between $\overline{CE}$ and Cc (data enters the master when both Cc and $\overline{CE}$ are LOW and data transfers to the slave when either $\overline{CE}$ or Cc, or both, go HIGH).

Asynchronous set and reset controls are provided. The reset controls are individual and the set controls are pairwise.

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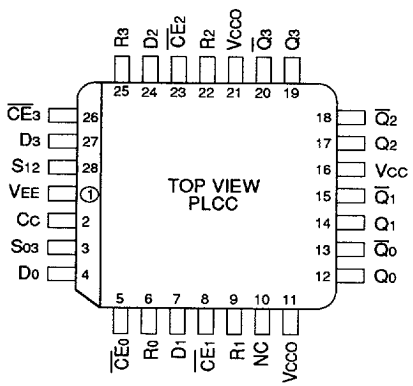
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0-D_3	Data Inputs
$\overline{CE}_0$-$\overline{CE}_3$	Clock Enables (Individual)
R_0-R_3	Resets
Cc	Common Clock
S_{03}, S_{12}	Sets (paired)
Q_0-Q_3	True Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Inverting Outputs

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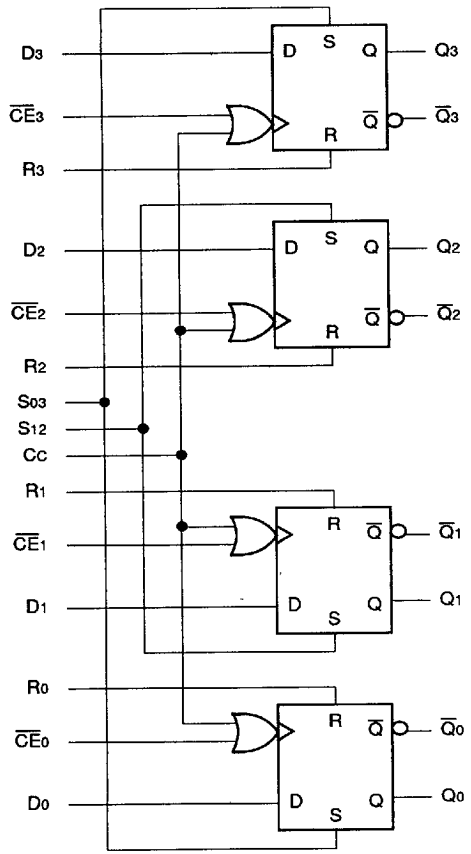
BLOCK DIAGRAM



TRUTH TABLE

Pin	State	Mode
Cc	L	Individual clocking with $\overline{CE}_n$
$\overline{CE}$	L	Common clocking with Cc

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Ty+p.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	Cc	—	—	350	—	—	350	—	—	350		
	S	—	—	450	—	—	450	—	—	450		
	R	—	—	300	—	—	300	—	—	300		
	$\overline{CE}$	—	—	300	—	—	300	—	—	300		
	D	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	58	70	—	58	70	—	58	70		
	100E	—	58	70	—	58	70	—	67	81		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	$\overline{CE}$	360	500	700	360	500	700	360	500	700		
	Cc	325	500	675	325	500	675	325	500	675		
	R	350	550	725	350	550	725	350	550	725		
	S	350	550	725	350	550	725	350	550	725		
t_s	Set-up Time, D	150	20	—	150	20	—	150	20	—	ps	2
t_h	Hold Time, D	175	–20	—	175	–20	—	150	–20	—	ps	2
t_{RR}	Reset Recovery Time	400	150	—	400	150	—	400	150	—	ps	—
t_{PW}	Minimum Pulse Width Clk, S, R	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	480	675	300	480	675	300	480	675	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Set-up/hold times guaranteed for both Cc and $\overline{CE}$.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E131JC	J28-1	Commercial
SY100E131JC	J28-1	Commercial