RAD-TOLERANT CLASS-V, PHASE SHIFT RESONANT CONTROLLER

Check for Samples: UC1875-SP

FEATURES

- **QML-V Qualified, SMD 5962-94555**
- **Rad-Tolerant: 50 kRad (Si) TID** (1)
- **Zero to 100% Duty Cycle Control**
- **Programmable Output Turn-On Delay**
- **Compatible with Voltage or Current Mode Topologies**
- **Practical Operation at Switching Frequencies to 1 MHz**
- **Four 2-A Totem Pole Outputs**
- **10 MHz Error Amplifier**
- **Undervoltage Lockout**
- **Low Startup Current – 150 µA**
- **Outputs Active Low During UVLO**
- **Soft-Start Control**
- **Latched Overcurrent Comparator With Full Cycle Restart**
- **Trimmed Reference**

(1) Radiation tolerance is a typical value based upon initial device qualification with a dose rate = 10 mrad/sec and applies to the 5962-9455502 devices. Radiation lot acceptance testing is available – contact factory for details.

APPLICATIONS

- **Power FPGAs**

DESCRIPTION

The UC1875-SP implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This circuit may be configured to provide control in either voltage or current mode operation, with a separate overcurrent shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

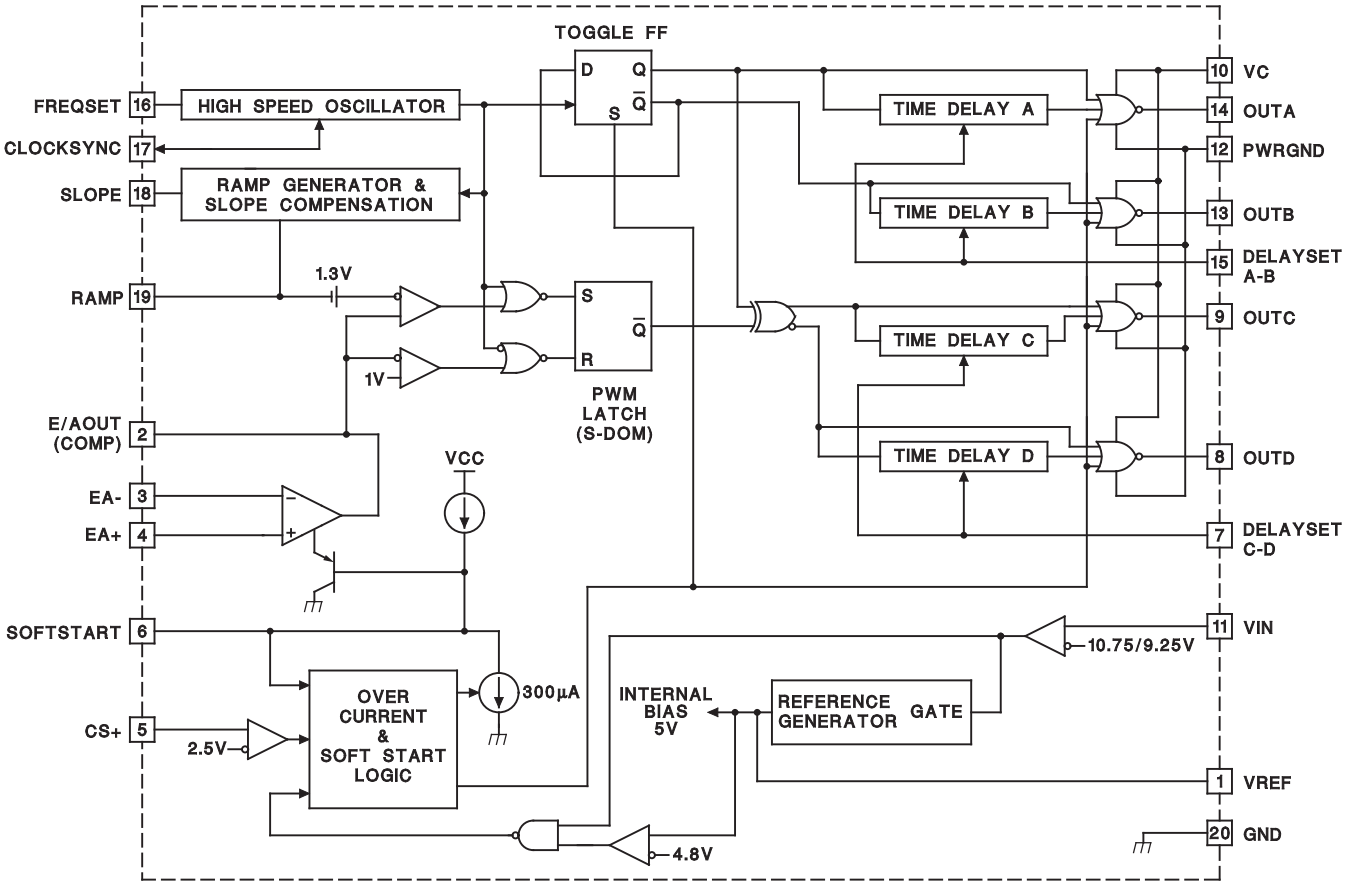
With the oscillator capable of operation at frequencies in excess of 2 MHz, overall switching frequencies to 1 MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75 V threshold. 1.5 hysteresis is built in for reliable, boot-strapped chip supply. Overcurrent protection is provided, and will latch the outputs in the OFF state within 70 nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

Additional features include an error amplifier with bandwidth in excess of 7 MHz, a 5 V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

This device is available in hermetically sealed cerdip, surface mount, and ceramic leadless chip carrier packages for –55°C to +125°C operation.

BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP (J)	5962-9455501VRA	5962-9455501VRA
		5962-9455502VRA	5962-9455502VRA
	LCCC (FK)	5962-9455501V3A	5962-9455501V3A
	CFP (W)	5962-9455502VKA	5962-9455502VKA

ABSOLUTE MAXIMUM RATINGS(1)

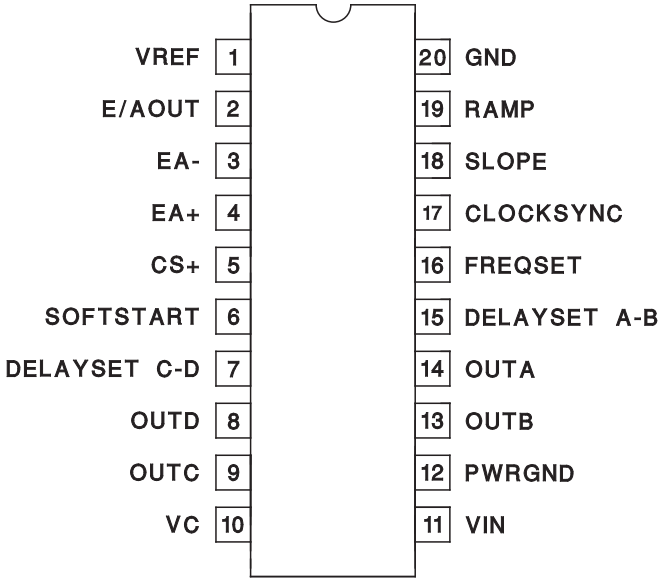
PARAMETER	VALUE		UNIT
	MIN	MAX	
Supply voltage (VC, VIN)		20	V
Output current, source or sink			
DC		0.5	A
Pulse (0.5 µs)		3	A
Analog inputs			
(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19)	–0.3	5.3	V
Storage temperature range	–65	150	°C
Maximum junction temperature, J_{Tmax}		150	
Thermal Resistance T_{JC}			
J package		7	°C/W
W package		5.4	
FK package		5.6	

(1) Pin references are to 20-pin packages. All voltages are with respect to ground. Currents are positive into, negative out of the device terminals.

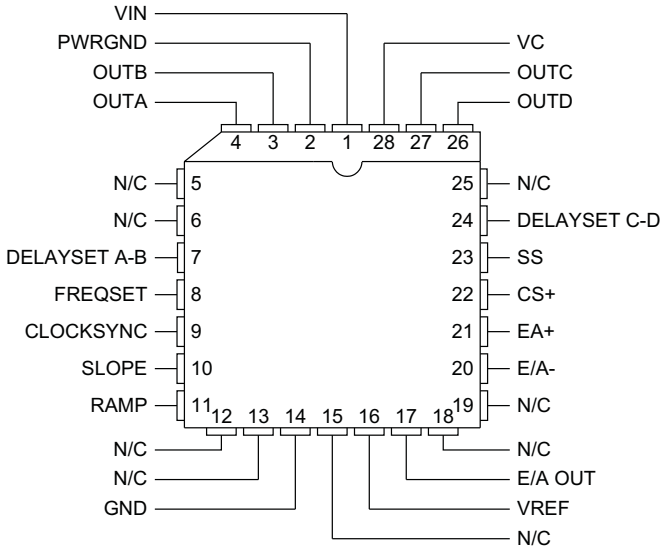
DEVICE INFORMATION

	UVLO Turn-On	UVLO Turn-Off	Delay Set
UCC1875-SP	10.75V	9.25V	Yes

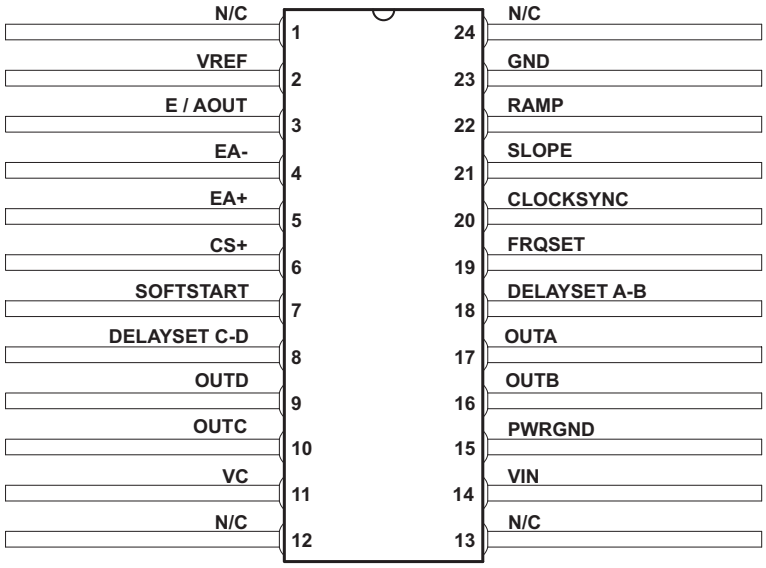
DIL - 20 Pin
J Package
(TOP VIEW)



LCCC - 28 Pin
FK Package
(TOP VIEW)



CFP - 24 Pin
W Package
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A-B)}$ = $C_{(DELAYSET\ C-D)}$ = 0.01 µF, $I_{(DELAYSET\ A-B)}$ = $I_{(DELAYSET\ C-D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Undervoltage Lockout						
Start threshold				10.75	11.75	V
UVLO hysteresis			0.5	1.25	2	V
Supply Current						
I_{IN} Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			150	600	µA
I_C Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			10	100	µA
I_{IN}				30	44	mA
I_C				15	30	mA
Voltage Reference						
Output voltage	T_J = 25°C		4.92	5	5.08	V
Line regulation	11 V < VIN < 20 V			1	10	mV
Load regulation	I_{VREF} = –10 mA			5	20	mV
Total variation	Line, Load, Temperature		4.9		5.1	V
Noise Voltage	10 Hz to 10 kHz			50		µVrms
Long Term Stability	T_J = 125°C, 1000 hours			2.5		mV
Short circuit current	VREF = 0 V, T_J = 25°C			60		mA
Error Amplifier						
Offset voltage				5	15	mV
Input bias current				0.6	3	µA
AVOL	1 V < $V_{(E/AOUT)}$ < 4 V		60	90		dB
CMMR	1.5 V < V_{CM} < 5.5 V		75	95		dB
PSRR	11 V < VIN < 20 V		85	100		dB
Output sink current	$V_{(E/AOUT)}$ = 1 V		1	2.5		mA
Output source current	$I_{(E/AOUT)}$ = 4 V			–1.3	–0.5	mA
Output voltage high	$I_{(E/AOUT)}$ = –0.5 mA		4	4.7	5	V
Output voltage low	$I_{(E/AOUT)}$ = 1 mA		0	0.5	1	V
Unity Gain BW	See (1)	01 device	5			MHz
		02 device	7			MHz
Slew rate	See (1)		6	11		V/µsec
PWM Comparator						
RAMP offset voltage	T_J = 25°C (2)			1.3		V
Zero phase shift voltage	See (3)		0.55	0.9		V
PWM phase shift (4) (5)	$V_{(E/AOUT)}$ > (Ramp Peak + Ramp Offset)	01 device	98	99.5	102	%
		02 device	96	100	104	%
	$V_{(E/AOUT)}$ < Zero Phase Shift Voltage		0	0.5	2	%
Output skew (4) (5)	$V_{(E/AOUT)}$ > 1 V			5	±20	nsec
Ramp to output delay (6) (1)				65	125	nsec

(1) Not production tested.
(2) Ramp offset voltage has a temperature coefficient of about –4 mV/°C.
(3) The zero phase shift voltage has a temperature coefficient of about –2 mV/°C.

(4) Phase shift percentage (0% = 0 , 100% = 180) is defined as $\theta = \frac{200}{T}\phi\%$ where is the phase shift, and and T are defined in Figure 1. At 0% phase shift, is the output skew.
(5) Not production tested at –55·C.
(6) Ramp delay to output time is defined in Figure 1

ELECTRICAL CHARACTERISTICS (continued)

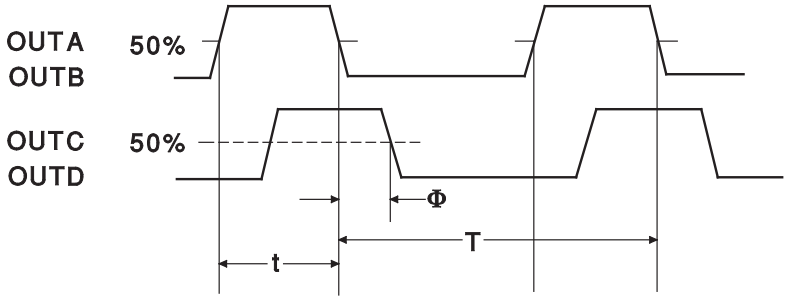
–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A-B)}$ = $C_{(DELAYSET\ C-D)}$ = 0.01 µF, $I_{(DELAYSET\ A-B)}$ = $I_{(DELAYSET\ C-D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Oscillator						
Initial accuracy	T_A = 25°C	01 device	0.85	1	1.15	MHz
		02 device	0.85	1	1.19	
Voltage stability	11 V < VIN < 20 V			0.2	2	%
Total variation	Line, Temperature		0.8		1.2	MHz
Sync pin threshold	T_J = 25°C			3.8		V
Clock out peak	T_J = 25°C			4.3		
Clock out low	T_J = 25°C			3.3		
Clock out pulse width	$R_{(CLOCKSYNC)}$ = 3.9 kΩ			30	100	nsec
Maximum frequency (7)	$R_{(FREQUEST)}$ = 5 kΩ		2			MHz
Ramp Generator/Slope Compensation						
Ramp current, minimum	$I_{(SLOPE)}$ = 10 µA, $V_{(FREQSET)}$ = VREF			–11	–14	µA
Ramp current, maximum	$I_{(SLOPE)}$ = 1 mA, $V_{(FREQSET)}$ = VREF		–0.8	–0.95		mA
Ramp valley				0		V
Ramp peak - clamping level	$R_{(FREQSET)}$ = 100 kΩ		3.8	4.1	5	V
Current Limit						
Input bias	V_{CS+} = 3 V			2	5	µA
Threshold voltage			2.4	2.5	2.6	V
Delay to output (8)				85	150	nsec
Soft Start/Reset Delay						
Charge current	$V_{(SOFTSTART)}$ = 0.5 V		–20	–9	–3	µA
Discharge current	$V_{(SOFTSTART)}$ = 1 V		120	230		
Restart threshold			4.3	4.7		V
Discharge level				300		mV
Output Drivers						
Output low level	I_{OUT} = 50 mA			0.2	0.4	V
Output high level	I_{OUT} = –50 mA			1.5	2.5	
Delay Set						
Delay set voltage	$I_{(DELAY)}$ = –500 µA		2.3	2.4	2.6	V
Delay time (8)	$I_{(DELAY)}$ = –250 µA (9)		150	250	600	nsec

(7) Not production tested at –55·C.
(8) Not production tested.

(9) Delay time can be programmed via resistors from the delay set pins to ground. Delay time = $\frac{62.5 \times 10^{-12}}{I_{(DELAY)}}$.

Where $I_{(DELAY)}$ = $\frac{\text{Delay set voltage}}{R_{(DELAY)}}$. The Recommended range for $I_{(DELAY)}$ is 25 µA ≤ $I_{(DELAY)}$ ≤ 1 mA.



Duty Cycle = t/T, Period = T

T_{DHL} (A to C) = T_{DHL} (B to D) = Φ

Figure 1. Phase Shift, Output Skew and Delay Time Definitions

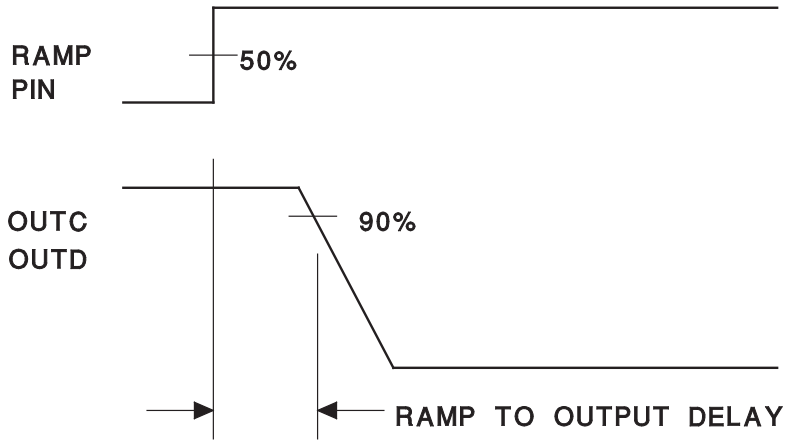


Figure 2. Ramp to Delay Output

PIN DESCRIPTIONS

CLKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (Error Amplifier Output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (Current Sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5 V (separate from VREF). When the voltage at this pin exceeds 2.5 V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise -- this condition will not prematurely deliver power to the load.

FREQSET (Oscillator Frequency Set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELSETA-B, DELSETC-D (Output Delay Control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA– (Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (Error Amplifier Non-Inverting Input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (Signal Ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA – OUTD (Outputs A-D): The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (Power Ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (Voltage Ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{Sense Voltage}}{R_{(SLOPE)} \times C_{(RAMP)}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Because of the 1.3 V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of $R_{(SLOPE)}$ and $C_{(RAMP)}$.

SLOPE (Set Ramp Slope/Slope Compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

SOFTSTART:(soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8 V by an internal 9 µA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5 V), SOFTSTART will be pulled to GND and them ramp to 4.8 V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

VC (Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors

VIN (Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12 V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE

When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100 µA to a current in excess of 20 µA. If the UC1875-SP is not connected to a well bypassed supply, it may immediately enter UVLO again.

VREF: This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75 V. For best results bypass VREF with a 0.1 µF, low ESR, low ESL, capacitor to the GND pin.

APPLICATION INFORMATION

Undervoltage Lockout Section

When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600 µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75 V.

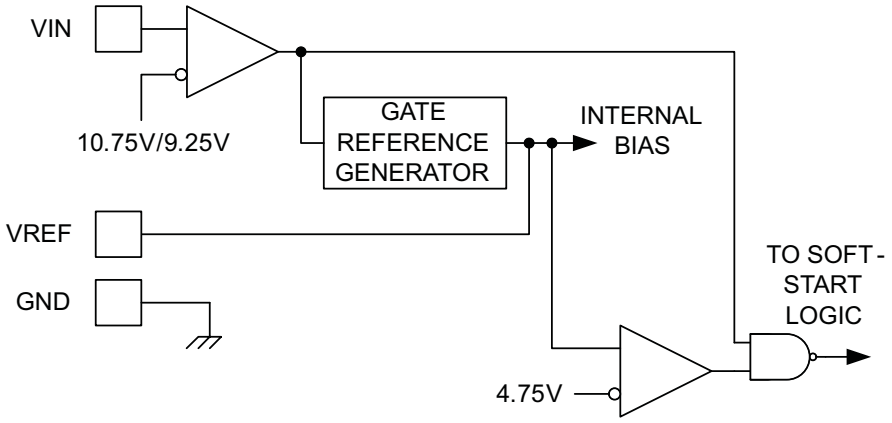
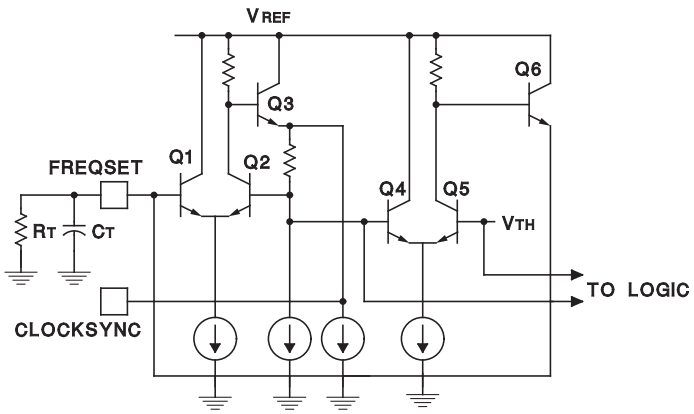
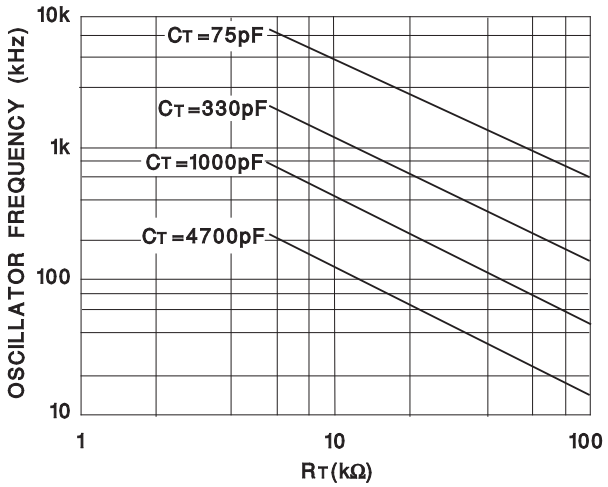


Figure 3. Undervoltage Circuit

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.





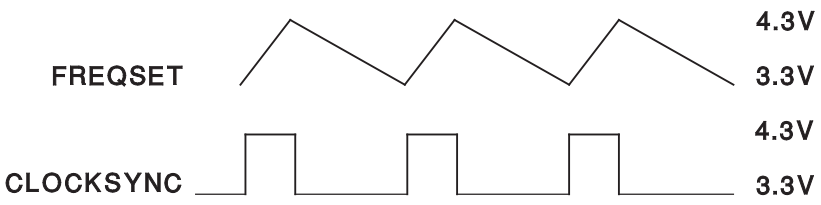


Figure 4. Simplified Oscillator Schematic

Synchronizing The Oscillator

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875-SP device by connecting the CLOCKSYNC of each UC1875-SP to the others:

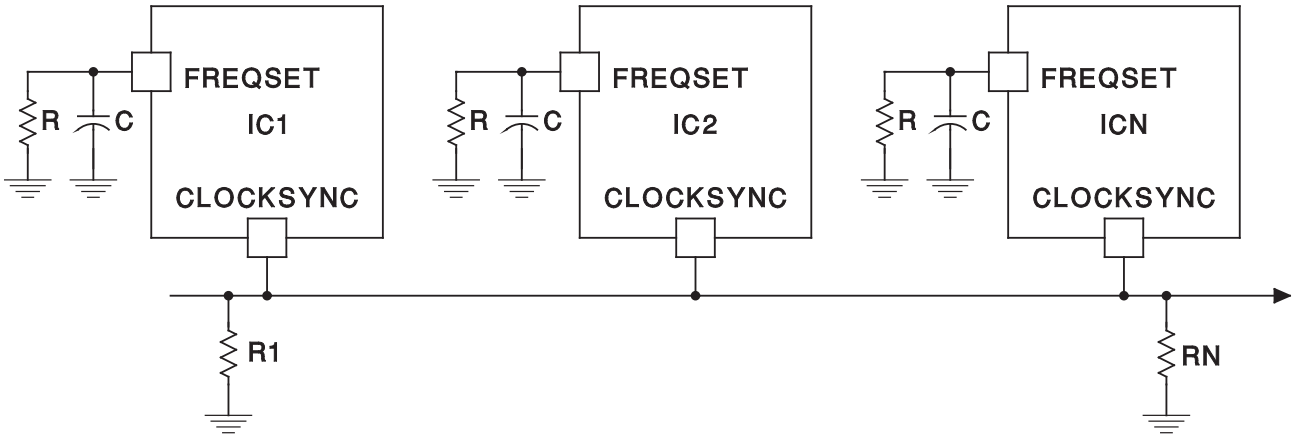


Figure 5.

ALL ICs will sync to the chip with the fastest local oscillator.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Syncing to External TTL/CMOS

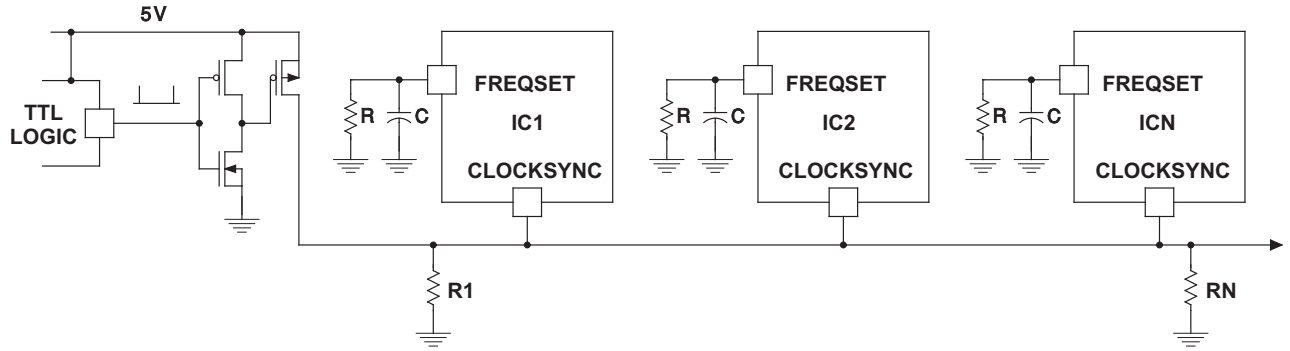


Figure 6.

ICs will sync to the fastest chip or TTL clock if it is higher frequency.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Although the UC1875-SP has a local oscillator frequency, the device will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in Figure 6.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

Delay Blocks and Output Stages

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

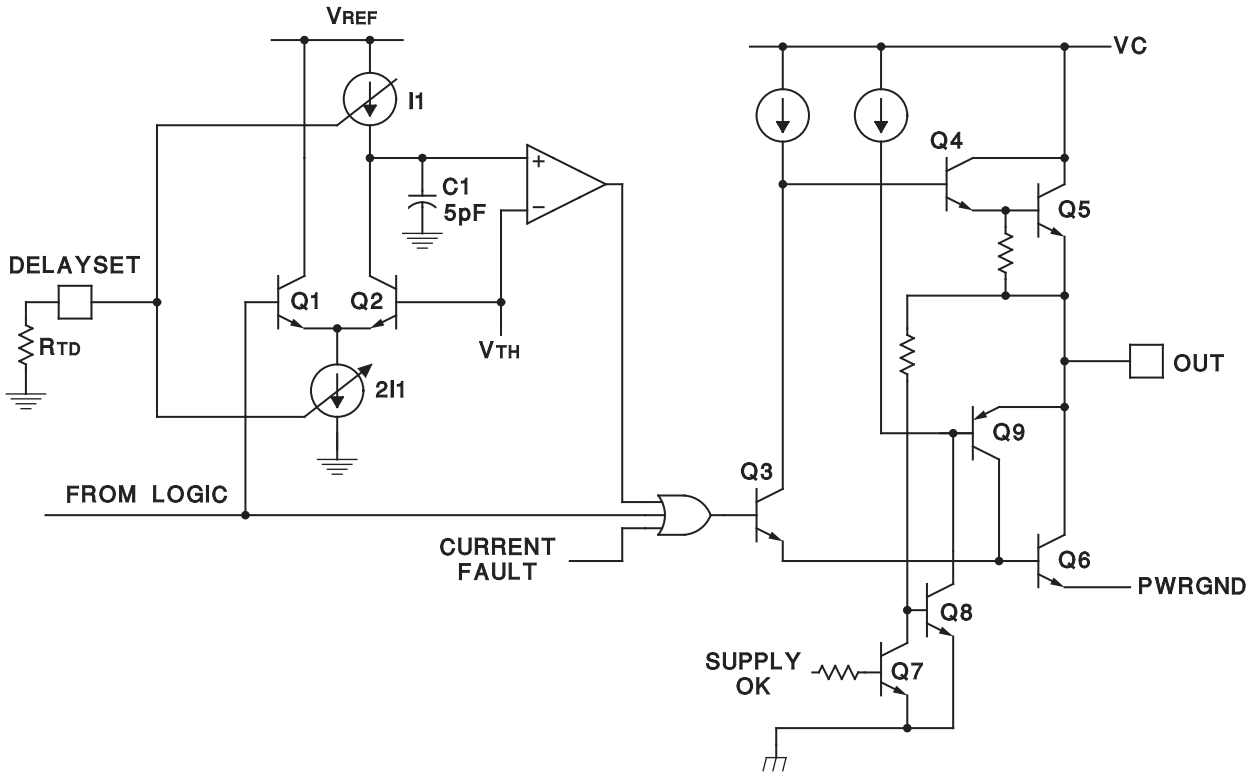


Figure 7.

The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD}. The voltage on the Delay Set pins is internally regulated to 2.5 V and the range of dead time control is from 50 to 200 nanoseconds.

NOTE

There is no way to disable the delay circuitry, and the delay time must be programmed.

Output Switch Orientation

The four outputs of the UC1875-SP interfaces to the full bridge converter switches as shown in Figure 8

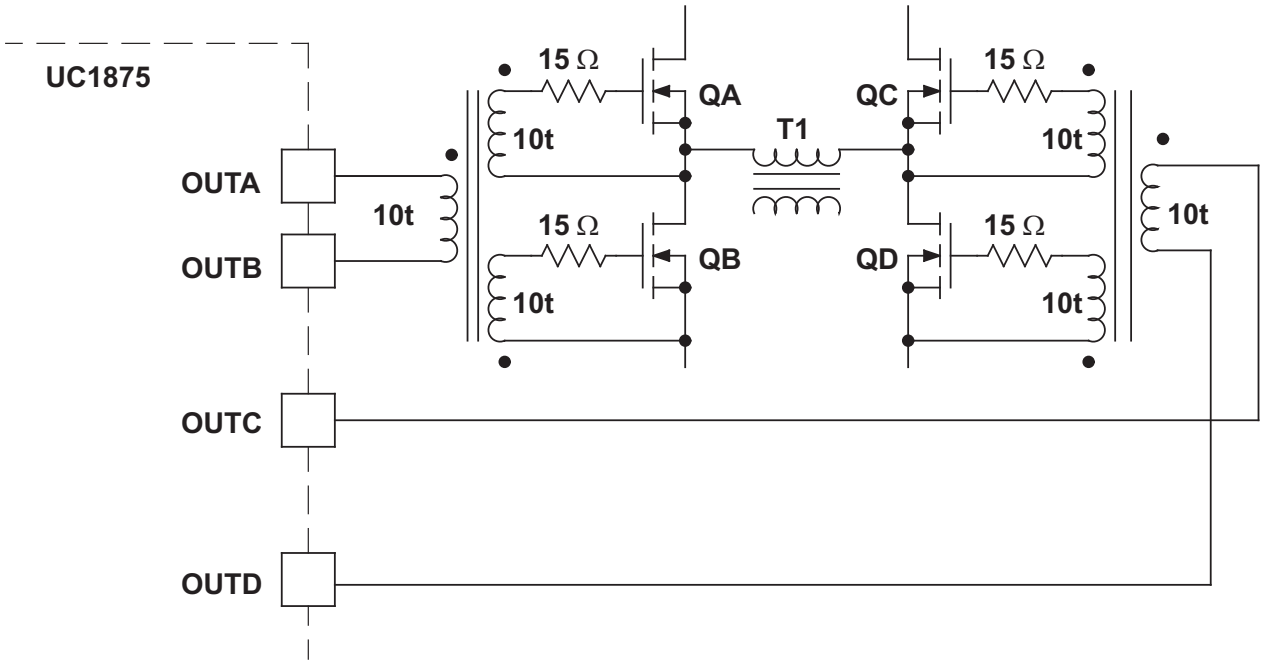


Figure 8. 3 Winding Bifilar, AWG 30 Kynar Insulation

Fault/SoftStart

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency “hiccup” retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.

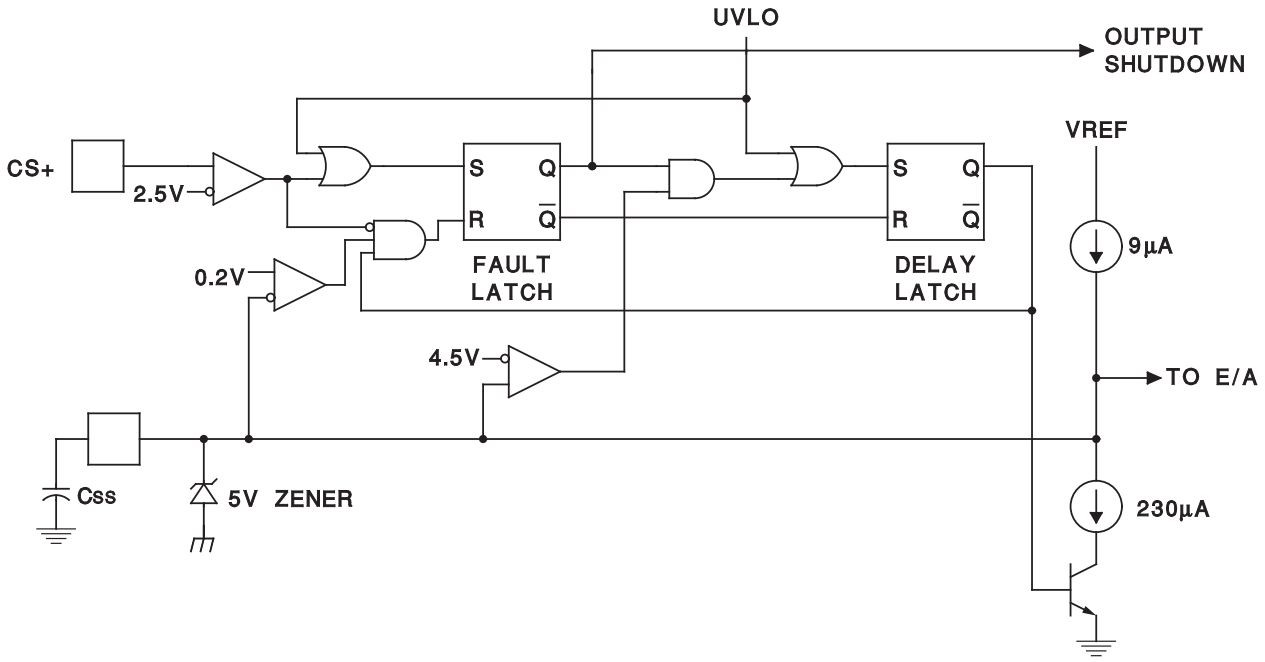


Figure 9.

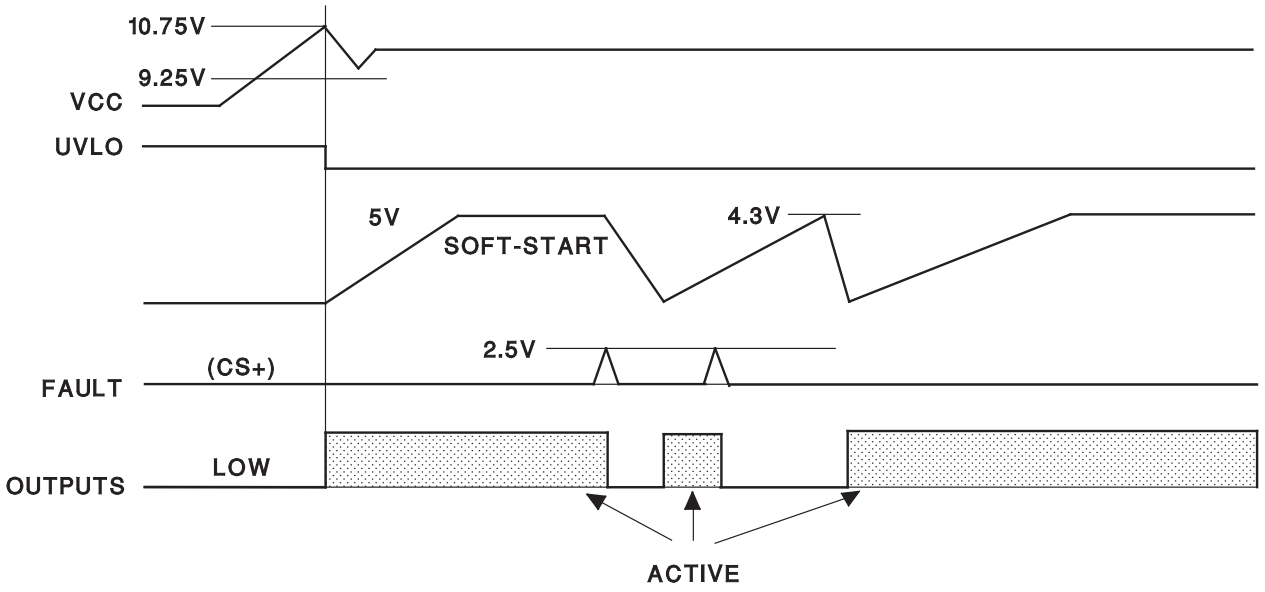


Figure 10.

Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

Figure 11 shows a voltage-mode configuration. With $R_{(SLOPE)}$ tied to a stable voltage source, the waveform on $C_{(RAMP)}$ will be a constant-slope ramp, providing conventional voltage-mode control. If $R_{(SLOPE)}$ is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

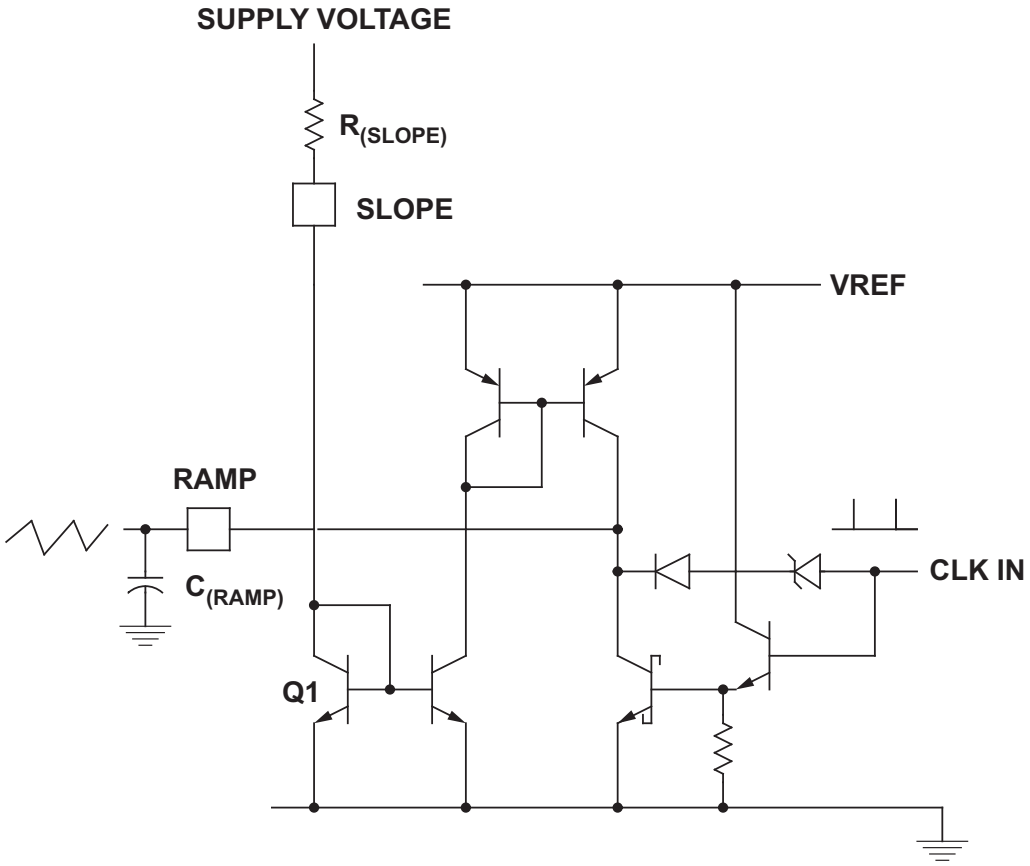


Figure 11. Voltage Mode Operation

1. Simple voltage mode operation achieved by placing $R_{(SLOPE)}$ between VIN and SLOPE
2. Voltage Feedforward achieved by placing $R_{(SLOPE)}$ between supply voltage and SLOPE pin of UC1875-SP.

RAMP:

$$\frac{dV}{dT} = \frac{V_{Rslope}}{R_{SLOPE} \times C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9455501V3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9455501V3A UC1875L QMLV	Samples
5962-9455501VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9455501VRA UC1875JQMLV	Samples
5962-9455502VKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9455502VKA UC1875W-SP	Samples
5962-9455502VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9455502VRA UC1875J-SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1875-SP :

- Catalog: UC1875

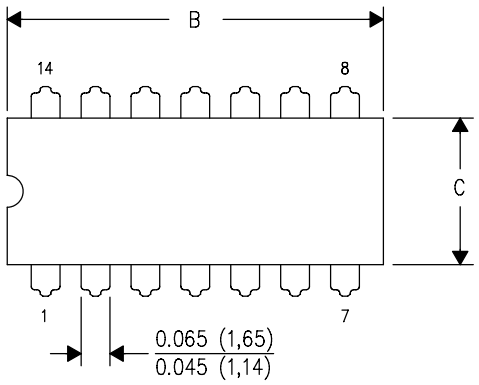
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

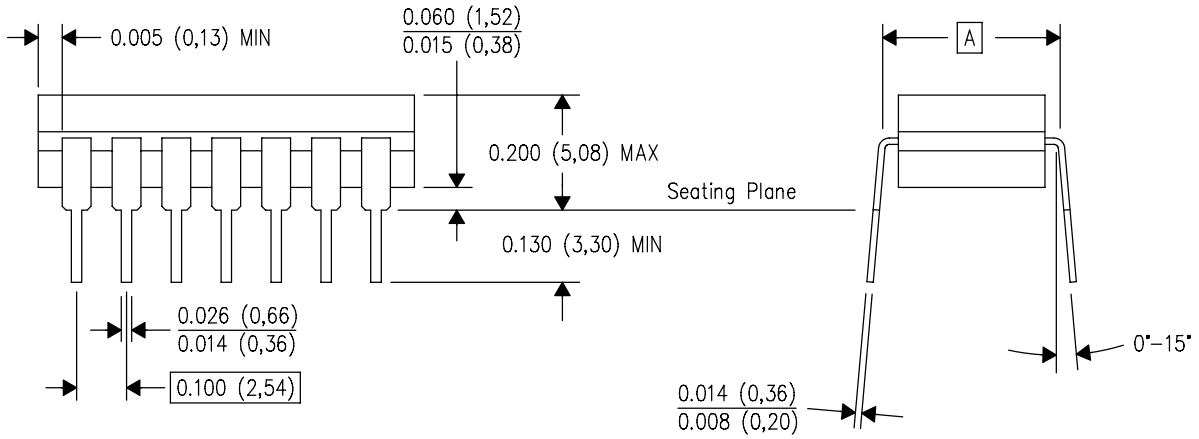
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



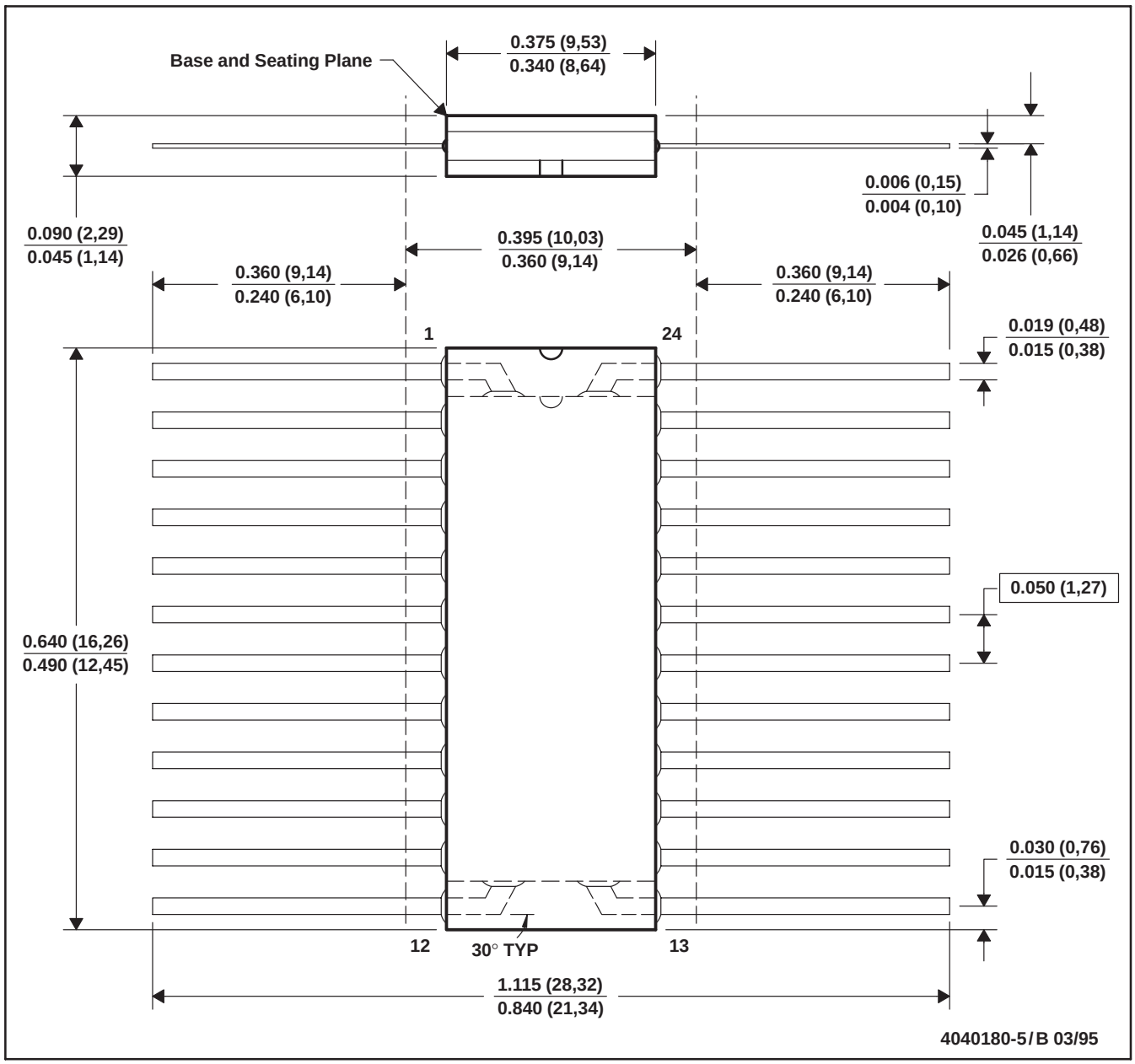
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

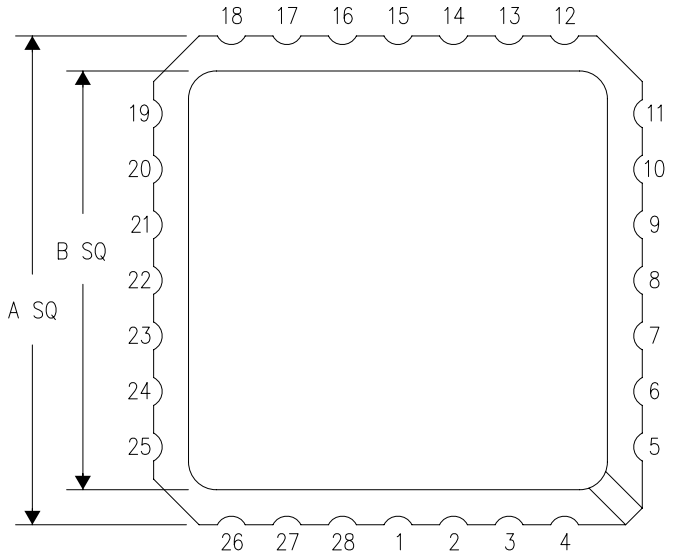
W (R-GDFP-F24) **CERAMIC DUAL FLATPACK**



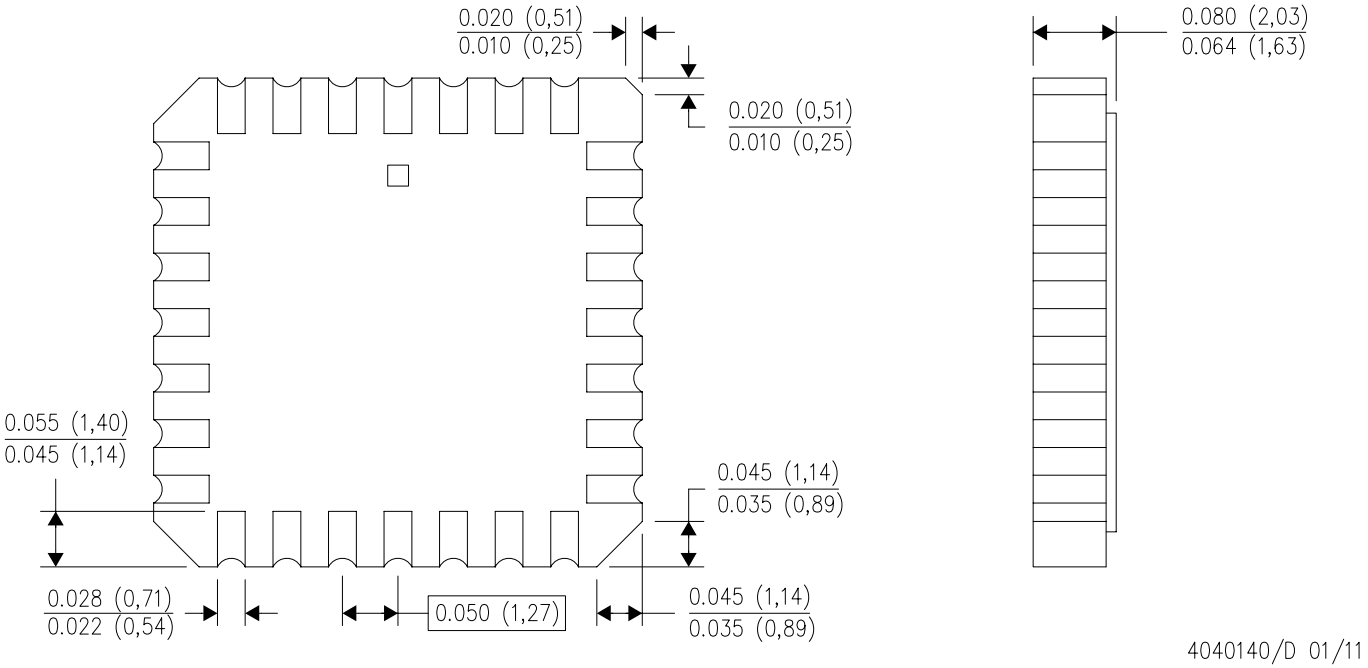
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

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