TEXAS INSTRUMENTS

# ADS8381EVM

# User's Guide

*September 2004* *Data Acquistion*

*SLAU133A*

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third−party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products & application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Secruity | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

**EVM IMPORTANT NOTICE**

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

**EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the input voltage range of ±6 V and the output voltage range of 0 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

# Preface

# Read This First

## *About This Manual*

This users guide describes the characteristics, operation, and use of the ADS8381 18-bit, 580-kHz, parallel interface, analog-to-digital converter evaluation board. A complete circuit description, schematic diagram, and bill of materials are included.

## *How to Use This Manual*

This document contains the following chapters:

- ❏ Chapter 1 – EVM Overview
- ❏ Chapter 2 – Analog Interface
- ❏ Chapter 3 – Digital Interface
- ❏ Chapter 4 – Power Supply Requirements
- ❏ Chapter 5 – Using the EVM
- ❏ Chapter 6 − ADS8381EVM BOM, Layout, and Schematic

## *Related Documentation From Texas Instruments*

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477−8924 or the Product Information Center (PIC) at (972) 644−5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our Web site at www.ti.com

| **Data Sheets:** | **Literature Number:** |
|---|---|
| ADS8381 | SLAS364 |
| REF3040 | SBVS032 |
| REF3020 | SBVS032 |
| SN74AHC138 | SCLS258 |
| SN74AHC245 | SCLS230 |
| SN74AHC1G04 | SCLS318 |
| THS4031 | SLOS224 |

## FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

## Trademarks

TMS320C5000™ and TMS320C6000™ DSP platforms are trademarks of Texas Instruments Incorporated.

# Contents

# Figures



# Tables

# Chapter 1

# EVM Overview

This chapter contains the features of the ADS8381EVM.

**Topic** **Page**

## 1.1 Features

- ❏ Full-featured evaluation board for the high-speed ADS8381 18-bit, single channel, parallel interface, SAR-type analog-to-digital converters.
- ❏ Onboard signal conditioning
- ❏ Onboard reference
- ❏ Input and output digital buffer
- ❏ Onboard decoding for stacking multiple EVMs

Chapter 2

# Analog Interface

The ADS8381 analog-to-digital converter has both a positive and negative analog input pin. Ground for the negative input is provided on the EVM (via SJP3) close the device, or a user-furnished ground wire may be attached. The negative input pin has a range of –200 mV up to 200 mV, and is shorted on the EVM via SJP3. A signal for the positive input pin can be applied at connector P1, pin 2 (shown in Table 2−1 ), or applied to the center pin of SMA connector J2.

*Table 2−1. Analog Input Connector*

| Description | Signal Name | Connector.Pin# | | Signal Name | Description |
|---|---|---|---|---|---|
| Pin tied to Ground | AGND | P1.1 | P1.2 | + | Noninverting Input Channel |
| Reserved | N/A | P1.3 | P1.4 | N/A | Reserved |
| Reserved | N/A | P1.5 | P1.6 | N/A | Reserved |
| Reserved | N/A | P1.7 | P1.8 | N/A | Reserved |
| Pin tied to Ground | AGND | P1.9 | P.10 | N/A | Reserved |
| Pin tied to Ground | AGND | P1.11 | P1.12 | N/A | Reserved |
| Reserved | N/A | P1.13 | P1.14 | N/A | Reserved |
| Pin tied to Ground | AGND | P1.15 | P1.16 | N/A | Reserved |
| Pin tied to Ground | AGND | P1.17 | P1.18 | N/A | Reserved |
| Reserved | N/A | P1.19 | P1.20 | REF+ | External Reference Input |

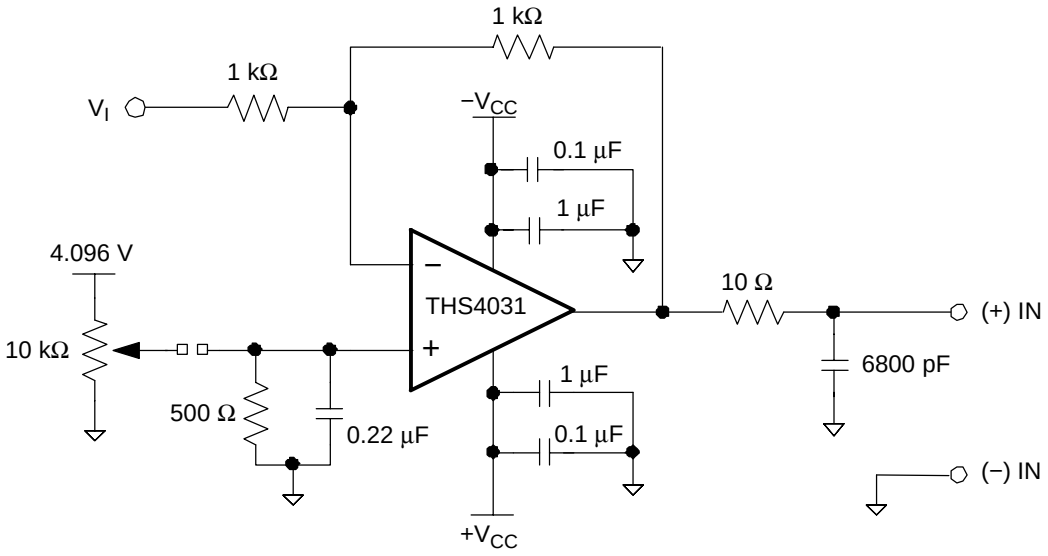
**Topic** **Page**

## 2.1 Signal Conditioning

The factory recommends the analog input to any SAR-type converter be buffered and low-pass filtered. It is important to note that the input buffer circuit of the ADS8381EVM, shown in Figure 2−1, uses the THS4031 in an *inverting* gain-of-one configuration. The amplifier is not stable in a *conventional* gain-of-one configuration. The THS4031 was selected for its low noise, high slew rate, and fast settling time. The low-pass filter resistor and capacitor values are selected such that ADS8381EVM meets the 100-kHz AC performance specifications listed in the data sheet. The series resistor works with the capacitor to filter the input signal, but also isolates the amplifier from the 6800-pF capacitive load. The capacitor to ground at the input of the A/D works with the series resistor to filter the input signal, and acts like a charge reservoir. This external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode.

The EVM has a provision to offset the input voltage by adjusting R23, a 10-kΩ potentiometer.

*Figure 2−1. Input Buffer Circuit*



## 2.2 Reference

The ADS8381EVM provides an onboard 4.096-V reference circuit. This reference voltage can be applied directly to the VREF pin of the converter; it does not need to be buffered. The EVM also has provision for a user-supplied external reference voltage. This voltage can be filtered, as needed, by routing the signal through amplifier U1.

The EVM allows users to select from two reference sources. Set SJP1 and SJP2 to select onboard reference voltage (REF3040), or a user-supplied reference voltage via P1 pin 20. See Table 2−2 for jumper settings. See Chapter 6 for the full schematic.

*Table 2−2. Solder Short Jumper Setting*

| Reference Designator | Description | Jumper Setting | |
|---|---|---|---|
| | | 1−2 | 2−3 |
| SJP1 | Select REF3040 output for reference voltage | Installed† | |
| | Select buffered reference voltage | | Installed |
| SJP2 | Select U3, REF3040, as 4.096-V reference | Installed† | |
| | Buffer the user−supplied reference voltage | | Installed |
| SJP3 | Short (−)IN pin to ground | Installed† | N/A |
| SJP4 | Apply offset voltage to A/D buffer | Installed† | N/A |
| SJP5 | Set amplifier U1 negative supply to ground | Installed | |
| | Set amplifier U1 negative supply to $-V_{CC}$ | | Installed† |
| SJP6 | Set amplifier U2 negative supply to ground | Installed | |
| | Set amplifier U2 negative supply to $-V_{CC}$ | | Installed† |

† Factory-set condition

# Chapter 3

# Digital Interface

The ADS8381EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW−110−22−F−D−VS−K and TSM−110−01−T−DV−P provide a convenient dual-row-header/socket combination at P2 and P3. Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for a variety of mating connector options.

*Table 3−1. Pinout for Parallel Control Connector P2*

| Connector.Pin | Signal | Description |
|---|---|---|
| P2.1 | $\overline{DC}\_\overline{CS}$ | Daughtercard Board Select pin |
| P2.3 | | |
| P2.5 | | |
| P2.7 | A0 | Address line from processor |
| P2.9 | A1 | Address line from processor |
| P2.11 | A2 | Address line from processor |
| P2.13 | | |
| P2.15 | | |
| P2.17 | | |
| P2.19 | $\overline{INTc}$ | Set jumper W3 to select BUSY or inverted signal to be applied to this pin. |

**Note:** All even-numbered pins of P2 are tied to DGND.

Read ($\overline{RD}$) and conversion start ($\overline{CONVST}$) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8381EVMs into processor memory. See Table 3−2 for jumper settings. Note, the evaluation module does not allow the chip select ($\overline{CS}$) line of the converter to be assigned to different memory locations. It is therefore suggested that the $\overline{CS}$ line be grounded or wired to an appropriate signal of the processor.

*Table 3−2. Jumper Settings*

| Reference Designator | Description | Jumper Settings | |
|---|---|---|---|
| | | 1−2 | 2−3 |
| W1 | Set A[2..0] = 0x1 to generate $\overline{RD}$ pulse | Installed† | Not installed |
| | Set A[2..0] = 0x2 to generate $\overline{RD}$ pulse | Not installed | Installed |
| W2 | Set A[2..0] = 0x3 to generate $\overline{CONVST}$ pulse | Installed† | Not installed |
| | Set A[2..0] = 0x4 to generate $\overline{CONVST}$ pulse | Not installed | Installed |
| W3 | Apply BUSY to P3 pin 19 | Not installed | Installed† |
| | Apply inverted BUSY to P3 pin 19 | Installed | Not installed |

† Factory-set condition

The data bus is available at connector P3; see Table 3−3 for pinout information.

*Table 3−3. Data Bus Connector P3*

| Connector.Pin | Signal | Description |
|---|---|---|
| P3.1 | D0 | Buffered Data Bit 0 (LSB) |
| P3.3 | D1 | Buffered Data Bit 1 |
| P3.5 | D2 | Buffered Data Bit 2 |
| P3.7 | D3 | Buffered Data Bit 3 |
| P3.9 | D4 | Buffered Data Bit 4 |
| P3.11 | D5 | Buffered Data Bit 5 |
| P3.13 | D6 | Buffered Data Bit 6 |
| P3.15 | D7 | Buffered Data Bit 7 |
| P3.17 | D8 | Buffered Data Bit 8 |
| P3.19 | D9 | Buffered Data Bit 9 |
| P3.21 | D10 | Buffered Data Bit 10 |
| P3.23 | D11 | Buffered Data Bit 11 |
| P3.25 | D12 | Buffered Data Bit 12 |
| P3.27 | D13 | Buffered Data Bit 13 |
| P3.29 | D14 | Buffered Data Bit 14 |
| P3.31 | D15 | Buffered Data Bit 15 |
| P3.33 | D16 | Buffered Data Bit 16 |
| P3.35 | D17 | Buffered Data Bit 17 (MSB) |

**Note:** All even-numbered pins of P3 are tied to DGND.

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J4; see Table 3−4.

*Table 3−4. Pinout for Converter Control Connector J4*

| Connector.Pin | Signal | Description |
|---|---|---|
| J4.1 | $\overline{CS}$ | Chip Select pin. Active low |
| J4.3 | $\overline{RD}$ | Read pin. Active low |
| J4.5 | $\overline{CONVST}$ | Convert start pin. Active low |
| J4.7 | BYTE | Byte select input. Used for 8-bit bus reading. |
| J4.9 | BUS 18/$\overline{16}$ | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer. |
| J4.11 | BUSY | Converter status output. High when a conversion is in progress. |

**Note:** All even-numbered pins of P4 are tied to DGND.

Chapter 4

# Power Supply Requirements

The EVM accepts four power supplies.

- ❑ A dual ±Vs DC supply for the dual supply op amps. Recommend a ±6-VDC supply.
- ❑ A single +5.0-VDC supply for analog section of the board (A/D + Reference).
- ❑ A single +5.0-V or +3.3-VDC supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1) Wire in the voltages at test points on the EVM. See Table 4−1.

*Table 4−1. Power Supply Test Points*

| Test Point | Signal | Description |
|---|---|---|
| TP16 | +BVDD | Apply +3.3 V or +5.0 V. See ADC data sheet for full range. |
| TP20 | +AVCC | Apply +5.0 V. |
| TP14 | +VA | Apply +6.0 V. Positive supply for amplifier. |
| TP18 | −VA | Apply –6.0 V. Negative supply for amplifier. |

2) Use the power connector J1, and derive the voltages elsewhere. The pinout for this connector is shown below. If using this connector, set the W4 jumper to connect +3.3 V or +5 V from connector to +BVDD. Short between pins 1−2 to select +5 VD, or short between pins 2−3 to select +3.3 VD as the source for the digital buffer voltage supply (+BVDD).

*Table 4−2. Power Connector, J1, Pinout*

| Signal | Power Connector − J1 | | Signal |
|---|---|---|---|
| +VA (+6 V) | 1 | 2 | –VA (–6 V) |
| +5 VA | 3 | 4 | N/C |
| DGND | 5 | 6 | AGND |
| N/C | 7 | 8 | N/C |
| +3.3 VD | 9 | 10 | +5 VD |

# Chapter 5

# Using the EVM

The ADS8381EVM serves three functions

1) As a reference design
2) As a prototype board and
3) As software test platform

**Topic** **Page**

## 5.1 As a Reference Board

As a reference design, the ADS8381EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for a 100-kHz sine wave; therefore, users may need to adjust the resistor and capacitor values of the A/D input RC circuit. In AC type applications where signal distortion is a concern, polypropylene capacitors should be used in the signal path.

## 5.2 As a Prototype Board

As a prototype board, the buffer circuit consists of a standard 8-pin SOIC footprint and resistor pads for inverting and noninverting configurations. The ADS8381EVM can be used to evaluate both dual-supply and single-supply amplifiers. The EVM comes installed with a dual-supply amplifier as it allows the user to take advantage of the full input voltage range of the converter. For applications that require single-supply operation (and a smaller input voltage range), the THS4031 can be replaced with a single-supply amplifier like the OPA300. Pad jumper SJP6 should be shorted between pads 1 and 2, as it shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied via test point TP14 or connector J1, pin 1.

## 5.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5−6K interface card. The 5−6K interface card sits on the TMS320C5000™ and TMS320C6000™ DSP platform starter kit (DSK). The ADS8381EVM is then mapped into the processor memory space. This card also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8381 analog-to-digital converter. See the 5−6K interface card user's guide (SLAU104) for more information.

For the software engineer, the ADS8381EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide 3 address lines (A2, A1, and A0) and address-valid line ($\overline{\text{DC\_CS}}$) to connector P2. To choose the address combinations that generate $\overline{\text{RD}}$ and $\overline{\text{CONVST}}$, set jumpers as shown in Table 3−2. Recall that the chip select ($\overline{\text{CS}}$) signal is not memory-mapped or tied to P2; therefore, it must be controlled via a general purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and to control via J3.

Chapter 6

# ADS8381EVM BOM, Layout, and Schematic

This chapter contains the ADS8381EVM bill of materials, the layouts, and the schematic.

**Topic** **Page**

## 6.1 ADS8381EVM Bill of Materials

Table 6−1 contains a complete bill of materials for the ADS8381EVM. The schematic diagram also is provided for reference. Contact the Product Information Center or send an e−mail to dataconvapps@list.ti.com for questions regarding this EVM.

*Table 6−1. ADS8381EVM Bill Of Materials*

| Reference Designator | QTY | Value | Footprint | Mfr | Mfr's Part Number | Description |
|---|---|---|---|---|---|---|
| R4, R21 | 2 | 0 Ω | 603 | Panasonic−ECG or Alternate | ERJ−3GEY0R00V | 0 Ω 1/16 W 5% 0603 SMD |
| R1 | 1 | 0 Ω | 805 | Panasonic−ECG or Alternate | ERJ−6GEY0R00V | 0.0 Ω 1/10W 5% 0805 SMD |
| R13 | 1 | 10 Ω | 805 | Panasonic−ECG or Alternate | ERJ−6ENF10R0V | 10.0 Ω 1/10W 1% 0805 SMD |
| R24 | 1 | 50 Ω | 805 | Panasonic−ECG or Alternate | ERJ−6ENF49R9V | 49.9 Ω 1/10W 1% 0805 SMD |
| R14, R15 | 2 | 100 Ω | 603 | Panasonic−ECG or Alternate | ERJ−3EKF1000V | 100 Ω 1/16W 1% 0603 SMD |
| R25 | 1 | 100 Ω | 805 | Not installed | Not installed | |
| R2 | 1 | NI | 805 | Not installed | Not installed | |
| R6, R10 | 2 | 1k | 805 | Panasonic−ECG or Alternate | ERJ−6ENF1001V | 1.00 kΩ 1/10W 1% 0805 SMD |
| R16, R17, R18, R19, R20 | 5 | 10k | 603 | Panasonic−ECG or Alternate | ERJ−3EKF1002V | 10.0 kΩ 1/16W 1% 0603 SMD |
| R7 | 1 | 10k | 805 | Panasonic−ECG or Alternate | ERA−S15J103V | 10 kΩ 1/10W 1500 PPM 5%0805 |
| R3 | 1 | NI | 603 | Not installed | Not installed | |
| R11 | 1 | NI | 805 | Not installed | Not installed | |
| C3, C5, C11, C23 | 4 | 1 nF | 1206 | Kemet or Alternate | C1206C102J5GACTU | 1000 pF 50 V ceramic NPO 1206 |
| C39 | 1 | 6800 pF | TH | WIMA or Alternate | MKP2 6800/630/5 | 6800 pF polypropylene capacitor |
| C21, C41, C44, C46, C48, C53, C56, C65, C50 | 9 | 0.01 µF | 603 | Kemet or Alternate | C0603C103J5RACTU | 10000 pF 50 V ceramic X7R 0603 |
| C10, C20 | 2 | 0.01 µF | 805 | Kemet or Alternate | C0805C103K5RACTU | 10000 pF 50 V ceramic X7R 0805 |
| C4, C26 | 2 | 0.01 µF | 1206 | Kemet or Alternate | C1206C103J5RACTU | 10000 pF 50 V ceramic X7R 1206 |
| C25, C40, C42, C43, C47, C51, C52, C54, C55, C57, C58, C59, C64, C38 | 14 | 0.1 µF | 603 | Kemet or Alternate | C0603C104K3RACTU | 0.1 µF 25 V ceramic X7R 0603 |

| Reference Designator | QTY | Value | Footprint | Mfr | Mfr's Part Number | Description |
|---|---|---|---|---|---|---|
| C7, C9, C15, C22, C32, C34, C36 | 7 | 0.1 µF | 805 | Kemet or Alternate | C0805C104J5RACTU | Capacitor, 0.1 µF 50 V ceramic X7R 0805 |
| C8, C16, C31, C37 | 4 | 1 µF | 805 | Panasonic − ECG or Alternate | ECJ−GVB1C105K | Capacitor, 1 µF 16 V ceramic X5R 0805 |
| C2, C28 | 2 | 1 µF | 1206 | Kemet or Alternate | C1206C105K3RACTU | Capacitor, 1.0 µF 25 V ceramic X7R 1206 |
| C33 | 1 | 0.22 µF | 805 | Panasonic−ECG or Alternate | ECJ−2VB1C224K | Capacitor, .22 µF 16 V ceramic X7R 0805 |
| C63 | 1 | 0.47 µF | 603 | Panasonic− ECG or Alternate | ECJ−1VF1C474Z | Capacitor .47 µF 16V ceramic Y5V 0603 |
| C62 | 1 | 10 µF | 805 | Not installed | Not installed | |
| C1, C6, C12, C19 | 4 | 10 µF | 1206 | Panasonic−ECG or Alternate | ECJ−3YB1C106M | Capacotor, 10 µF 16 V ceramic X5R 1206 |
| C14, C24, C27, C29, C49 | 5 | 10 µF | 3528 | Kemet or Alternate | T491B106K016AS | Capacitor, TANT 10 µF 16 V 10% SMT |
| C17 | 1 | 47 µF | 1206 | TDK Corporation or Alternate | C3216X5R0J476M | Capacitor, CER 47 µF 6.3 V X5R 20% 1206 |
| C13, C18, C45, C60, C61 | 5 | NI | 603 | Not installed | Not installed | |
| C30, C35, R5 | 3 | NI | 805 | Not installed | Not installed | |
| RP1, RP3 | 2 | 1 kΩ | CTS_742 | CTS Corporation | 742C163102JTR | Resistor Array, 1 kΩ 16TERM 8RES SMD |
| RP2 | 1 | 100 Ω | CTS_742 | CTS Corporation | 742C163101JTR | Resistor Array, 100 Ω 16TERM 8RES SMD |
| RP4 | 1 | 1 kΩ | CTS_742_4RES | CTS Corporation | 744C083102JTR | Resistor ARAY 1 kΩ 16TERM 4RES SMD |
| R23 | 1 | 10kΩ | BOURNS 32X4W | Bourns | 3214W−1−103E | TRIMPOT, 10 kΩ 4MM Top Adj SMD |
| L1, L2, L3, L4 | 4 | BLM21AJ601SN1L | 1206 | MURATA ERIE | BLM31PG601SN1L | Chip, Ferrite Beads− 600 Ω @ 100 MHz |
| U1 | 1 | OPA627 | 8−SOP(D) | Texas Instruments | OPA627AU | Amplifier |
| U2 | 1 | THS4031 | 8−SOP(D) | Texas Instruments | THS4031IDR | 100-MHz low-noise high-speed amplifier |
| U3 | 1 | REF3040 | 3−SOT−23 | Texas Instruments | REF3040AIDBZT | REF3040 50 ppm/°C, 50 µA in SOT23−3 CMOS voltage reference |
| U4 | 1 | ADS8381 | Socket 48QFP | Texas Instruments | ADS8381IPFB | ADS8381 18 bit 580 KSPS |
| U5, U6, U7, U8 | 4 | SN74AHC245PWR | 20−TSSOP(PW) | Texas Instruments | SN74AHC245PWR | Octal bus transceiver, 3-state |

| Reference Designator | QTY | Value | Footprint | Mfr | Mfr's Part Number | Description |
|---|---|---|---|---|---|---|
| U9 | 1 | SOIC−8 Footprint | 8−SOP(D) | Not installed | Not installed | Footprint for 8-pin SOIC reference operates from +5 V. |
| U10 | 1 | REF3020 | 3−SOT−23 | Not installed | Not installed | REF3020 50 ppm/°C, 50 μA in SOT23−3 CMOS voltage reference |
| U11 | 1 | SN74AHC138PWR | 16−TSSOP(PW) | Texas Instruments | SN74AHC138PWR | 3−Line to 8−Line Decoder/Demultiplexer |
| U12 | 1 | SN74AHC1G04DBV | 5−SOT(DBV) | Texas Instruments | SN74AHC1G04DBVR | Single inverter gate |
| J1 | 1 | 5X2X.1 | 5X2X.1_SMT_SOCKET | Samtec | SSW−105−22−S−D−VS | 0.025" SMT socket – bottom side of PWB |
| | | | | Samtec | TSM−105−01−T−D−V−P | 0.025" SMT plug – top side of PWB |
| J2 | 1 | SMA_PCB_MT | SMA_JACK | Johnson Components Inc. | 142−0701−301 | Right Angle SMA Connector |
| J4 | 1 | 6X2X.1 | 6X2X.1_SMT_plug_&_socket | Samtec | SSW−106−22−S−D−VS | 0.025" SMT Socket− bottom side of PWB |
| | | | | Samtec | TSM−106−01−T−D−V−P | 0.025" SMT PLUG − top side of PWB |
| P3 | 1 | 18X2X.1_SMT_PLUG_&_SOCK-ET | 18X2.1_SMT_PLUG_&_SOCKET | Samtec | SSW−118−22−S−D−VS | 0.025" SMT socket − bottom side of PWB |
| | | | | Samtec | TSM−118−01−T−D−V−P | 0.025" SMT plug − top side of PWB |
| P1, P2 | 2 | 10X2X.1 | 10X2X.1_SMT_PLUG_&_SOCKET | Samtec | SSW−110−22−S−D−VS | 0.025" SMT socket − bottom side of PWB |
| | | | | Samtec | TSM−110−01−T−D−V−P | 0.025" SMT plug − top side of PWB |
| SJP3, SJP4 | 2 | SJP2 | SJP2 | Not installed | Not installed | Pad 2 position Jumper |
| SJP1, SJP2, SJP5, SJP6 | 4 | SJP3 | SJP3 | Not installed | Not installed | Pad 3 Postion Jumper |
| W1, W2 | 4 | 3pos_jumper | 3pos_jump | Samtec | TSW−103−07−L−S | 3 Position Jumper_0.1" spacing |
| W3, W4 | | | | | | |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP14, TP15, TP16, TP17, TP18, TP19, TP20 | 16 | TP_0.025 | test_point2 | Keystone Electronics | 5000K–ND | Test Point − Single 0.025" Pin |

## 6.2 ADS8381EVM Layout

*Figure 6−1. Top Layer—Layer 1*

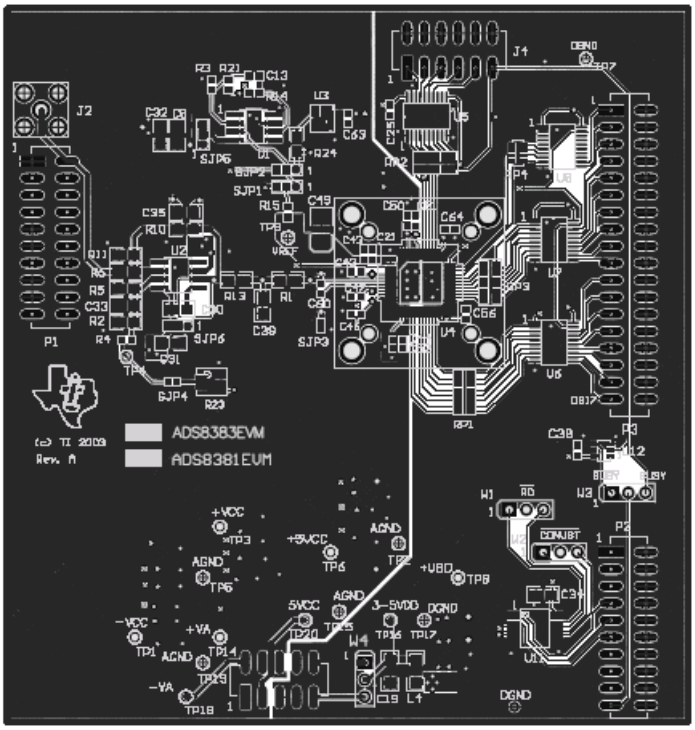



*Figure 6−2. Ground Plane—Layer 2*

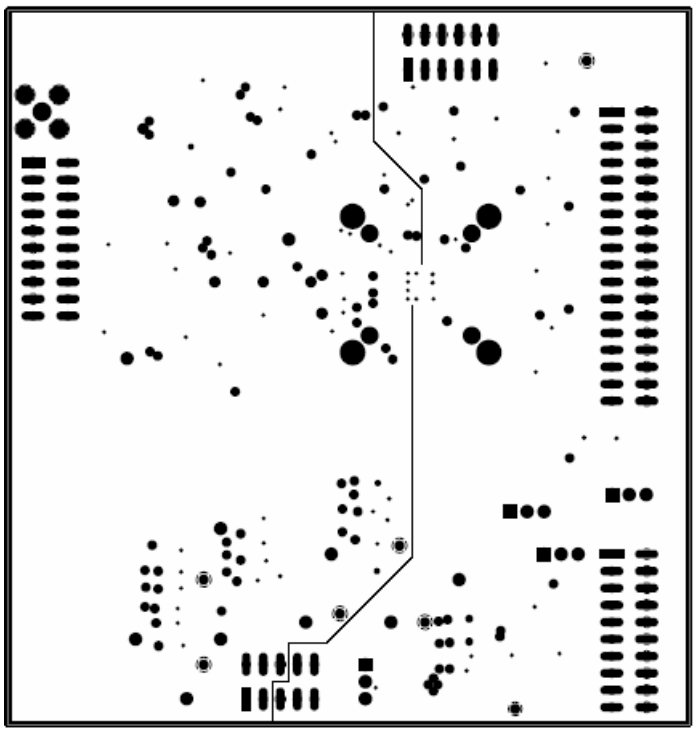


*Figure 6−3. Power Plane—Layer 3*

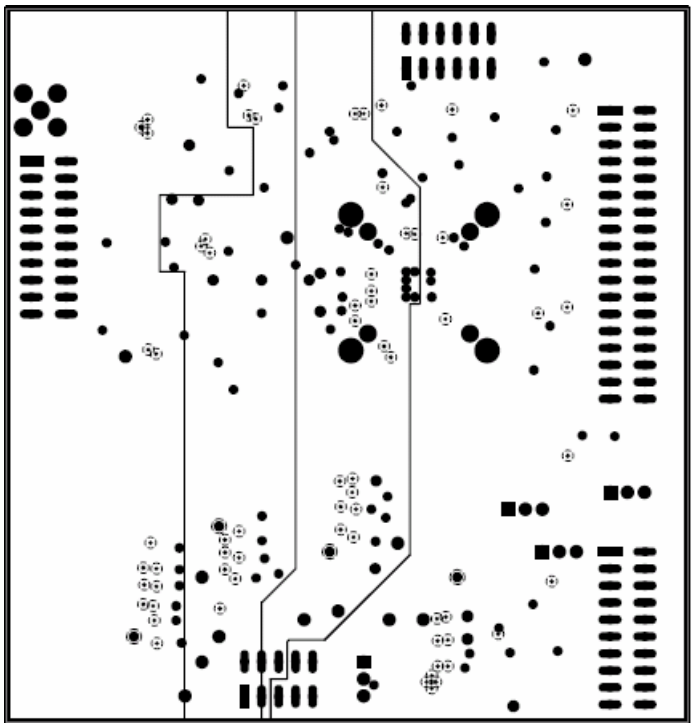
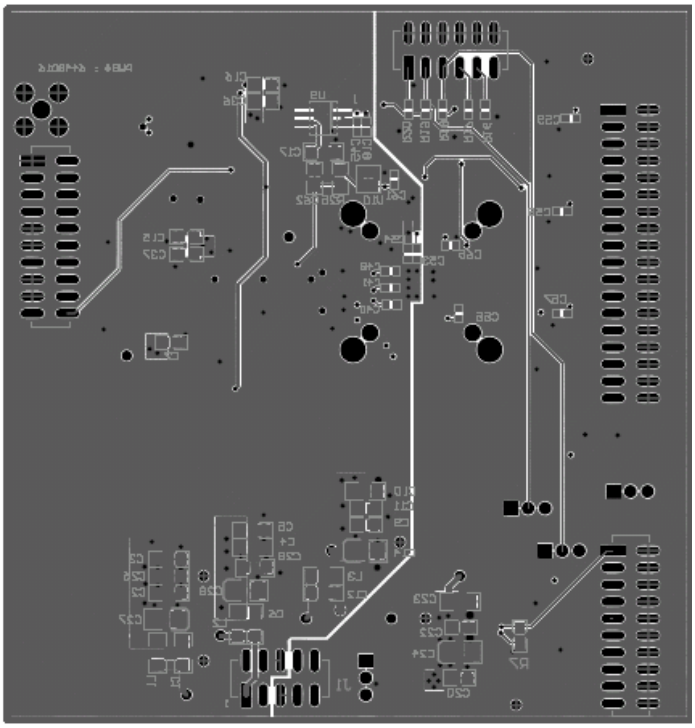


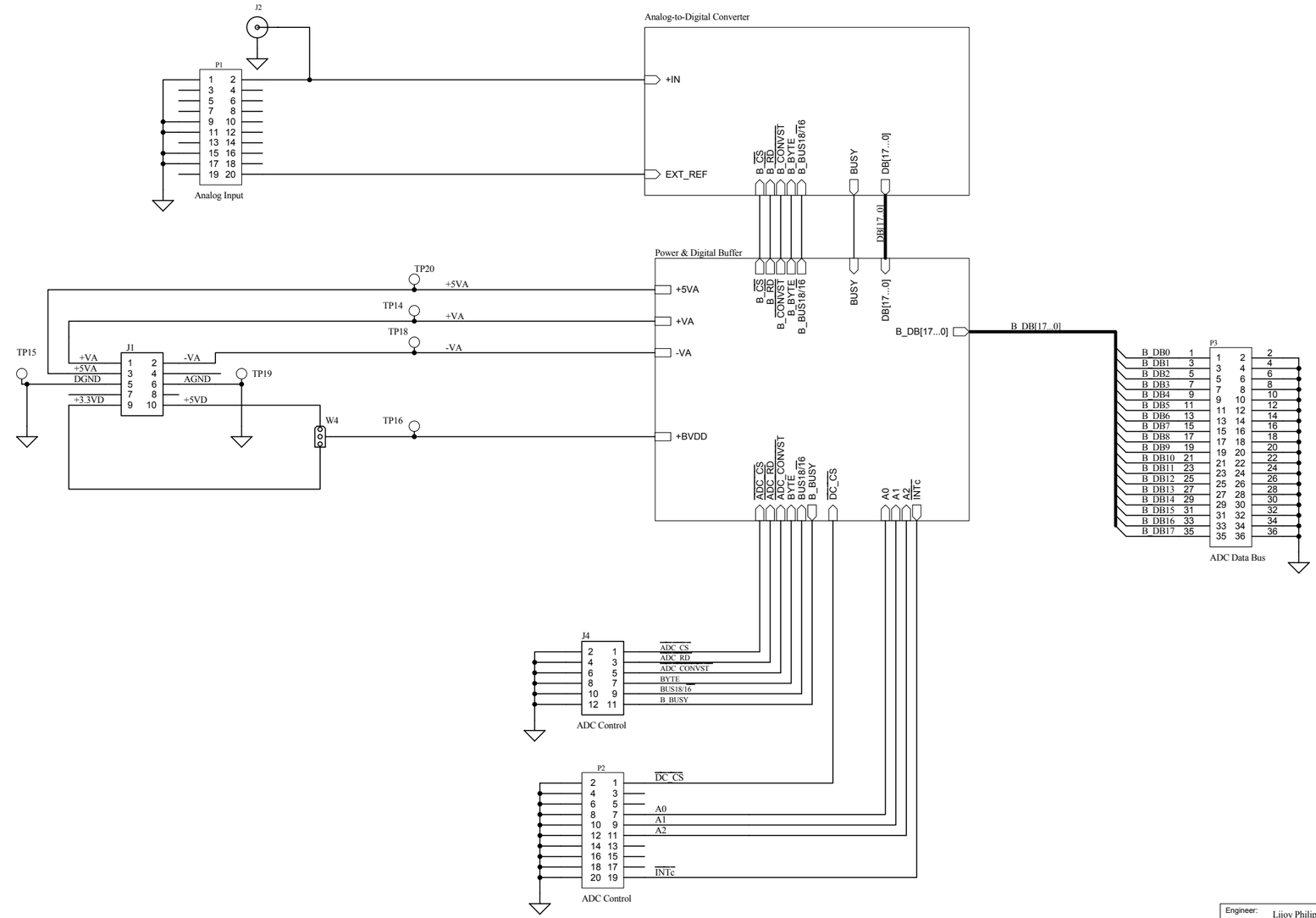
*Figure 6−4. Bottom Layer—Layer 4*



## 6.3 ADS8381EVM Schematic

The schematic follows this page.

| Revision History | | |
|---|---|---|
| REV | ECN Number | Approved |
| | | |
| | | |
| | | |
| | | |

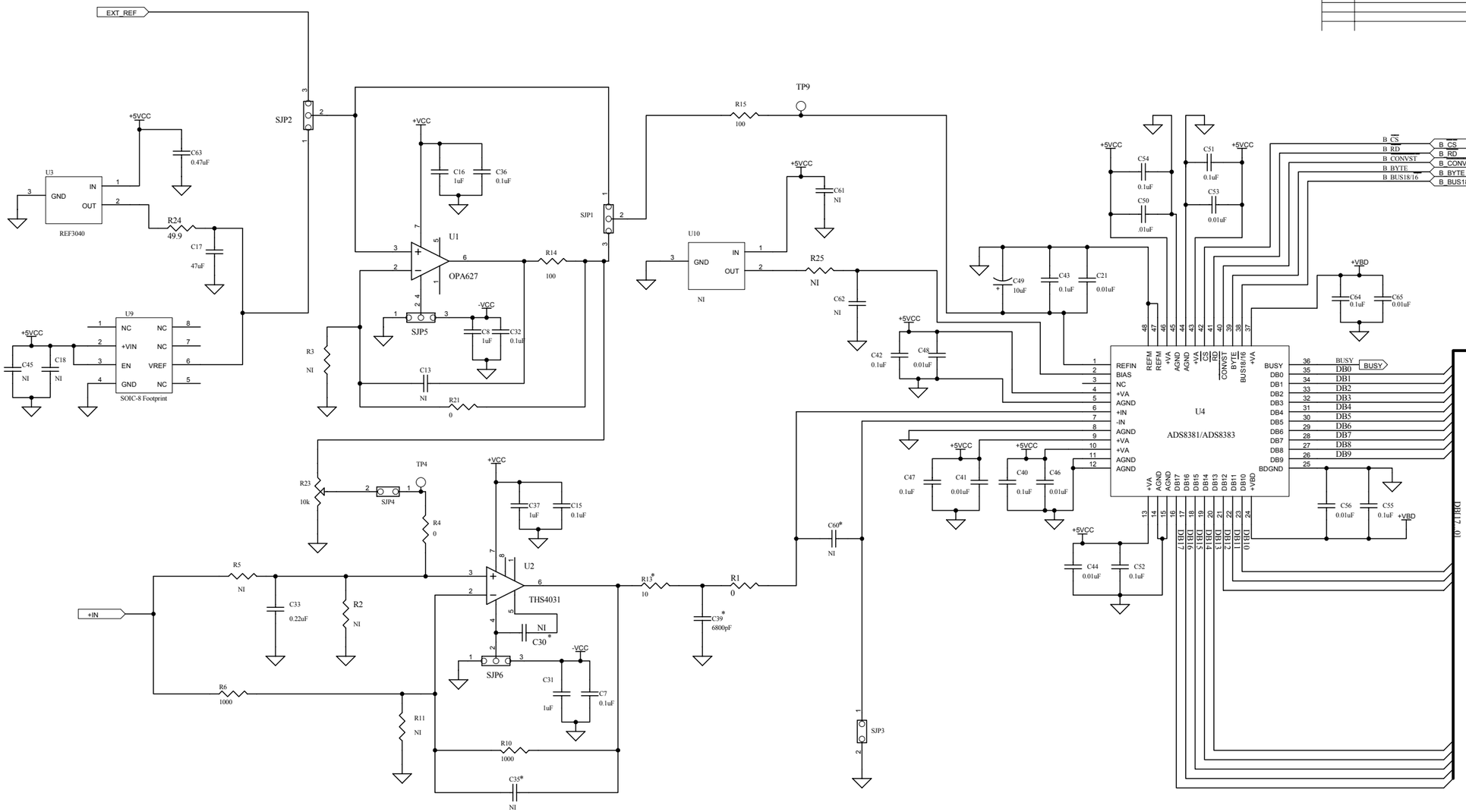




TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243


| | |
|---|---|
| TITLE: | ADS8381/ADS8383EVM Block Diagram |
| Engineer: | Lijoy Philipose |
| Drawn By: | Lijoy Philipose |
| FILE: | BlockDiagram.sch |
| DOCUMENT CONTROL #: | 6448017 |
| REV: | A |
| DATE: | 23-Sep-2004 |
| SIZE: | |
| SHEET: | 1 OF: 3 |

| Revision History | | |
|---|---|---|
| REV | ECN Number | Approved |
| | | |
| | | |
| | | |
| | | |



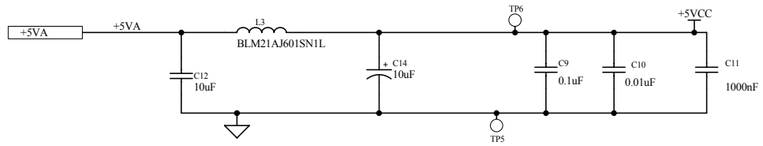

| | |
|---|---|
| Engineer: | Lijoy Philipose |
| Drawn By: | Lijoy Philipose |
| FILE: | Analog-to-Digital Converter |

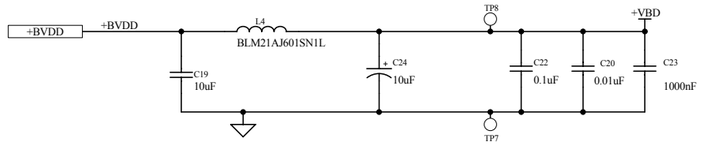
TEXAS INSTRUMENTS

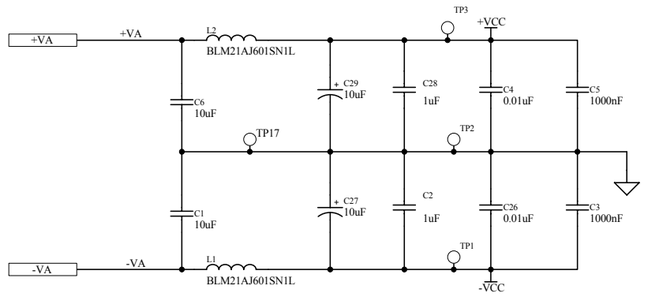
12500 TI Boulevard. Dallas, Texas 75243

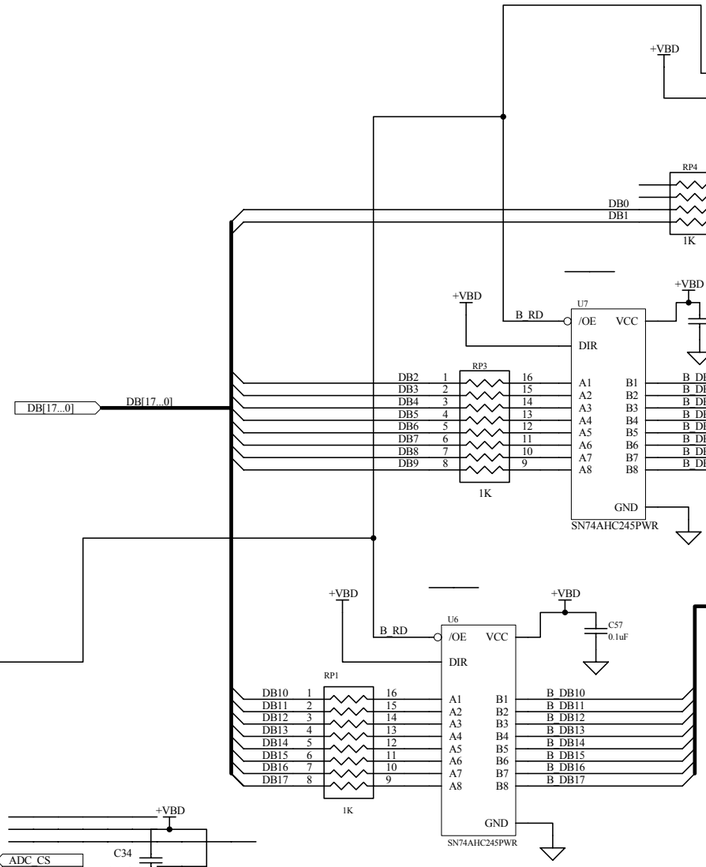
| | | | |
|---|---|---|---|
| TITLE: ADS8381/ADS8383EVM Analog Circuits | | | |
| DOCUMENT CONTROL #: 6448017 | | | REV: A |
| DATE: 23-Sep-2004 | SIZE: | SHEET: 2 | OF: 3 |

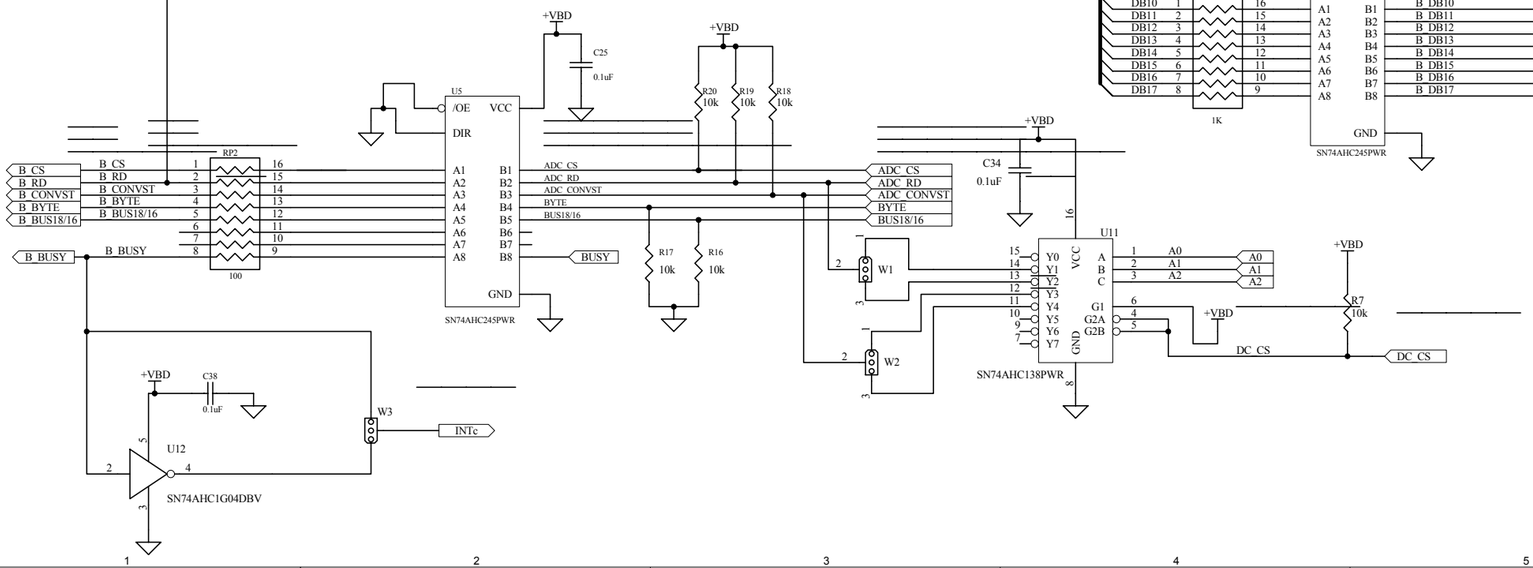
| Revision History | | |
|---|---|---|
| REV | ECN Number | Approved |
| | | |
| | | |
| | | |
| | | |




| | |
|---|---|
| Engineer: | Lijoy Philipose |
| Drawn By: | Lijoy Philipose |
| FILE: | Power & Digital Buffer |

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

| | | | |
|---|---|---|---|
| TITLE: Power Supply & Digital Buffer Circuits | | | |
| DOCUMENT CONTROL #: 6448017 | | | REV: A |
| DATE: 23-Sep-2004 | SIZE: B | SHEET: 3 | OF: 3 |