

## X4 SRAM Nonvolatile Controller Unit

### Features

- Power monitoring and switching for 3-volt battery-backup applications
- Write-protect control
- 2-input decoder for control of up to 4 banks of SRAM
- 3-volt primary cell inputs
- Less than 10ns chip-enable propagation delay
- 5% or 10% supply operation

### General Description

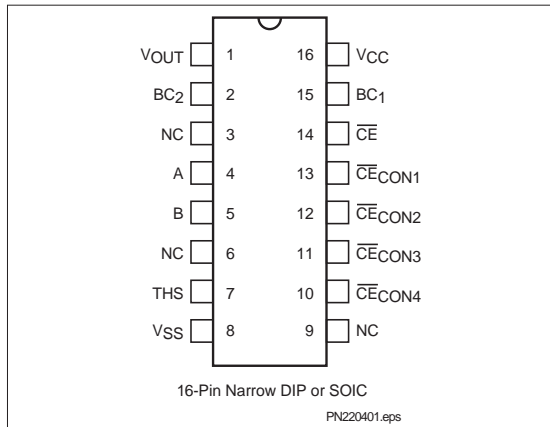
The CMOS bq2204A SRAM Nonvolatile Controller Unit provides all necessary functions for converting up to four banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V VCC input for an out-of-tolerance condition. When out-of-tolerance is detected, the four conditioned chip-enable outputs are forced inactive to write-protect up to four banks of SRAM.

During a power failure, the external SRAMs are switched from the VCC supply to one of two 3V backup supplies. On a subsequent power-up, the SRAMs are write-protected until a power-valid condition exists.

During power-valid operation, a two-input decoder transparently selects one of up to four banks of SRAM.

### Pin Connections



### Pin Names

VOUT	Supply output
BC <sub>1</sub> –BC <sub>2</sub>	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	chip-enable active low input
$\overline{CECON1}$ – $\overline{CECON4}$	Conditioned chip-enable outputs
A–B	Decoder inputs
NC	No connect
VCC	+5 volt supply input
VSS	Ground

### Functional Description

Up to four banks of CMOS static RAM can be battery-backed using the VOUT and conditioned chip-enable output pins from the bq2204A. As VCC slews down during a power failure, the conditioned chip-enable outputs  $\overline{CECON1}$  through  $\overline{CECON4}$  are forced inactive independent of the chip-enable input  $\overline{CE}$ .

This activity unconditionally write-protects the external SRAM as VCC falls below an out-of-tolerance threshold VPFD. VPFD is selected by the threshold select input pin, THS. If THS is tied to VSS, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to VCC, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to VSS or VCC for proper operation.

If a memory access is in process to any of the four external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time  $t_{WPT}$ , all four chip-enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

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As the supply continues to fall past  $V_{PFD}$ , an internal switching device forces  $V_{OUT}$  to one of the two external backup energy sources.  $\overline{CECON1}$  through  $\overline{CECON4}$  are held high by the  $V_{OUT}$  energy source.

During power-up,  $V_{OUT}$  is switched back to the 5V supply as  $V_{CC}$  rises above the backup cell input voltage sourcing  $V_{OUT}$ . Outputs  $\overline{CECON1}$  through  $\overline{CECON4}$  are held inactive for time  $t_{CER}$  (120ms maximum) after the power supply has reached  $V_{PFD}$ , independent of the  $\overline{CE}$  input, to allow for processor stabilization.

During power-valid operation, the  $\overline{CE}$  input is passed through to one of the four  $\overline{CECON}$  outputs with a propagation delay of less than 10ns. The  $\overline{CE}$  input is output on one of the four  $\overline{CECON}$  output pins depending on the level of the decode inputs at A and B as shown in the Truth Table.

The A and B inputs are usually tied to high-order address pins so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

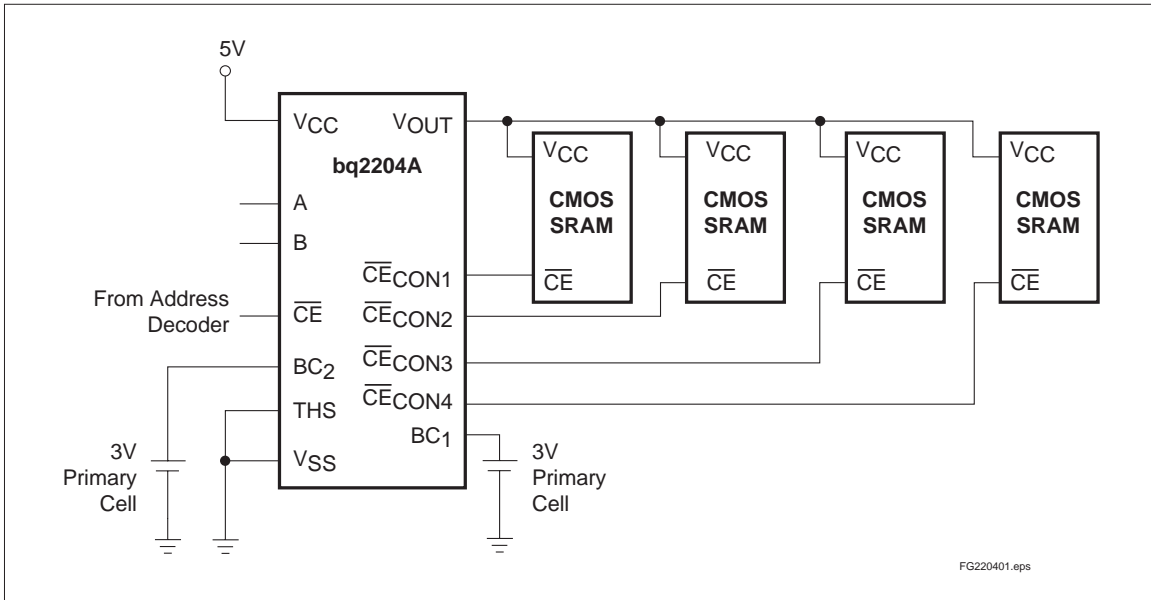


Figure 1. Hardware Hookup (5% Supply Operation)

FG220401.eps

## Energy Cell Inputs—BC<sub>1</sub>, BC<sub>2</sub>

Two backup energy source inputs are provided on the bq2204A. The BC<sub>1</sub> and BC<sub>2</sub> inputs accept a 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If no primary cell is to be used on either BC<sub>1</sub> or BC<sub>2</sub>, the unused input should be tied to V<sub>SS</sub>.

V<sub>CC</sub> falling below V<sub>VPFD</sub> starts the comparison of BC<sub>1</sub> and BC<sub>2</sub>. The BC input comparison continues until V<sub>CC</sub> rises above V<sub>VS0</sub>. Power to V<sub>OUT</sub> begins with BC<sub>1</sub> and switches to BC<sub>2</sub> only when V<sub>BC1</sub> is less than V<sub>BC2</sub> minus V<sub>B<sub>SO</sub></sub>. The controller alternates to the higher BC voltage only when the difference between the BC input voltages is greater than V<sub>B<sub>SO</sub></sub>. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V<sub>OUT</sub> and  $\overline{\text{CE}}_{\text{CON1-4}}$  are internally isolated from BC<sub>1</sub> and BC<sub>2</sub> by either of the following conditions:

- Initial connection of a battery to BC<sub>1</sub> or BC<sub>2</sub>, or
- Presentation of an isolation signal on  $\overline{\text{CE}}$ .

A valid isolation signal requires  $\overline{\text{CE}}$  low as V<sub>CC</sub> crosses both V<sub>VPFD</sub> and V<sub>VS0</sub> during a power-down. See Figure 2. Between these two points in time,  $\overline{\text{CE}}$  must be brought to the point of (0.48 to 0.52)\*V<sub>CC</sub> and held for at least 700ns. The isolation signal is invalid if  $\overline{\text{CE}}$  exceeds 0.54\*V<sub>CC</sub> at any point between V<sub>CC</sub> crossing V<sub>VPFD</sub> and V<sub>VS0</sub>.

The appropriate battery is connected to V<sub>OUT</sub> and  $\overline{\text{CE}}_{\text{CON1-4}}$  immediately on subsequent application and removal of V<sub>CC</sub>.

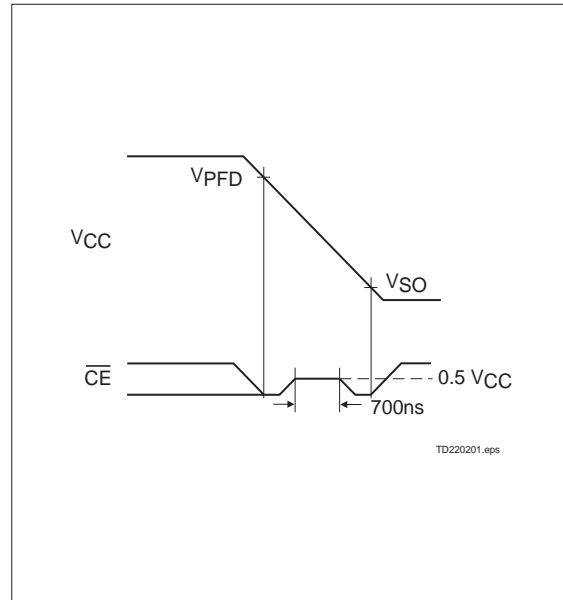


Figure 2. Battery Isolation Signal

## Truth Table

Input			Output			
$\overline{\text{CE}}$	A	B	$\overline{\text{CE}}_{\text{CON1}}$	$\overline{\text{CE}}_{\text{CON2}}$	$\overline{\text{CE}}_{\text{CON3}}$	$\overline{\text{CE}}_{\text{CON4}}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

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## Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
VCC	DC voltage applied on VCC relative to VSS	-0.3 to +7.0	V	
VT	DC voltage applied on any pin excluding VCC relative to VSS	-0.3 to +7.0	V	$V_T \leq V_{CC} + 0.3$
TOPR	Operating temperature	0 to 70	°C	Commercial
		-40 to +85	°C	Industrial "N"
TSTG	Storage temperature	-55 to +125	°C	
TBIAS	Temperature under bias	-40 to +85	°C	
TSOLDER	Soldering temperature	260	°C	For 10 seconds
IOUT	VOUT current	200	mA	

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
VCC	Supply voltage	4.75	5.0	5.5	V	THS = VSS
		4.50	5.0	5.5	V	THS = VCC
VSS	Supply voltage	0	0	0	V	
VIL	Input low voltage	-0.3	-	0.8	V	
VIH	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	
VBC1, VBC2	Backup cell voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
THS	Threshold select	-0.3	-	$V_{CC} + 0.3$	V	

**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  or  $V_{BC}$ .

**DC Electrical Characteristics** ( $T_A = T_{OPR}$ ,  $V_{CC} = 5V \pm 10\%$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
ILI	Input leakage current	-	-	$\pm 1$	$\mu A$	$V_{IN} = V_{SS}$ to $V_{CC}$
VOH	Output high voltage	2.4	-	-	V	$I_{OH} = -2.0mA$
VOHB	VOH, BC supply	$V_{BC} - 0.3$	-	-	V	$V_{BC} > V_{CC}$ , $I_{OH} = -10\mu A$
VOL	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0mA$
ICC	Operating supply current	-	3	6	mA	No load on outputs.
V <sub>PF</sub> D	Power-fail detect voltage	4.55	4.62	4.75	V	THS = $V_{SS}$
		4.30	4.37	4.50	V	THS = $V_{CC}$
V <sub>SO</sub>	Supply switch-over voltage	-	$V_{BC}$	-	V	
ICCDR	Data-retention mode current	-	-	100	nA	$V_{OUT}$ data-retention current to additional memory not included.
V <sub>BC</sub>	Active backup cell voltage	-	$V_{BC1}$	-	V	$V_{BC1} > V_{BC2} + V_{BSO}$
		-	$V_{BC2}$	-	V	$V_{BC2} > V_{BC1} + V_{BSO}$
V <sub>BSO</sub>	Battery switch-over voltage	0.25	0.4	0.6	V	
I <sub>OUT1</sub>	$V_{OUT}$ current	-	-	160	mA	$V_{OUT} > V_{CC} - 0.3V$
I <sub>OUT2</sub>	$V_{OUT}$ current	-	100	-	$\mu A$	$V_{OUT} > V_{BC} - 0.2V$

**Note:** Typical values indicate operation at  $T_A = 25^\circ C$ ,  $V_{CC} = 5V$  or  $V_{BC}$ .

**Capacitance** ( $T_A = 25^\circ C$ ,  $F = 1MHz$ ,  $V_{CC} = 5.0V$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C <sub>IN</sub>	Input capacitance	-	-	8	pF	Input voltage = 0V
C <sub>OUT</sub>	Output capacitance	-	-	10	pF	Output voltage = 0V

**Note:** This parameter is sampled and not 100% tested.

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## AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)

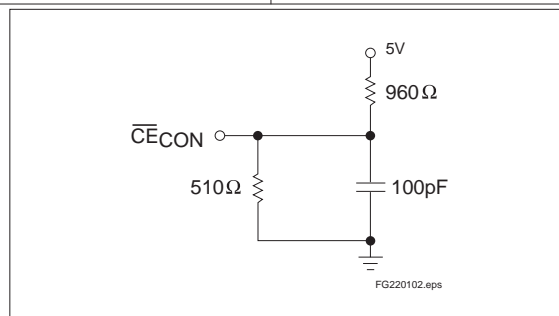


Figure 3. Output Load

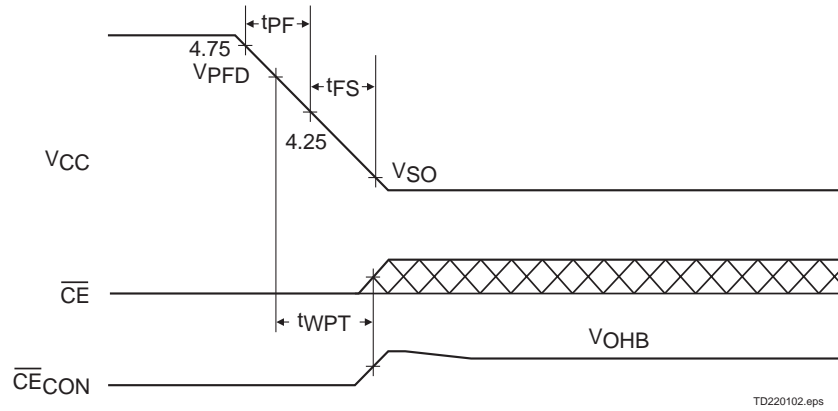
## Power-Fail Control ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
tPF	V <sub>CC</sub> slew, 4.75V to 4.25V	300	-	-	μs	
tFS	V <sub>CC</sub> slew, 4.25V to V <sub>SO</sub>	10	-	-	μs	
tPU	V <sub>CC</sub> slew, 4.25V to 4.75V	0	-	-	μs	
tCED	chip-enable propagation delay	-	7	10	ns	
tAS	A,B set up to $\overline{CE}$	0	-	-	ns	
tCER	chip-enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V <sub>CC</sub> passes V <sub>PF<math>\overline{D}</math></sub> on power-up.
tWPT	Write-protect time	40	100	150	μs	Delay after V <sub>CC</sub> slews down past V <sub>PF<math>\overline{D}</math></sub> before SRAM is write-protected.

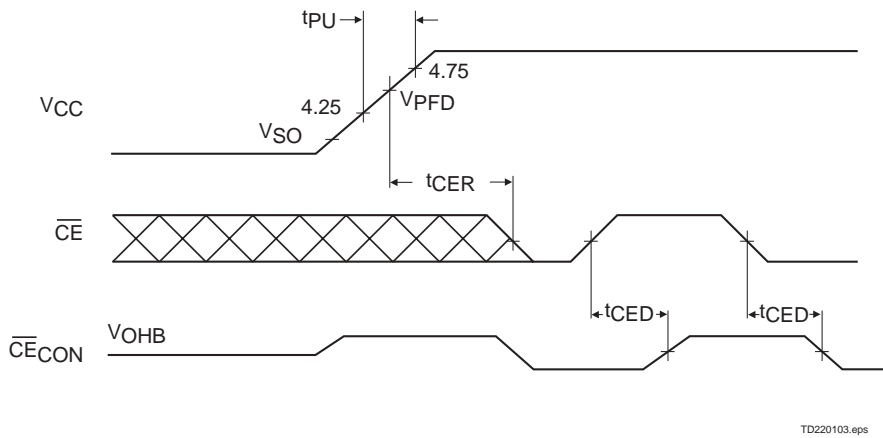
**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

**Caution:** Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

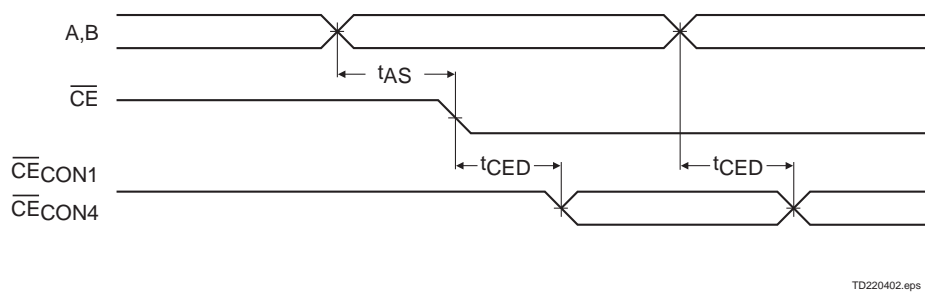
**Power-Down Timing**



**Power-Up Timing**



**Address-Decode Timing**



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## Data Sheet Revision History

Change No.	Page No.	Description of Change	Nature of Change
1	All	bq2204A replaces bq2204.	
1	1, 4-5	10% tolerance requires the THS pin to be tied to VCC, not VOUT.	
1	3	Energy cell input selection process alternates between BC1 and BC2.	

**Note:** Change 1 = Dec. 1992 changes from Sept. 1991

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">BQ2204APN</a>	Last Time Buy	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	2204APN
BQ2204APN.B	Last Time Buy	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	2204APN
<a href="#">BQ2204ASN</a>	Last Time Buy	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2204A
<a href="#">BQ2204ASN-N</a>	Last Time Buy	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2204A
BQ2204ASN-N.B	Last Time Buy	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2204A
BQ2204ASN.B	Last Time Buy	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2204A
<a href="#">BQ2204ASNTR</a>	Last Time Buy	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2204A
BQ2204ASNTR.B	Last Time Buy	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2204A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2204ASNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2204ASNTR	SOIC	D	16	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ2204APN	N	PDIP	16	25	506	13.97	11230	4.32
BQ2204APN.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2204ASN	D	SOIC	16	40	506.6	8	3940	4.32
BQ2204ASN-N	D	SOIC	16	40	506.6	8	3940	4.32
BQ2204ASN-N.B	D	SOIC	16	40	506.6	8	3940	4.32
BQ2204ASN.B	D	SOIC	16	40	506.6	8	3940	4.32

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