

## CMOS 8-Input NOR/OR Gate

High-Voltage Types (20-Volt Rating)

■ CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

|                                                                       |                                                    |
|-----------------------------------------------------------------------|----------------------------------------------------|
| Voltages referenced to $V_{SS}$ Terminal)                             | –0.5V to +20V                                      |
| INPUT VOLTAGE RANGE, ALL INPUTS                                       | –0.5V to $V_{DD}$ +0.5V                            |
| DC INPUT CURRENT, ANY ONE INPUT                                       | ±10mA                                              |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                              |                                                    |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                 | 500mW                                              |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                              |                                                    |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ | 100mW                                              |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )                                 | –55 $^\circ\text{C}$ to $+125^\circ\text{C}$       |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                               | –65 $^\circ\text{C}$ to $+150^\circ\text{C}$       |
| LEAD TEMPERATURE (DURING SOLDERING):                                  |                                                    |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max    | +265 $^\circ\text{C}$                              |

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                        | Min. | Max. | Units |
|-----------------------------------------------------------------------|------|------|-------|
| Supply-Voltage Range<br>(For $T_A$ Full Package<br>Temperature Range) | 3    | 18   | V     |

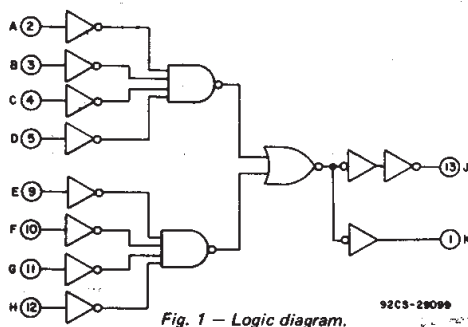


Fig. 1 – Logic diagram.

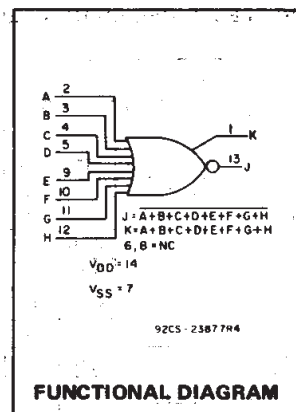
### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC                                | TEST CONDITIONS | LIMITS            |      | UNITS |
|-----------------------------------------------|-----------------|-------------------|------|-------|
|                                               |                 | $V_{DD}$<br>VOLTS | TYP. | MAX.  |
| Propagation Delay Time,<br>$t_{PHL}, t_{PLH}$ |                 | 5                 | 150  | 300   |
|                                               |                 | 10                | 75   | 150   |
|                                               |                 | 15                | 55   | 110   |
| Transition Time,<br>$t_{THL}, t_{TLH}$        |                 | 5                 | 100  | 200   |
|                                               |                 | 10                | 50   | 100   |
|                                               |                 | 15                | 40   | 80    |
| Input Capacitance, $C_{IN}$                   | Any Input       |                   | 5    | 7.5   |
|                                               |                 |                   |      | pF    |

### Features:

- Medium-Speed Operation:  
 $t_{PHL}, t_{PLH} = 75\text{ ns}$  (typ.) at  $V_{DD} = 10\text{ V}$
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1\text{ }\mu\text{A}$  at 18 V over full package-temperature range:  
100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package-temperature range):  
1 V at  $V_{DD} = 5\text{ V}$   
2 V at  $V_{DD} = 10\text{ V}$  2.5 V at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

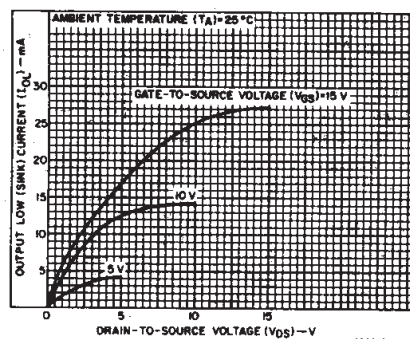


Fig. 2 – Typical output low (sink) current characteristics.

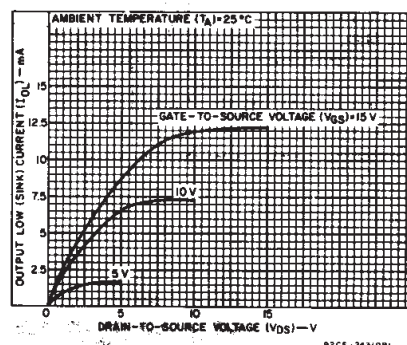


Fig. 3 – Minimum output low (sink) current characteristics.

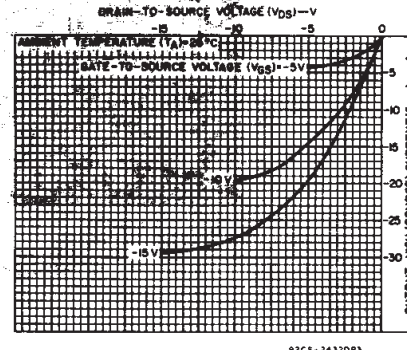


Fig. 4 – Typical output high (source) current characteristics.

# CD4078B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) |                                       |       |       |       | +25   |                   |      |       |
|                                                             |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current,<br>I <sub>DD</sub> Max.        | —                     | 0.5                    | 5                      | 0.25                                  | 0.25  | 7.5   | 7.5   | —     | 0.01              | 0.25 | μA    |
|                                                             | —                     | 0.10                   | 10                     | 0.5                                   | 0.5   | 15    | 15    | —     | 0.01              | 0.5  |       |
|                                                             | —                     | 0.15                   | 15                     | 1                                     | 1     | 30    | 30    | —     | 0.01              | 1    |       |
|                                                             | —                     | 0.20                   | 20                     | 5                                     | 5     | 150   | 150   | —     | 0.02              | 5    |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0.5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 |      | mA    |
|                                                             | 0.5                   | 0.10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               |      |       |
|                                                             | 1.5                   | 0.15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               |      |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0.5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                |      | mA    |
|                                                             | 2.5                   | 0.5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              |      |       |
|                                                             | 9.5                   | 0.10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              |      |       |
|                                                             | 13.5                  | 0.15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              |      |       |
| Output Voltage:<br>Low Level,<br>V <sub>OL</sub> Max.       | —                     | 0.5                    | 5                      | 0.05                                  |       |       |       |       | 0                 | 0.05 | V     |
|                                                             | —                     | 0.10                   | 10                     | 0.05                                  |       |       |       |       | 0                 | 0.05 |       |
|                                                             | —                     | 0.15                   | 15                     | 0.05                                  |       |       |       |       | 0                 | 0.05 |       |
| Output Voltage:<br>High Level,<br>V <sub>OH</sub> Min.      | —                     | 0.5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 |      | V     |
|                                                             | —                     | 0.10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                |      |       |
|                                                             | —                     | 0.15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                |      |       |
| Input Low<br>Voltage,<br>V <sub>IL</sub> Max.               | 0.5,4.5               | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1.9                   | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 0.5,4.5               | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1.9                   | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       |                       | 0.18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

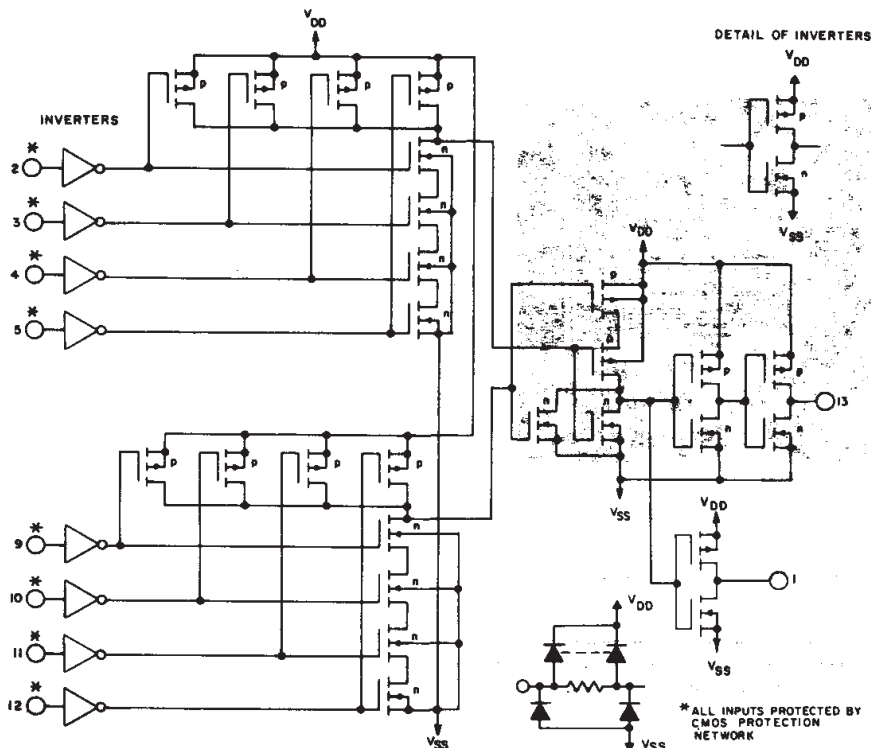


Fig. 8 — Schematic diagram.

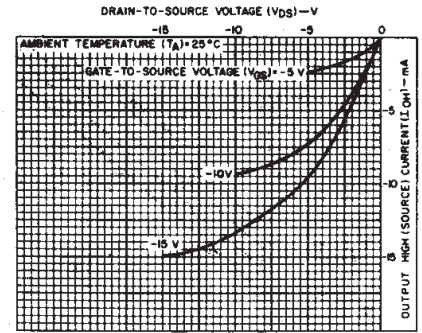


Fig. 5 — Minimum output high (source) current characteristics.

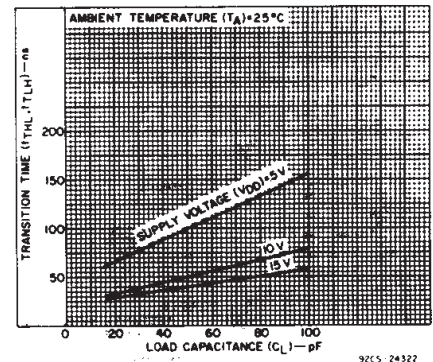


Fig. 6 — Typical transition time as a function of load capacitance.

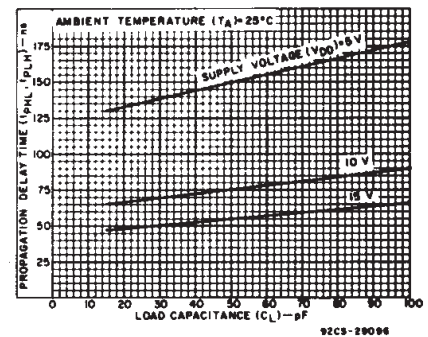


Fig. 7 — Typical propagation delay time as a function of load capacitance.

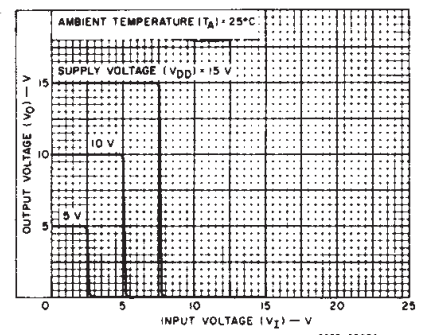


Fig. 9 — Typical voltage transfer characteristics (NOR output).

## CD4078B Types

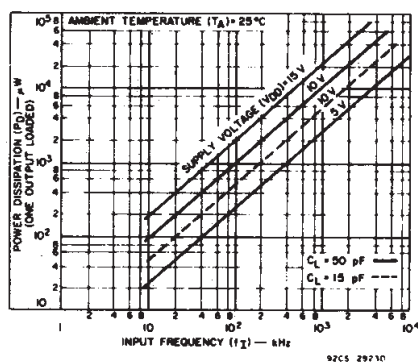


Fig. 10 - Typical dynamic power dissipation as a function of frequency.

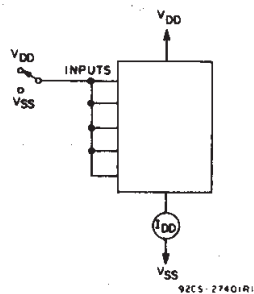


Fig. 11 - Quiescent-device-current test circuit.

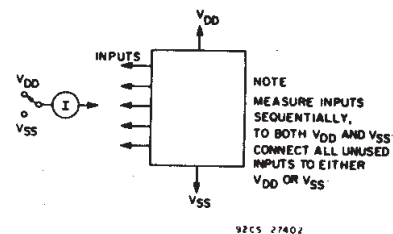


Fig. 12 - Input current test circuit.

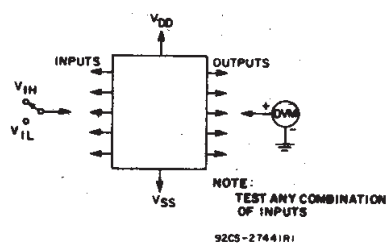


Fig. 13 - Input-voltage test circuit.

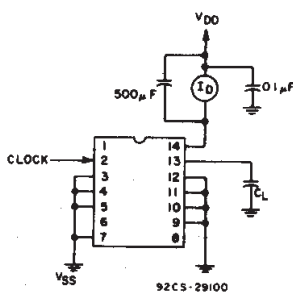
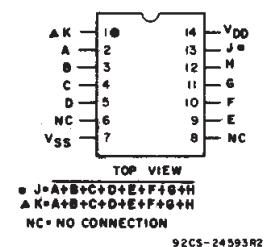
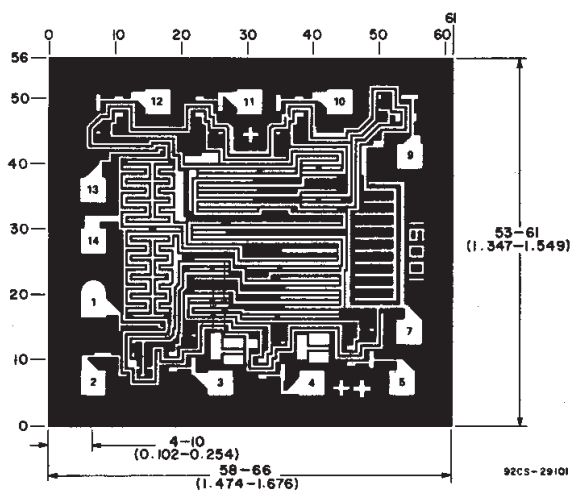


Fig. 14 - Dynamic power dissipation test circuit.



## TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)     |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------|
| <a href="#">7704402CA</a>  | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7704402CA<br>CD4078BF3A |
| <a href="#">CD4078BE</a>   | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4078BE                |
| CD4078BE.A                 | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4078BE                |
| <a href="#">CD4078BF</a>   | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4078BF                |
| CD4078BF.A                 | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4078BF                |
| <a href="#">CD4078BF3A</a> | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7704402CA<br>CD4078BF3A |
| CD4078BF3A.A               | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7704402CA<br>CD4078BF3A |
| <a href="#">CD4078BM</a>   | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CD4078BM                |
| <a href="#">CD4078BM96</a> | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4078BM                |
| CD4078BM96.A               | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4078BM                |
| <a href="#">CD4078BMT</a>  | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CD4078BM                |
| <a href="#">CD4078BNSR</a> | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4078B                 |
| CD4078BNSR.A               | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4078B                 |
| <a href="#">CD4078BPW</a>  | Obsolete      | Production           | TSSOP (PW)   14 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CM078B                  |
| <a href="#">CD4078BPWR</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM078B                  |
| CD4078BPWR.A               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM078B                  |
| CD4078BPWRE4               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM078B                  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD4078B, CD4078B-MIL :**

- Catalog : [CD4078B](#)
- Military : [CD4078B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

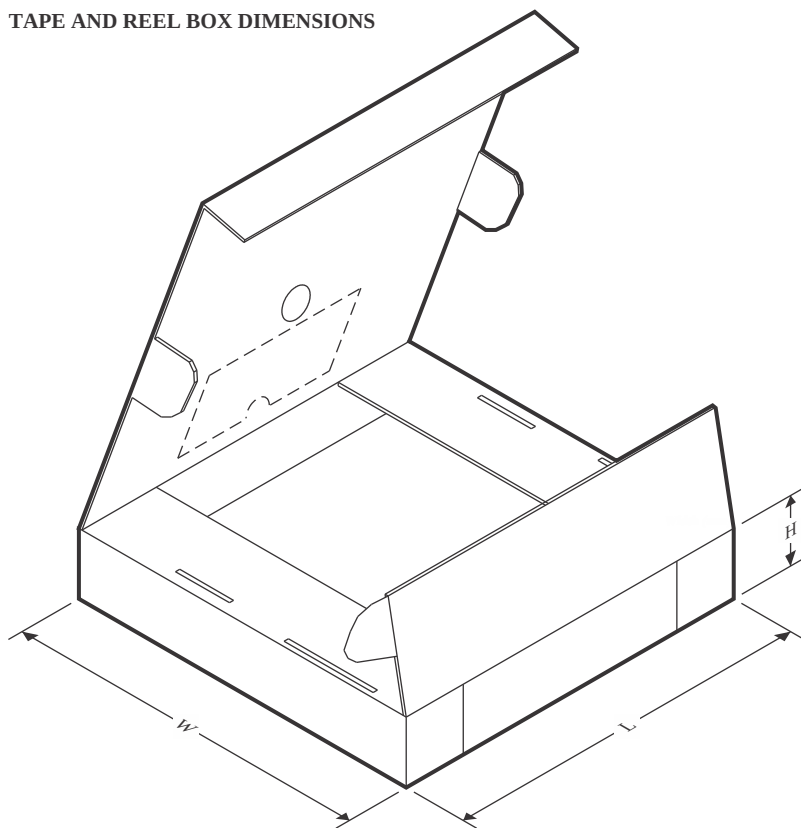
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

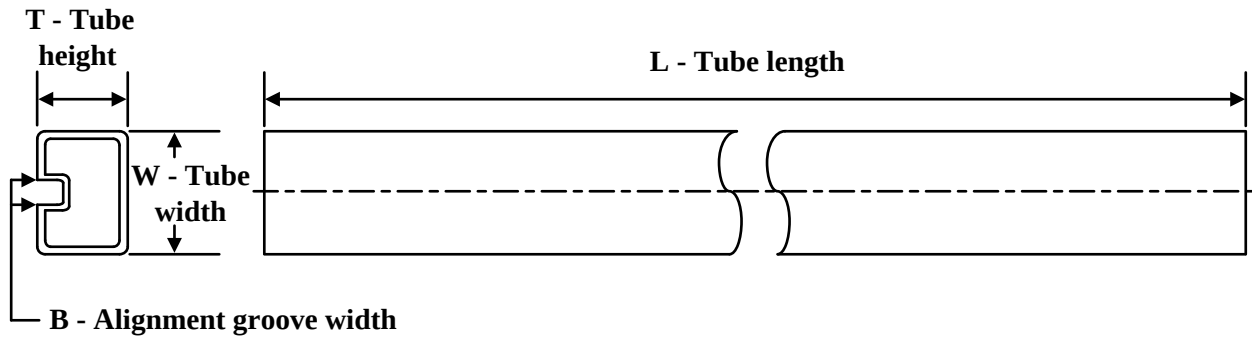
| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4078BM96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD4078BNSR | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4078BPWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

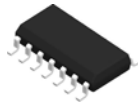
| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4078BM96 | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| CD4078BNSR | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| CD4078BPWR | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


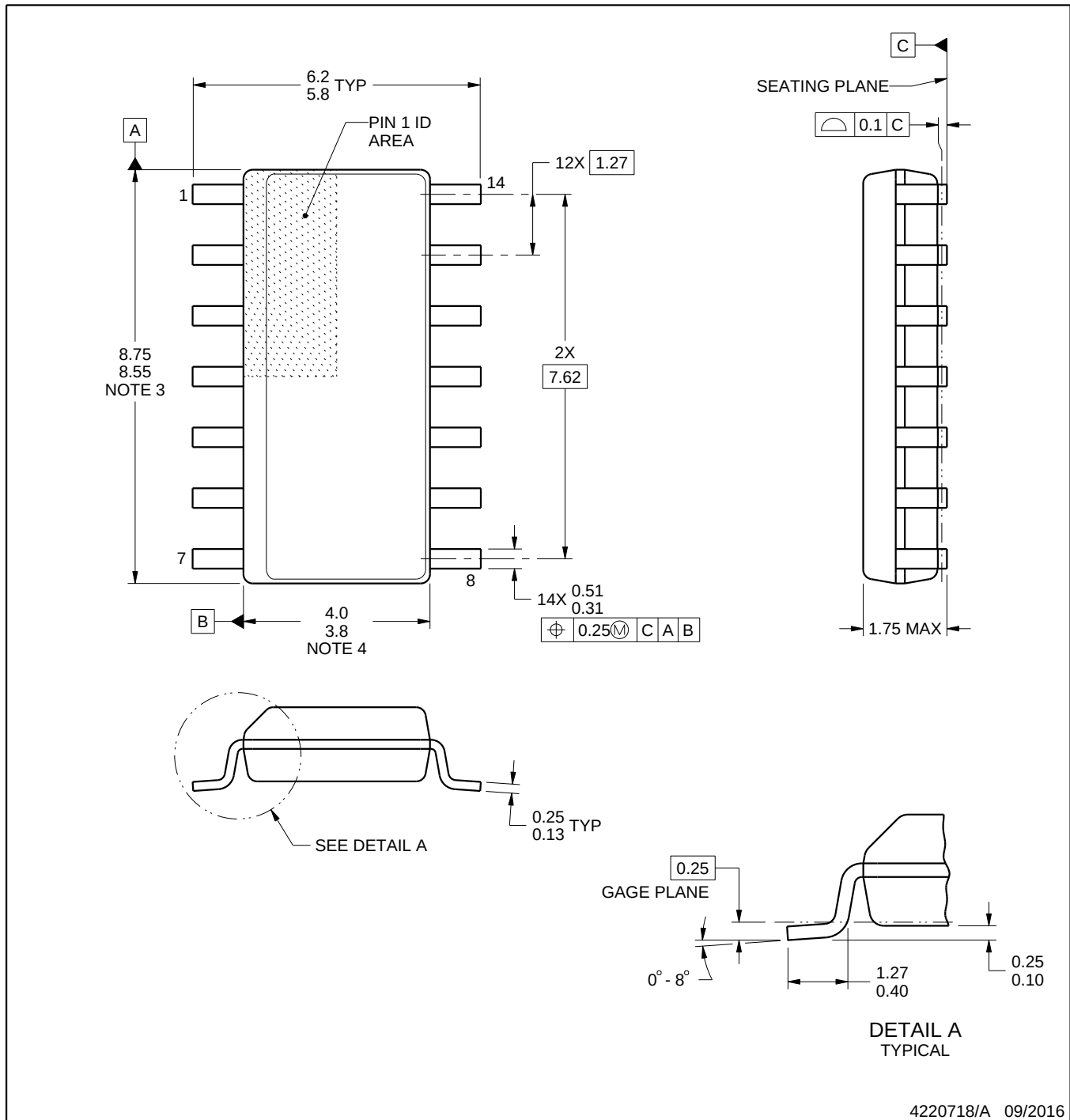
\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4078BE   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4078BE   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4078BE.A | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4078BE.A | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |



**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

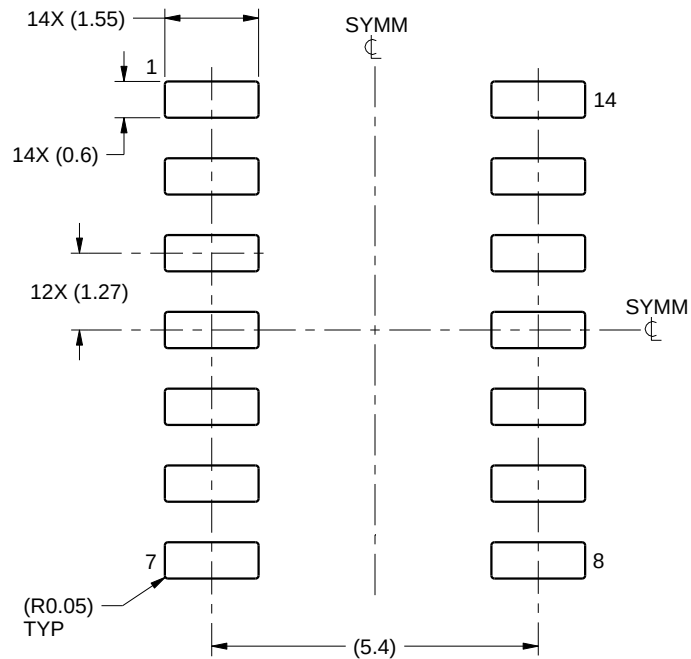
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

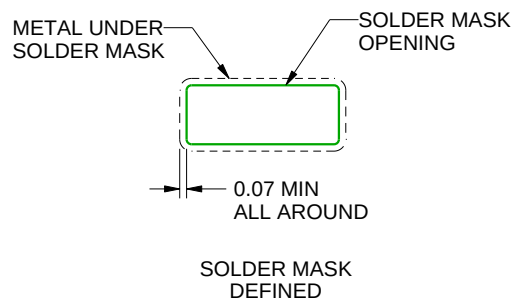
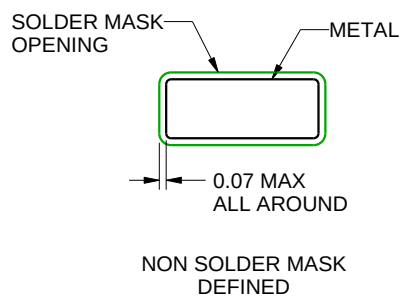
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

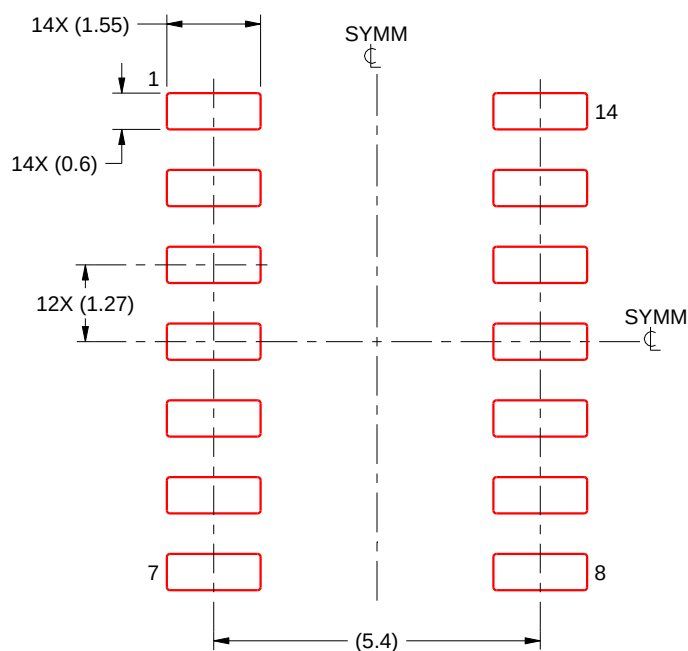
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

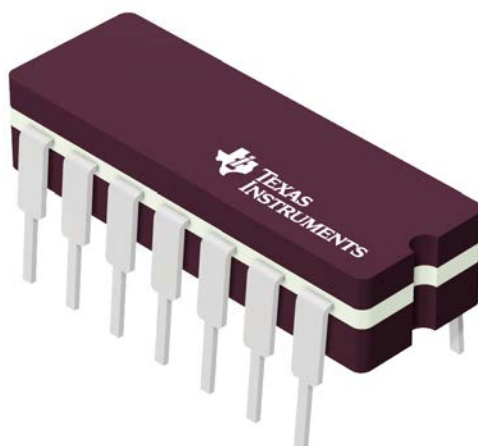
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

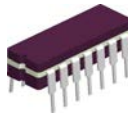
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

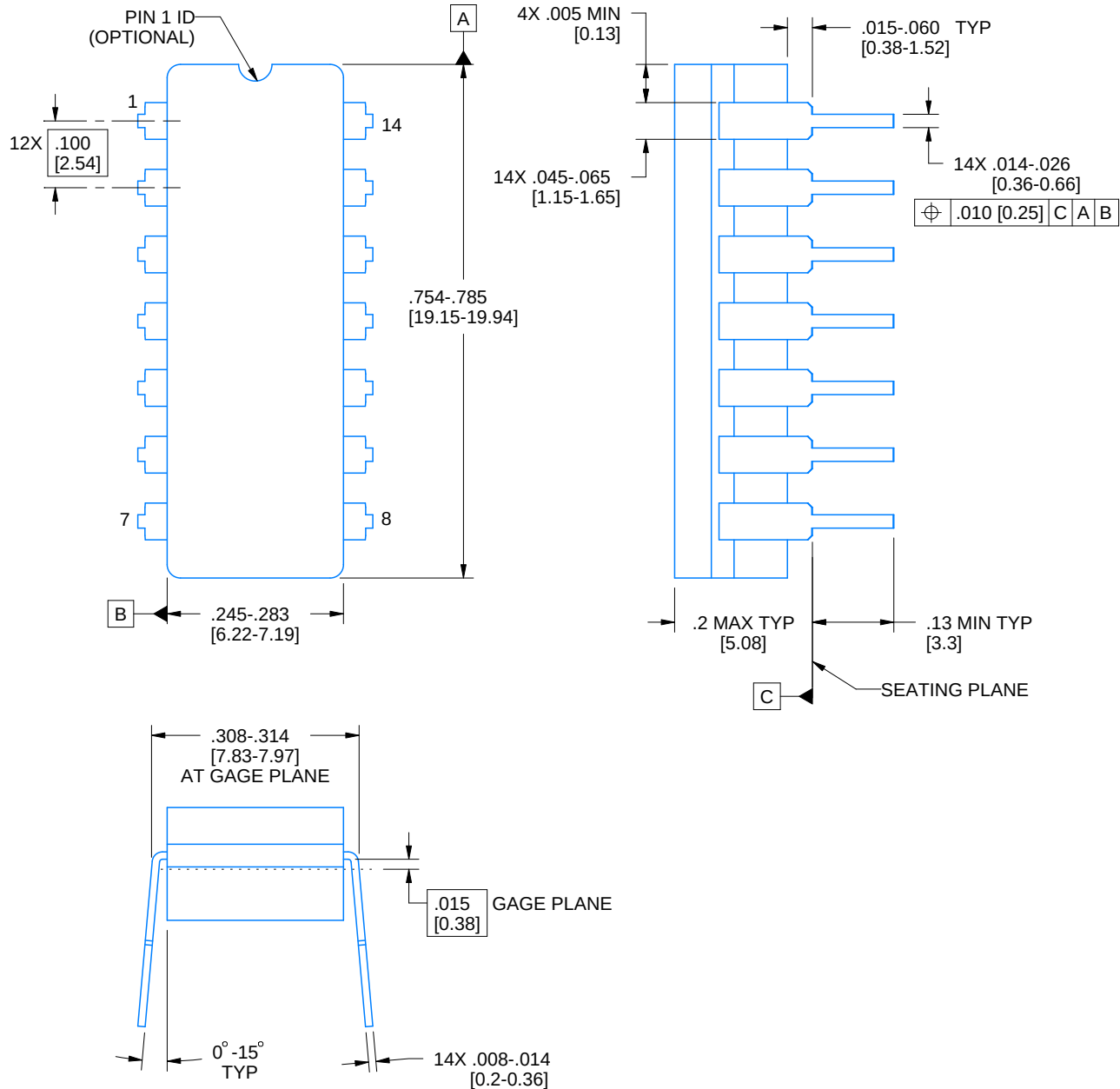
J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

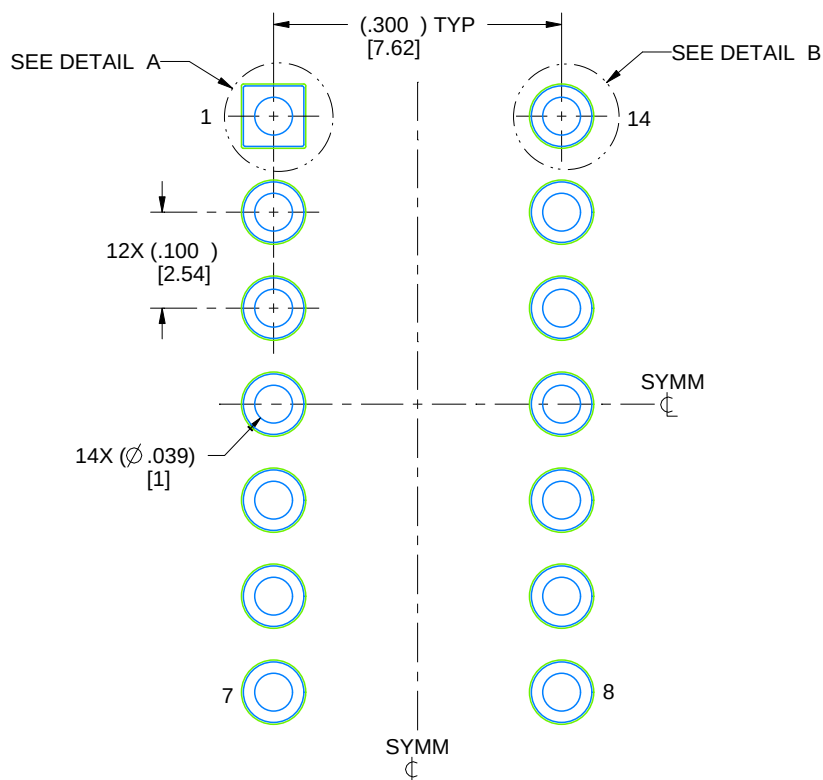
### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

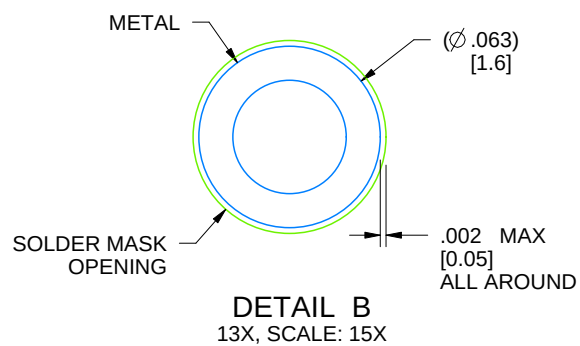
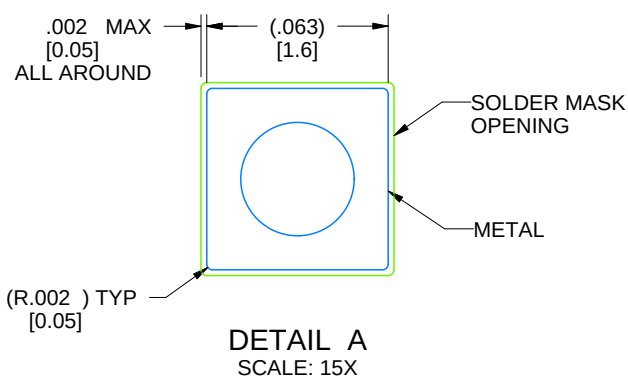
**J0014A**

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

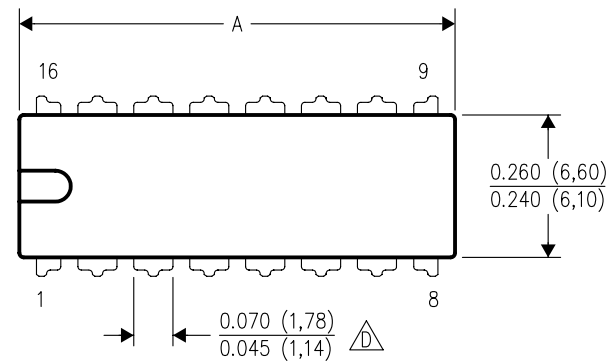


4214771/A 05/2017

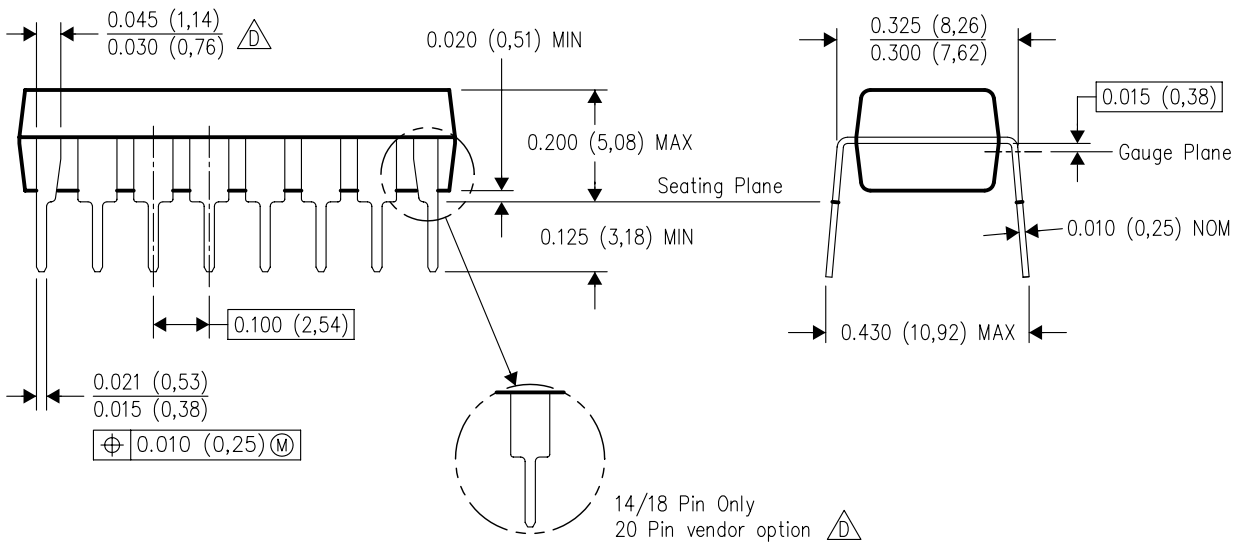
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



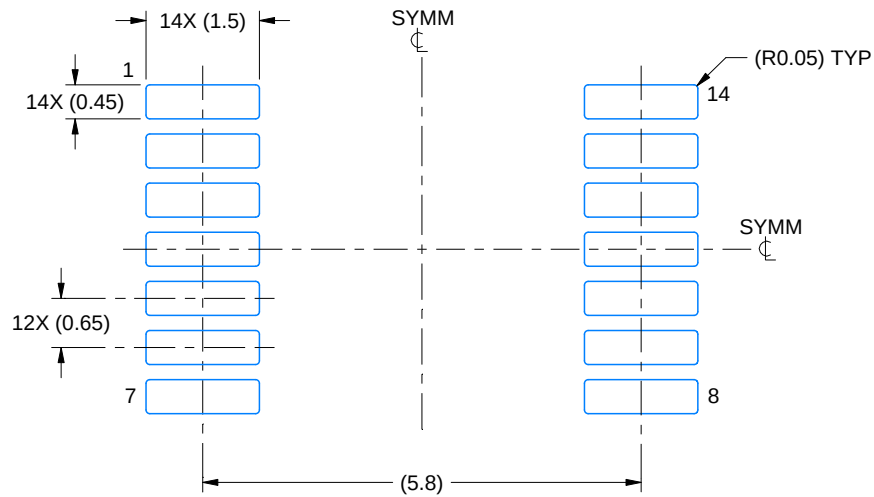


# EXAMPLE BOARD LAYOUT

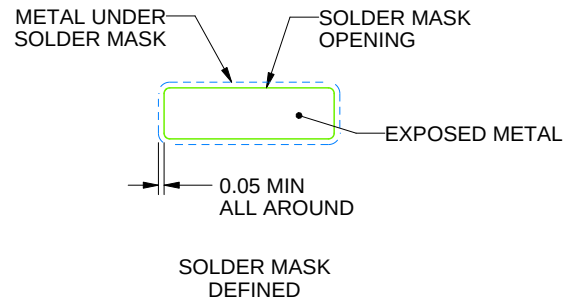
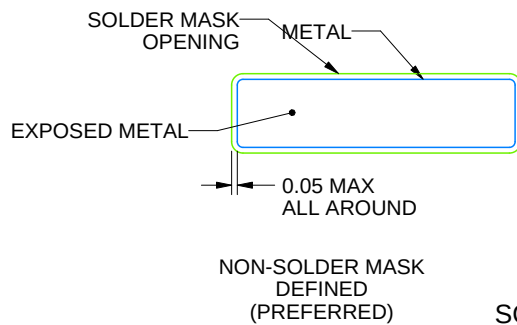
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

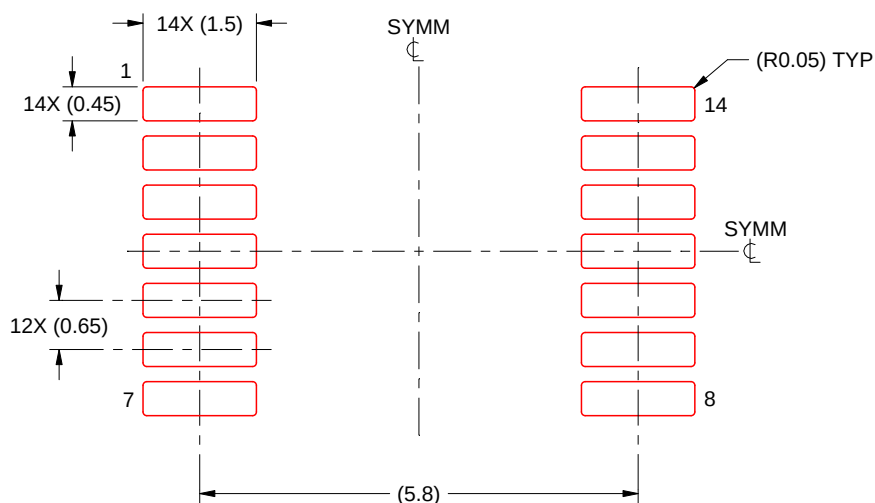
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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