LM3224 615kHz/1.25MHz Step-up PWM DC/DC Converter

Check for Samples: LM3224

FEATURES

- **Operating Voltage Range of 2.7V to 7V**
- **615kHz/1.25MHz Pin Selectable Frequency Operation**
- **Over Temperature Protection**
- **Optional Soft-Start Function**
- **8-Lead VSSOP Package**

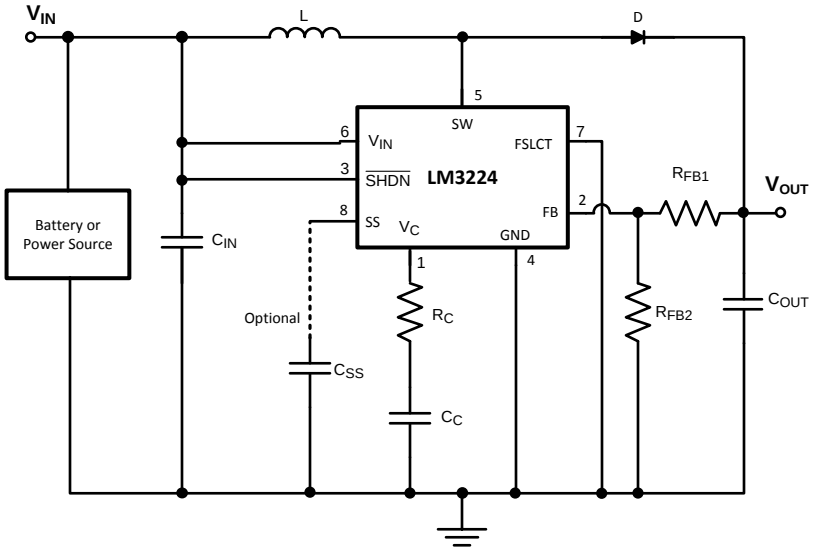
APPLICATIONS

- **TFT Bias Supplies**
- **Handheld Devices**
- **Portable Applications**
- **GSM/CDMA Phones**
- **Digital Cameras**
- **White LED Flash/Torch Applications**

DESCRIPTION

The LM3224 is a step-up DC/DC converter with a 0.15Ω (typ.), 2.45A (typ.) internal switch and pin selectable operating frequency. With the ability to convert 3.3V to multiple outputs of 8V, -8V, and 23V, the LM3224 is an ideal part for biasing TFT displays. With the high current switch it is also ideal for driving high current white LEDs for flash applications. The LM3224 can be operated at switching frequencies of 615kHz and 1.25MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. An external soft-start pin allows the user to control the amount of inrush current during start up. The LM3224 is available in a low profile 8-lead VSSOP package.

Typical Application Circuit



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Connection Diagram

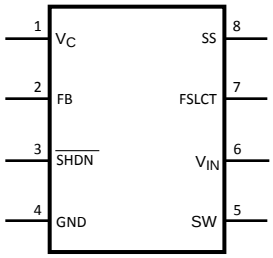

Figure 1. 8-Lead Plastic VSSOP
Top View
Package Number DGK0008A

PIN DESCRIPTIONS

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low. This pin has an internal pulldown resistor so the default condition is off. The pin must be pulled high to turn on the device.
4	GND	Analog and power ground.
5	SW	Power switch input. Switch connected between SW pin and GND pin.
6	V_{IN}	Analog power input.
7	FSLCT	Switching frequency select input. V_{IN} = 1.25MHz. Ground = 615kHz.
8	SS	Soft-start Pin.

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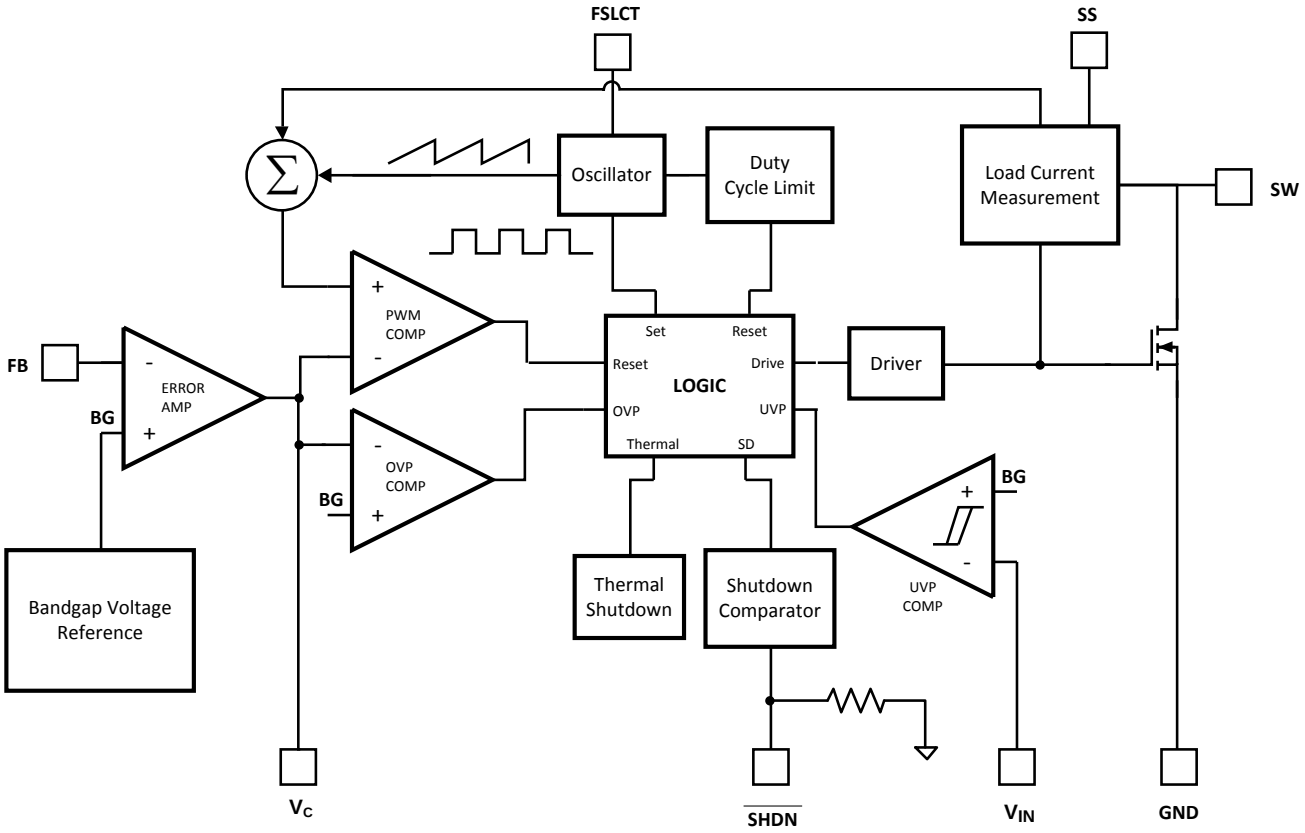
Block Diagram



General Description

The LM3224 utilizes a PWM control scheme to regulate the output voltage over all load conditions. The operation can best be understood referring to the block diagram and Figure 21 of the *Operation* section. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor, cycle 1 of Figure 21 (a). During this cycle, the voltage at the V_C pin controls the peak inductor current. The V_C voltage will increase with larger loads and decrease with smaller. This voltage is compared with the summation of the SW voltage and the ramp compensation. The ramp compensation is used in PWM architectures to eliminate the sub-harmonic oscillations that occur during duty cycles greater than 50%. Once the summation of the ramp compensation and switch voltage equals the V_C voltage, the PWM comparator resets the driver logic turning off the NMOS power device. The inductor current then flows through the schottky diode to the load and output capacitor, cycle 2 of Figure 21 (b). The NMOS power device is then set by the oscillator at the end of the period and current flows through the NMOS power device once again.

The LM3224 has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the NMOS power device when the die temperature reaches excessive levels. The UVP comparator protects the NMOS power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM3224 also features a shutdown mode decreasing the supply current to 0.1µA (typ.).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1) (2)(2)

V_{IN}		7.5V
SW Voltage		21V
FB Voltage (3)		7V
V_C Voltage (4)		1.26V ± 0.3V
$\overline{SHDN}$ Voltage		7.5V
FSLCT		7.5V
Maximum Junction Temperature		150°C
Power Dissipation(5)		Internally Limited
Lead Temperature		300°C
Vapor Phase (60 sec.)		215°C
Infrared (15 sec.)		220°C
ESD Susceptibility (6)	Human Body Model	2kV
	Machine Model	200V

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications

(2) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics().

(3) The FB pin should never exceed V_{IN}.

(4) Under normal operation the V_C pin may go to voltages above this value. This maximum rating is for the possibility of a voltage being applied to the pin, however the V_C pin should never have a voltage directly applied to it.

(5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

(6) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Conditions

Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Supply Voltage	2.7V to 7V
Maximum Output Voltage	20V

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Electrical Characteristics(1)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). V_{IN} = 2.7V, FSLCT = $\overline{SHDN}$ = V_{IN}, and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_Q	Quiescent Current	FB = 2V (Not Switching)		1.3	**2.0**	mA
		V_{SHDN} = 0V		0.1	**2.0**	µA
V_{FB}	Feedback Voltage		**1.2285**	1.26	**1.2915**	V
I_{CL} (3)	Switch Current Limit	V_{IN} = 2.7V (4)	1.9	2.45	2.8	A
		V_{IN} = 3V, V_{OUT} = 8V		2.1		
		V_{IN} = 3V, V_{OUT} = 5V		2.2		
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 7V		0.085	0.15	%/V
I_B	FB Pin Bias Current (5)(6)			35	**250**	nA
I_{SS}	SS Pin Current		**7.5**	11	**13**	µA
V_{SS}	SS Pin Voltage		**1.2090**	1.2430	**1.2622**	
V_{IN}	Input Voltage Range		**2.7**		**7**	V
g_m	Error Amp Transconductance	ΔI = 5µA	40	87	135	µmho
A_V	Error Amp Voltage Gain			78		V/V
D_{MAX}	Maximum Duty Cycle		**85**	92.5		%
f_S	Switching Frequency	FSLCT = Ground	**450**	615	**750**	kHz
		FSLCT = V_{IN}	**0.9**	1.25	**1.5**	MHz
I_{SHDN}	Shutdown Pin Current	V_{SHDN} = 2.7V		2.4	**5.0**	µA
		V_{SHDN} = 0.3V		0.3	**1.2**	
I_L	Switch Leakage Current	V_{SW} = 20V		0.2	**8.0**	µA
R_{DSON}	Switch R_{DSON}	V_{IN} = 2.7V, I_{SW} = 1A		0.15	**0.4**	Ω
Th_{SHDN}	Shutdown Threshold	Output High	**1.2**	0.8		V
		Output Low		0.8	**0.3**	V
UVP	On Threshold		**2.3**	2.5		V
	Off Threshold			2.6	**2.7**	V

(1) All limits ensured at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Duty cycle affects current limit due to ramp generator.
(4) Current limit at 0% duty cycle. See Typical Performance Characteristics for Switch Current Limit vs. V_{IN}
(5) Bias current flows into FB pin.
(6) The FB pin should never exceed V_{IN}.

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Typical Performance Characteristics

$\overline{SHDN}$ Pin Current vs. $\overline{SHDN}$ Pin Voltage

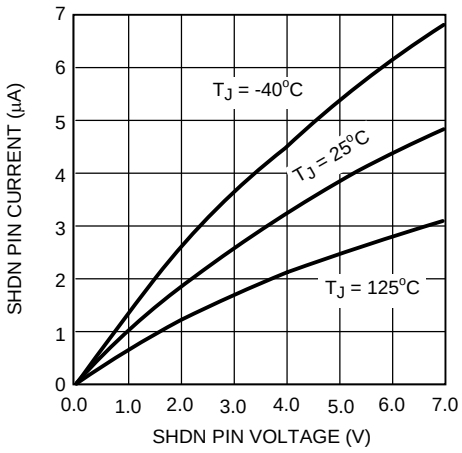

Figure 2.

SS Pin Current vs. Temperature

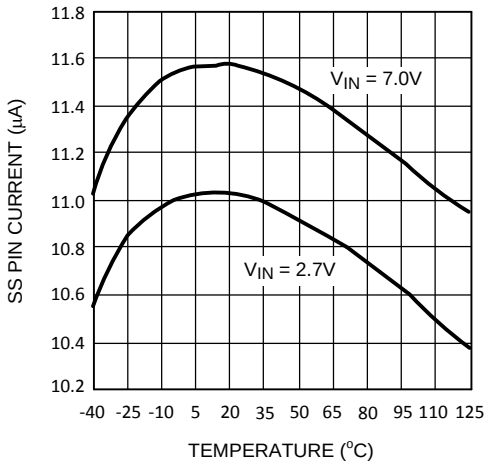

Figure 3.

FSLCT Pin Current vs. FSLCT Pin Voltage

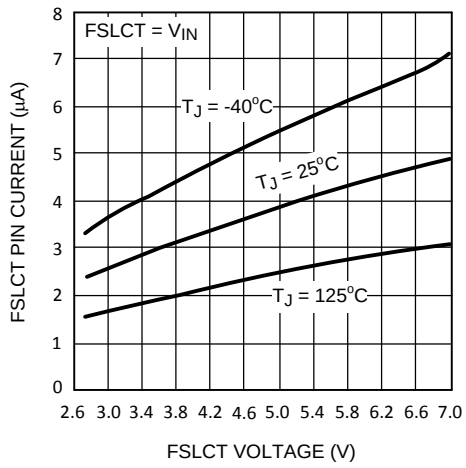

Figure 4.

FB Pin Current vs. Temperature

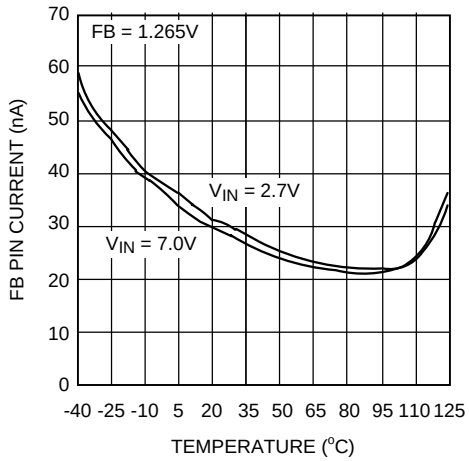

Figure 5.

NMOS R_{DSON} vs. Input Voltage

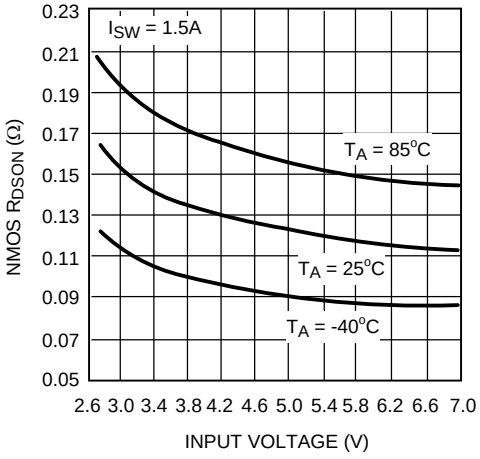

Figure 6.

615kHz Non-switching I_Q vs. Input Voltage

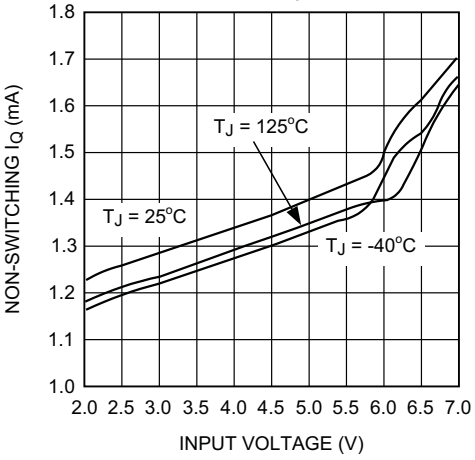

Figure 7.

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Typical Performance Characteristics (continued)

1.25MHz Non-switching I_Q vs. Input Voltage

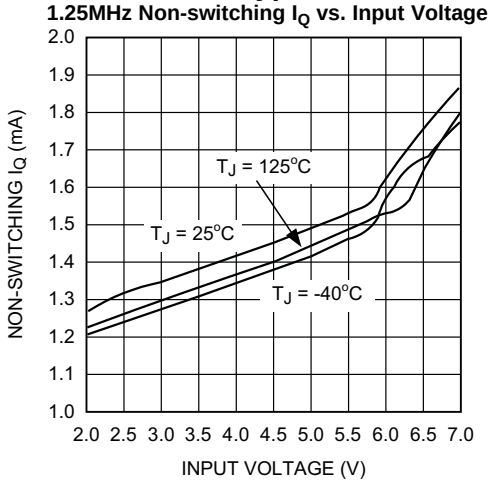

Figure 8.

615kHz Switching I_Q vs. Input Voltage

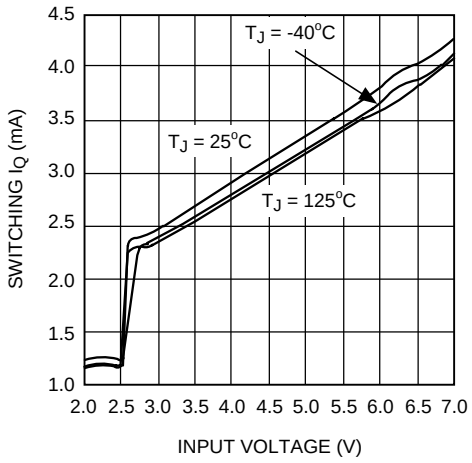

Figure 9.

1.25MHz Switching I_Q vs. Input Voltage

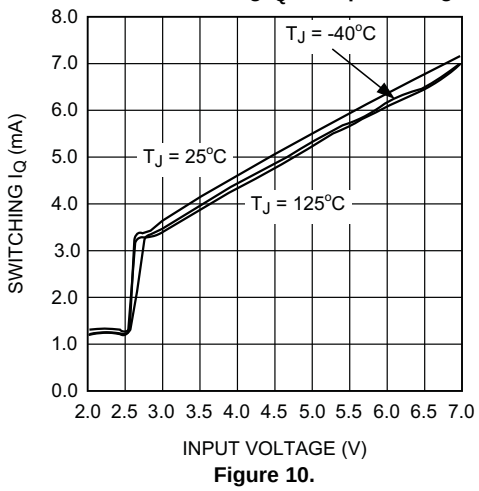

Figure 10.

615kHz Switching I_Q vs. Temperature

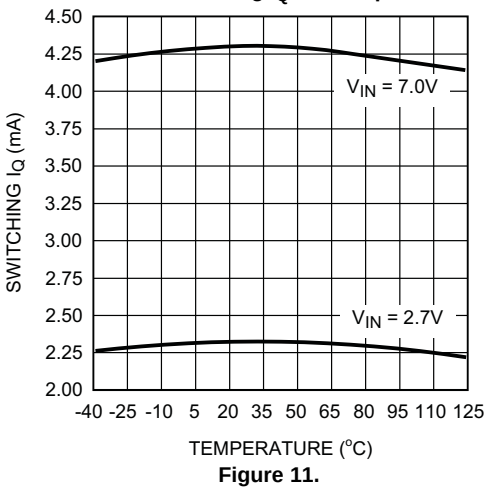

Figure 11.

1.25MHz Switching I_Q vs. Temperature

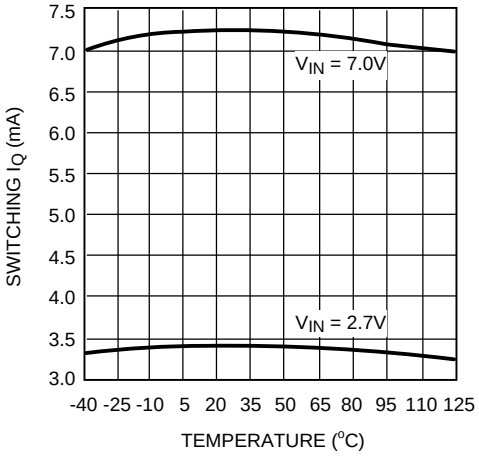

Figure 12.

615kHz Switching Frequency vs. Temperature

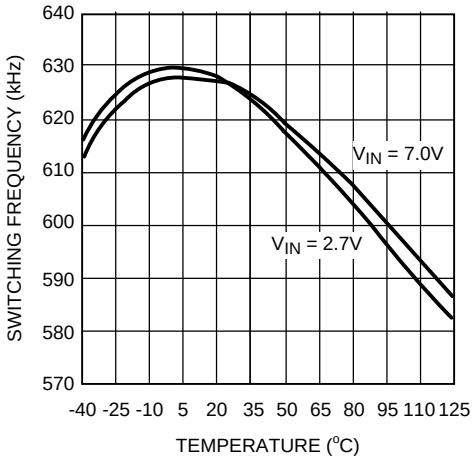

Figure 13.

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Typical Performance Characteristics (continued)

1.25MHz Switching Frequency vs. Temperature

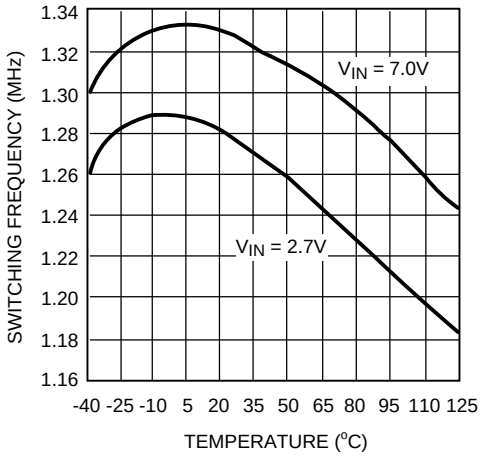

Figure 14.

615kHz Maximum Duty Cycle vs. Temperature

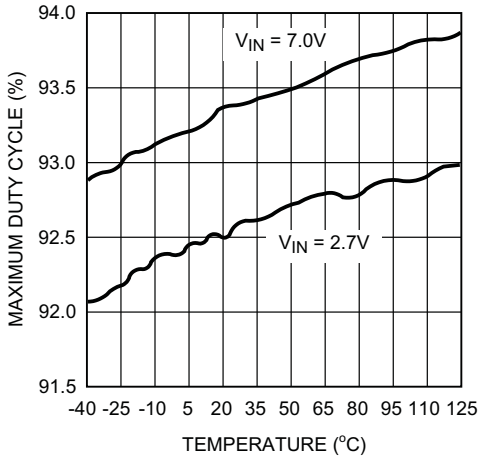

Figure 15.

1.25MHz Maximum Duty Cycle vs. Temperature

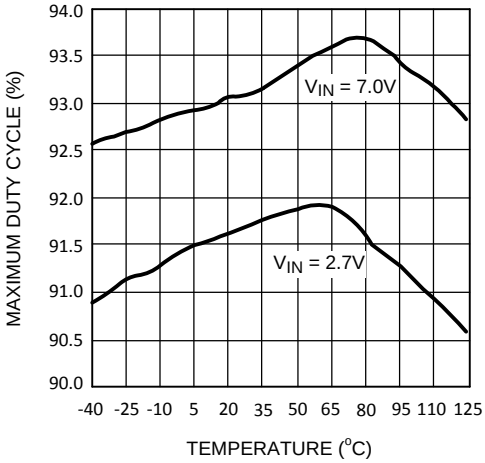

Figure 16.

Switch Current Limit vs. V_{IN}

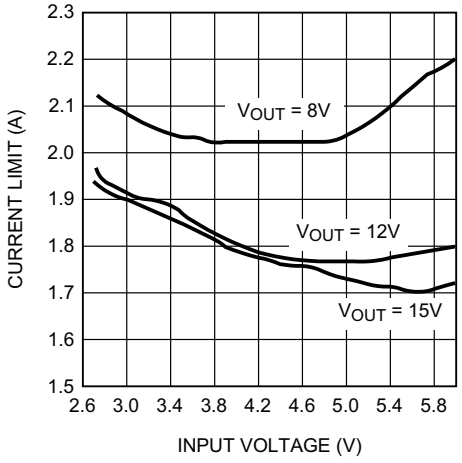

Figure 17.

Switch Current Limit vs. Temperature

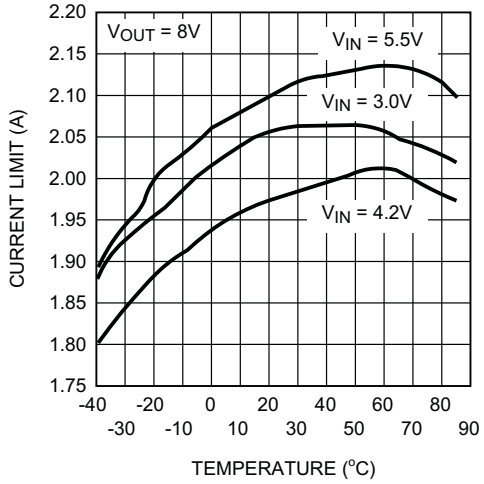

Figure 18.

Switch Current Limit vs. Temperature

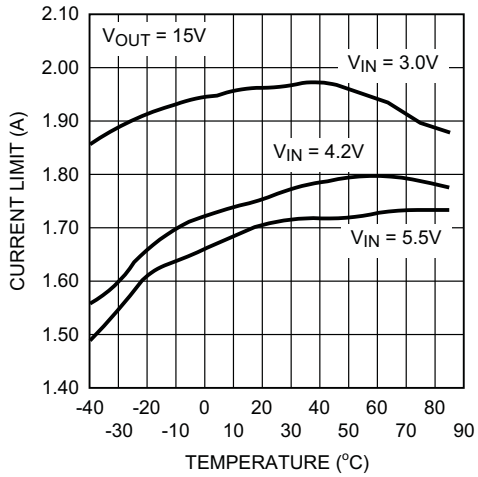

Figure 19.

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Typical Performance Characteristics (continued)

1.25MHz Efficiency vs. Load Current

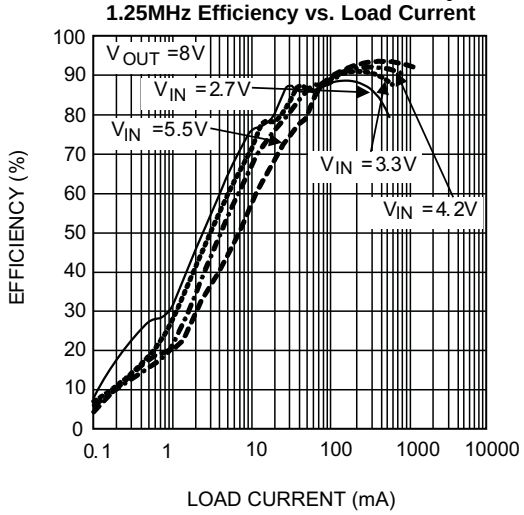

Figure 20.

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OPERATION

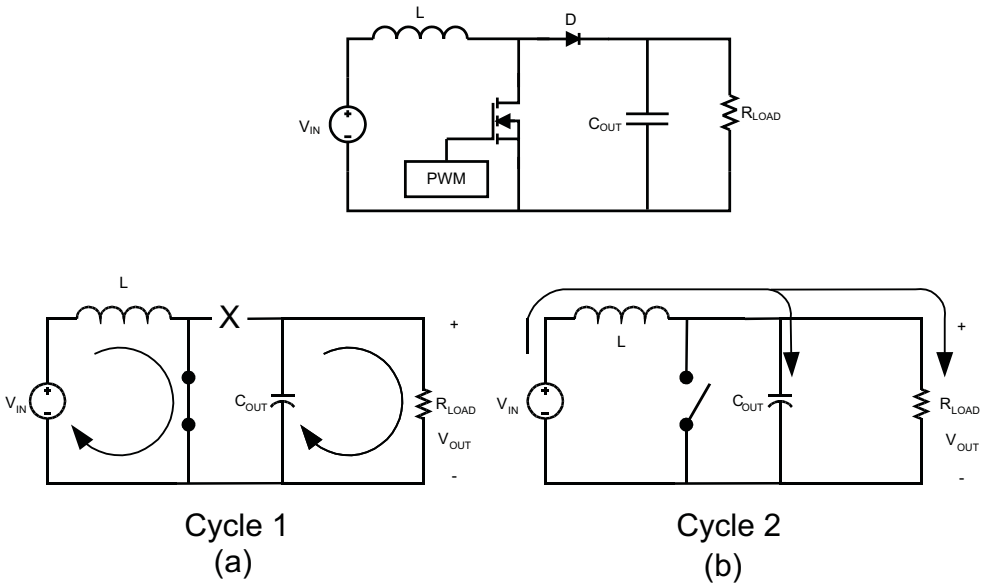

Figure 21. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM3224 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 21 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in Figure 21 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D}, \quad D' = (1-D) = \frac{V_{IN}}{V_{OUT}} \tag{1}$$

where

- D is the duty cycle of the switch

D and D′ will be required for design calculations.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the typical operating circuit. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.26}{1.26} \ \Omega \tag{2}$$

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SOFT-START CAPACITOR

The LM3224 has a soft-start pin that can be used to limit the inductor inrush current on start-up. The external SS pin is used to tailor the soft-start for a specific application but is not required for all applications and can be left open when not needed. When used, a current source charges the external soft-start capacitor, Css. The soft-start time can be estimated as:

$$Tss = Css*1.24V/Iss \quad (3)$$

THERMAL SHUTDOWN

The LM3224 includes thermal shutdown protection. If the die temperature exceeds 140°C the regulator will shut off the power switch, significantly reducing power dissipation in the device. The switch will remain off until the die temperature is reduced to approximately 120°C. If the cause of the excess heating is not removed (excessive ambient temperature, excessive power dissipation, or both) the device will continue to cycle on and off in this manner to protect from damage.

INTRODUCTION TO COMPENSATION

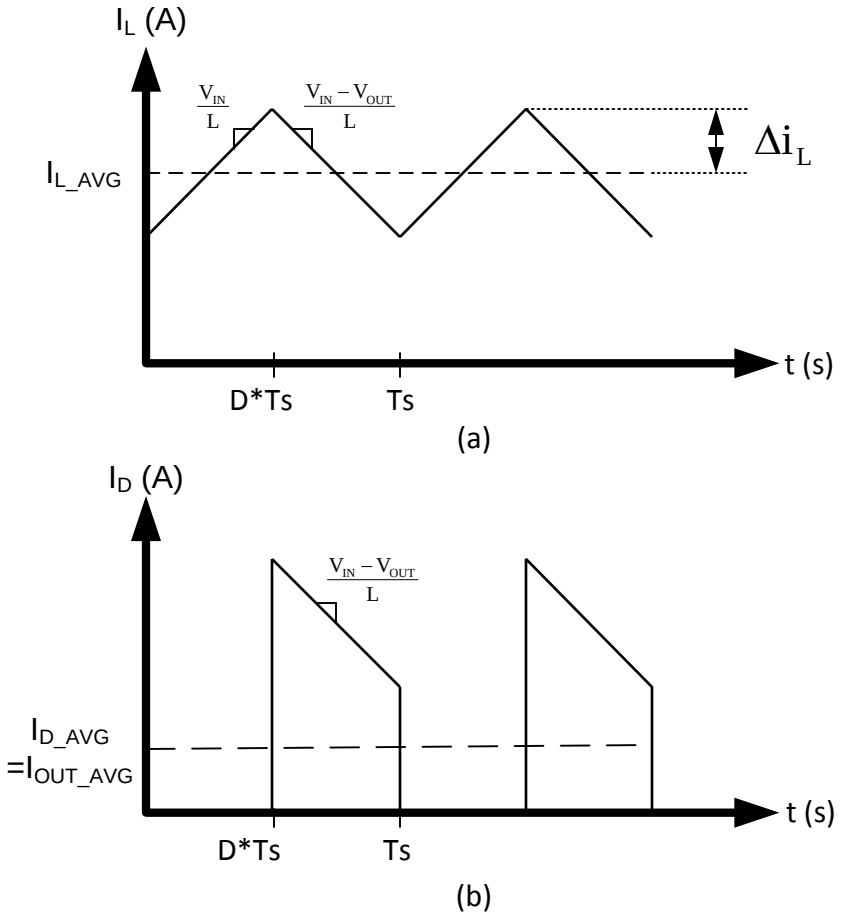

Figure 22. (a) Inductor current. (b) Diode current.

The LM3224 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see Figure 22 (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 10µH to 15µH inductor is recommended for most 615 kHz applications, while a 4.7µH to 10µH inductor may be used for most 1.25 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM3224 provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM3224 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz} \quad (4)$$

where

- R_O is the output impedance of the error amplifier (approximately 900kΩ) (5)

For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 100kΩ (R_C can be up to 200kΩ if C_{C2} is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ C_C ≤ 10nF. Refer to the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation, in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144\ fs} \left(\frac{D}{D'} - 1 \right) \text{ (in H)}$$

where

- fs is the switching frequency
- D is the duty cycl
- R_{DSON} is the ON resistance of the internal switch taken from the graph "NMOS R_{DSON} vs. Input Voltage" in the *Typical Performance Characteristics* section. (6)

This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in Figure 22 (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2Lfs} \text{ (in Amps)} \quad (7)$$

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The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or I_{LOAD}/D') plus Δi_L. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or Δi_L is greater than the average inductor current. Therefore, continuous conduction mode occurs when Δi_L is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in Figure 22 (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM3224, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin.

To ensure a bandwidth of ½ or less of the frequency of the RHP zero, calculate the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C2} as discussed later in this section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle \left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \right) \frac{g_m R_O D'}{R_{DSON}} \{[(\omega c Leff)// R_L]//R_L\} \right\rangle \text{ (in dB)} \quad (8)$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)} \quad (9)$$

$$Leff = \frac{L}{(D')^2} \quad (10)$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)} \quad (11)$$

$$mc \cong 0.072fs \text{ (in V/s)} \quad (12)$$

$$m1 \cong \frac{V_{IN} R_{DSON}}{L} \text{ (in V/s)}$$

where

- R_L is the minimum load resistance
- V_{IN} is the minimum input voltage
- g_m is the error amplifier transconductance found in the *Electrical Characteristics* table
- R_{DSON} is the value chosen from the graph "NMOS R_{DSON} vs. Input Voltage" in the *Typical Performance Characteristics* section (13)

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INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful condtions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)} \tag{14}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)} \tag{15}$$

where

- R_L is the minimum load resistance corresponding to the maximum load current (16)

The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section. Some suitable capacitor vendors include Vishay, Taiyo-Yuden, and TDK.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where

- I_{LOAD} is the maximum load current. (17)

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where

- R_O is the output impedance of the error amplifier, approximately 900kΩ (18)

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Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)} \tag{19}$$

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \text{ (in Hz)} \tag{20}$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10f_{ZC}$.

CHECKING THE DESIGN

With all the poles and zeros calculated the crossover frequency can be checked as described in the section *DC Gain and Open-loop Gain*. The compensation values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimum performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

POWER DISSIPATION

The output power of the LM3224 is limited by its maximum power dissipation. The maximum power dissipation is determined by the formula

$$P_D = (T_{jmax} - T_A)/\theta_{JA}$$

where

- T_{jmax} is the maximum specidfied junction temperature (125°C)
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance of the package (21)

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in the typical operating circuit, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note *Layout Guidelines for Switching Power Supplies* (SNVA021).

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APPLICATION INFORMATION

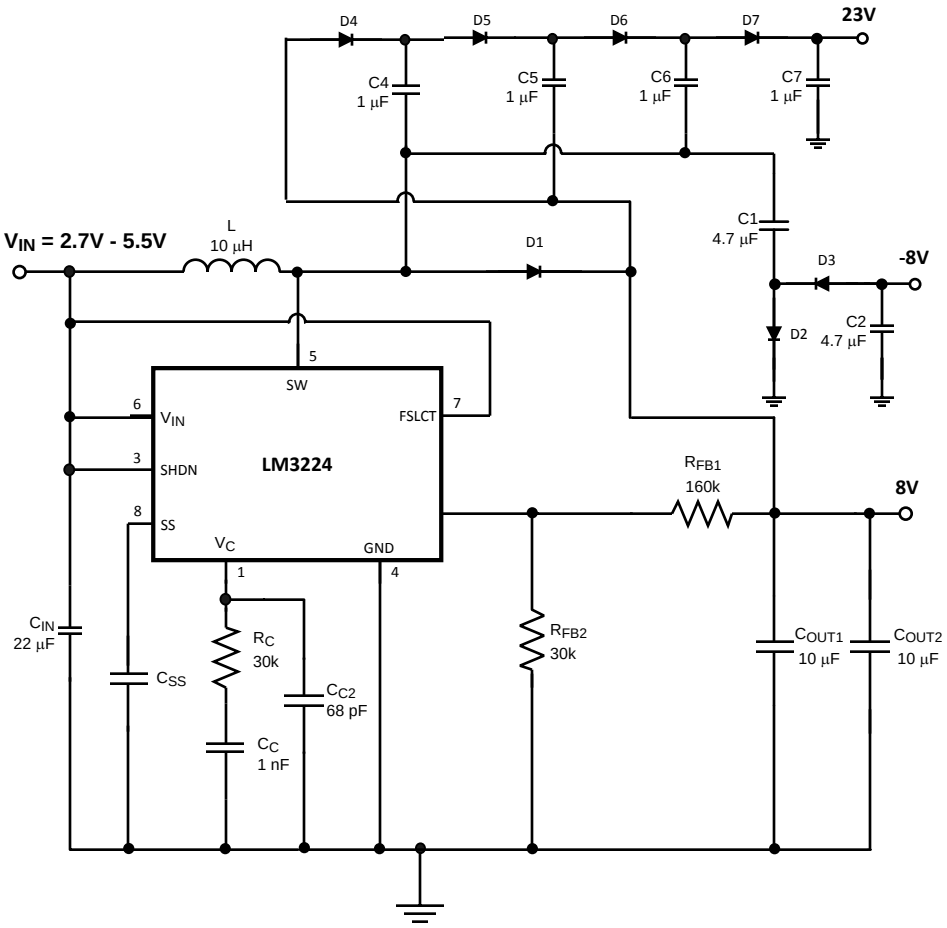

Figure 23. Triple Output TFT Bias (615 kHz operation)

TRIPLE OUTPUT TFT BIAS

The circuit in Figure 23 shows how the LM3224 can be configured to provide outputs of 8V, −8V, and 23V, convenient for biasing TFT displays. The 8V output is regulated, while the −8V and 23V outputs are unregulated.

The 8V output is generated by a typical boost topology. The basic operation of the boost converter is described in the OPERATION section. The output voltage is set with R_{FB1} and R_{FB2} by:

$$R_{FB1} = R_{FB2} \frac{V_{OUT} - 1.26}{1.26} \Omega \quad (22)$$

The compensation network of R_C and C_C are chosen to optimally stabilize the converter. The inductor also affects the stability. When operating at 615 kHz, a 10uH inductor is recommended to insure the converter is stable at duty cycles greater than 50%. Refer to the COMPENSATION section for more information.

The -8V output is derived from a diode inverter. During the second cycle, when the transistor is open, D2 conducts and C1 charges to 8V minus a diode drop (≅0.4V if using a Schottky). When the transistor opens in the first cycle, D3 conducts and C1's polarity is reversed with respect to the output at C2, producing -8V.

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The 23V output is realized with a series of capacitor charge pumps. It consists of four stages: the first stage includes C4, D4, and the LM3224 switch; the second stage uses C5, D5, and D1; the third stage includes C6, D6, and the LM3224 switch; the final stage is C7 and D7. In the first stage, C4 charges to 8V when the LM3224 switch is closed, which causes D5 to conduct when the switch is open. In the second stage, the voltage across C5 is VC4 + VD1 - VD5 = VC4 ≅ 8V when the switch is open. However, because C5 is referenced to the 8V output, the voltage at C5 is 16V when referenced to ground. In the third stage, the 16V at C5 appears across C6 when the switch is closed. When the switch opens, C6 is referenced to the 8V output minus a diode drop, which raises the voltage at C6 with respect to ground to about 24V. Hence, in the fourth stage, C7 is charged to 24V when the switch is open. From the first stage to the last, there are three diode drops that make the output voltage closer to 24 - 3xVDIODE (about 22.8V if a 0.4V forward drop is assumed).

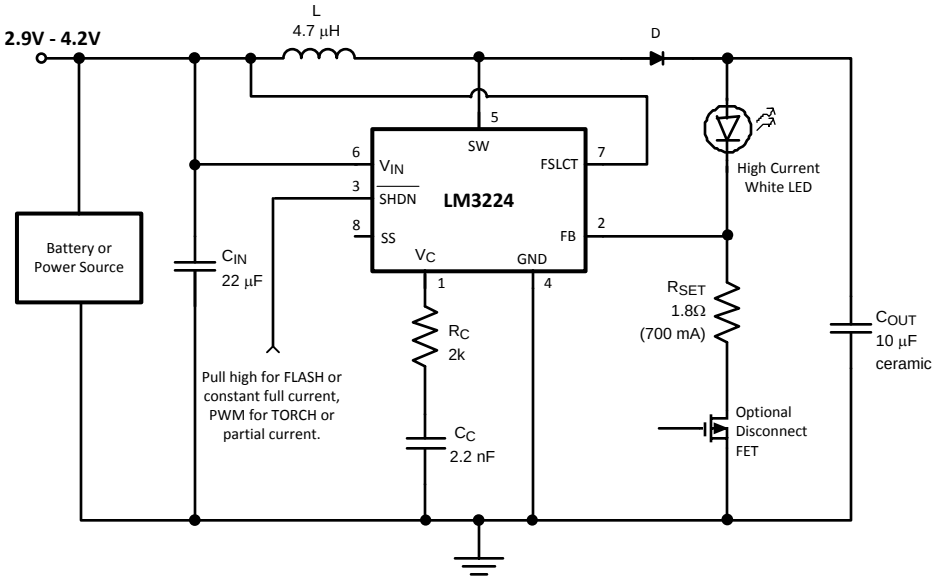

Figure 24. PWM White LED Flash/Torch Driver

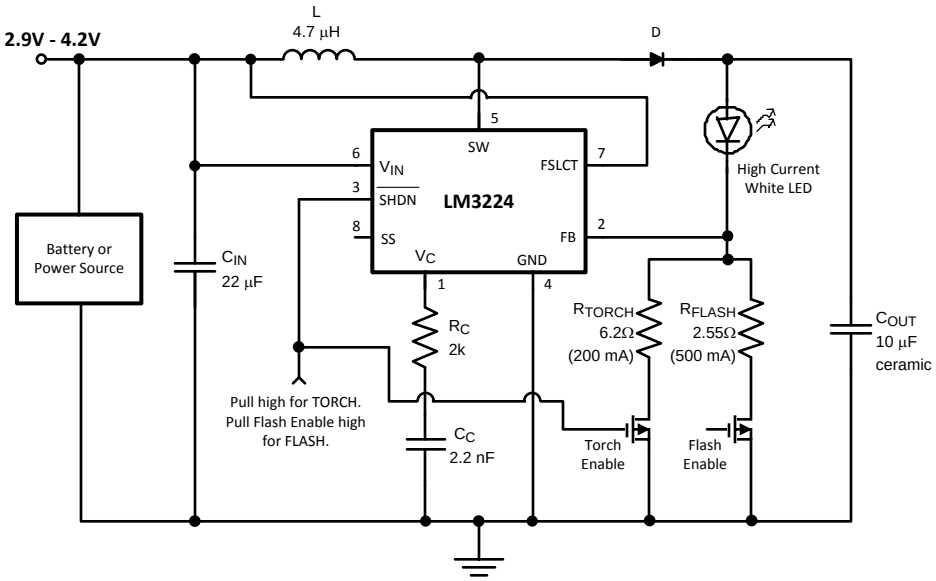

Figure 25. Continuously Operating White LED Flash/Torch Driver

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The LM3224 can be configured to drive high current white LEDs for the flash and torch functions of a digital camera, camera phone, or any other similar light source. The flash/torch can be set up with the circuit in Figure 24 by using the resistor R_{SET} to determine the amount of current that will flow through the LED using the equation:

$$I_{LED} = V_{FB}/R_{SET} \quad (23)$$

If the flash and torch modes will both be used the resistor R_{SET} can be chosen for the higher current flash value. To flash the circuit pull the $\overline{SHDN}$ high for the time duration needed for the flash. To enable a lower current torch mode a PWM signal can be applied to the $\overline{SHDN}$ pin. The torch current would then be approximately the percent ON time of the PWM signal multiplied by the flash (or maximum) current. The optional disconnect FET can be used to eliminate leakage current through the LEDs when the part is off and also to disconnect the LED when the input voltage exceeds the forward voltage drop of the LED. The maximum output current the LM3224 can supply in this configuration is shown in Table 1.

Figure 25 is another method of driving a high current white LED. This circuit has a higher component count but allows the switcher to remain on continuously for torch mode reducing stress on the supply. The two FETs also double for a disconnect function as described above. In this circuit the device and the torch enable FET are turned on setting a lower current through the LED. When flash is needed the flash enable FET is turned on to increase the current for the amount of time desired. The minimum ensured maximum output current for this circuit is the same as for Figure 24.

Table 1. Maximum LED Drive current (F_{SW}=1.25MHz, L=4.7µH, LED V_{FMAX}=4V (V_{OUT}=5.26V)

V_{IN}	LED Drive Current (mA)
4.2	1077
4.1	1047
4.0	1017
3.9	987
3.8	958
3.7	929
3.6	900
3.5	871
3.4	842
3.3	814
3.2	785
3.1	757
3.0	729
2.9	701
2.8	673
2.7	646

Table 2. Some Recommended Inductors (Others May Be Used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 and DT3316 series	www.coilcraft.com 800-3222645
TDK	SLF10145 series	www.component.tdk.com 847-803-6100
Pulse	P0751 and P0762 series	www.pulseeng.com
Sumida	CDRH8D28 and CDRH8D43 series	www.sumida.com

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Table 3. Some Recommended Input And Output Capacitors (Others May Be Used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com 407-324-4140
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com 408-573-4150
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
MuRata	High capacitance MLCC ceramic	www.murata.com

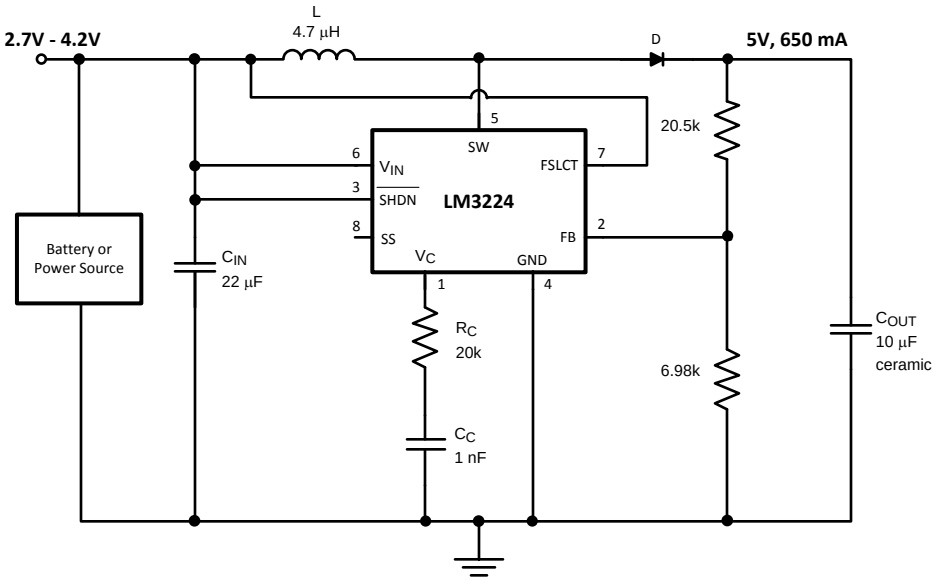

Figure 26. 1.25MHz, 5V Output

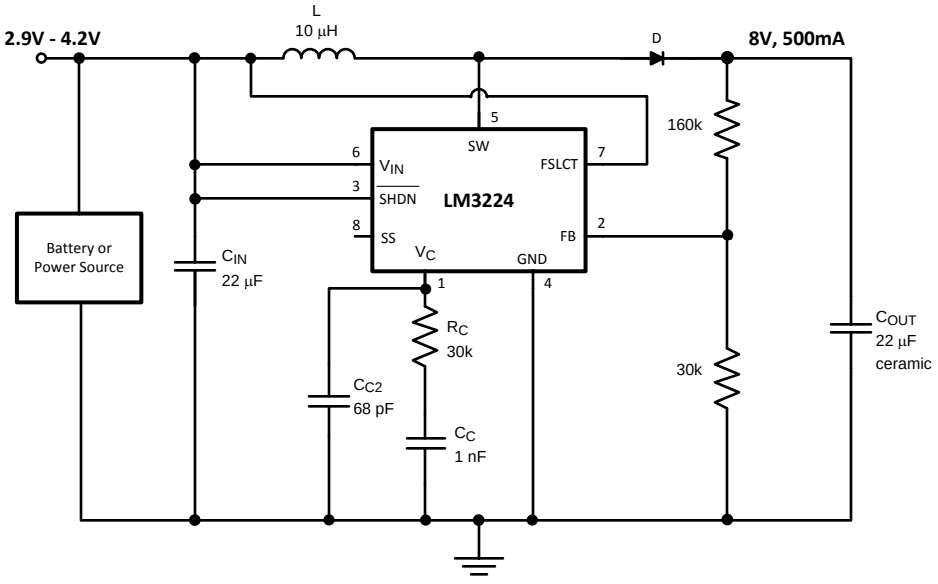

Figure 27. 1.25MHz, 8V Output

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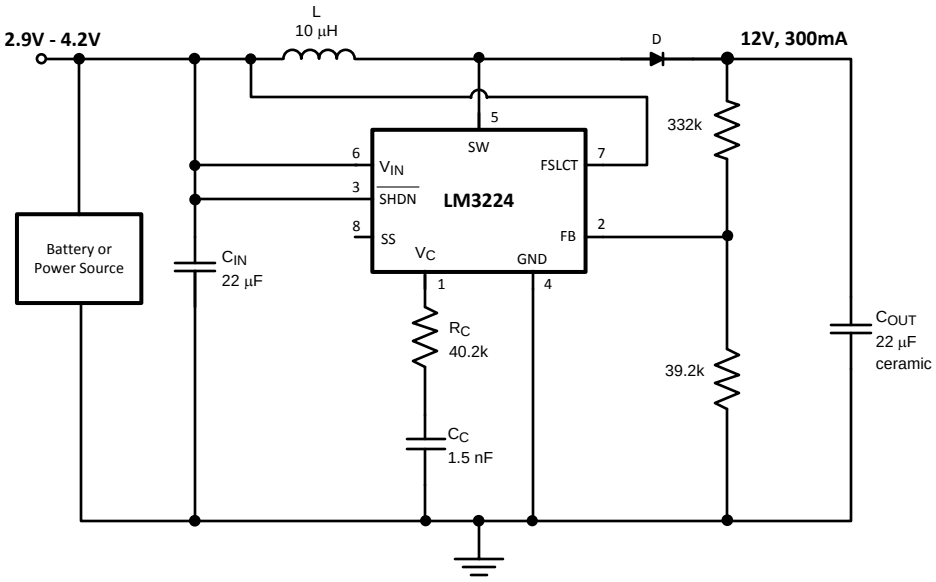

Figure 28. 1.25MHz, 12V Output

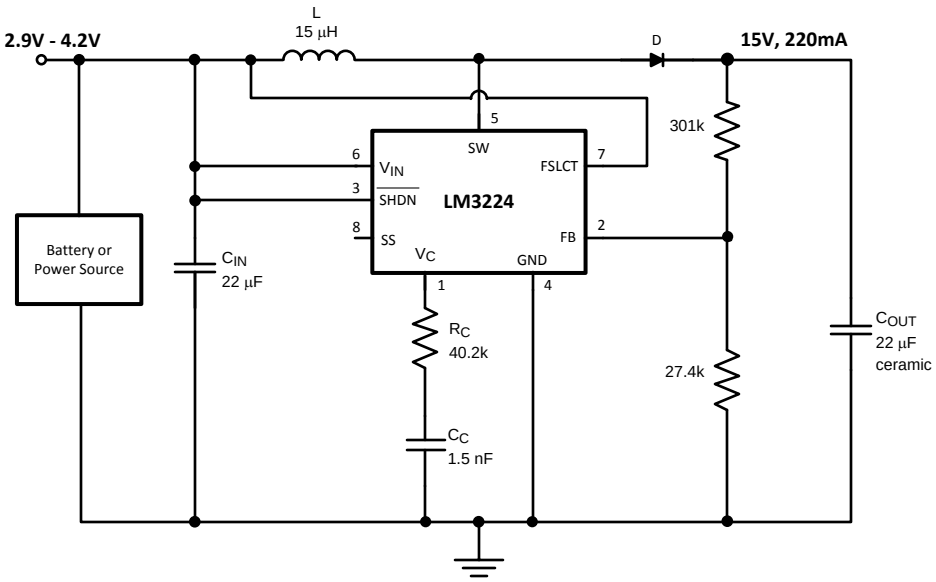

Figure 29. 1.25MHz, 15V Output

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REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3224MM-ADJ/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SEKB
LM3224MM-ADJ/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SEKB
LM3224MM-ADJ/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SEKB
LM3224MMX-ADJ/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	SEKB
LM3224MMX-ADJ/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SEKB
LM3224MMX-ADJ/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SEKB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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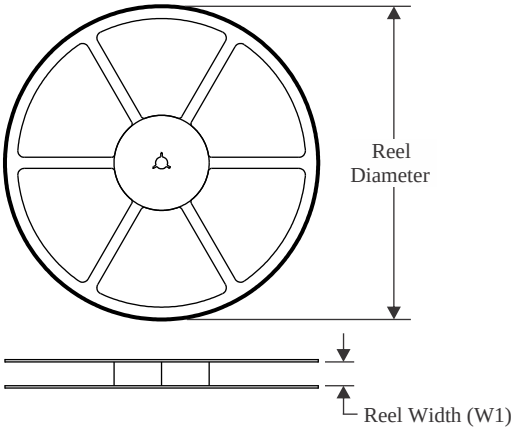
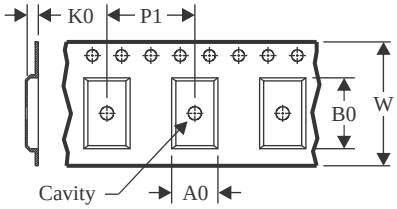
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

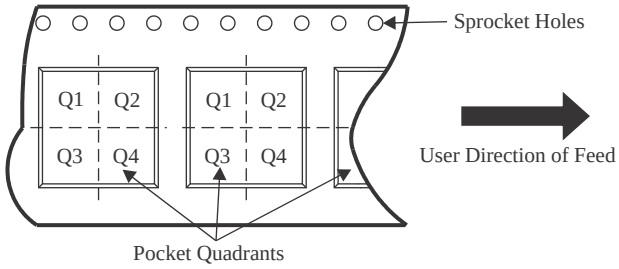


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

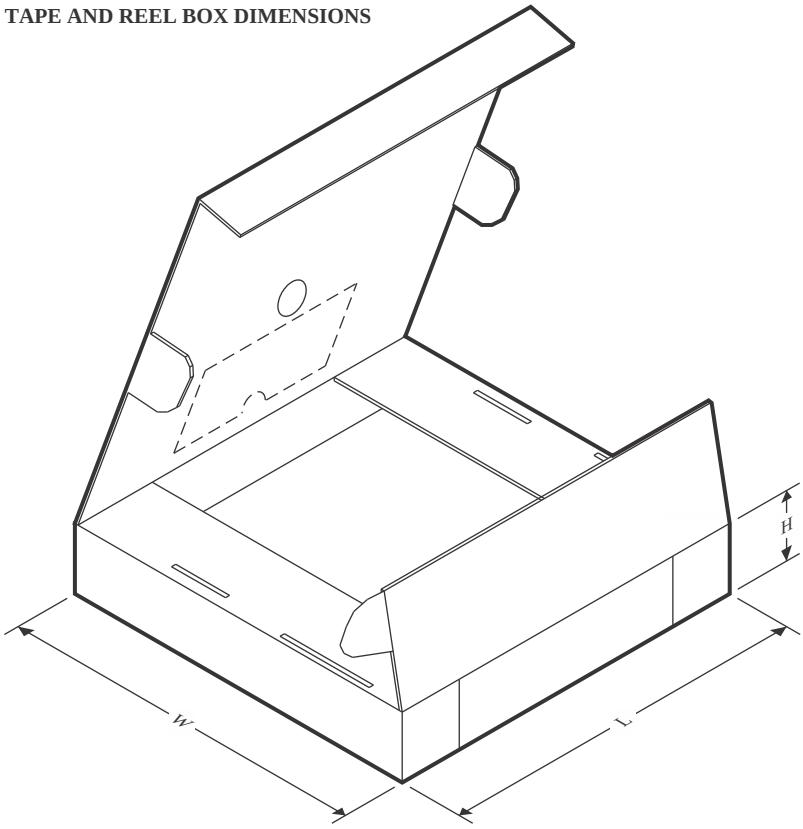
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3224MM-ADJ/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3224MMX-ADJ/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

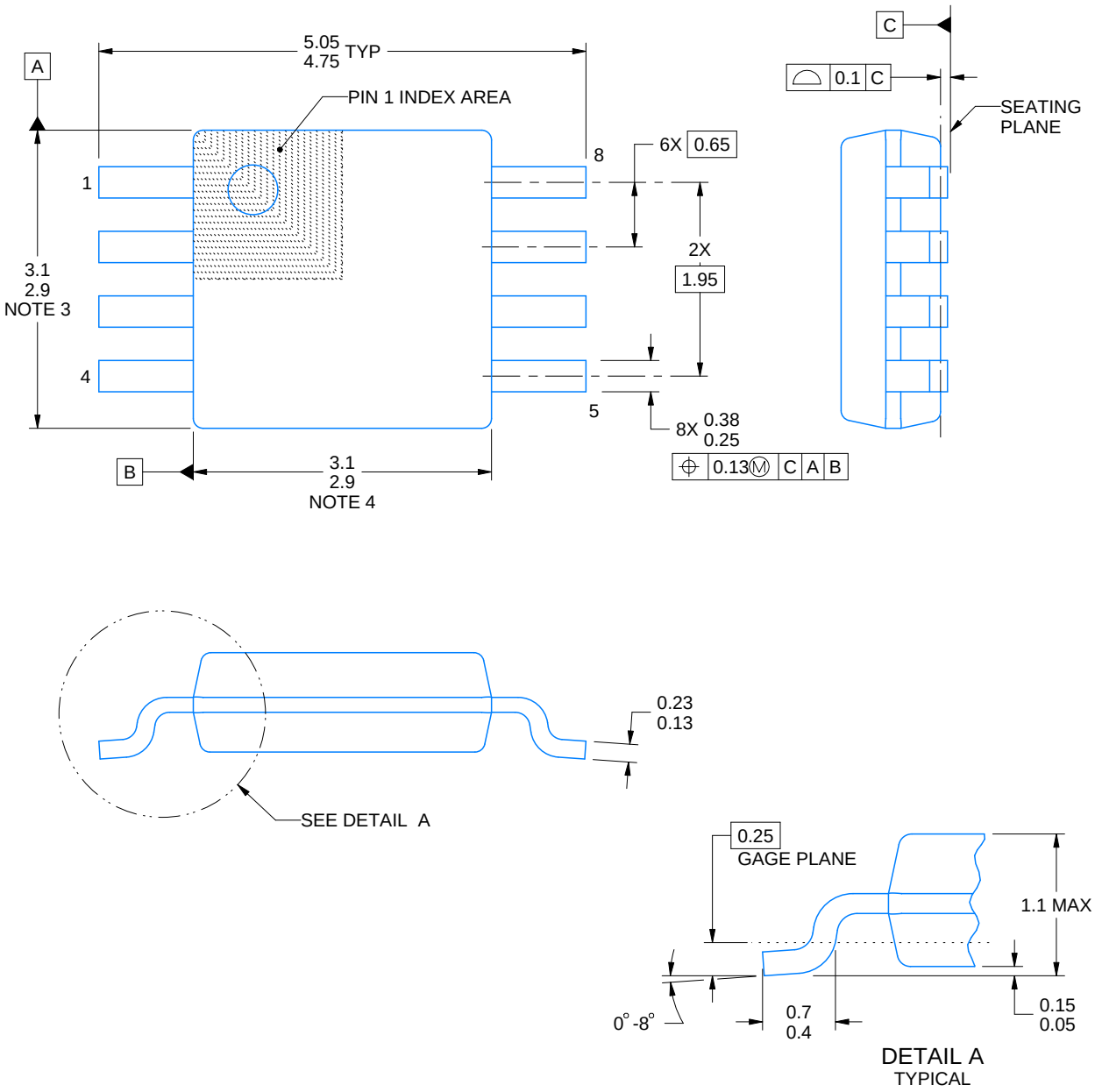
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3224MM-ADJ/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3224MMX-ADJ/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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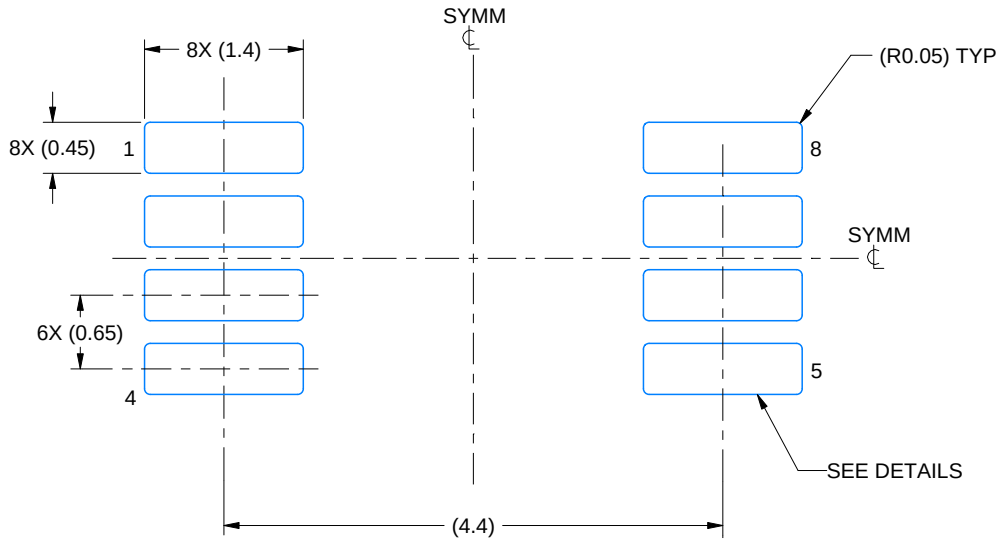
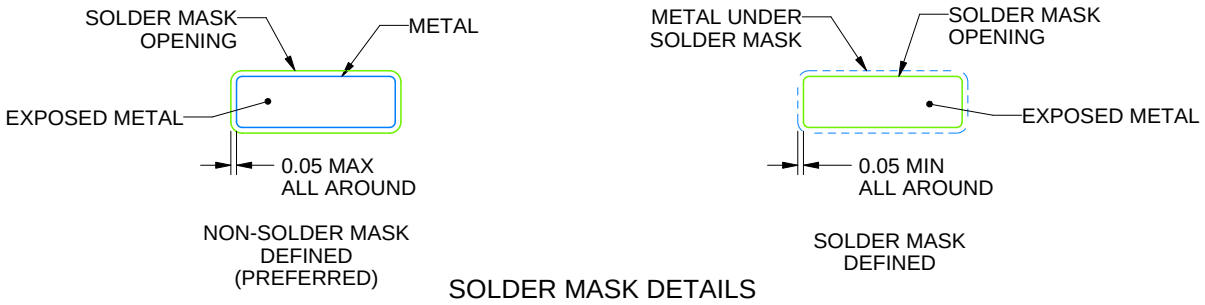
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

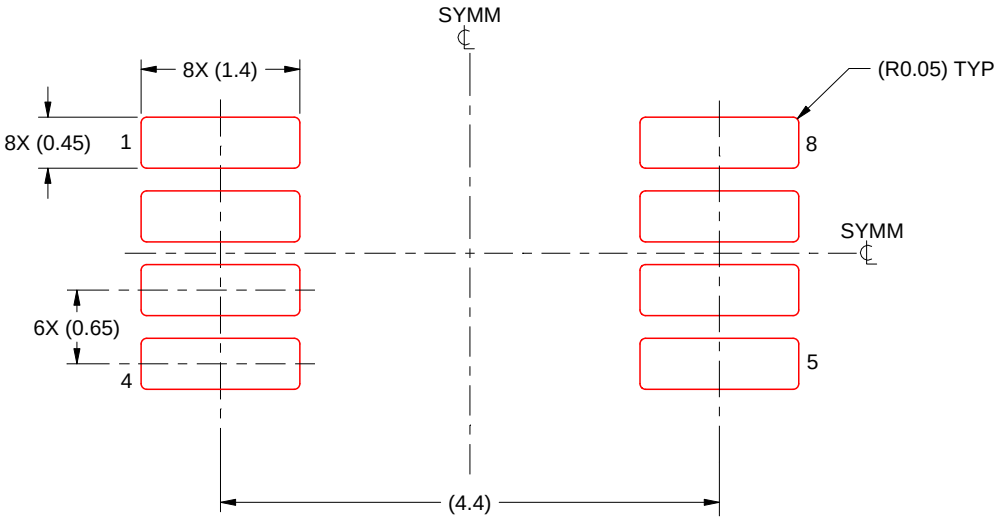


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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