LM4834 Boomer® Audio Power Amplifier Series 1.75W Audio Power Amplifier with DC Volume Control and Microphone Preamp

Check for Samples: LM4834

FEATURES

- **PC98 Compliant**
- **"Click and Pop" Suppression Circuitry**
- **Stereo Line Level Outputs with Mono Input Capability for System Beeps**
- **Microphone Preamp with Buffered Power Supply**
- **DC Volume Control Interface**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Multimedia Monitors**
- **Desktop and Portable Computers**

APPLICATIONS

- **THD at 1.1W Continuous Average Output Power into 8Ω at 1kHz 0.5% (max)**
- **Output Power into 4Ω at 1.0% THD+N 1.75W (typ)**
- **THD at 70mW Continuous Average Output Power into 32Ω at 1kHz 0.1% (typ)**
- **Shutdown Current 1.0µA (max)**
- **Supply Current 17.5mA (typ)**

DESCRIPTION

The LM4834 is a monolithic integrated circuit that provides DC volume control, and a bridged audio power amplifier capable of producing 1.75W into 4Ω with less than 1.0% (THD). In addition, the headphone/lineout amplifier is capable of driving 70 mW into 32Ω with less than 0.1%(THD). The LM4834 incorporates a volume control and an input microphone preamp stage capable of driving a 1 kΩ load impedance.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components in surface mount packaging. The LM4834 incorporates a DC volume control, a bridged audio power amplifier and a microphone preamp stage, making it optimally suited for multimedia monitors and desktop computer applications.

The LM4834 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Block Diagram

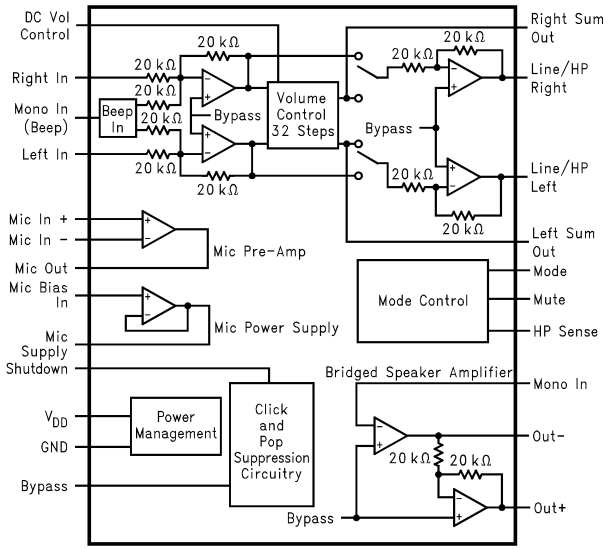

Figure 1. LM4834 Block Diagram

Connection Diagram

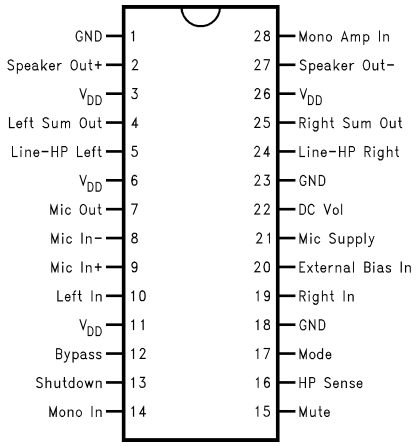

Figure 2. SSOP Package
Top View
See Package Number DB for SSOP

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		-65°C to +150°C
Input Voltage		−0.3V to V_{DD}+0.3V
Power Dissipation(3)		Internally limited
ESD Susceptibility(4)		2000V
Pin 5		1500V
ESD Susceptibility(5)		200V
Junction Temperature		150°C
Soldering Information Small Outline Package	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
θ_{JC} (typ)—DB		29°C/W
θ_{JA} (typ)—DB		95°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditionsfor which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics*state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the deviceis within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$.For the LM4834MS, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 95°C/W assuming the DB package.

(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

(5) Machine Model, 220 pF–240 pF discharged through all pins.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤TA ≤ 85°C
Supply Voltage	4.5 ≤ V_{DD} ≤ 5.5V

Electrical Characteristics for Entire IC(1)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4834		Units (Limits)
			Typical(2)	Limit(3)	
V_{DD}	Supply Voltage			4.5	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O= 0A	17.5	26	mA (max)
I_{SD}	Shutdown Current	$V_{pin13} = V_{DD}$	0.6	2.0	µA (max)

(1) All voltages are measured with respect to the ground pins, unlessotherwise specified. All specifications are tested using the typical application as shown in Figure 3.

(2) Typicals are measured at 25°C and represent the parametric norm.

(3) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Electrical Characteristics for Volume Attenuators[1]

The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4834		Units (Limits)
			Typical[2]	Limit[3]	
C_{RANGE}	Attenuator Range	Gain with $V_{pin\ 22}$ = 5V	2.6	3.65	dB (max)
		Attenuation with $V_{pin\ 22}$ = 0V	-75	-88	dB (min)
A_M	Mute Attenuation	$V_{pin\ 15}$ = 5V, Sum Out	-92	-105	dB (max)
		$V_{pin\ 15}$ = 5V, Line Out/Headphone Amp	-92	-105	dB (max)

(1) All voltages are measured with respect to the ground pins, unlessotherwise specified. All specifications are tested using the typical application as shown in Figure 3.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Electrical Characteristics for Microphone Preamp and Power Supply[1]

The following specifications apply forV_{DD} = 5V unless otherwise noted. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4834		Units (Limits)
			Typical[2]	Limit[3]	
V_{OS}	Offset Voltage	V_{IN} = 0V	0.9		mV
SNR	Signal to Noise Ratio	V_{DD} = 5V, R_L = 1k, f = 1 kHz, V_{OUT} = 4.7V , A-Wtd Filter	123		dB
V_{SWING}	Output Voltage Swing	f = 1 kHz, THD < 1.0%, R_L = 1 kΩ	4.72		V
E_{NO}	Input Referred Noise	A-Weighted Filter	1.2		µV
PSRR	Power Supply Rejection Ratio	f = 120 Hz, V_{RIPPLE}= 200 mVrms, C_B= 1µF	28		dB
V_S	Mic Power Supply	R_L = 1 kΩ, Bias In = 2.5V	2.5	2.5	V (min)

(1) All voltages are measured with respect to the ground pins, unlessotherwise specified. All specifications are tested using the typical application as shown in Figure 3.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Electrical Characteristics for Line/Headphone Amplifier[1]

The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4834		Units (Limits)
			Typical[2]	Limit[3]	
P_O	Output Power	THD = 0.1%; f = 1kHz; R_L = 32Ω	70		mW
		THD = 10%; f = 1 kHz; R_L = 32Ω	95		mW
THD+N	Total Harmonic Distortion+Noise	V_{OUT} = 4V_{P-P}, 20 Hz <f < 20 kHz, R_L = 10kΩ, A_{VD} = −1	0.05		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f =120 Hz, V_{RIPPLE} = 200 mVrms	30		dB
SNR	Signal to Noise Ratio	V_{DD}=5V, P_{OUT}=75mW, R_L = 32Ω, A-Wtd Filter	102		dB

(1) All voltages are measured with respect to the ground pins, unlessotherwise specified. All specifications are tested using the typical application as shown in Figure 3.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Electrical Characteristics for Bridged Speaker Amplifer(1)(2)

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4834		Units (Limits)
			Typical(3)	Limit(4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	30	mV (max)
P_O	Output Power	THD = 0.5% (max);f = 1 kHz; R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%;f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_O = 1W, 20 Hz< f < 20 kHz, R_L = 8Ω, A_{VD} = 2	0.3		%
		P_O = 340 mW, R_L = 32Ω	1.0		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f = 120 Hz,V_{RIPPLE} = 200 mVmrs	58		dB
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_{OUT} = 1.1W, R_L= 8Ω, A-Wtd Filter	93		dB

(1) All voltages are measured with respect to the ground pins, unlessotherwise specified. All specifications are tested using the typical application as shown in Figure 3.

(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditionsfor which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics*state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the deviceis within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.

(3) Typicals are measured at 25°C and represent the parametric norm.

(4) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Typical Application

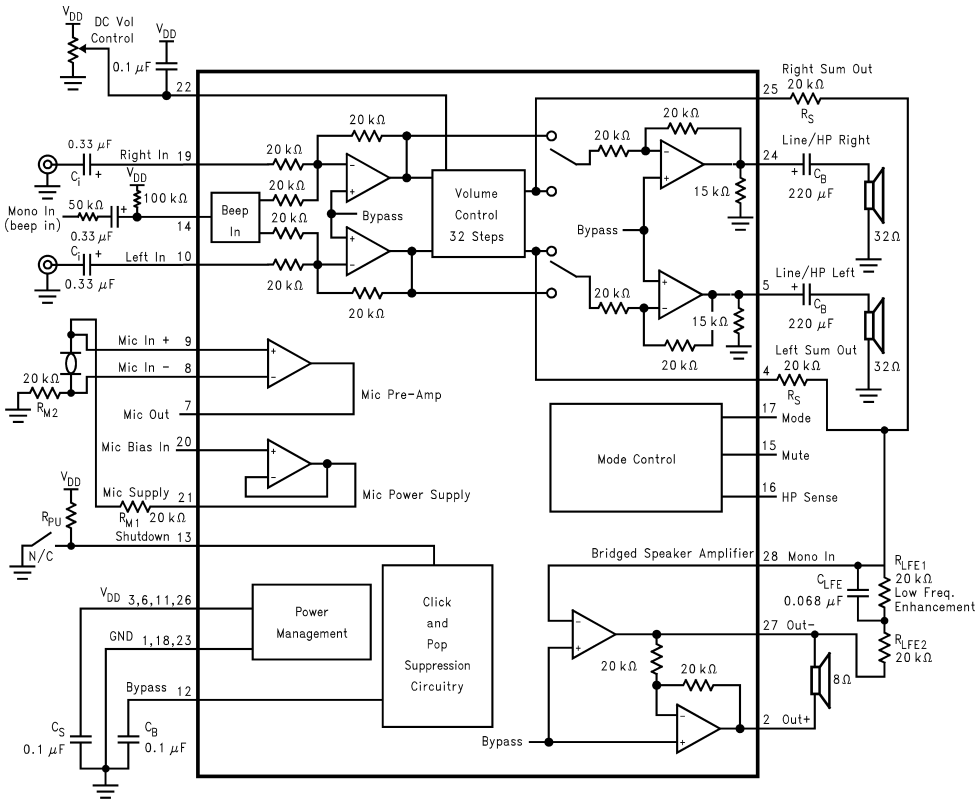

Figure 3. Typical Application Circuit

Truth Table for Logic Inputs

Mode	Mute	HP Sense	DC Vol. Control	Line/HP Left	Line/HP Right	Speaker Out
0	0	0	Adjustable	Fixed Level	Fixed Level	Vol. Changes
0	0	1	Adjustable	Fixed Level	Fixed Level	Muted
0	1	X	_	Fixed Level	Fixed Level	Muted
1	0	0	Adjustable	Vol. Changes	Vol. Changes	Vol. Changes
1	0	1	Adjustable	Vol. Changes	Vol. Changes	Muted
1	1	X	_	Muted	Muted	Muted

External Components Description
Figure 3

Components.		Functional Description
1.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
2.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
3.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.
4.	C_O	Output coupling capacitor which blocks the DC voltage at the amplifiers output. Forms a high pass filter with R_L at $f_o = 1/(2\pi R_L C_O)$.
5.	R_S	Summing resistor that combines the right and left line level outputs into the mono input of the bridged amplifier. The two summing resistors in parallel determine the value of the input resistance of the bridged amplifier.
6.	R_{LFE}	Resistor for the bridged power amplifier in series with R_F at high frequencies. Used in conjunction with C_{LFE} to increase closed-loop gain at low frequencies.
7.	R_F	Feedback resistor which sets the closed-loop gain in conjunction with the equivalent R_S for the bridged power amplifier.
8.	R_{M1}	Resistor in series with Microphone supply pin and the microphone for biasing differential input microphones.
9.	R_{M2}	Resistor in series with reference ground and the microphone used for biasing differential input microphones.

Typical Performance Characteristics

THD+N vs Frequency Bridged Power Amp

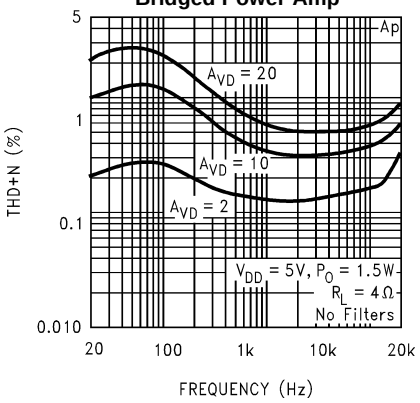

Figure 4.

THD+N vs Frequency Bridged Power Amp

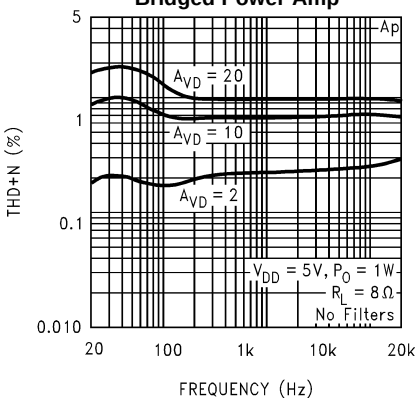

Figure 5.

THD+N vs Frequency Bridge Power Amp

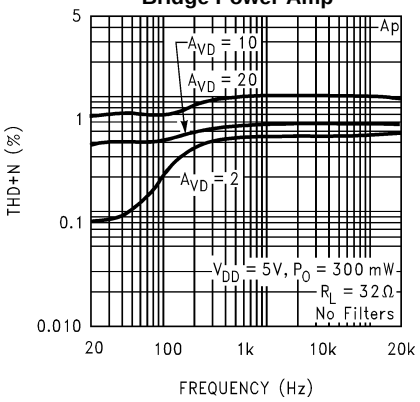

Figure 6.

THD+N vs Frequency Line Out/HP Amplifiers

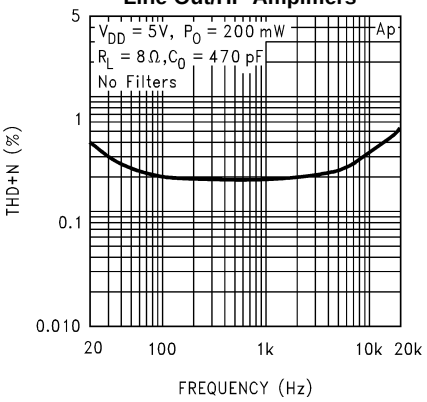

Figure 7.

THD+N vs Frequency Line Out/HP Amplifiers

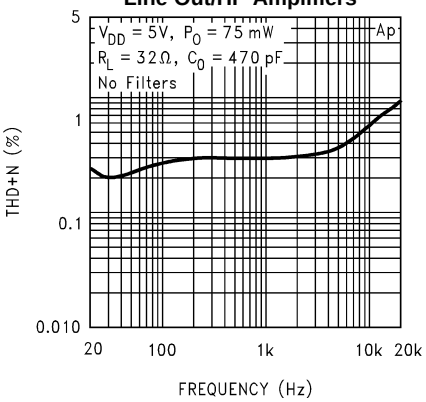

Figure 8.

THD+N vs Frequency Line Out/HP Amplifiers

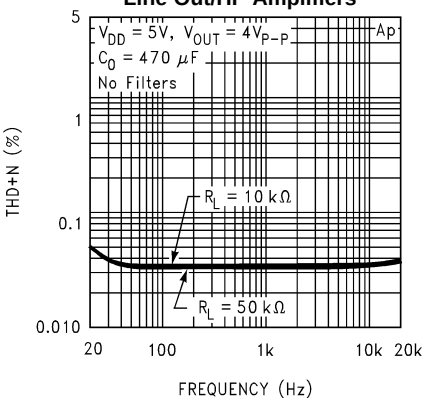

Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Output Power Bridged Power Amp

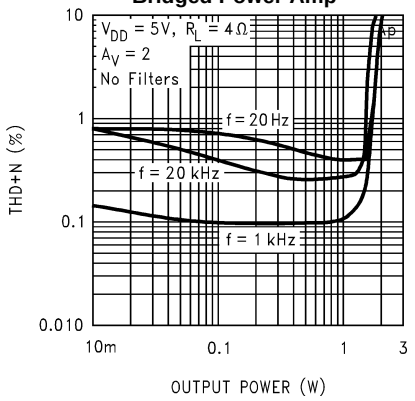

Figure 10.

THD+N vs Output Power Bridged Power Amp

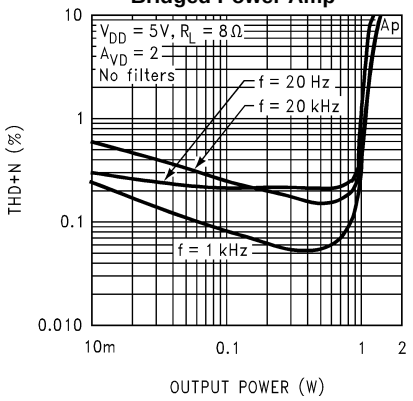

Figure 11.

THD+N vs Output Power Bridged Power Amp

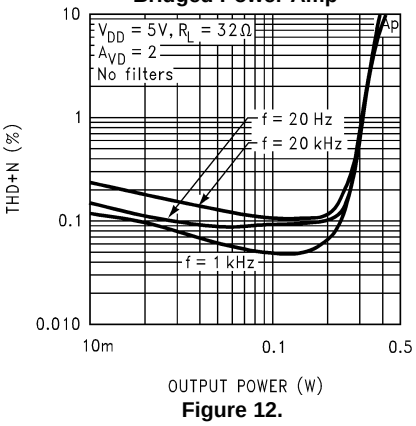

Figure 12.

THD+N vs Output Power Line Out/HP Amplifiers

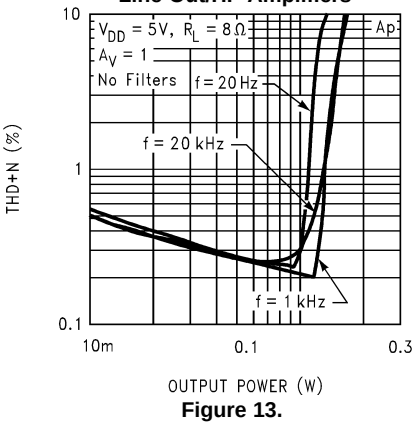

Figure 13.

THD+N vs Output Power Line Out/HP Amplifiers

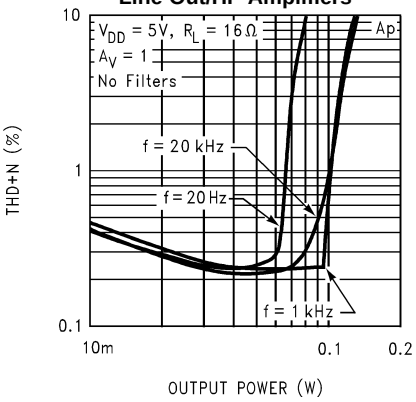

Figure 14.

THD+N vs Output Power Line Out/HP Amplifiers

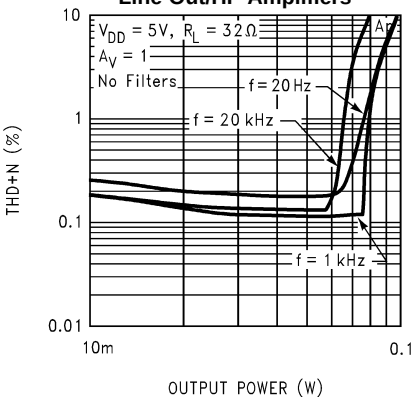

Figure 15.

Typical Performance Characteristics (continued)

Output Power vs Load Resistance Bridged Power Amp

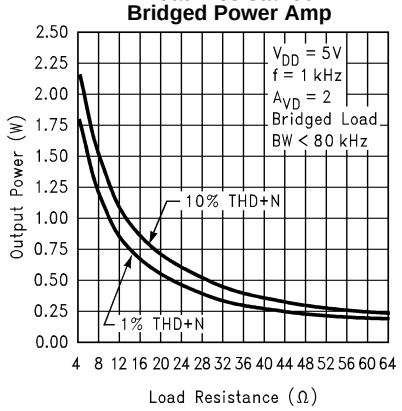

Figure 16.

Output Power vs Load Resistance Line Out/HP Amplifiers

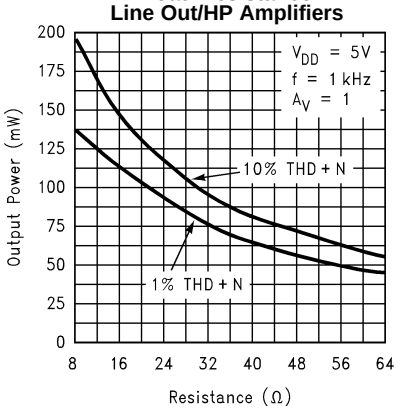

Figure 17.

Volume Control Characteristics

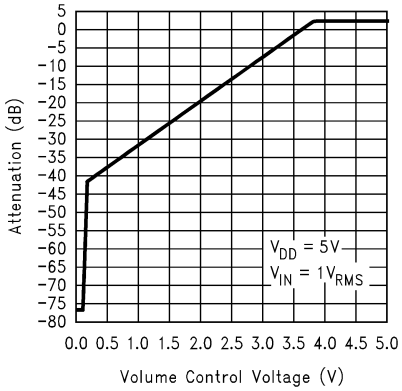

Figure 18.

Noise Floor Bridged Power Amp

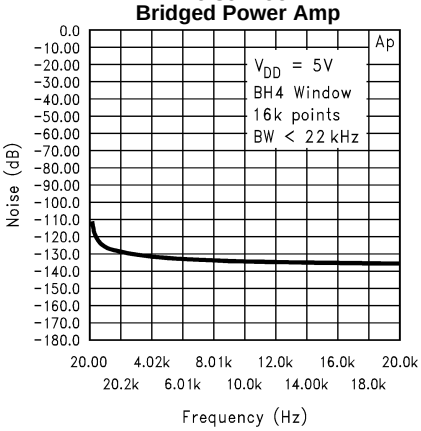

Figure 19.

Noise Floor Line Out/HP Amp

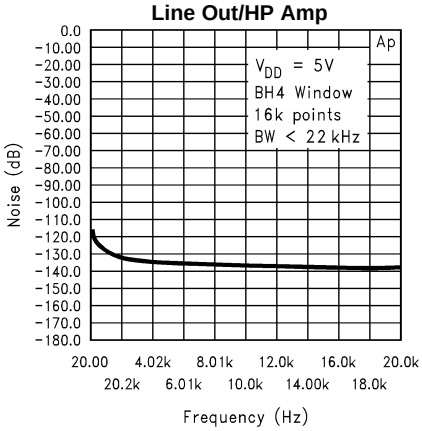

Figure 20.

Noise Floor Mic Preamp

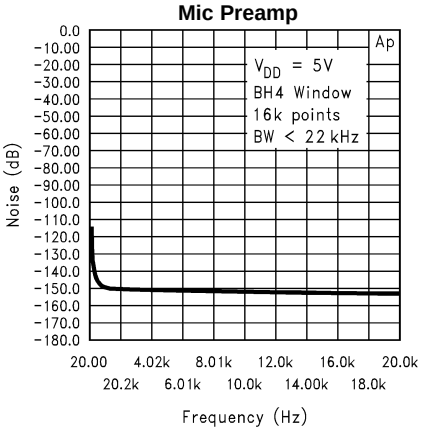

Figure 21.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio Bridged Power Amp

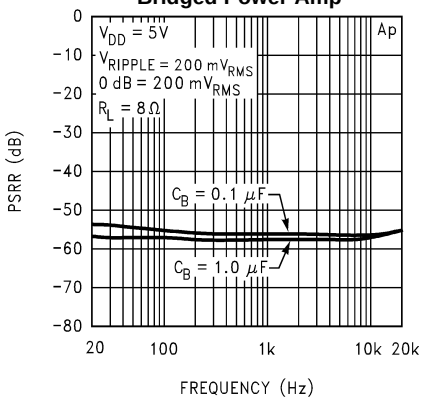

Figure 22.

Power Supply Rejection Ratio Line Out/HP Amplifiers

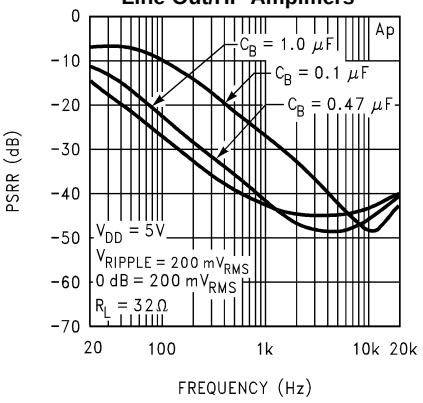

Figure 23.

Power Supply Rejection Ratio Mic Preamp

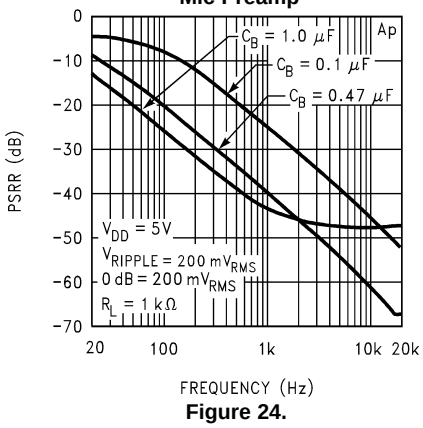

Figure 24.

Power Dissipation vs Output Power Bridged Power Amp

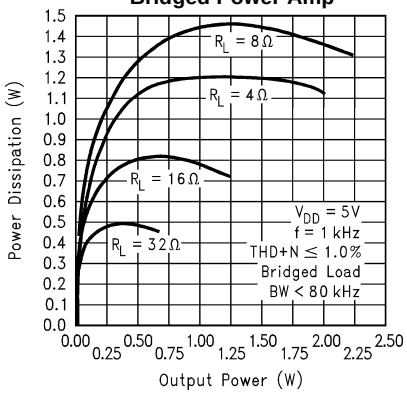

Figure 25.

Power Dissipation vs Output Power Line Out/HP Amplifiers

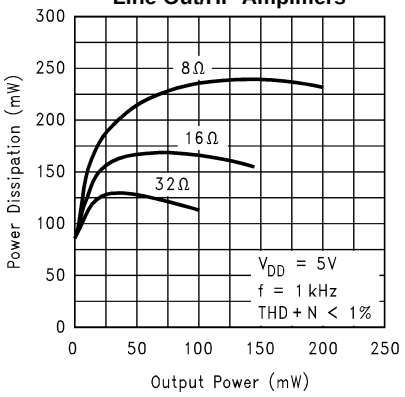

Figure 26.

Low Frequency Enhancement Characteristics Bridged Power Amp

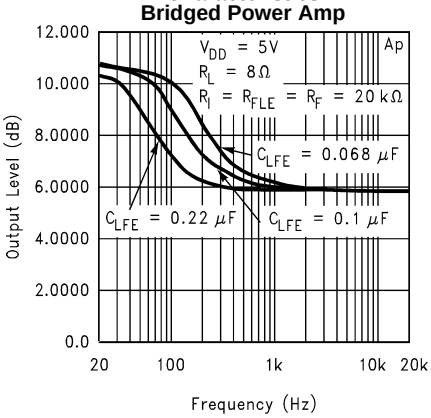

Figure 27.

Typical Performance Characteristics (continued)

Power Derating Curve

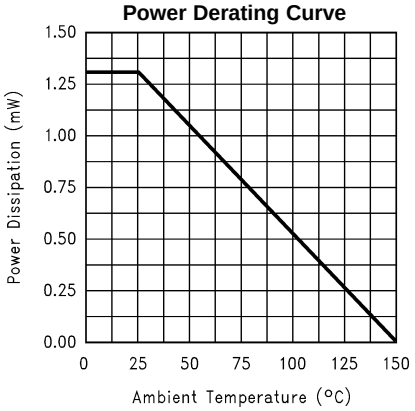

Figure 28.

Open Loop Frequency Response Bridged Power Amp

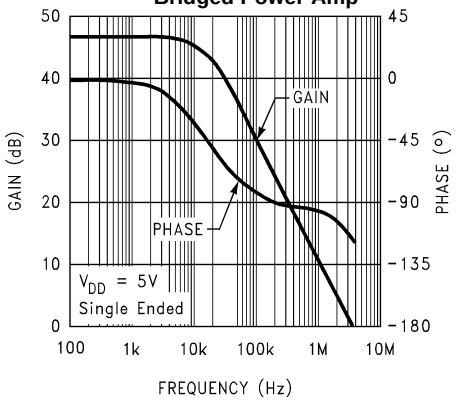

Figure 29.

Crosstalk Line Out/HP Amplifiers

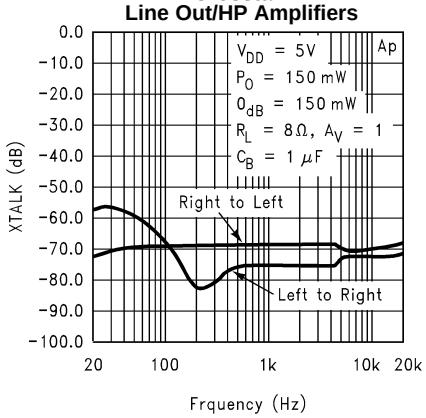

Figure 30.

APPLICATION INFORMATION

BEEP IN FUNCTION

The Beep In pin (pin 14) is a mono input, for system beeps, that is mixed into the left and right input. This Beep In pin will allow an input signal to pass through to the Sum Out and Line/HP output pins. The minimum potential for the input of the Beep In signal is 300mV. Beep in signals less than $300mV_{P-P}$ will not pass through to the output. The beep in circuitry provides left-right signal isolation to prevent crosstalk at the summed input. As shown in the Figure 3, it is required that a resistor and capacitor is placed in series with the Beep In pin and the node tied to V_{DD} through a 100kΩ resistor. The recommended value for the input resistor is between 120kΩ to 10kΩ and the input capacitor is between .22Fμ and .47μF. The input resistor can be changed to vary the amplitude of the beep in signal. Higher values of the input resistor will reduce the amplifier gain and attenuate the beep in signal. In cases where system beeps are required when the system is in a suspended mode, the LM4834 must be brought out of shutdown before the beep in signal is input.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4834 contains a shutdown pin to externally turn off the bias circuitry. The LM4834 will shutdown when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half supply. It is best to switch between ground and the supply V_{DD} to provide maximum device performance. By switching the shutdown pin to V_{DD}, the LM4834 supply current draw will be minimized. While the device will be disabled with shutdown pin voltages less than V_{DD}, the idle current may be greater than the typical value of 0.6 μA.The shutdown pin should not be floated, since this may result in an unwanted shutdown condition.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjuction with an external pull-up resistor. When the switch is closed,the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will shutdown the LM4834. This scheme prevents the shutdown pin from floating.

MODE FUNCTION

The LM4834 was designed to operate in two modes. In mode 0 (lineout mode),where the mode pin (pin 17) is given a logic level low, the attenuation at the Line/HP outputs are fixed at a gain of 1.4. In mode 1 (headphone mode), where the mode pin is given a logic level high, the attenuation of the Line/HP outputs is controlled through the DC voltage at pin 22. The signal levels of the Left and Right Sum Out pins are always controlled by the DC potential at pin 22 regardless of the mode of the IC. In mode 0, pin 5 and pin 24 are line out drivers. In mode 1, pin 5 and pin 24 are headphone drivers.

MUTE FUNCTION

By placing a logic level high on the mute pin (pin 15), the Right and Left Sum Out pins will be muted. If the LM4834 is in the headphone mode, the HP/Line out pins as well as the Sum Out pins are muted. The mute pin must not be floated.

HP SENSE FUNCTION

The LM4834 possesses a headphone sense pin (pin 16) that mutes the bridged amplifier, when given a logic high, so that headphone or line out operation can occur while the bridged connected load will be muted.

Figure 31 shows the implementation of the LM4834's headphone control function using a single-supply.The voltage divider of R1, R2, R4, and R5 sets the voltage at the HP sense pin (pin 16) to be approximately 50 mV when there are no headphones plugged into the system. This logic-low voltage at the HP sense pin enables bridged power amplifier. Resistor R4 limits the amount of current flowing out of the HP sense pin when the voltage at that pin goes below ground resulting from the music coming from the headphone amplifier. Resistor R1, R4, and R5 form a resistor divider that prevents false triggering of the HP sense pin when the voltage at the output swings near the rail, since V_{IH} is about 2.5V.

When a set of headphones are plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors R1, R2, R4, and R5. Resistor R1 then pulls up the HP sense pin, enabling the headphone function and disabling the bridged amplifier. The headphone amplifier then drives the headphones, whoseimpedance is in parallel with resistor R2 and R3. Also shown in Figure 31 are the electrical connections for the headphone jack and plug. A 3-wire plug consists of a Tip, Ring and Sleeve, where the Tip and Ring are signal carrying conductors and the Sleeve is the common ground return. One control pin contact for each headphone jack is sufficient to indicate that the user has inserted a plug into a jack and that another mode of operation is desired.

The LM4834 can be used to drive both a bridged 8Ω internal speaker and a pair of 32Ω speakers without using the HP sense pin. In this case the HP sense is controlled by a microprocessor or a switch.

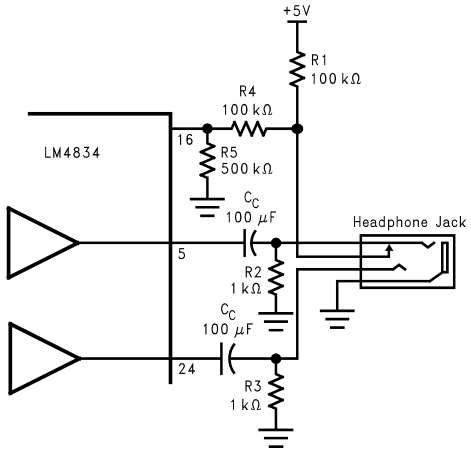

Figure 31. Headphone Input Circuit

DC VOLUME CONTROL

The DC voltage at the DC Volume Control pin (pin 22) determines the attenuation of the Sum Out and Line/HP amplifiers. If the DC potential of pin 22 is at 4V the internal amplifiers are set at a gain of 1.4 (2.9dB). The attenuation of the amplifiers increase until 0V is reached. The attenuator range is from 2.9dB (pin22 = 4V) to -75dB (pin22 = 0V). Any DC voltage greater than 4V will result in a gain of 2.9dB. When the mode pin is given a logic low, the Line/HP amplifier will be fixed at a gain of 2.9dB regardless of the voltage of pin 22. Refer to the Typical Performance Characteristics for detailed information of the attenuation characteristics of the DC Volume Control pin.

MICROPHONE PREAMPLIFIER

The microphone preamplifier is intended to amplify low-level signals. The mic input can be directly connected to a microphone network or to low level signal inputs. The mic amplifier has enough output capability to drive a 1kΩ load. A power supply buffer is included for microphones which require external biasing.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a bridged amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = 4(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

Along with the bridged amplifier, the LM4834 also incorporates two single-ended amplifiers. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

Even with the power dissipation of the bridged amplifier andthe two single-ended amplifiers, the LM4834 does not require heatsinking. The power dissipation from the three amplifiers, must not be greater than the package power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA} \quad (3)$$

For the LM4834 SSOP package, θ_{JA} = 95°C/W and T_{JMAX} = 150°C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 and Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, with an 8Ω bridged load and 32Ω single ended loads, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 82°C provided that device operation is around the maximum power dissipation points. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers.

GROUNDING

In order to achieve the best possible performance, there are certain grounding techniques to be followed. All input reference grounds should be tied with their respective source grounds and brought back to the power supply ground separately from the output load ground returns. Bringing the ground returns for the output loads back to the supply separately will keep large signal currents from interfering with the stable AC input ground references.

LAYOUT

As stated in the GROUNDING section, placement of ground return lines is imperative in maintaining the highest level of system performance. It is not only important to route the correct ground return lines together, but also to be aware of where the ground return lines are routed with respect to each other. The output load ground returns should be physically located as far as possible from low signal level lines and their ground return lines. Critical signal lines are those relating to the microphone amplifier section, since these lines generally work at very low signal levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5 volt regulator with 10 µF and a 0.1 µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4834. The selection of bypass capacitors, especially C_B, is thus dependant upon desired PSRR requirements, click and pop performance as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS system cost, and size constraints. It is also recommended to decouple each of the V_{DD} pins with a 0.1µF capacitor to ground.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4834 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4834 bridged amplifier should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. Both the input coupling capacitor, C_I, and the output coupling capacitor form first order high pass filters which limit low frequency response given in Equation 4 and Equation 5.

$$f_{IC} = 1/(2\pi R_i C_i) \quad (4)$$

$$f_{OC} = 1/(2\pi R_L C_O) \quad (5)$$

These values should be chosen based on required frequency response.

Selection of Input and Output Capacitor Size

Large input and output capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. In many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz–150 Hz. In this case, usinga large input or output capacitor may not increase system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}.) This charge comes from the output through the feedback and is apt to create pops once the device is enabled. By minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

CLICK AND POP CIRCUITRY

The LM4834 contains circuitry to minimize turn-on transients or “click and pops”. In this case, turn-on refers to either power supply turn-on or the device coming out of shutdown mode. When the device is turning on, the amplifiers are internally configured as unity gain buffers. An internal current source ramps up the voltage of the bypass pin. Both the inputs and outputs ideally track the voltage at the bypass pin. The device will remain in buffer mode until the bypass pin has reached its half supply voltage, 1/2 V_{DD}. As soon as the bypass node is stable, the device will become fully operational.

Although the bypass pin current source cannot be modified, the size of the bypass capacitor, C_B, can be changed to alter the device turn-on time and the amount of “click and pop”. By increasing C_B, the amount of turn-on pop can be reduced. However, the trade-off for using a larger bypass capacitor is an increase in the turn-on time for the device. Reducing C_B will decrease turn-on time and increase “click and pop”.

There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for different values of C_B:

C_B	T_{ON}
0.01 µF	20 ms
0.1 µF	200 ms
0.22 µF	420 ms
0.47 µF	840 ms
1.0 µF	2 sec

In order to eliminate “click and pop”, all capacitors must be discharged before turn-on. Rapid on/off switching of the device or shutdown function may cause the “click and pop” circuitry to not operate fully, resulting in increased “click and pop” noise.

In systems where the line out and headphone jack are the same, the output coupling cap, C_O, is of particular concern. $C_O$is chosen for a desired cutoff frequency with a headphone load. This desired cutoff frequency will change when the headphone load is replaced by a high impedance line out load(powered speakers). The input impedance of headphones are typically between 32Ω and 64Ω. Whereas, the input impedance of powered speakers can vary from 1kΩ top 100kΩ. As the RC time constant of the load and the output coupling capacitor increases, the turn off transients are increased.

To improve click and pop performance in this situation, external resistors R6 and R7 should be added. The recommended value for R6 is between 150Ω to 1kΩ. The recommended value for R7 is between 100Ω to 500Ω. To achieve virtually clickless and popless performance R6 = 150Ω, R7 = 100Ω, C_O = 220µF, and C_B = 0.47µF should be used. Lower values of R6 will result in better click and pop performance. However, it should be understood that lower resistance values of R6 will increase quiescent current.

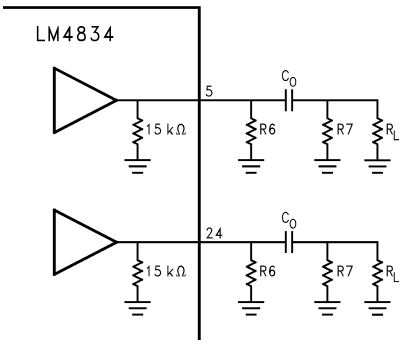

Figure 32. Resistors for Varying Output Loads

LOW FREQUENCY ENHANCEMENT

In some cases, a designer may want to improve the low frequency response of the bridged amplifier. This low frequency boost can be useful in systems where speakers are housed in small enclosures. A resistor, R_{LFE}, and a capacitor, C_{LFE}, in parallel, can be placed in series with the feedback resistor of the bridged amplifier as seen in Figure 33.

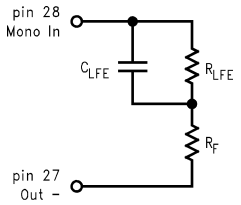

Figure 33. Low Frequency Enhancement

At low frequencies the capacitor will be virtually an open circuit. At high frequencies the capacitor will be virtually a short circuit. As a result of this, the gain of the bridge amplifier is increased at low frequencies. A first order pole is formed with a corner frequency at:

$$f_c = 1/(2\pi R_{LFE} C_{LFE}) \quad (6)$$

The resulting low frequency differential gain of this bridged amplifier becomes:

$$2(R_f + R_{LFE}) / R_i = A_{vd} \quad (7)$$

With R_F = 20kΩ, R_{LFE} = 20kΩ, and C_{LFE} = 0.068 µF, a first order pole is formed with a corner frequency of 120 Hz. At low frequencies the differential gain will be 4, assuming R_S = 20k. The low frequency boost formulas assume that C_O, C_i, f_{IC}, f_{OC} allow the appropriate low frequency response.

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