# LMD18400 Quad High Side Driver

**Check for Samples: LMD18400**

## FEATURES

- **Four Independent Outputs with >3A Peak, 1A Continuous Current Capability**
- **1.3Ω Maximum ON Resistance Over Temperature**
- **True Instantaneous Power Limit for Each Switch**
- **High Survival Voltage (60 $V_{DC}$, 80V Transient)**
- **Shorted Load (to Ground and Supply) Protection**
- **Overvoltage Shutdown at $V_{CC}$ > 35V**
- **LS TTL/CMOS Compatible Logic Inputs and Outputs**
- **<10 µA Supply Current in "Sleep" Mode**
- **−5V Output Clamp for Discharging Inductive Loads**
- **Serial Data Interface for 11 Diagnostic Checks:**
  - **Switch ON/OFF Status**
  - **Open or Shorted Load**
  - **Operating Temperature**
  - **Excessive Supply Voltage**
- **Two Direct-output Error Flags**

## APPLICATIONS

- **Relay and Solenoid Drivers**
- **High Impedance Automotive Fuel Injector Drivers**
- **Lamp Drivers**
- **Power Supply Switching**
- **Motor Drivers**

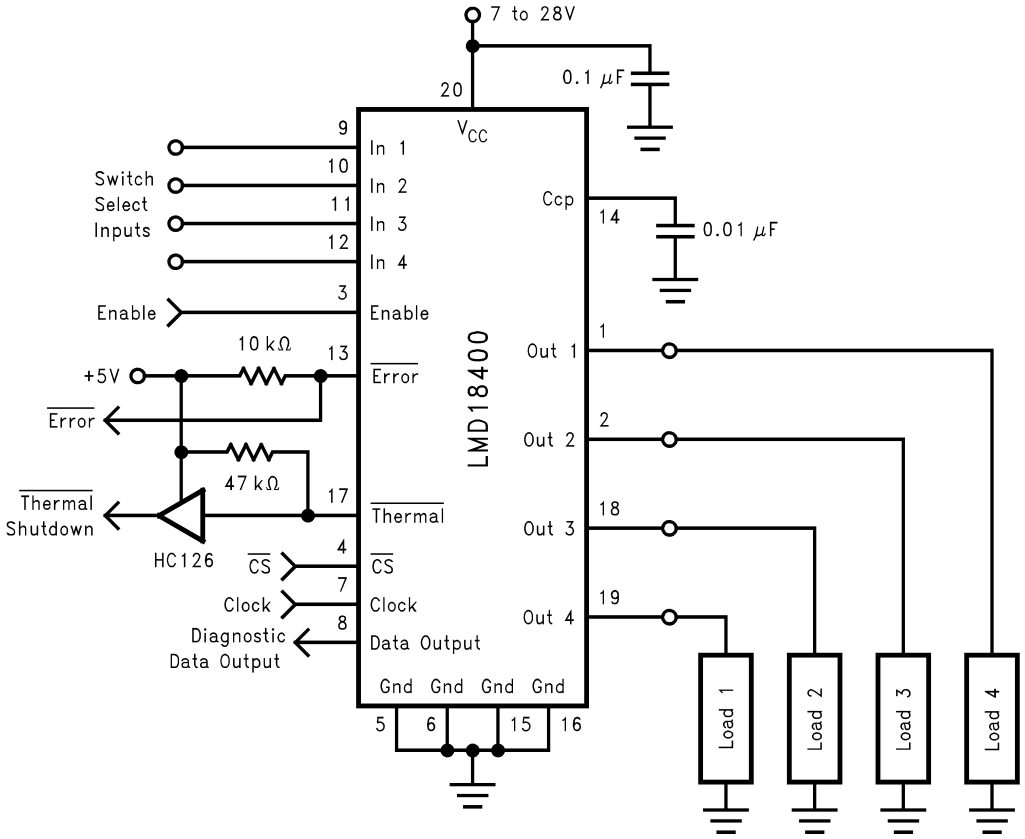
## DESCRIPTION

The LMD18400 is a fully protected quad high side driver. It contains four common-drain DMOS N-channel power switches, each capable of switching a continuous 1 Amp load (>3 Amps transient) to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The device can be disabled to produce a "sleep" condition reducing the supply current to less than 10 µA. Separate ON/OFF control of each switch is provided through standard LSTLL/CMOS logic compatible inputs.

A MICROWIRE compatible serial data interface is built in to provide extensive diagnostic information. This information includes switch status readback, output load fault conditions and thermal and overvoltage shutdown status. There are also two direct-output error flags to provide an immediate indication of a general system fault and an indication of excessive operating temperature.

The LMD18400 is packaged in a special power dissipating leadframe that reduces the junction to case thermal resistance to approximately 20°C/W.

## Typical Application




## Connection Diagram

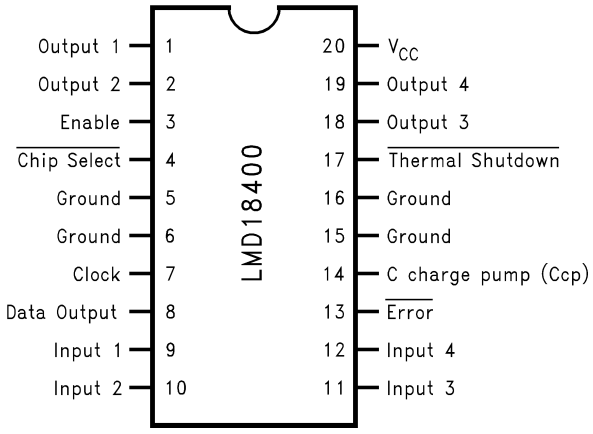



**Figure 1. See Package Number NFH0020A**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | |
|---|---|
| Supply Survival Voltage (Pin 20) | |
| Transient (t = 10 ms) | 80V |
| Continuous | −0.5V to +60V |
| Output Transient Current (Each Switch) | 3.75A |
| Output Transient Current (Total, All Switches) | 6A |
| Output Steady State Current (Each Switch) | 1A |
| Logic Input Voltage (Pins 3, 9, 10, 11, 12) | −0.3V to +16V |
| Logic Input Voltage (Pins 4, 7) | −0.3V to +6V |
| Error Flag Voltage | 16V |
| ESD Susceptibility (3) | 2000V |
| Power Dissipation (4) | 5W Internally Limited |
| Junction Temperature ($T_{JMAX}$150°C) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +260°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model; 100 pF discharge through a 1.5 kΩ resistor. All pins except pins 8 and 13 which are protected to 1000V and pins 1, 2, 18 and 19 which are protected to 500V.
(4) The maximum power dissipation is a function of $T_{JMAX}$, $\theta_{JA}$, and $T_A$ and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX}–T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will eventually go into thermal shutdown. For the LMD18400 the junction-to-ambient thermal resistance, $\theta_{JA}$, is 60°C/W. With sufficient heatsinking the maximum continuous power dissipation for the package will be, $I_{DCMAX}^2 \times R_{ON(MAX)} \times 4$ switches $1A^2 \times 1.3\Omega \times 4 = 5.2W$).

## OPERATING RATINGS(1)

| | |
|---|---|
| Ambient Temperature Range ($T_A$) | −25°C to +85°C |
| Supply Voltage Range | 7V to 28V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 12V, $C_{CP}$ = 0.01 µFd, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −25°C ≤ $T_A$ ≤ +85°C, all other limits are for $T_A = T_J$ = +25°C.

| Parameter | Conditions | Typical (1) | Limit (2) | Units (Limit) |
|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | |
| Supply Current | Enable Input = 0V | 0.04 | 10 | µA (Max) |
| | Enable Input = 5V, Inputs = 0V | 7.5 | 15 | mA (Max) |
| | Enable Input = 5V, Inputs = 5V Open Loads | 7.5 | 15 | mA (Max) |

(1) Typical values are at $T_J$ = +25°C and represent the most likely parametric norm.
(2) All limits are 100% production tested at +25°C. Limits at temperature extremes are specified through correlation and accepted Statistical Quality Control (SQC) methods.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{CC}$ = 12V, $C_{CP}$ = 0.01 µFd, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −25°C ≤ $T_A$ ≤ +85°C, all other limits are for $T_A$ = $T_J$ = +25°C.

| Parameter | Conditions | Typical (1) | Limit (2) | Units (Limit) |
|---|---|---|---|---|
| Output Leakage | Enable Input = 0V, Inputs = 0V (Pins 1, 2, 18, 19) | 0.01 | 300 | µA (Max) |
| Rds ON | $I_{OUT}$ = 1A, (3) | 0.8 | **1.3** | Ω (Max) |
| Short Circuit Current | $V_{CC}$ = 12V, (3) | 1.2 | 0.6 | A (Min) |
| | $V_{CC}$ = 7V, (3) | 2.4 | | A |
| | $V_{CC}$ = 28V, (3) | 0.6 | | A |
| Maximum Output Current | $V_{CC}$ − $V_O$ = 4V, (3) | 3.75 | | A |
| Lead Error Threshold Voltage | Pins 1, 2, 18, 19 | 4.1 | | V |
| Open Load Detection Current | Pins 1, 2, 18, 19 | 150 | | µA |
| Negative Clamp Output Voltage | $I_O$ = 1A, (3) | −5 | | V |
| Overvoltage Shutdown Threshold | | 31 | 40 | V (Max) |
| Overvoltage Shutdown Hysteresis | | 0.75 | | V |
| Error Output Leakage Current | $V_{PIN\ 13}$ = 12V | 0.001 | 10 | µA (Max) |
| Thermal Warning Temperature | $V_{PIN\ 13}$ < 0.8V | 145 | | °C |
| Thermal Shutdown Temperature | $V_{PIN\ 17}$ < 0.8V | 170 | | °C |
| Thermal Warning Temperature | $V_{PIN\ 13}$ < 0.8V | 145 | | °C |
| **AC CHARACTERISTICS** | | | | |
| Switch Turn-On Delay ($t_{d(ON)}$) | Enable (Pin 3) = 5V, $I_{OUT}$ = 1A | 5 | 10 | µs (Max) |
| Switch Turn-On Rise Time ($t_{ON}$) | $I_{OUT}$ = 1A | 7 | 15 | µs (Max) |
| Switch Turn-Off Delay ($t_{d(OFF)}$) | Enable (Pin 3) = 5V, $I_{OUT}$ = 1A | 0.5 | 2 | µs (Max) |
| Switch Turn-Off Fall Time ($t_{OFF}$) | $I_{OUT}$ = 1A | 0.15 | 1 | µs (Max) |
| Enable Time ($t_{EN}$) | Measured with Switch 1, Pin 9 = 5V | 30 | 50 | µs (Max) |
| Error Reporting Delay ($t_{Error}$) | Enable (Pin 3) = 5V, Switch 1 Load Opened | 75 | 150 | µs (Max) |
| Data Setup Time ($t_{DS}$) | $C_L$ = 30 pF | 200 | 500 | ns (Min) |
| TRI-STATE Control ($t_{1H}$, $t_{OH}$) | Pin 8, Hi-Z Enable Time | 2 | | µs |
| Data Clock Frequency | | 3 | 1 | MHz (Max) |
| **DIGITAL CHARACTERISTICS** | | | | |
| Logic “1” Input Voltage | Pins 3, 4, 7, 9, 10, 11, 12 | | **2.0** | V (Min) |
| Logic “0” Input Voltage | Pins 3, 4, 7, 9, 10, 11, 12 | | **0.8** | V (Max) |
| Logic “1” Input Current | Pins 4, 7 | 0.001 | **1** | µA (Max) |
| Logic “0” Input Current | Pins 4, 7 | −0.001 | **−1** | µA (Max) |
| TRI-STATE Output Current | Pin 8, Pin 4 = 5V | 0.05 | 10 | µA (Max) |
| | Pin 8 = 0V | −0.05 | −10 | µA (Max) |
| Enable Input Current | Pin 3 = 2.4V | 12 | **25** | µA (Max) |
| Channel Input Resistance | Pins 9, 10, 11, 12 | 75 | **15** | kΩ (Min) |
| Error Output Sink Current | Pin 13 = 0.8V | 4 | **1.6** | mA (Min) |
| Logic “1” Output Voltage | Pin 8 | | | |
| | $I_{OUT}$ = −360 µA | 4.4 | **2.4** | V (Min) |
| | $I_{OUT}$ = −10 µA | 5.1 | **4.5** | V (Min) |
| | $I_{OUT}$ = −10 µA | | **5.5** | V (Min) |
| Logic “0” Output Voltage | Pin 8 $I_{OUT}$ = 100 µA | | **0.4** | V (Max) |
| Thermal Shutdown Output Source Current | Pin 17 = 2.4V | 5 | 3 | µA (Min) |
| Thermal Shutdown Output Sink Current | Pin 17 = 0.8V | 360 | 250 | µA (Min) |

(3) Pulse Testing techniques used. Pulse width is < 5 ms with a duty cycle < 1%.

## TIMING SPECIFICATION DEFINITIONS

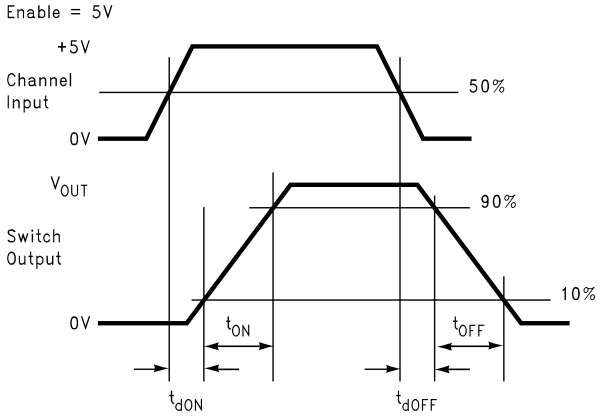



**Figure 2. Switching Turn ON/OFF**

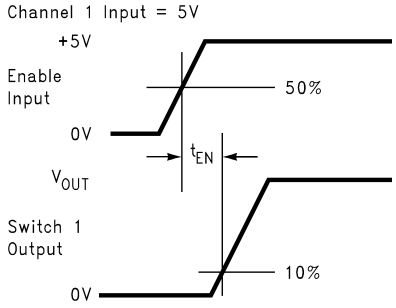



**Figure 3. Enable Turn-On**

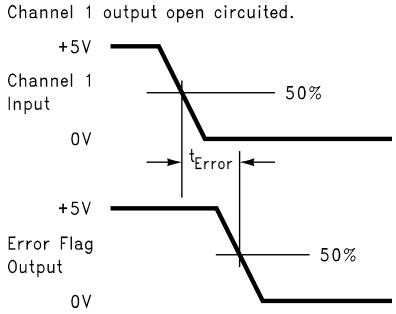



**Figure 4. Error Reporting Delay**

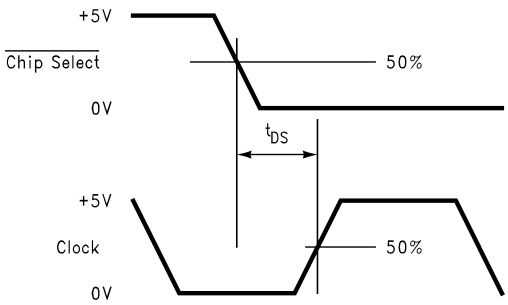



**Figure 5. Data Setup Time**

## TYPICAL PERFORMANCE CHARACTERISTICS

For all curves, $V_{CC}$ = 12V, Temperature is the junction temperature unless otherwise noted.

**Switch ON Resistance vs Temperature**

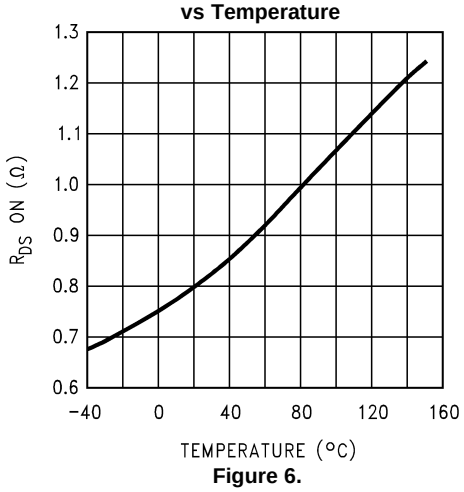



**Figure 6.**

**"Sleep Mode" Supply Current vs Temperature**

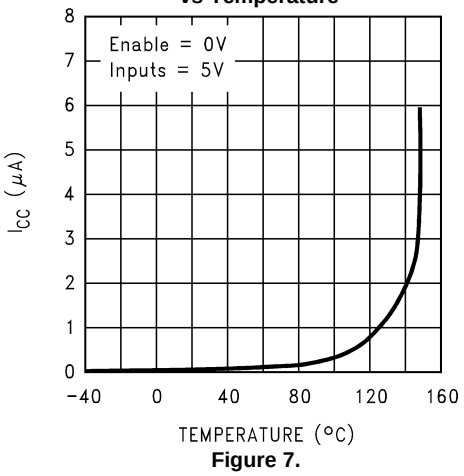



**Figure 7.**

**Maximum Power Dissipation vs Ambient Temperature**

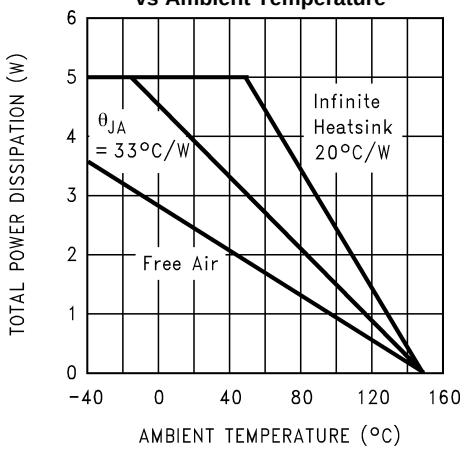



**Figure 8.**

**Short Circuit Current vs Temperature**

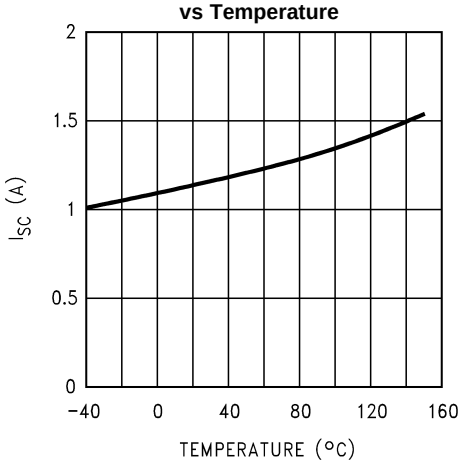



**Figure 9.**

**Clamp Characteristics vs Temperature**

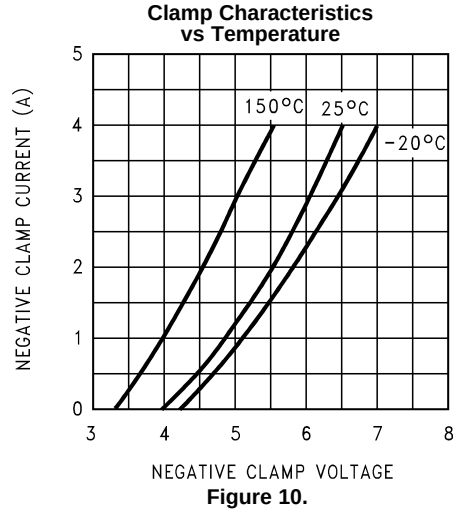



**Figure 10.**

**Error Sense Threshold Voltage vs Temperature**

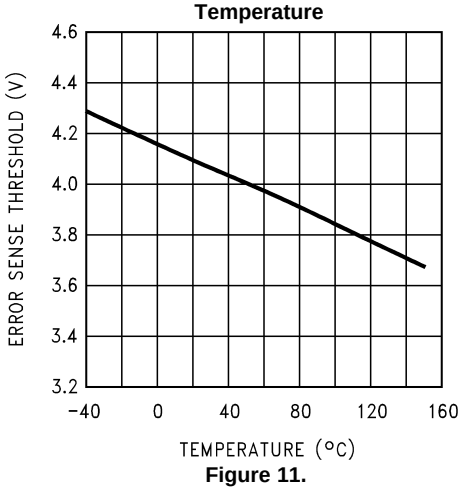



**Figure 11.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For all curves, $V_{CC}$ = 12V, Temperature is the junction temperature unless otherwise noted.

**Turn ON Rise Time vs Temperature**

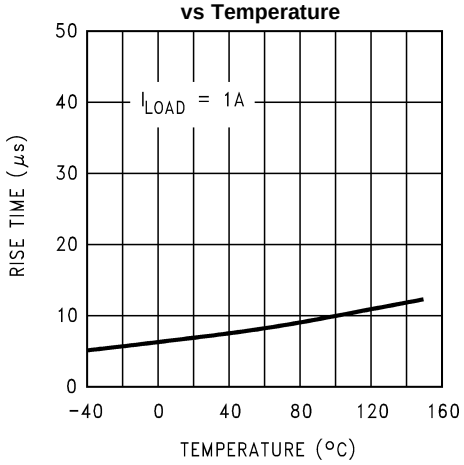



**Figure 12.**

**Turn ON Delay Time vs Temperature**

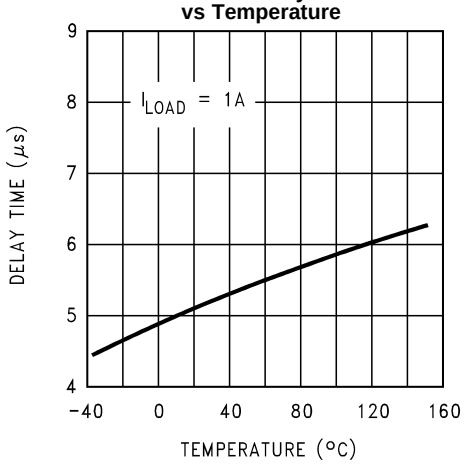



**Figure 13.**

**Turn OFF Time vs Temperature**

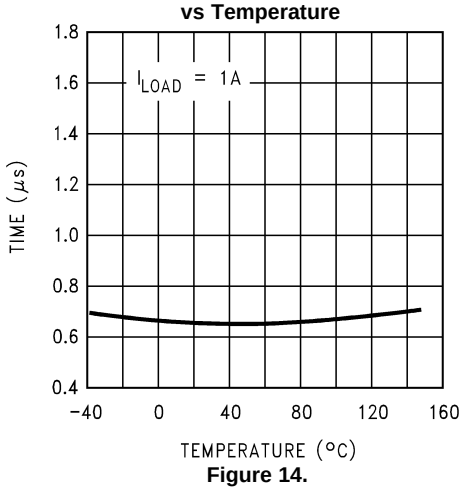



**Figure 14.**

**Switch Select Logic Input Resistance vs Temperature**

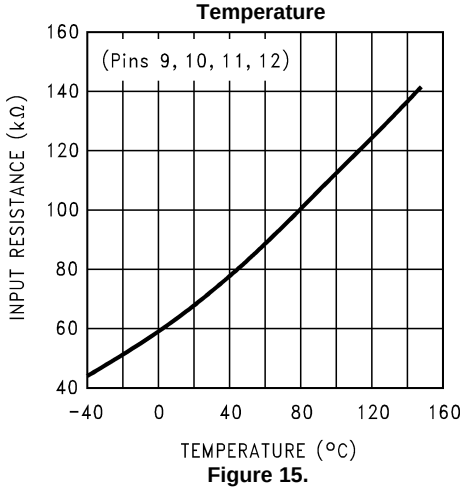



**Figure 15.**

**Enable Threshold Voltage vs Temperature**

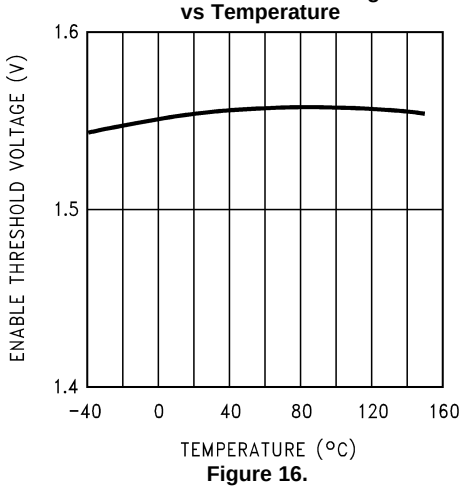



**Figure 16.**

**Error Output Voltage vs Sink Current**

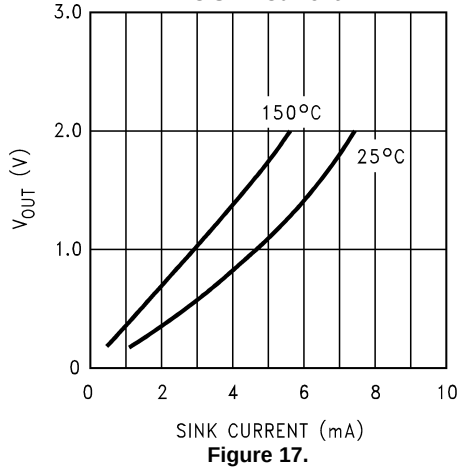
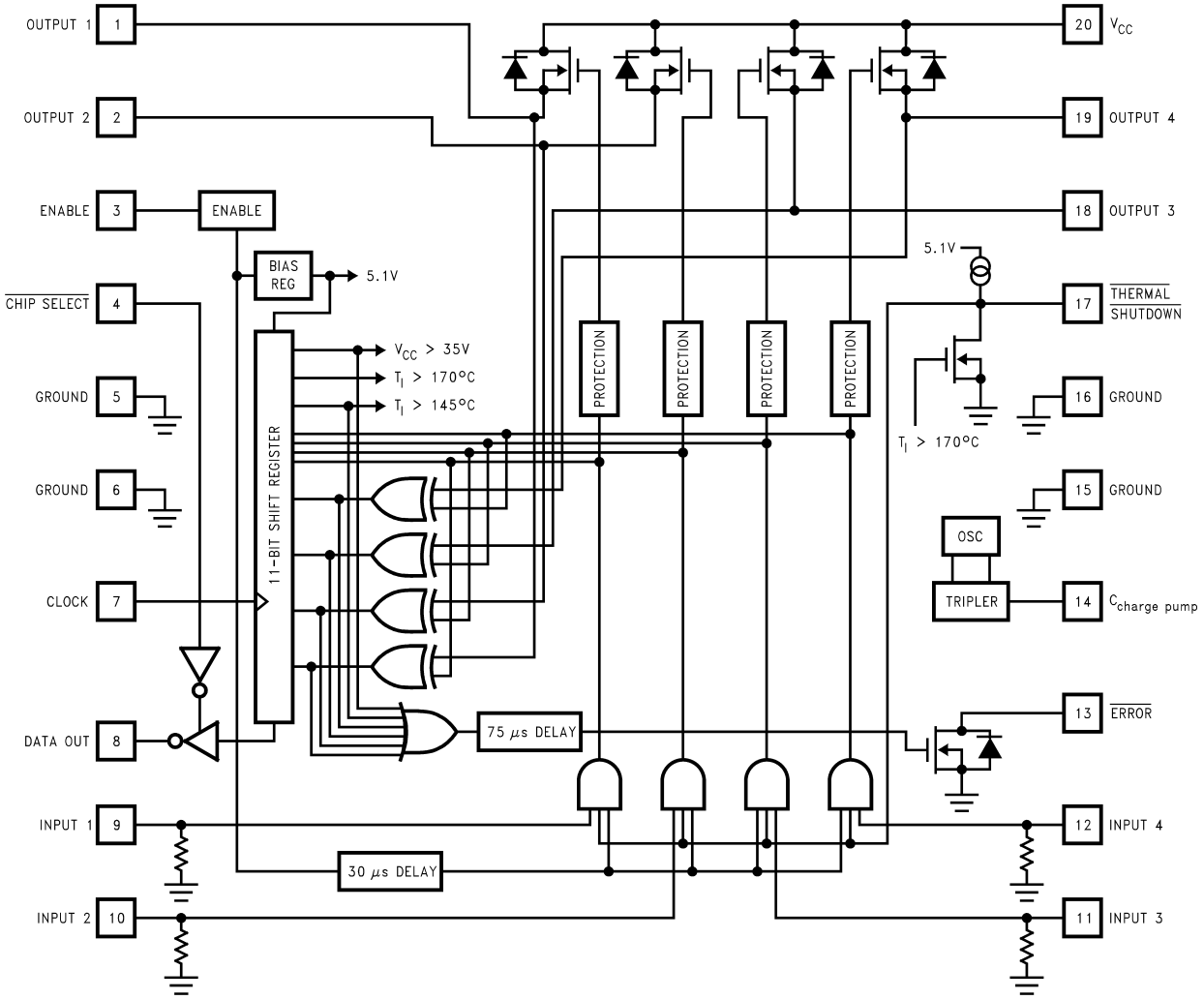



**Figure 17.**

## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| Enable Input (Pin 3) | Chip Select Input (Pin 4) | Switch Control Input (Pins 9, 10, 11, 12) | Error Output (Pin 13) | Thermal SD Output (Pin 17) | Conditions |
|---|---|---|---|---|---|
| 0 | X | X | 1 | 0 | "Sleep" Mode, $I_{SUPPLY}$ < 10 µA |
| 1 | X | 0 | 1 | 1 | Selected Switch is OFF |
| 1 | X | 1 | 1 | 1 | Selected Switch is ON, Normal Operation |
| 1 | X | 0 | 0 | 1 | Switch is OFF but:<br>a. Load is Open Circuited, or<br>b. Load is Shorted to $V_{CC}$, or<br>c. $T_J$ > +145°C, or<br>d. $V_{CC}$ > +35V |
| 1 | X | 1 | 0 | 1 | Switch is ON, but:<br>a. Load is Shorted to Ground, or<br>b. Switch is in Power Limit, or<br>c. $T_J$ > +145°C, or<br>d. $V_{CC}$ > +35V and Switch is Actually OFF |
| 1 | X | 1 | 0 | 0 | $T_J$ > +170°C, All Switches are OFF |
| 1 | 1 | X | X | X | Data Output Pin is TRI-STATE |
| 1 | 0 | X | X | X | Data Output Pin is Enabled and Ready to Output Diagnostic Information |

# APPLICATIONS INFORMATION

## BASIC OPERATION

High-side drivers are used extensively in automotive and industrial applications to switch power to ground referred loads. The major advantage of using high-side drive, as opposed to low-side drive, is to protect the load from being energized in the event that the load drive wire is inadvertently shorted to ground as shown in Figure 18. A high-side driver can sense a shorted condition and open the power switch to disable the load and eliminate the excessive current drain on the power supply. The LMD18400 can control and protect up to four separate ground referenced loads.

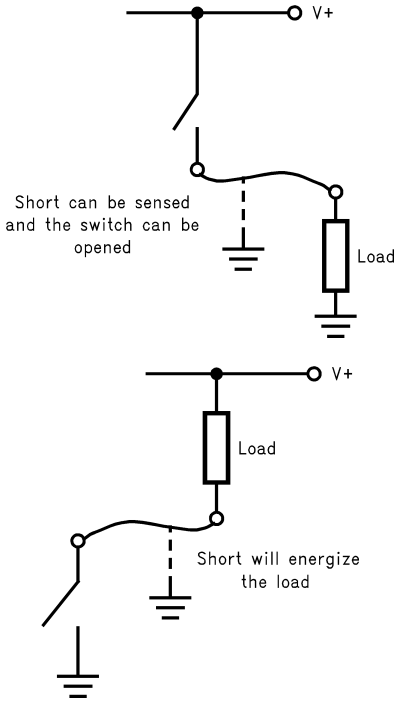



**Figure 18. High-Side vs Low-Side Drive**

The LMD18400 combines low voltage CMOS logic control circuitry with a high voltage DMOS process. Each DMOS power switch has an individual ON/OFF control input. When commanded ON, the output of the switch will connect the load to the $V_{CC}$ supply through a maximum resistance of 1.3Ω (the ON resistance of the DMOS switch). The voltage applied to the load will depend upon the load current and the designed current capability of the LMD18400. When a switch is commanded OFF, the load will be disconnected from the supply except for a small leakage current of typically less than 0.01 µA.

The LMD18400 can be continually connected to a live power source, a car battery for example, while drawing less than 10 µA from the power source when put into a “sleep” condition. This “sleep” mode is enacted by taking the Enable Input (pin 3) low. During this mode the supply current for the device is typically only 0.04 µA. Special low current consumption standby circuitry is used to hold the DMOS switches OFF to eliminate the possibility of supply voltage transients from turning on any of the loads (a common problem with MOS power devices). When in the “sleep” mode, all diagnostic and logic circuitry is inactive. When the Enable Input is taken to a logic 1, the switches become “armed” and ready to respond to their control input after a short, 30 µs, enable delay time. This delay interval prevents the switches from transient turn-on. Figure 19 shows the switch control logic.

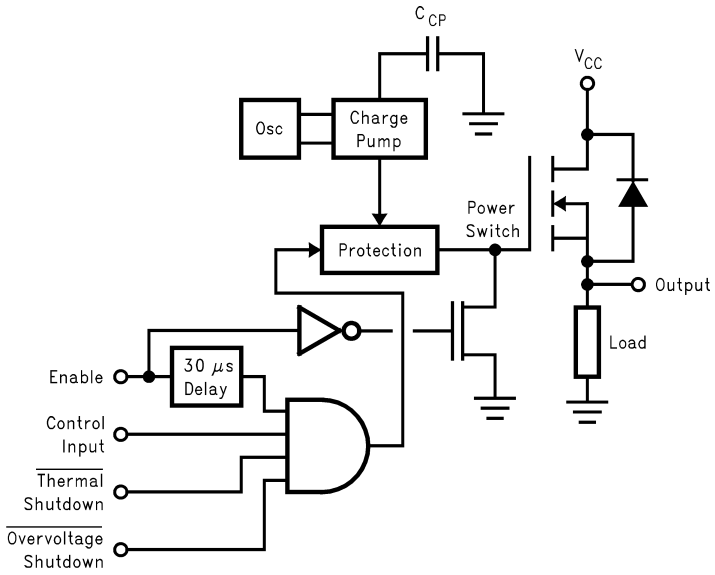



**Figure 19. Control Logic for Each Power Switch**

Each DMOS switch is turned ON when its gate is driven approximately 3.5V more positive than its source voltage. Because the source of the switch is the output terminal to the load it can be taken to a voltage very near the $V_{CC}$ supply potential. To ensure that there is sufficient voltage available to drive the gates of the DMOS device a charge pump circuit is built in. This circuit is controlled by an internal 300 kHz oscillator and using an external 10 nF capacitor connected from pin 14 to ground generates a voltage that is approximately 20V greater than the $V_{CC}$ supply voltage. This provides sufficient gate voltage drive for each of the switches which is applied under command of standard 5V logic input levels.

The turn-on time for each switch is approximately 12 µs when driving a 1A load current. This relatively slow switching time is beneficial in minimizing electromagnetic interference (EMI) related problems created from switching high current levels.

## PROTECTION CIRCUITRY

The LMD18400 has extensive protection circuitry built in. With any power device, protection against excessive voltage, current and temperature conditions is essential. To achieve a “fail-safe” system implementation, the loads are deactivated automatically by the LMD18400 in the event of any detected overvoltage or over-temperature fault conditions.

### Voltage Protection

The $V_{CC}$ supply can range from −0.5V to +60 $V_{DC}$ without any damage to the LMD18400. The CMOS logic circuitry is biased from an internal 5.1V regulator which protects these lower voltage transistors from the higher $V_{CC}$ potentials. In order to protect the loads connected to the switch outputs however, an overvoltage shutdown circuit is employed. Should the $V_{CC}$ potential exceed 35V all of the switches are turned OFF thereby disconnecting the loads. This 35V threshold has 750 mV of hysteresis to prevent potential oscillations.

Additionally, there is an undervoltage lockout feature built in. With $V_{CC}$ less than 5V it becomes uncertain whether the logic circuitry can hold the switches in their commanded state. To avoid this uncertainty, all of the switches are turned OFF when $V_{CC}$ drops below approximately 5V. Figure 20 illustrates the shutoff of an output during a 0V to 80V $V_{CC}$ supply transient.

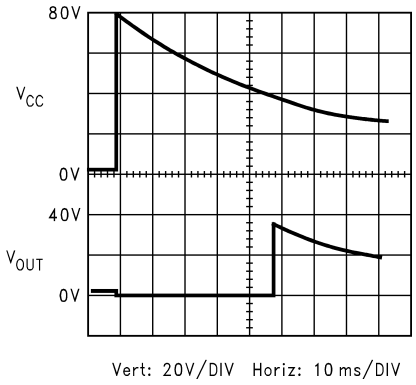



**Figure 20. Overvoltage/Undervoltage Shutdown**

The LMD18400 has been designed to drive all types of loads. When driving a ground referenced inductive load such as a relay or solenoid, the voltage across the load will reverse in polarity as the field in the inductor collapses when the power switch is turned OFF. This will pull the output pin of the LMD18400 below ground. This negative transient voltage is clamped at approximately −5V to protect the IC. This clamping action is not done with diodes but rather the power DMOS switch turning back on momentarily to conduct the inductor current as it de-energizes as shown in Figure 21.

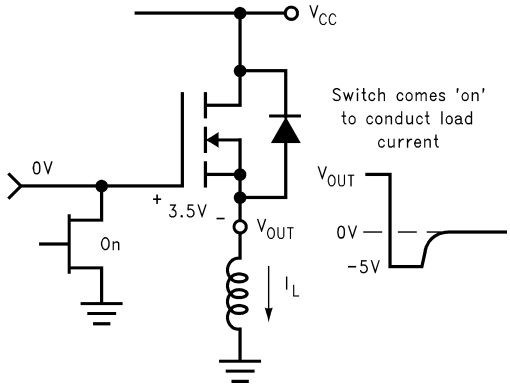



**Figure 21. Turn-OFF Conditions with an Inductive Load**

When the output inductance produces a negative voltage, the gate of the DMOS transistor is clamped at 0V. At −3.5V, the source of the power device is less than the gate by enough to cause the switch to turn ON again. During this negative transient condition the power limiting circuitry to protect the switch is disabled due to the gate being held at 0V. The maximum current during this clamping interval, which is equal to the steady state ON current through the inductor, should be kept less than 1A. Another concern during this interval has to do with the size of an inductive load and the amount of time required to de-energize it. With larger inductors it may be possible for the additional power dissipation to cause the die temperature to exceed the thermal shutdown limit. If this occurs all of the other switches will turn OFF momentarily (see section on THERMAL MANAGEMENT).

### Power Limiting

The LMD18400 utilizes a true instantaneous power limit circuit rather than simple current limiting to protect each switch. This provides a higher transient current capability while still maintaining a safe power dissipation level. The power dissipation in each switch (the product of the Drain-to-Source voltage and the output current, $V_{ds} \times I_{OUT}$) is continually monitored and limited to 15W by varying the gate voltage and therefore the ON resistance of the switch. Basically the ON resistance will be as low as possible until 15W is being dissipated. To maintain 15W, the ON resistance increases to reduce the load current. This results in a decrease of the output voltage. For resistive loads, the output voltage when in power limit will be:

$$V_{OUT}\ (\text{in Power Limit}) = \frac{V_{CC} - \sqrt{V_{CC}^{\,2} - 60\,R_L}}{2} \quad (1)$$

This provides a maximum transient current, and drain-to-source voltage characteristic as shown in Figure 22.

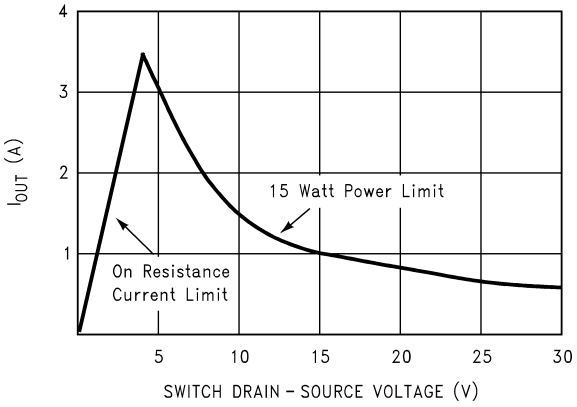



**Figure 22. Maximum Output Current with Instantaneous Power Limiting**

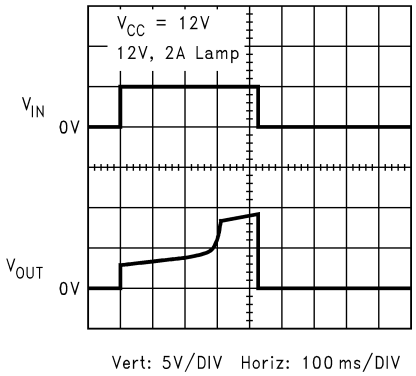



**Figure 23. Driving a Lamp / Soft Turn-On of a Lamp Load**

The steady state current to the load is limited by the package power dissipation, ambient temperature and the ON resistance of the switch which has a positive temperature coefficient as shown in the Typical Performance Characteristics.

This dynamic current limiting of the switches is beneficial when driving lamp and large capacitive loads. Lamps require a large inrush current, on the order of 10 times the normal operating current, when first switched on with a cold filament. The LMD18400 will limit this initial current to the level where 15W is dissipated in the switch. As the filament warms up the voltage across the lamp increases thereby decreasing the voltage across the switch which permits more current to fully light the lamp. With limited inrush current the lifetime of a lamp load is increased significantly. Figure 23 illustrates the soft turn-on of a lamp load.

The same principle of increasing output current as the voltage across the load increases allows large capacitive loads to be charged more quickly by an LMD18400 driver than as opposed to a driver with a fixed 1A current limit protection scheme. Figure 24 shows the output response while driving a large capacitive load.

### Thermal Protection

The die temperature of the LMD18400 is continually monitored. Should any conditions cause the die temperature to rise to +170°C, all of the power switches are turned OFF automatically to reduce the power dissipation. It is important to realize that the thermal shutdown affects all four of the switches together. That is, if just one switch load is enough to heat the die to the thermal shutdown threshold, all of the other switches, regardless of their power dissipation conditions, will be switched OFF. All of the switches will be re-enabled when the die temperature has cooled to approximately +160°C. Until the high temperature forcing conditions have been removed the switches will cycle ON and OFF thus maintaining an average die temperature of +165°C. The LMD18400 will signal that excessive temperatures exist through several diagnostic output signals (see DIAGNOSTICS).

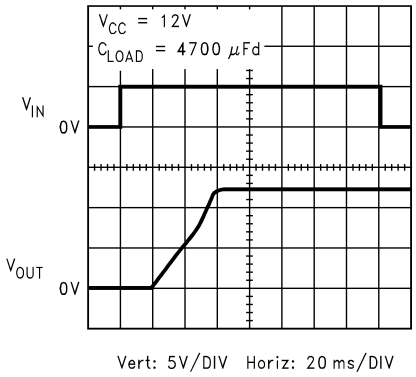



**Figure 24. Driving a Large Capacitive Load**

## DIAGNOSTICS

The LMD18400 has extensive circuit diagnostic information reporting capability. Use of this information can produce systems with intelligent feedback of switch status as well as load fault conditions for troubleshooting purposes. All of the diagnostic information is contained in an 11-bit word. This data can be clocked out of the LMD18400 in a serial fashion as shown in Figure 25. The shift register is parallel loaded with the diagnostic data whenever the Chip Select input is at a Logic 1 and changes to the serial shift mode when Chip Select is taken to a Logic 0. The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is specified to be at least 2.4V with a 360 µA load.

The data interface is MICROWIRE compatible in that data is clocked out of the LMD18400 on the falling edge of the clock, to be clocked into the controlling microprocessor on the rising edge. Any number of devices can share a common data output line because the data output pin is held in a high impedance (TRI-STATE) condition until the device is selected by taking its Chip Select Input low. Following Chip Select going low there is a short data setup time interval (500 ns Min) required. This is necessary to allow the first data bit of information to be established on the data output line prior to the first rising clock edge which will input the data bit into the controller. When all 11 bits of diagnostic data have been shifted out the data output goes to a Logic 1 level until the Chip Select line is returned high.

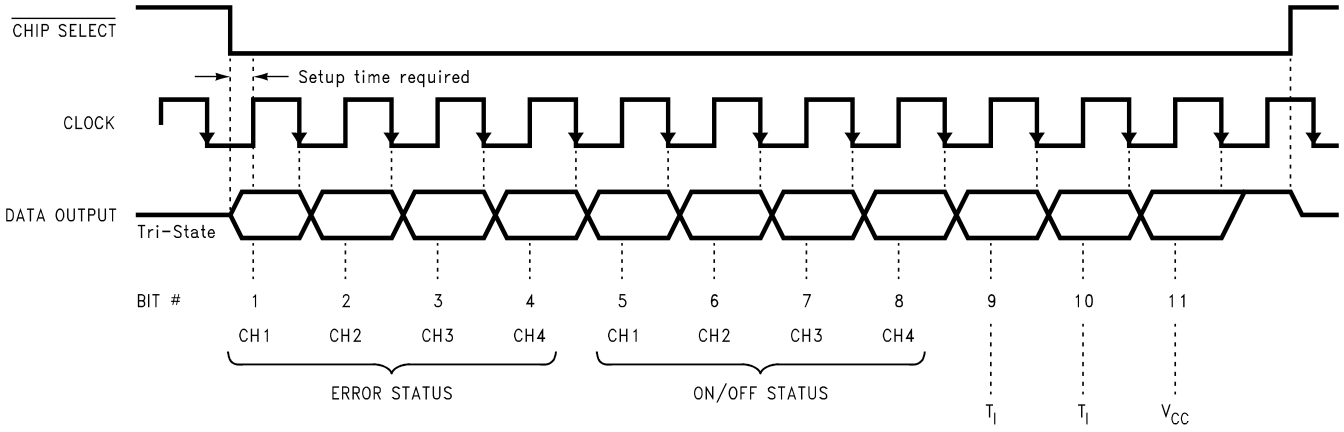
Figure 25 also indicates the significance of the diagnostic data bits. The first 4 bits indicate an output load error condition, one for each channel in succession (see LOAD ERROR DETECTION).

Bits 5 through 8 provide a readback of the commanded ON/OFF status of each switch.

A unique feature of the LMD18400 is that it provides an early warning of excessive operating temperature. Should the die temperature exceed +145°C, bit 9 will be set to a Logic 0. Acting on this information a system can be programmed to take corrective action, shutting OFF specific loads perhaps, while the LMD18400 is still operating normally (not yet in thermal shutdown). If this early warning is ignored and the device continues to rise in temperature, the thermal shutdown circuitry will come into action at a die temperature of +170°C. Should this occur bit 10 of the diagnostic data stream will be set to a Logic 0 indicating that the device is in thermal shutdown and all of the outputs have been shut OFF.

The final data bit, bit 11, indicates an overvoltage condition on the $V_{CC}$ supply ($V_{CC}$ is greater than 35V) and again indicates that all of the drivers are OFF.

The diagnostic data can be read periodically by a controller or only in the event of a general system error indication to determine the cause of any system problem. This general indication of a fault is provided by an Error Flag output (pin 13). This pin goes low whenever any type of error is detected. There is a built-in delay of approximately 75 µs from the time an error is detected until pin 13 is taken low. This is to help mask short duration error conditions such as may be caused by driving highly capacitive loads (>2 µF). A lamp load may generate a shorted load error for several hundred milliseconds as it turns on which should be ignored.




| | | | | | |
|---|---|---|---|---|---|
| LOGIC 1 | LOAD OK | SWITCH OFF | <145°C | <170°C | <35V |
| LOGIC 0 | LOAD ERROR | SWITCH ON | >145°C | >170°C | >35V |

**Figure 25. Serial Diagnostic Data Assignments**

The Error Flag output pin is an open drain transistor which requires a pull-up resistor to a positive voltage of up to 16V. Typically this pull-up is to the same 5V supply which is biasing the Enable input and any other external logic circuitry. The Error Flag pins of several LMD18400 packages can be connected together with just one pull-up resistor to provide an all-encompassing general system error indication. Upon detection of an error, each device could then be polled for diagnostic information to determine the source of the fault condition.

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached +170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 µA) current source so use of a buffer on this pin is recommended.

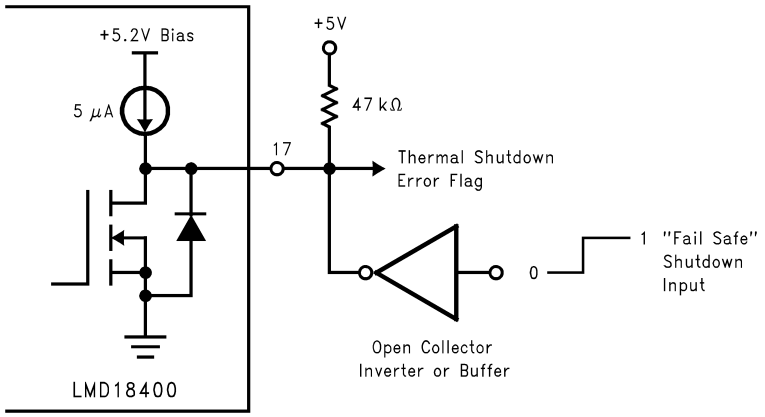



**Figure 26. Thermal Shutdown Flag and Shutdown Input**

A useful feature of pin 17 is that it can also be used as a shutdown input. Driving this pin low immediately switches all of the drivers OFF, just the same as if thermal shutdown temperatures has been reached, yet all of the control logic and diagnostic circuits remain active. This is useful in designing “fail-safe” systems where the loads can be disabled under any sort of externally detected system fault condition. The diagnostic logic however does not distinguish between normal thermal shutdown or the fact that pin 17 has been driven low. As such, various switch errors and an over-temperature indication will be reported in the diagnostic data stream.

Figure 26 illustrates the use of pin 17 as both an output thermal shutdown flag and as an input to shut down only the switches. Directly tying pin 17 to +5V will prevent the internal thermal shutdown circuitry from disabling the switches. For reliability purposes however this is not recommended as there will then be no limit to the maximum die temperature.

Refer to the TRUTH TABLE for a summary of the action of these direct-output error flags.

## LOAD ERROR DETECTION

An important feature of the LMD18400 is the ability to detect open or shorted load connections. Figure 27 illustrates the detection circuit used with each of the drivers.

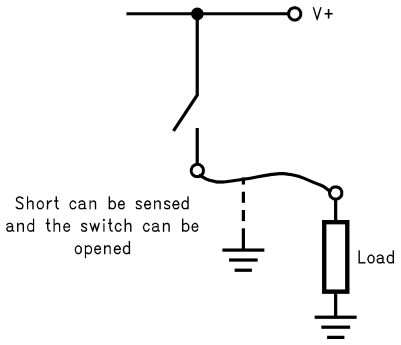



**Figure 27. Detection Circuitry for Open/Shorted Loads**

A voltage comparator monitors the voltage to the load and compares it to a fixed 4.1V reference level. When a switch is OFF, the ground referenced load should have no voltage across it. Under this condition, an internal 50 kΩ resistor connected to $V_{CC}$ will provide a small amount of current to the load. If the load resistance is large enough to create a voltage greater than 4.1V an Open Load Error will be indicated for that switch. The maximum load resistance that will not generate an Open Load Error when a switch is OFF can be found by:

$$R_{Max} = \frac{4.1V}{V_{CC} - 4.6V} \times 50\,k\Omega; \text{ for no Open Load Indication} \quad (2)$$

To make this Open Load Error threshold more sensible, an external pull-up resistor can be added from the output to the $V_{CC}$ supply.

Also when a switch is commanded OFF, should the load be shorted to the $V_{CC}$ supply, this same circuitry will again indicate an error.

When a switch is commanded ON, the load is expected to have a voltage across it that approaches the $V_{CC}$ potential. If the output voltage is less than the 4.1V threshold an error will again be reported, indicating that the load is either shorted to ground or that the driver is in power limit and not able to pull the output voltage any closer to $V_{CC}$. The minimum load resistance that will not generate a Shorted Load Error when a switch is ON can be found by:

$$R_{Min} = \frac{4.1V\ (V_{CC} - 4.1V)}{15W}; \text{ for no Shorted Load Error} \quad (3)$$

Figure 28 indicates the range of load resistance for normal operation, open load, and shorted load or power limit indication.

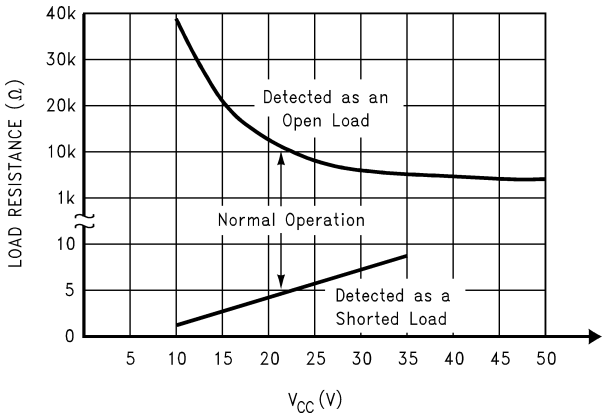



**Figure 28. Load Resistance Detected as Errors**

## THERMAL MANAGEMENT

It is particularly important to consider the total amount of power being dissipated by all four switches in the LMD18400 at all times. Any combination of the switches driving loads will cause an increase in the die temperature. Should the die temperature reach the thermal shutdown threshold of +170°C, all of the switches will be disabled.

Careful calculation of the worst case total power dissipation required at any point in time, together with providing sufficient heatsinking will prevent this from occurring.

The LMD18400 is packaged with a special leadframe that helps dissipate heat through the two ground pins on each side of the package. The thermal resistance from junction-to-case ($\theta_{JC}$) for this package is approximately 20°C/W. The thermal resistance from junction-to-ambient ($\theta_{JA}$), without any heatsinking, is approximately 60°C/W. Figure 29 illustrates how the copper foil of a printed circuit board can be designed to provide heatsinking and reduce the overall junction-to-ambient thermal resistance.

The power dissipation in each switch is equal to:

$$P_{D\ (Each\ Switch)} = I_{LOAD}^{2} \times R_{ON} \quad or \quad \frac{(V_{CC} - V_{OUT})^2}{R_{ON}} \tag{4}$$

where

- $R_{ON}$ is the ON resistance of the switch (1.3Ω maximum)

These equations hold true until the power dissipation reaches the maximum limit of 15W. With resistive loads, the 15W power limit threshold will be reached when:

$$R_L \leq \frac{V_{CC}^{2}}{60W} \tag{5}$$

Inductive loads will create additional power dissipation when switched OFF. Figure 30 shows the idealized voltage and current waveforms for an inductive load.

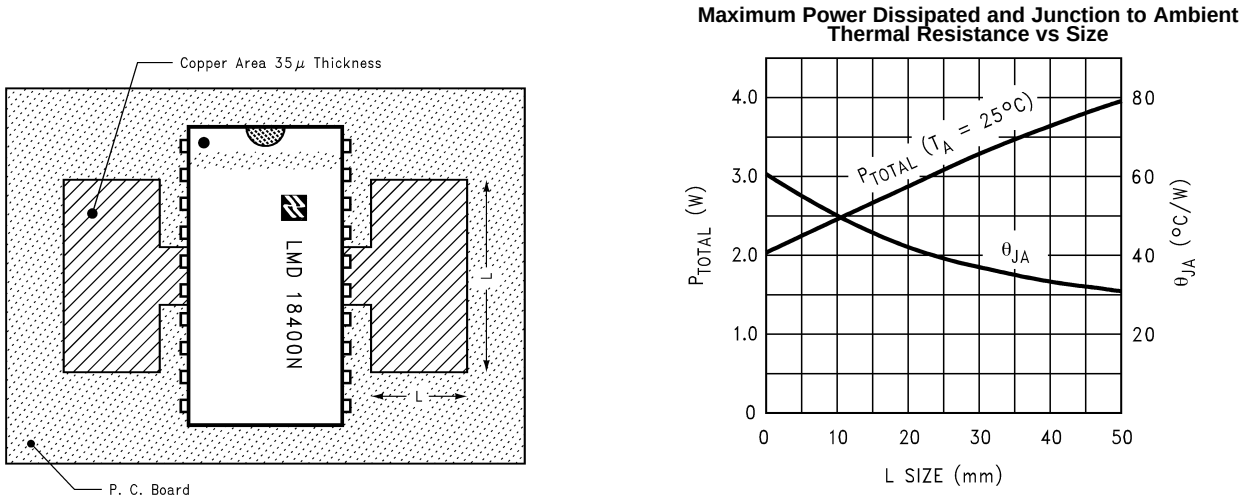



**Figure 29. Recommended PC Board Layout to Reduce the Thermal Resistance from Junction-to-Ambient**

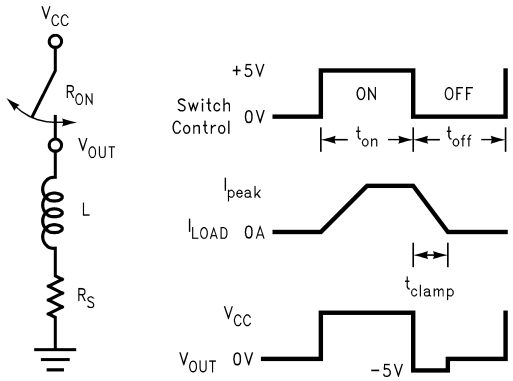



**Figure 30. Switching an Inductive Load**

When switched ON, the worst case power dissipation is:

$$P_{D(ON)} = I_{Peak}^{2} \times R_{ON}; \text{ where } I_{Peak} = \frac{V_{CC}}{R_{ON} + R_S} \tag{6}$$

The steady-state ON current of the inductor should be kept less than 1A per power switch.

The additional power dissipation during turn-off, as the inductor is de-energized and the voltage across the inductor is clamped to −5V, can be found by:

$$P_{D(OFF)} = \frac{(V_{CC} + 5V) \times I_{Peak}}{2} \tag{7}$$

for the time interval, $t_{CLAMP}$. which is the time required for the inductor current to fall to zero:

$$t_{Clamp} = \frac{I_{Peak} \times L}{5V} \tag{8}$$

The size of the inductor will determine the time duration for this additional power dissipation interval. Even though the peak current is kept less than 1A, the switch during this interval will see a voltage across it of $V_{CC}$ + 5V with no power limit protection. If the inductor is too large, the time interval may be long enough to heat the die temperature to +170°C thereby shutting OFF all other loads on the package.

The total average power dissipation during a full ON/OFF switching cycle of an inductive load will be:

$$P_{D(tot)} = \left[ I_{Peak}^2 \, R_{ON} \, t_{ON} + \frac{I_{Peak}^2 \, L \, (V_{CC} + 5V)}{10} \right] \frac{1}{t_{ON} + t_{OFF}} \quad (9)$$

Due to the common cut-off of all loads forced by thermal shutdown, the thermal time constants of the package become a concern. Figure 31 provides an indication of the time it takes to heat the die to thermal shutdown with a step increase in package power dissipation from an initial junction temperature of +25°C. This data was measured using a PC board layout providing a thermal resistance from junction to ambient of approximately 35°C/W. Less heatsinking will, of course, result in faster thermal shutdown of the power switches.

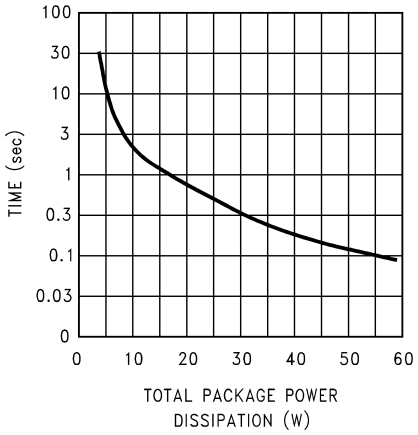



**Figure 31. Approximate time required for the die to reach the 170°C thermal shutdown point from 25°C for different total package power dissipation levels.**

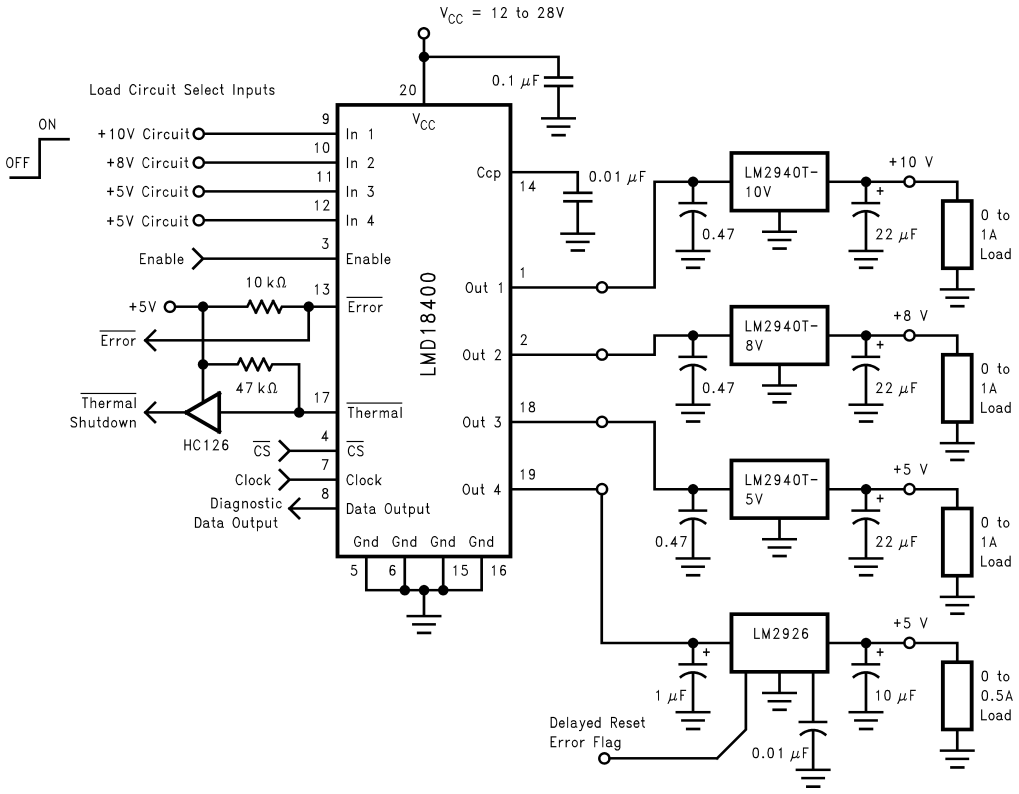



**Figure 32. ON/OFF Switching of Multiple Voltage Regulated Circuit Loads**

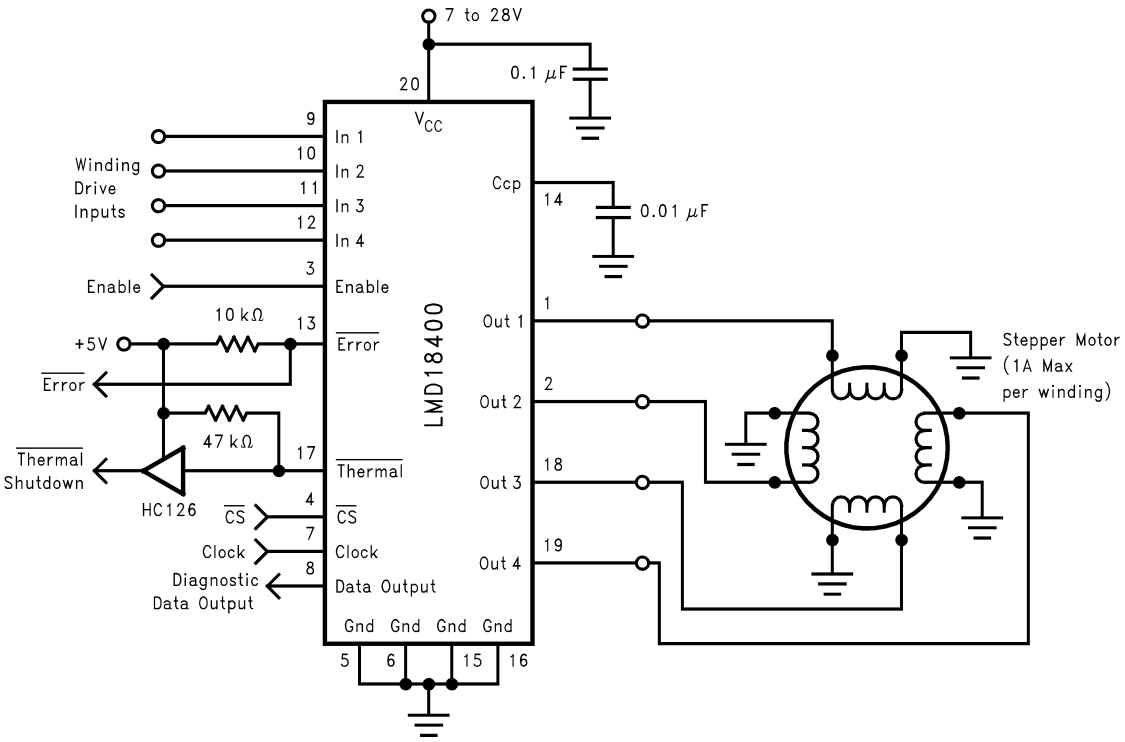



**Figure 33. Unipolar Drive for a 4-Phase Stepper Motor**

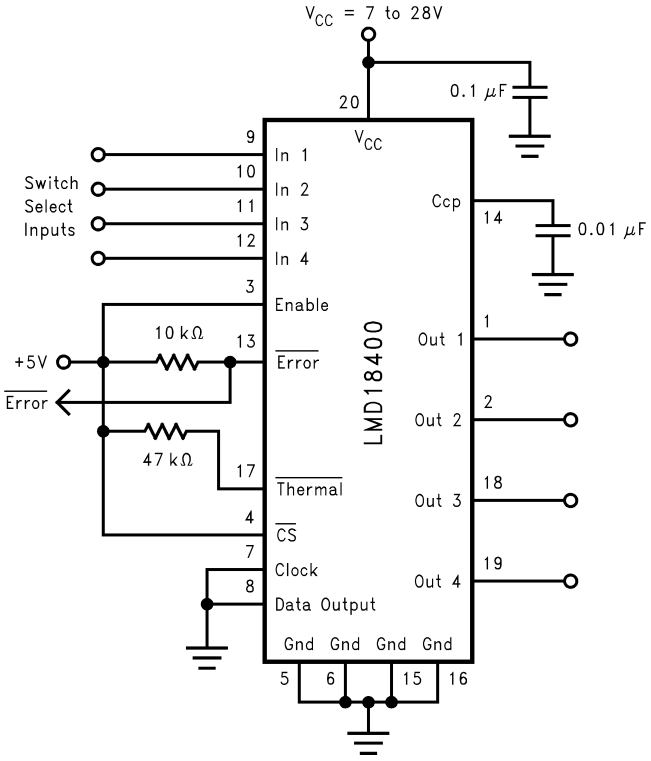
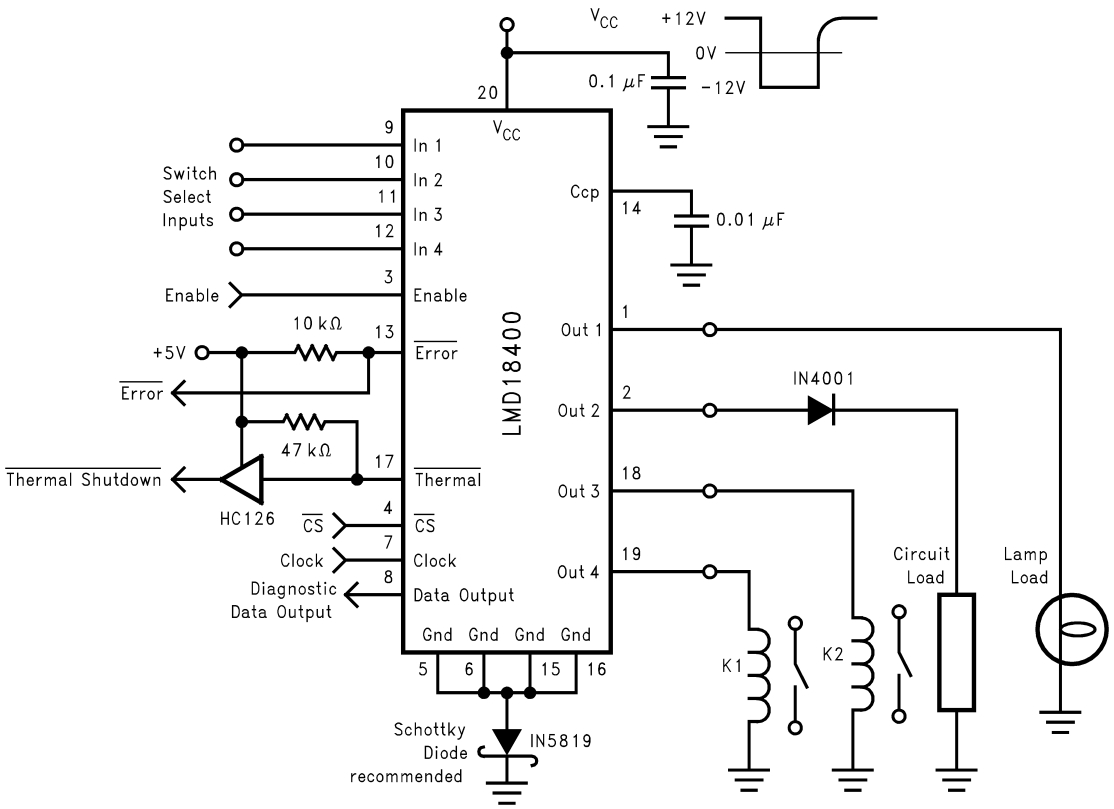



**Figure 34. Recommended Connection If No Diagnostics are Required**




Loads will be energized through the intrinsic diodes in parallel with the power switches. The Schottky diode will add approximately 0.2V to the logic input switching thresholds and the logic output low levels.

**Figure 35. Simple protection of the LMD18400 against supply voltage reversal**

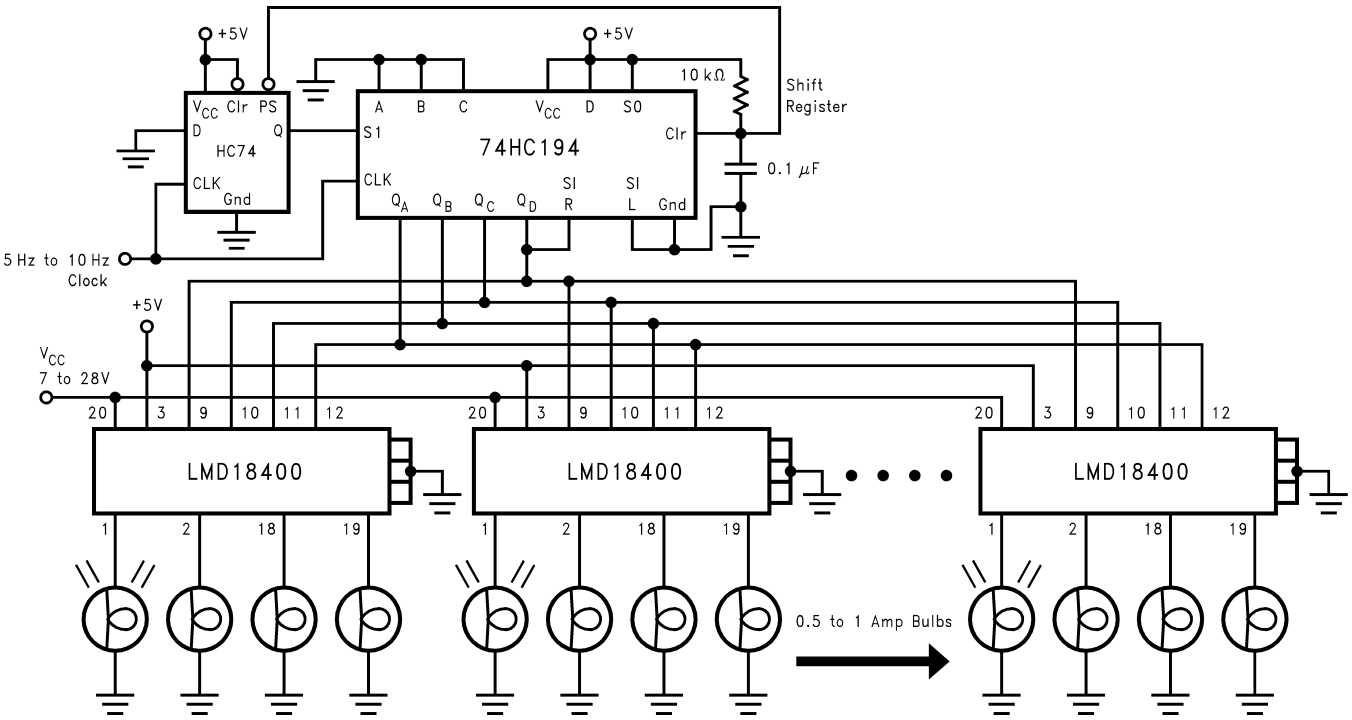
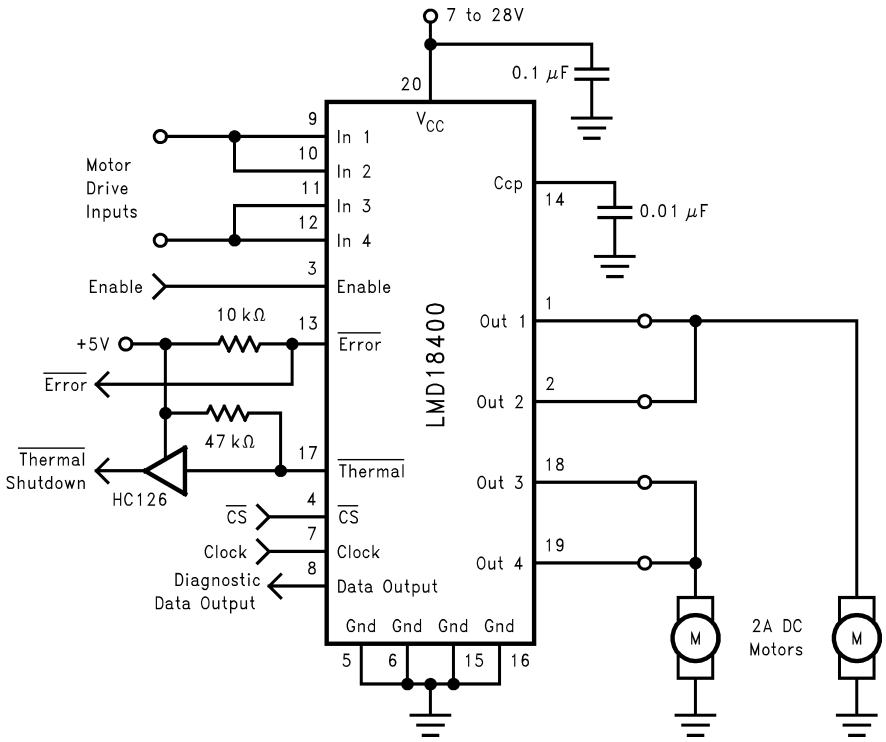



**Figure 36. Simple Light "Chaser"**




Positive temperature coefficient of the switch ON resistance provides ballasting to evenly share the load current between the switches. Any combination of switches can be paralleled. Required peak load current will depend upon the motor load. Motor speed control can be provided by a PWM signal of up to 20 kHz applied to the motor drive input lines.

**Figure 37. Paralleling switches for higher current capability**

## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 21 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMD18400N | NRND | PDIP | NFH | 20 | 18 | TBD | Call TI | Call TI | -25 to 85 | LMD18400N | |
| LMD18400N/NOPB | ACTIVE | PDIP | NFH | 20 | 18 | Pb-Free (RoHS) | SN | Level-1-NA-UNLIM | -25 to 85 | LMD18400N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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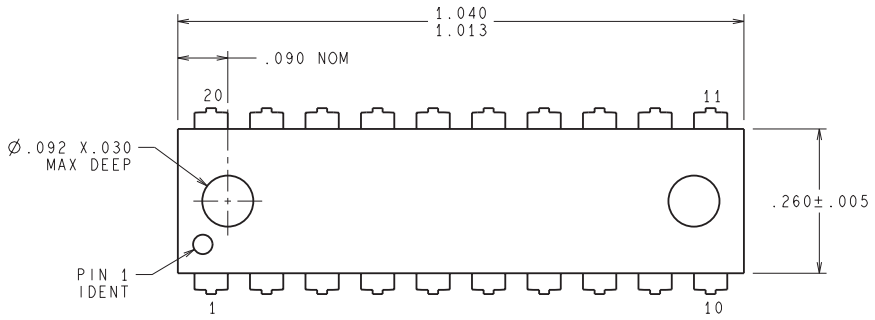
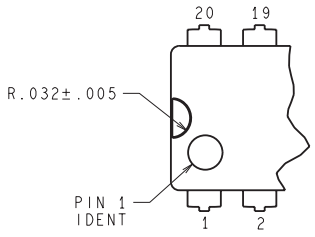
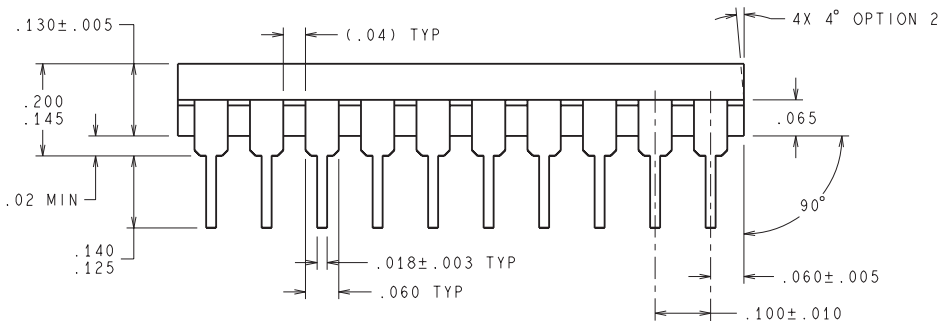
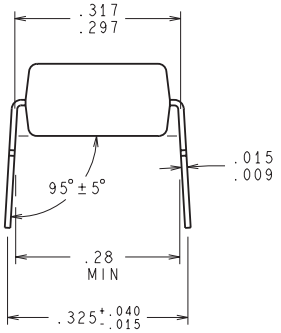



OPTION 1




OPTION 2




N20A (Rev G)

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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