LMK00301 3GHz 10-Output Ultra-Low Additive Jitter Differential Clock Buffer and Level Translator

1 Features

- 3:1 input multiplexer
  - Two universal inputs operate up to 3.1GHz and accept lvpecl, lvds, cml, sstl, hstl, hcsl, or single-ended clocks
  - One crystal input accepts 10MHz to 40Mhz crystal or single-ended clock
- Two banks with five differential outputs each
  - LVPECL, LVDS, HCSL, or Hi-Z (selectable per bank)
  - LVPECL additive jitter with LMK03806 clock source at 156.25MHz:
    - 20 fs RMS (10kHz to 1MHz)
    - 51 fs RMS (12kHz to 20MHz)
- Frequency range:
  - LVPECL (DC to 3100MHz)
  - LVDS (DC to 2100MHz)
  - HCSL (DC to 800MHz)
  - LVCMOS (DC to 250MHz)
- Additive RMS Jitter after PCIe Filters:
  - Gen 7: 9.38fs (LVPECL), 10.1fs (HCSL), 12.6fs (LVDS) (maxima)
  - Gen 6: 13.4fs (LVPECL), 14.3fs (HCSL), 18.0fs (LVDS) (maxima)
  - Gen 5: 21.8fs (LVPECL), 23.6fs (HCSL), 30.3fs (LVDS) (maxima)
- High PSRR: –65dBc (LVPECL) and –76dBc (LVDS) at 156.25MHz
- LVCMOS output with synchronous enable input
- Pin-controlled configuration
- V_{CC} core supply: 3.3V ± 5%
- Three independent V_{CCO} output supplies: 3.3V or 2.5V ± 5%
- Industrial temperature range: –40°C to +85°C

2 Applications

- Clock distribution and level translation for ADCs, DACs, multi-gigabit Ethernet, XAUI, fibre channel, SATA/SAS, SONET/SDH, CPRI, high-frequency backplanes
- Switches, routers, line cards, timing cards
- Servers, computing, PCI express (PCIe 3.0, 4.0, 5.0, 6.0, 7.0)
- Remote radio units and baseband units

3 Description

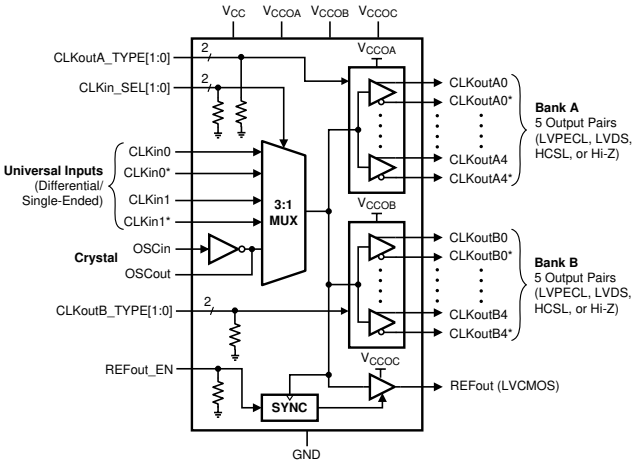
The LMK00301 is a 3GHz, 10-output differential fanout buffer intended for high-frequency, low-jitter clock and data distribution, and level translation. The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of five differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL, LVDS, or HCSL drivers, or disabled. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The LMK00301 operates from a 3.3V core supply and three independent 3.3V or 2.5V output supplies.

The LMK00301 provides high performance, versatility, and power efficiency, making the device designed for replacing fixed-output buffer devices while increasing timing margin in the system. The LMK00301 offers a design spin, the LMK00301A, that does not have power supply sequencing requirements between the core and output supply domains.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(3)
LMK00301(2)	RHS (WQFN, 48)	7.00mm × 7.00mm

(1) For more information, see Section 12.
(2) The LMK00301A is a design spin available as an orderable in orderable addendum at the end of the data sheet.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

ORDER NUMBER	REQUIRES POWER SEQUENCING
LMK00301	Yes(1)
LMK00301A	No(2)

(1) Requires power supply sequencing where all of the core and output supplies ramp at the same time or must be tied together.
(2) Does not have power supply sequencing requirements between the core and output supply domains.

5 Pin Configuration and Functions

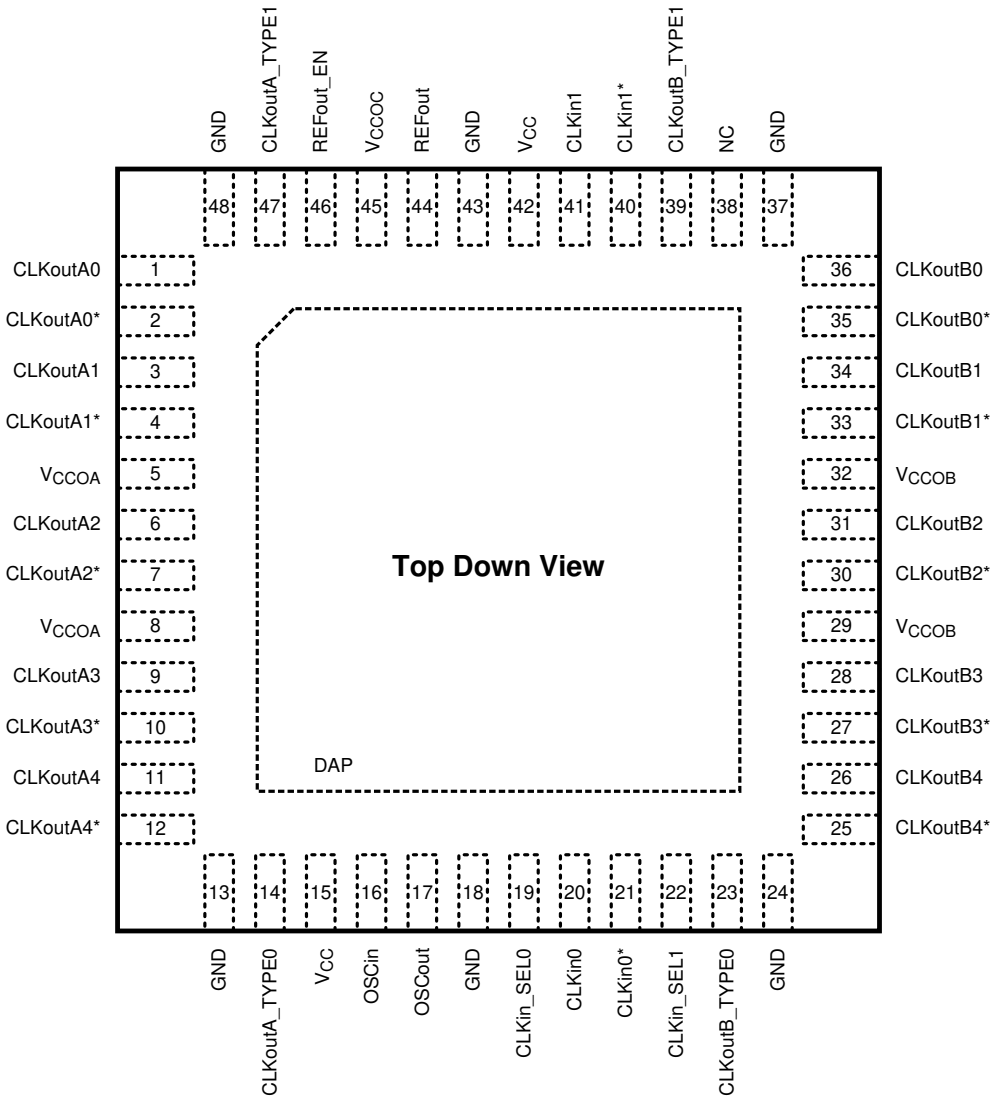


Figure 5-1. RHS Package 48-Pin WQFN Top View

Table 5-1. Pin Functions [4]

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKin_SEL0	19	I	Clock input selection pins [3]
CLKin_SEL1	22		
CLKin0	20	I	Universal clock input 0 (differential or single-ended)
CLKin0*	21		
CLKin1	40	I	Universal clock input 1 (differential or single-ended)
CLKin1*	40		
CLKoutA_TYPE0	14	I	Bank A output buffer type selection pins [3]
CLKoutA_TYPE1	47		
CLKoutB_TYPE0	23	I	Bank B output buffer type selection pins [3]
CLKoutB_TYPE1	39		
CLKoutA0	1	O	Differential clock output A0. Output type set by CLKoutA_TYPE pins.
CLKoutA0*	2		
CLKoutA1	3	O	Differential clock output A1. Output type set by CLKoutA_TYPE pins.
CLKoutA1*	4		
CLKoutA2	6	O	Differential clock output A2. Output type set by CLKoutA_TYPE pins.
CLKoutA2*	7		
CLKoutA3	9	O	Differential clock output A3. Output type set by CLKoutA_TYPE pins.
CLKoutA3*	10		
CLKoutA4	11	O	Differential clock output A4. Output type set by CLKoutA_TYPE pins.
CLKoutA4*	12		
CLKoutB4*	25	O	Differential clock output B4. Output type set by CLKoutB_TYPE pins.
CLKoutB4	26		
CLKoutB3*	27	O	Differential clock output B3. Output type set by CLKoutB_TYPE pins.
CLKoutB3	28		
CLKoutB2*	30	O	Differential clock output B2. Output type set by CLKoutB_TYPE pins.
CLKoutB2	31		
CLKoutB1*	33	O	Differential clock output B1. Output type set by CLKoutB_TYPE pins.
CLKoutB1	34		
CLKoutB0*	35	O	Differential clock output B0. Output type set by CLKoutB_TYPE pins.
CLKoutB0	36		
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
GND	13, 18, 24, 37, 43, 48	GND	Ground
NC	38	—	Not connected internally. Pin can be floated, grounded, or otherwise tied to any potential within the Supply Voltage range stated in *Absolute Maximum Ratings*.
OSCin	16	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
OSCout	17	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
REFout	44	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
REFout_EN	46	I	REFout enable input. Enable signal is internally synchronized to selected clock input. [3]
V_{CC}	15, 42	PWR	Power supply for Core and Input Buffer blocks. The Vcc supply operates from 3.3V. Bypass with a 0.1µF low-ESR capacitor placed very close to each Vcc pin.

Table 5-1. Pin Functions [4] (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CCOA}	5, 8	PWR	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3V or 2.5V. The V_{CCOA} pins are internally tied together. Bypass with a 0.1µF low-ESR capacitor placed very close to each Vcco pin. [2]
V_{CCOB}	29, 32	PWR	Power supply for Bank B Output buffers. V_{CCOB} can operate from 3.3V or 2.5V. The V_{CCOB} pins are internally tied together. Bypass with a 0.1µF low-ESR capacitor placed very close to each Vcco pin. [2]
V_{CCOC}	45	PWR	Power supply for REFout Output buffer. V_{CCOC} can operate from 3.3V or 2.5V. Bypass with a 0.1µF low-ESR capacitor placed very close to each Vcco pin. [2]

(1) I = Input, O = Output, PWR = Power
(2) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) is called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
(3) CMOS control input with internal pull-down resistor.
(4) Any unused output pin must be left floating with minimum copper length (see note in *Clock Outputs*), or properly terminated if connected to a transmission line, disabled, or set to Hi-Z, if possible. See *Clock Outputs* for output configuration and *Termination and Use of Clock Drivers* for output interface and termination techniques.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}, V_{CCO}	Supply voltages	-0.3	3.6	V
V_{IN}	Input voltage	-0.3	(V_{CC} + 0.3)	V
T_{STG}	Storage temperature	-65	+150	°C
T_L	Lead temperature (solder 4s)		+260	°C
T_J	Junction temperature		+150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model (MM)	±150	
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions. Pins listed as ±2000V can actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions. Pins listed as ±750V can actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Ambient Temperature Range	-40	25	85	°C
T_J	Junction Temperature			125	°C
V_{CC}	Core Supply Voltage Range	3.15	3.3	3.45	V
V_{CCO}	Output Supply Voltage Range (1) (2)	3.3 – 5% 2.5 – 5%	3.3 2.5	3.3 + 5% 2.5 + 5%	V

(1) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) is called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type
(2) Vcco for any output bank must be less than or equal to Vcc (Vcco ≤ Vcc).

6.4 Thermal Information

THERMAL METRIC(1) (2)		LMK00301 RHS0048A (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.5	°C/W
$R_{\theta JC(top)\ (DAP)}$	Junction-to-case (top) thermal resistance	7.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Specification assumes 16 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the package. Use the maximum number of vias in the board layout.

6.5 Electrical Characteristics

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION (2)							
I_{CC_CORE}	Core Supply Current, All Outputs Disabled	CLKinX selected			8.5	10.5	mA
		OSCin selected			10	13.5	mA
I_{CC_PECL}	Additive Core Supply Current, Per LVPECL Bank Enabled				20	27	mA
I_{CC_LVDS}	Additive Core Supply Current, Per LVDS Bank Enabled	LMK00301			26	32.5	mA
		LMK00301A			31	38	
I_{CC_HCSL}	Additive Core Supply Current, Per HCSL Bank Enabled				35	42	mA
I_{CC_CMOS}	Additive Core Supply Current, LVCMOS Output Enabled				3.5	5.5	mA
I_{CCO_PECL}	Additive Output Supply Current, Per LVPECL Bank Enabled	Includes Output Bank Bias and Load Currents, R_T = 50Ω to Vcco - 2V on all outputs in bank			165	197	mA
I_{CCO_LVDS}	Additive Output Supply Current, Per LVDS Bank Enabled	LMK00301			34	44.5	mA
		LMK00301A			24	33.5	
I_{CCO_HCSL}	Additive Output Supply Current, Per HCSL Bank Enabled	Includes Output Bank Bias and Load Currents, R_T = 50Ω on all outputs in bank	Vcco = 3.3V ± 5%		87	104	mA
			Vcco = 2.5V ± 5%				
I_{CCO_CMOS}	Additive Output Supply Current, LVCMOS Output Enabled	200MHz, C_L = 5pF	Vcco = 3.3V ± 5%		9	10	mA
			Vcco = 2.5V ± 5%		7	8	mA
POWER SUPPLY RIPPLE REJECTION (PSRR)							
$PSRR_{PECL}$	Ripple-Induced Phase Spur Level(3) Differential LVPECL Output	100kHz, 100mVpp Ripple Injected on Vcco, Vcco = 2.5V	156.25MHz		-65		dBc
			312.5MHz		-63		
$PSRR_{HCSL}$	Ripple-Induced Phase Spur Level(3) Differential HCSL Output		156.25MHz		-76		dBc
			312.5MHz		-74		
$PSRR_{LVDS}$	Ripple-Induced Phase Spur Level(3) Differential LVDS Output		156.25MHz		-72		dBc
			312.5MHz		-63		
CMOS CONTROL INPUTS (CLKin_SELn, CLKoutX_TYPEn, REFout_EN)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage			GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc, Internal pull-down resistor				50	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0V, Internal pull-down resistor		-5	0.1		µA
CLOCK INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)							

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{CLKin}	Input Frequency Range(10)	Functional up to 3.1GHz Output frequency range and timing specified per output type (refer to LVPECL, LVDS, HCSL, LVCMOS output specifications)		DC		3.1	GHz
V_{IHD}	Differential Input High Voltage	CLKin driven differentially				Vcc	V
V_{ILD}	Differential Input Low Voltage			GND			V
V_{ID}	Differential Input Voltage Swing(4)			0.15		1.3	V
V_{CMD}	Differential Input Common Mode Voltage	V_{ID} = 150mV		0.25		Vcc - 1.2	V
		V_{ID} = 350mV		0.25		Vcc - 1.1	
		V_{ID} = 800mV		0.25		Vcc - 0.9	
V_{IH}	Single-Ended Input High Voltage	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V_{CM} range				Vcc	V
V_{IL}	Single-Ended Input Low Voltage			GND			V
V_{I_SE}	Single-Ended Input Voltage Swing(15) (17)			0.3		2	Vpp
V_{CM}	Single-Ended Input Common Mode Voltage			0.25		Vcc - 1.2	V
ISO_{MUX}	Mux Isolation, CLKin0 to CLKin1	f_{OFFSET} > 50kHz, P_{CLKinX} = 0dBm	f_{CLKin0} = 100MHz		-84		dBc
			f_{CLKin0} = 200MHz		-82		
			f_{CLKin0} = 500MHz		-71		
			f_{CLKin0} = 1000MHz		-65		
CRYSTAL INTERFACE (OSCin, OSCout)							
F_{CLK}	External Clock Frequency Range(10)	OSCin driven single-ended, OSCout floating				250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200Ω (10 to 30MHz) ESR ≤ 125Ω (30 to 40MHz)(5)		10		40	MHz
C_{IN}	OSCin Input Capacitance				4		pF
LVPECL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing(10) (11)	V_{OD} ≥ 600mV, R_L = 100Ω differential	Vcco = 3.3V ± 5%, R_T = 160Ω to GND	1.0	1.2		GHz
			Vcco = 2.5V ± 5%, R_T = 91Ω to GND	0.75	1.0		
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing(10) (11)	V_{OD} ≥ 400mV, R_L = 100Ω differential	Vcco = 3.3V ± 5%, R_T = 160Ω to GND	1.5	3.1		GHz
			Vcco = 2.5V ± 5%, R_T = 91Ω to GND	1.5	2.3		
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10kHz to 20MHz(15) (6) (16)	Vcco = 2.5V ± 5%: R_T = 91Ω to GND, Vcco = 3.3V ± 5%: R_T = 160Ω to GND, R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		77	98	fs
			CLKin: 156.25MHz, Slew rate ≥ 3V/ns		54	78	
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1MHz to 20MHz(6)	Vcco = 3.3V, R_T = 160Ω to GND, R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		59		fs
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		64		
			CLKin: 625MHz, Slew rate ≥ 3V/ns		30		
$Jitter_{ADD}$	Additive RMS Jitter with LVPECL clock source from LMK03806(6) (7)	Vcco = 3.3V, R_T = 160Ω to GND, R_L = 100Ω differential	CLKin: 156.25MHz, J_{SOURCE} = 190 fs RMS (10kHz to 1MHz)		20		fs
			CLKin: 156.25MHz, J_{SOURCE} = 195 fs RMS (12kHz to 20MHz)		51		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10MHz(8) (9)	Vcco = 3.3V, R_T = 160Ω to GND, R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		-162.5		dBc/Hz
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		-158.1		
			CLKin: 625MHz, Slew rate ≥ 3V/ns		-154.4		
DUTY	Duty Cycle(10)	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	T_A = 25°C, DC Measurement, R_T = 50Ω to Vcco - 2V		Vcco - 1.2	Vcco - 0.9	Vcco - 0.7	V
V_{OL}	Output Low Voltage			Vcco - 2.0	Vcco - 1.75	Vcco - 1.5	V
V_{OD}	Output Voltage Swing(4)			600	830	1000	mV
t_R	Output Rise Time 20% to 80%(15)	R_T = 160Ω to GND, Uniform transmission line up to 10 in. with 50Ω characteristic impedance, R_L = 100Ω differential, C_L ≤ 5pF			175	300	ps

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_F	Output Fall Time 80% to 20%(15)				175	300	ps
LVDS OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing(10) (11)	V_{OD} ≥ 250mV, R_L = 100Ω differential		1.0	1.6		GHz
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing(10) (11)	V_{OD} ≥ 200mV, R_L = 100Ω differential		1.5	2.1		GHz
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10kHz to 20MHz(15) (6) (16)	R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		94	115	fs
			CLKin: 156.25MHz, Slew rate ≥ 3V/ns		70	90	
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1MHz to 20MHz(6)	Vcco = 3.3V, R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		89		fs
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		77		
			CLKin: 625MHz, Slew rate ≥ 3V/ns		37		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10MHz(8) (9)	Vcco = 3.3V, R_L = 100Ω differential	CLKin: 100MHz, Slew rate ≥ 3V/ns		-159.5		dBc/Hz
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		-157.0		
			CLKin: 625MHz, Slew rate ≥ 3V/ns		-152.7		
DUTY	Duty Cycle(10)	50% input clock duty cycle		45%		55%	
V_{OD}	Output Voltage Swing(4)	T_A = 25°C, DC Measurement, R_L = 100Ω differential		250	400	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			-50		50	mV
V_{OS}	Output Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			-35		35	mV
I_{SA} I_{SB}	Output Short Circuit Current Single Ended	T_A = 25°C, Single ended outputs shorted to GND		-24		24	mA
I_{SAB}	Output Short Circuit Current Differential	Complementary outputs tied together		-12		12	mA
t_R	Output Rise Time 20% to 80%(15)	Uniform transmission line up to 10 inches with 50Ω characteristic impedance, R_L = 100Ω differential, C_L ≤ 5pF			175	300	ps
t_F	Output Fall Time 80% to 20%(15)				175	300	ps
HCSL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{CLKout}	Output Frequency Range(10)	R_L = 50Ω to GND, C_L ≤ 5pF		DC		800	MHz
$Jitter_{ADD\_PCIe}$	Additive RMS Phase Jitter for PCIe 7.0[4]	PLL BW: 0.5 - 1MHz; CDR = 10MHz		2.79	6.28	10.1	fs
	Additive RMS Phase Jitter for PCIe 6.0[4]	PLL BW: 0.5 - 1MHz; CDR = 10MHz	CLKin: 100MHz, Slew rate ≥ 2V/ns	4.00	8.99	14.3	
	Additive RMS Phase Jitter for PCIe 5.0[4]		PCIe5.0 filter	3.64	12.9	23.6	
	Additive RMS Phase Jitter for PCIe 3.0(10)	PCIe Gen 3, PLL BW = 2–5MHz, CDR = 10MHz	CLKin: 100MHz, Slew rate ≥ 0.6V/ns	15.9	36.2	56.3	
	Additive RMS Phase Jitter for PCIe 4.0(4)	PCIe Gen 4, PLL BW = 2–5MHz, CDR = 10MHz	CLKin: 100MHz, Slew rate ≥ 1.8V/ns	15.9	36.2	56.3	
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1MHz to 20MHz(6)	Vcco = 3.3V, R_T = 50Ω to GND	CLKin: 100MHz, Slew rate ≥ 3V/ns		77		fs
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		86		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10MHz(8) (9)	Vcco = 3.3V, R_T = 50Ω to GND	CLKin: 100MHz, Slew rate ≥ 3V/ns		-161.3		dBc/Hz
			CLKin: 156.25MHz, Slew rate ≥ 2.7V/ns		-156.3		
DUTY	Duty Cycle(10)	50% input clock duty cycle	CLKin ≤ 400MHz	45%		55%	
V_{OH}	Output High Voltage	T_A = 25°C, DC Measurement,		520	810	920	mV
V_{OL}	Output Low Voltage			-150	0.5	150	mV
V_{CROSS}	Absolute Crossing Voltage (10) (12)	R_L = 50Ω to GND, C_L ≤ 5pF	CLKin ≤ 400MHz	160	350	460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} (10) (12)					140	mV
t_R	Output Rise Time 20% to 80%(15) (12)	250MHz, Uniform transmission line up to 10 inches with 50Ω characteristic impedance, R_L = 50Ω to GND, C_L ≤ 5pF			300	500	ps
t_F	Output Fall Time 80% to 20%(15) (12)				300	500	ps

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS OUTPUT (REFout)							
f_{CLKout}	Output Frequency Range(10)	C_L ≤ 5pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1MHz to 20MHz(6)	Vcco = 3.3V, C_L ≤ 5pF	100MHz, Input Slew rate ≥ 3V/ns		95		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10MHz(8) (9)	Vcco = 3.3V, C_L ≤ 5pF	100MHz, Input Slew rate ≥ 3V/ns		-159.3		dBc/Hz
DUTY	Duty Cycle(10)	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	1mA load		Vcco - 0.1			V
V_{OL}	Output Low Voltage					0.1	V
I_{OH}	Output High Current (Source)	Vo = Vcco / 2	Vcco = 3.3V		28		mA
			Vcco = 2.5V		20		
I_{OL}	Output Low Current (Sink)		Vcco = 3.3V		28		mA
			Vcco = 2.5V		20		
t_R	Output Rise Time 20% to 80%(15) (12)	250MHz, Uniform transmission line up to 10 inches with 50Ω characteristic impedance, R_L = 50Ω to GND, C_L ≤ 5pF			225	400	ps
t_F	Output Fall Time 80% to 20%(15) (12)				225	400	ps
t_{EN}	Output Enable Time(13)	C_L ≤ 5pF				3	cycles
t_{DIS}	Output Disable Time(13)					3	cycles

6.5 Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3V ± 5%, Vcco = 3.3V ± 5%, 2.5V ± 5%, -40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Typical values represent most likely parametric norms at Vcc = 3.3V, Vcco = 3.3V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PROPAGATION DELAY and OUTPUT SKEW							
t_{PD_PECL}	Propagation Delay CLKin-to-LVPECL(15)	R_T = 160Ω to GND, R_L = 100Ω differential, C_L ≤ 5pF		180	360	540	ps
t_{PD_LVDS}	Propagation Delay CLKin-to-LVDS(15)	R_L = 100Ω differential, C_L ≤ 5pF		200	400	600	ps
t_{PD_HCSL}	Propagation Delay CLKin-to-HCSL(15) (12)	R_T = 50Ω to GND, C_L ≤ 5pF		295	590	885	ps
t_{PD_CMOS}	Propagation Delay CLKin-to-LVCMOS(15) (12)	C_L ≤ 5pF	Vcco = 3.3V	900	1475	2300	ps
			Vcco = 2.5V	1000	1550	2700	
$t_{SK(O)}$	Output Skew LVPECL/LVDS/HCSL (10) (12) (14)	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.			30	50	ps
$t_{SK(PP)}$	Part-to-Part Output Skew LVPECL/LVDS/HCSL (15) (12) (14)				80	120	ps

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions or Notes. Typical specifications are estimations only and are not ensured.
(2) See *Power Supply Recommendations* for more information on current consumption and power dissipation calculations. Characteristics for both LMK00301 and LMK00301A are the same unless specified under the test conditions.
(3) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 × $10^{(PSRR / 20)}$) / (π × f_{CLK})] × 1E12
(4) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.
(5) The ESR requirements stated must be met to verify that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal can be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to *Crystal Interface* for crystal drive level considerations.
(6) For the 100MHz and 156.25MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2), where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625MHz clock input condition, Additive RMS Jitter is approximated using Method #2: J_{ADD} = SQRT(2×$10^{dBc/10}$) / (2×π×f_{CLK}), where dBc is the phase noise power of the Output Noise Floor integrated from 1 to 20MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + 10×$\log_{10}$(20MHz - 1MHz). The additive RMS jitter was approximated for 625MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the “Noise Floor vs. CLKin Slew Rate” and “RMS Jitter vs. CLKin Slew Rate” plots in *Typical Characteristics*.
(7) 156.25MHz LVPECL clock source from LMK03806 with 20MHz crystal reference (crystal part number: ECS-200-20-30BU-DU). Typical J_{SOURCE} = 190 fs RMS (10kHz to 1MHz) and 195 fs RMS (12kHz to 20MHz). Refer to the LMK03806 data sheet for more information.
(8) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10MHz, but for lower frequencies this measurement offset can be as low as 5MHz due to measurement equipment limitations.
(9) Phase noise floor degrades as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) is less susceptible to degradation in noise floor at lower slew rates due to the common mode noise rejection. Use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.
(10) Specification is verified by characterization and is not tested in production.
(11) See *Typical Characteristics* for output operation over frequency.
(12) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.
(13) Output Enable Time is the number of input clock cycles required for the output to be enabled after REFout_EN is pulled high. Similarly, Output Disable Time is the number of input clock cycles required for the output to be disabled after REFout_EN is pulled low. The REFout_EN signal must have an edge transition much faster than that of the input clock period for accurate measurement.
(14) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.
(15) Parameter is specified by design, not tested in production.
(16) 100MHz and 156.25MHz input source from Rohde & Schwarz SMA100A Low-Noise Signal Generator and Sine-to-Square-wave Conversion block
(17) For clock input frequency ≥ 100MHz, CLKinX can be driven with single-ended (LVCMOS) input swing up to 3.3Vpp. For clock input frequency < 100MHz, the single-ended input swing must be limited to 2Vpp maximum to prevent input saturation (refer to *Driving the Clock Inputs* for interfacing 2.5V/3.3V LVCMOS clock input < 100MHz to CLKinX).

6.6 Typical Characteristics

Unless otherwise specified: V_{CC} = 3.3V, V_{CCO} = 3.3V, T_A = 25°C, CLKin driven differentially, input slew rate ≥ 3V/ns. Consult Table 6-1 at the end of *Typical Characteristics* for graph notes.

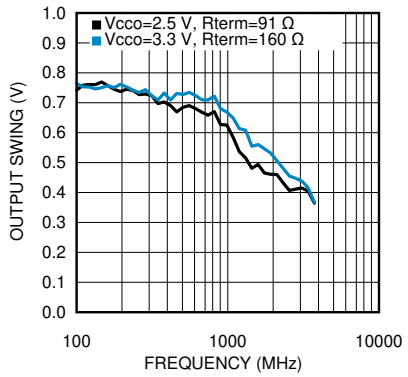


Figure 6-1. LVPECL Output Swing (V_{OD}) vs Frequency

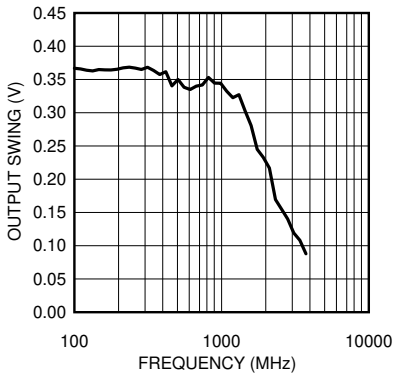


Figure 6-2. LVDS Output Swing (V_{OD}) vs Frequency

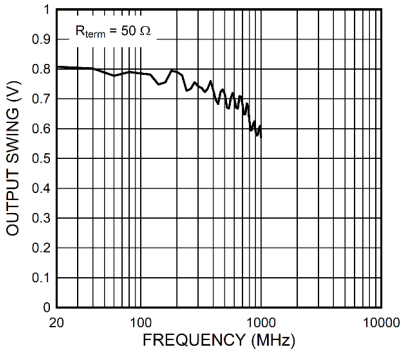


Figure 6-3. HCSL Output Swing (V_{OD}) vs Frequency

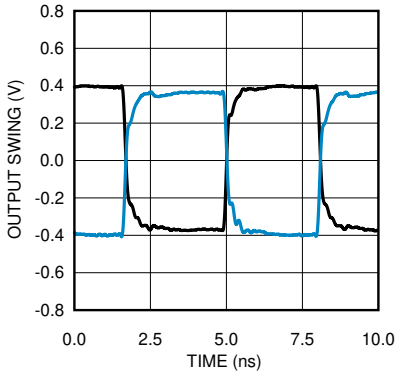


Figure 6-4. LVPECL Output Swing at 156.25MHz

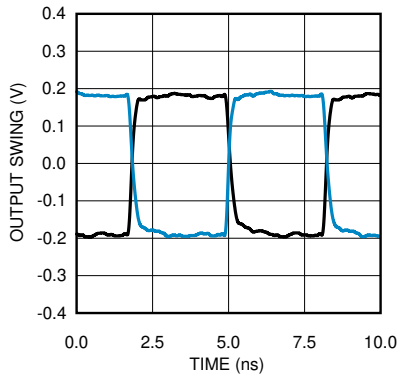


Figure 6-5. LVDS Output Swing at 156.25MHz

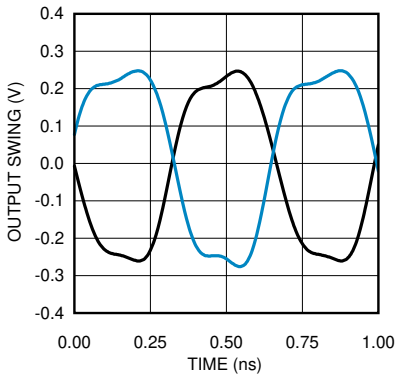


Figure 6-6. LVPECL Output Swing at 1.5GHz

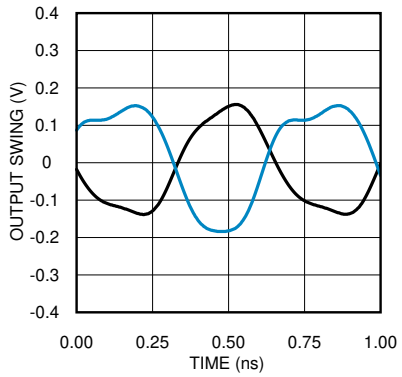


Figure 6-7. LVDS Output Swing at 1.5GHz

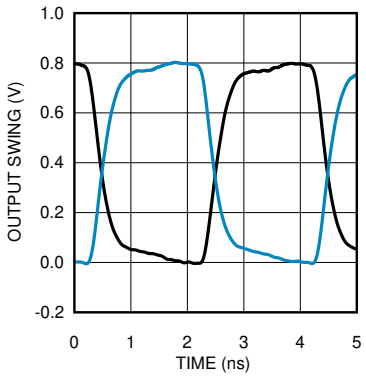


Figure 6-8. HCSL Output Swing at 250MHz

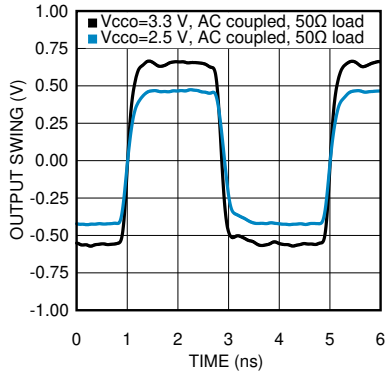


Figure 6-9. LVCMOS Output Swing at 250MHz

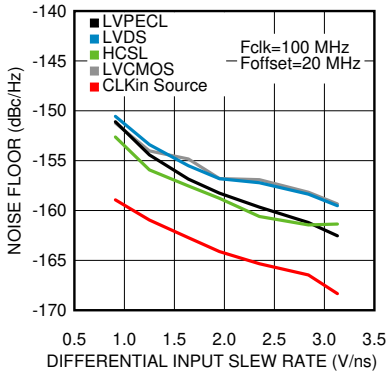


Figure 6-10. Noise Floor vs CLKin Slew Rate at 100MHz

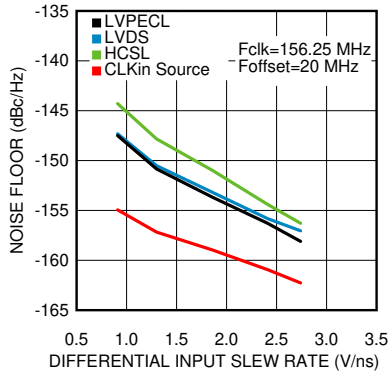


Figure 6-11. Noise Floor vs CLKin Slew Rate at 156.25MHz

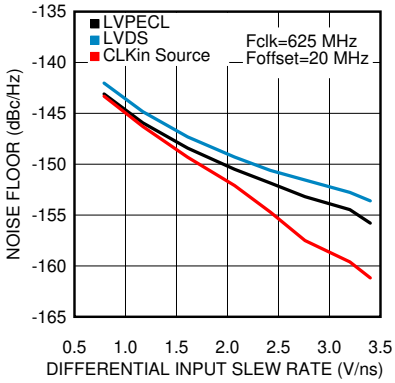
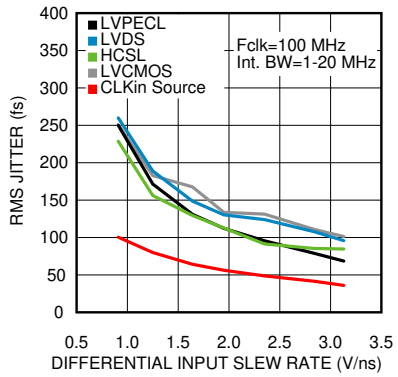
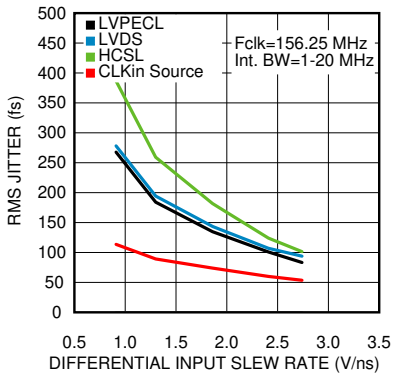


Figure 6-12. Noise Floor vs CLKin Slew Rate at 625MHz



See Note 1 in Graph Notes table

Figure 6-13. RMS Jitter vs CLKin Slew Rate at 100MHz



See Note 1 in Graph Notes table

Figure 6-14. RMS Jitter vs CLKin Slew Rate at 156.25MHz

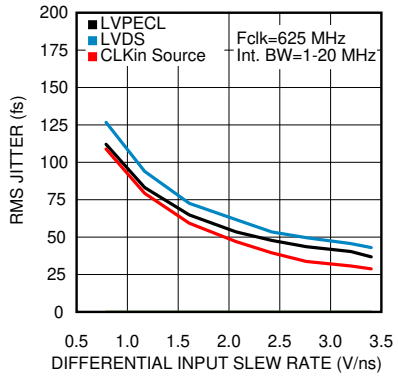


Figure 6-15. RMS Jitter vs CLKin Slew Rate at 625MHz

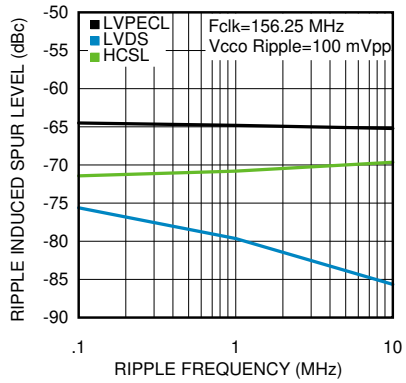


Figure 6-16. PSRR vs Ripple Frequency at 156.25MHz

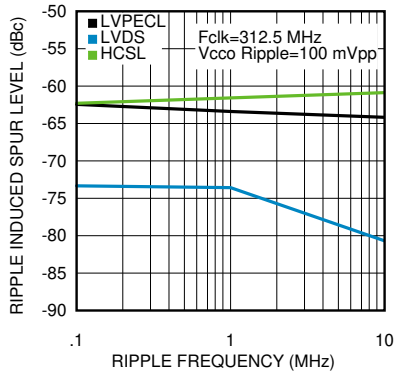


Figure 6-17. PSRR vs Ripple Frequency at 312.5MHz

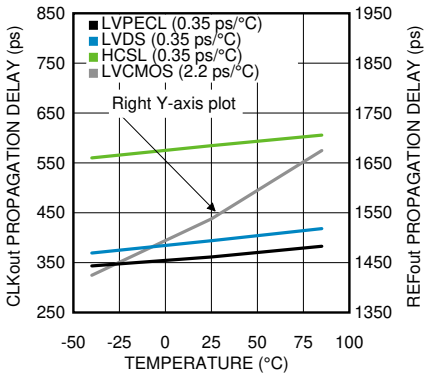
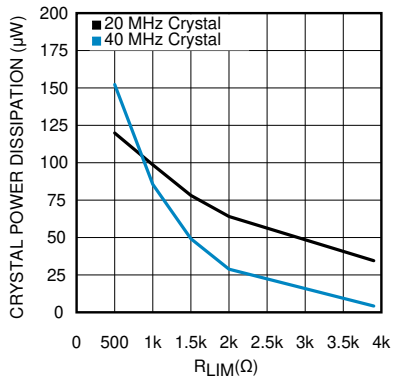
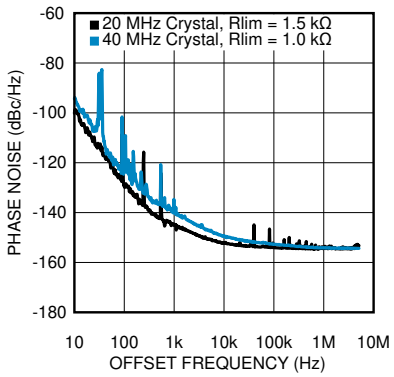


Figure 6-18. Propagation Delay vs Temperature



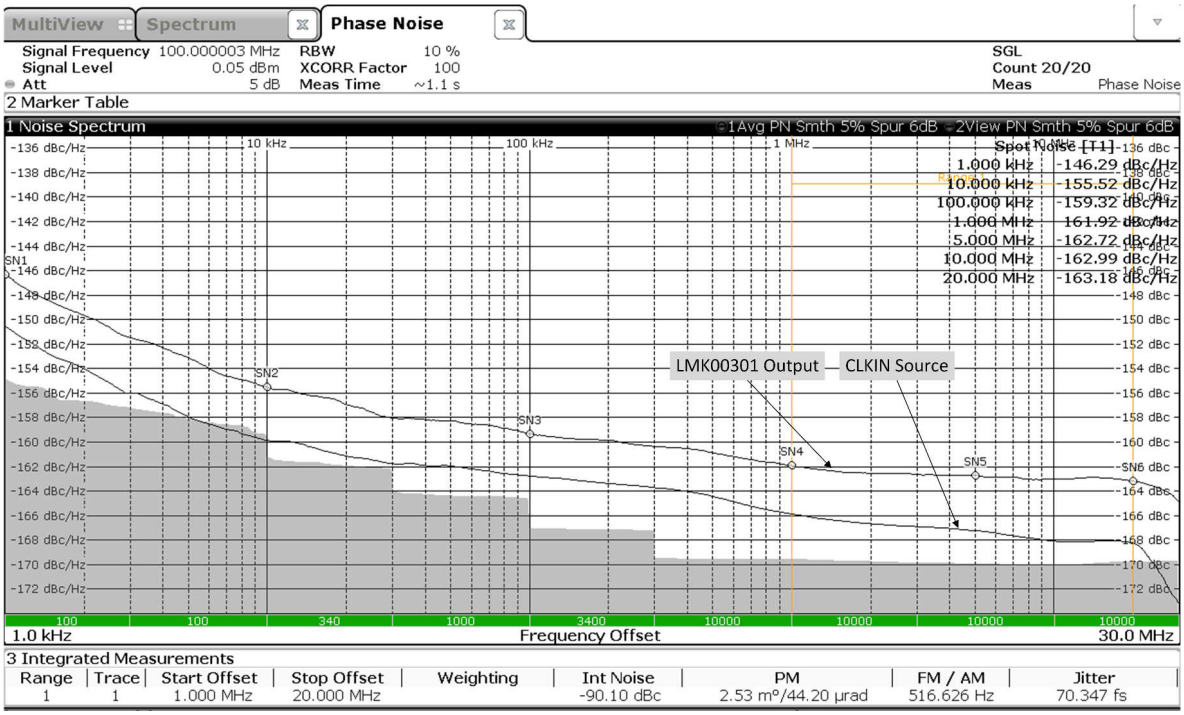
See Notes 2 and 3 in Graph Notes table

Figure 6-19. Crystal Power Dissipation vs R_{LIM}



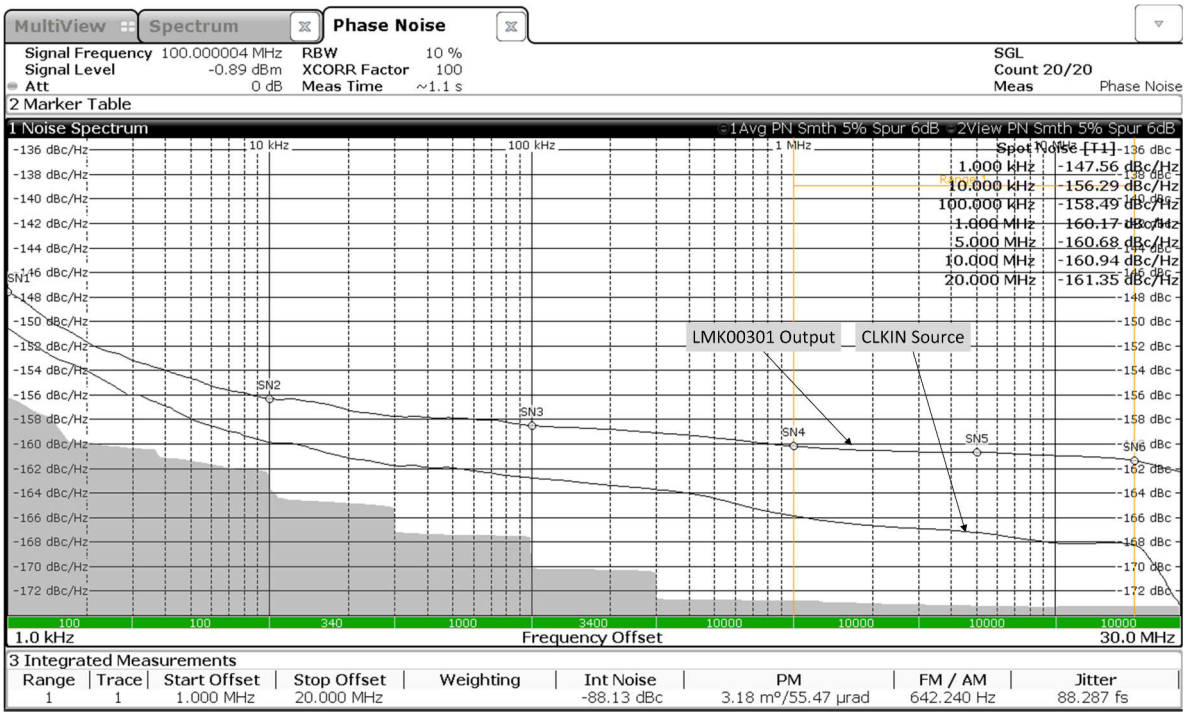
See Notes 2 and 3 in Graph Notes table

Figure 6-20. LVDS Phase Noise in Crystal Mode



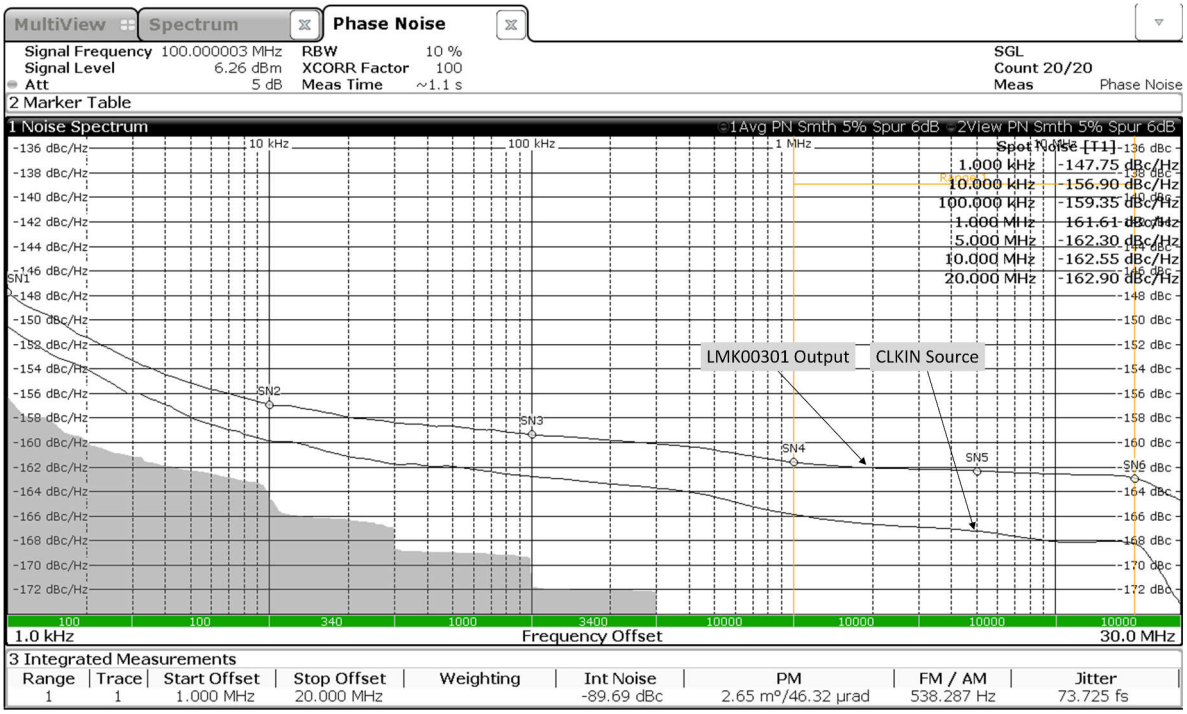
See Note 1 in Graph Notes table

Figure 6-21. HCSL Phase Noise at 100MHz



See Note 1 in Graph Notes table

Figure 6-22. LVDS Phase Noise at 100MHz



See Note 1 in Graph Notes table

Figure 6-23. LVPECL Phase Noise at 100MHz

Table 6-1. Graph Notes

NOTE	
(1)	The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each output buffer type and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: $J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2)$.
(2)	20MHz crystal characteristics: Abracon ABL series, AT cut, C_L = 18pF , C_0 = 4.4pF measured (7pF maximum), ESR = 8.5Ω measured (40Ω maximum), and Drive Level = 1mW maximum (100µW typical).
(3)	40MHz crystal characteristics: Abracon ABLS2 series, AT cut, C_L = 18pF , C_0 = 5pF measured (7pF maximum), ESR = 5Ω measured (40Ω maximum), and Drive Level = 1mW maximum (100µW typical).

7 Parameter Measurement Information

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so that the reader is able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, this signal only exists in reference to the differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 7-1 illustrates the two different definitions side-by-side for inputs and Figure 7-2 illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

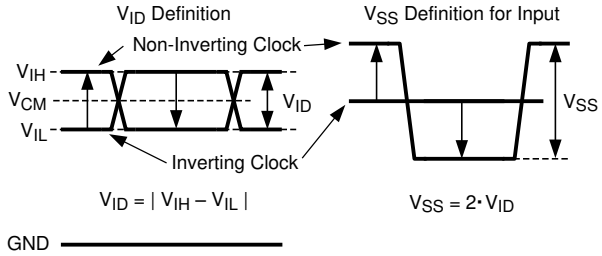


Figure 7-1. Two Different Definitions for Differential Input Signals

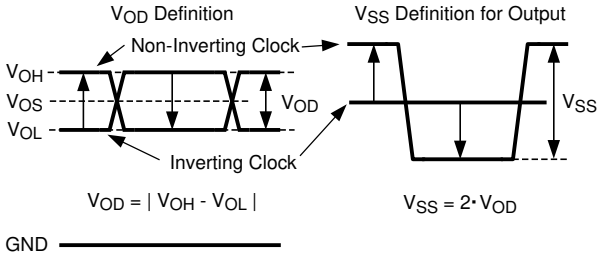


Figure 7-2. Two Different Definitions for Differential Output Signals

See also the AN-912 Common Data Transmission Parameters and their Definitions application note.

8 Detailed Description

8.1 Overview

The LMK00301 is a 10-output differential clock fanout buffer with low additive jitter that can operate up to 3.1GHz. The device features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 5 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and three independent output buffer supplies. The input selection and output buffer modes are controlled through pin strapping. The device is offered in a 48-pin WQFN package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

8.2 Functional Block Diagram

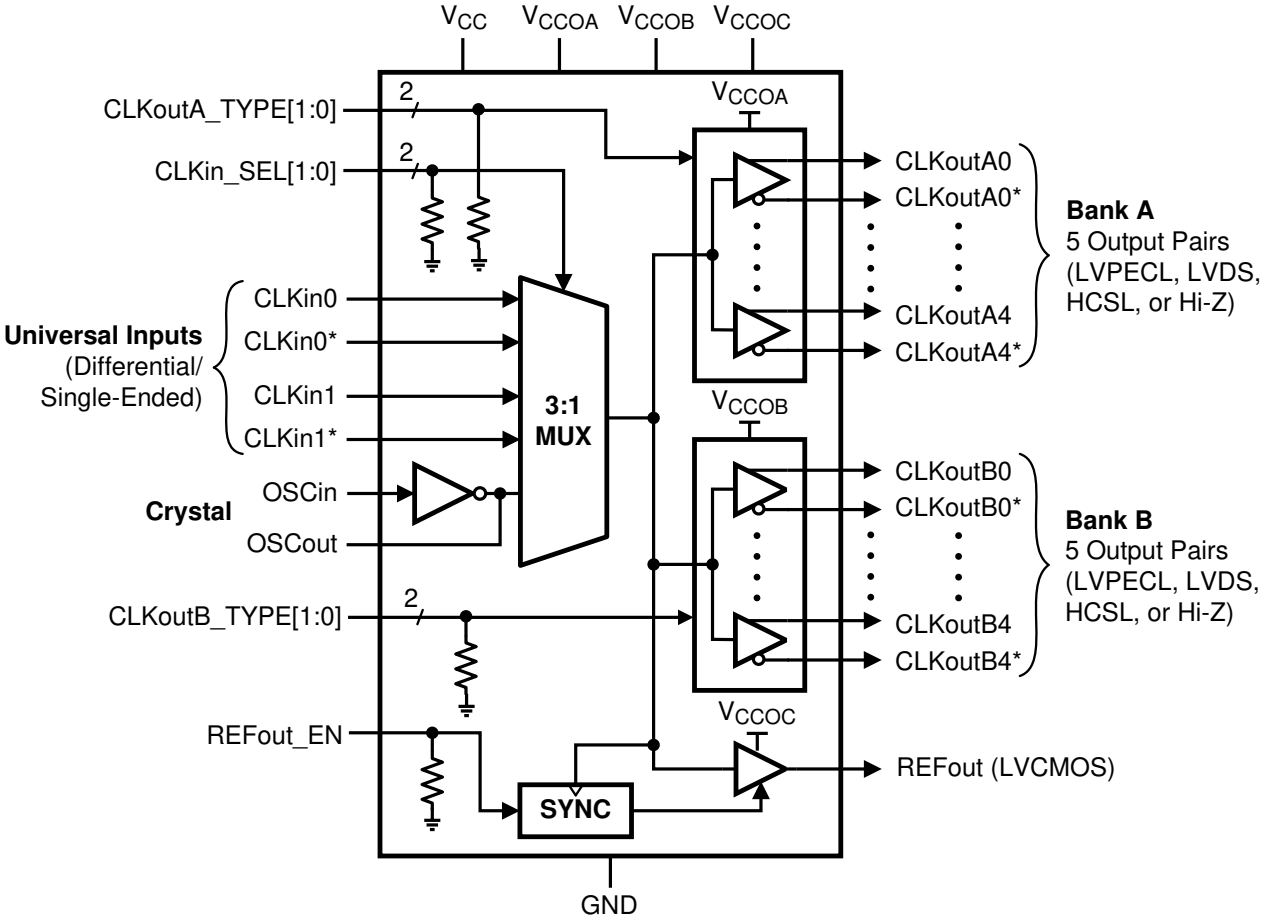


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 V_{CC} and V_{CCO} Power Supplies

The LMK00301 has separate 3.3V core (V_{CC}) and three independent 3.3V or 2.5V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) supplies. Output supply operation at 2.5V enables lower power consumption and output-level compatibility with 2.5V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to the respective V_{CCO} supply, while the output levels for LVDS and HCSL are relatively constant over the specified V_{CCO} range. See *Power Supply Recommendations* for additional supply related considerations, such as power dissipation, power supply bypassing, and power-supply ripple rejection (PSRR).

Note

Take care to verify the V_{CCO} voltages do not exceed the V_{CC} voltage to prevent turning-on the internal ESD protection circuitry.

8.4 Device Functional Modes

8.4.1 Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in Table 8-1. See *Driving the Clock Inputs* for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit starts up and the clock are distributed to all outputs. See *Crystal Interface* for more information. Alternatively, OSCin can be driven by a single-ended clock (up to 250MHz) instead of a crystal.

Table 8-1. Input Selection

CLKin_SEL1	CLKin_SEL0	SELECTED INPUT
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

Table 8-2 shows the output logic state versus input state when either CLKin0/CLKin0* or CLKin1/CLKin1* is selected. When OSCin is selected, the output state is an inverted copy of the OSCin input state.

Table 8-2. CLKin Input vs Output States

STATE OF SELECTED CLKin	STATE OF ENABLED OUTPUTS
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Logic low
CLKin logic low	Logic low
CLKin logic high	Logic high

8.4.2 Clock Outputs

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the CLKoutA_TYPE[1:0] and CLKoutB_TYPE[1:0] inputs, respectively, as shown in Table 8-3. For applications where all differential outputs are not required, any unused output pin must be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank is not used, TI recommends to disable (Hi-Z) the bank to reduce power. See *Termination and Use of Clock Drivers* for more information on output interface and termination techniques.

Note

For best soldering practices, the minimum trace length for any unused output pin must extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

Table 8-3. Differential Output Buffer Type Selection

CLKoutX_ TYPE1	CLKoutX_ TYPE0	CLKoutX BUFFER TYPE (BANK A OR B)
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

8.4.2.1 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the V_{CCO} voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in Table 8-4.

Table 8-4. Reference Output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout is enabled within three cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout is disabled within three cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1kΩ load to ground, then the output is pulled to low when disabled.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A common PCIe application, such as a server card, consists of several building blocks, which all need a reference clock. In the mostly used Common RefClk architecture, the clock is distributed from a single source to both RX and TX. This requires either a clock generator with high output count or a buffer like the LMK00301. The buffer simplifies the clocking tree and provides a cost and space optimized solution. While using a buffer to distribute the clock, consider the additive jitter. The LMK00301 is an ultra-low additive jitter PCIe clock buffer designed for all current and future PCIe generations.

9.2 Typical Application

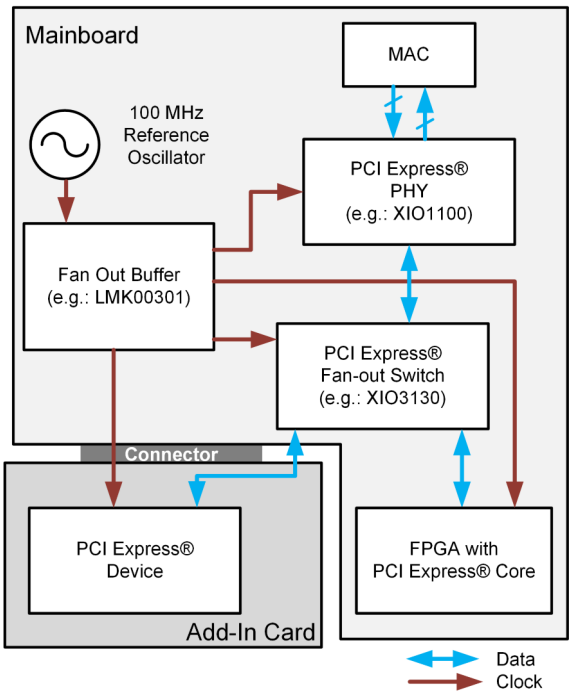


Figure 9-1. Example PCI Express Application

9.2.1 Design Requirements

9.2.1.1 Driving the Clock Inputs

The LMK00301 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept AC-coupled or DC-coupled, 3.3V or 2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in *Electrical Characteristics* . The device can accept a wide range of signals due to the wide input common-mode voltage range (V_{CM}) and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling can also be employed to shift the input signal to within the V_{CM} range. Refer to *Termination and Use of Clock Drivers* for signal interfacing and termination techniques.

To achieve the best possible phase noise and jitter performance, the input must have a high slew rate of 3V/ns (differential) or higher. Driving the input with a lower slew rate degrades the noise floor and jitter. For this reason,

TI recommends a differential signal input over a single-ended signal because this signal typically provides higher slew rate and common-mode-rejection. See the *Noise Floor vs CLKin Slew Rate* and *RMS Jitter vs CLKin Slew Rate* plots in *Typical Characteristics* section.

While TI recommends to drive the CLKin/CLKin* pair with a differential signal input, driving the pair with a single-ended clock is possible, provided the clock conforms to the Single-Ended Input specifications for CLKin pins listed in the *Electrical Characteristics*. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, place a 50Ω load resistor near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate must be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4V, so the input can be AC coupled as shown in Figure 9-2. The output impedance of the LVCMOS driver plus Rs must be close to 50Ω to match the characteristic impedance of the transmission line and load termination.

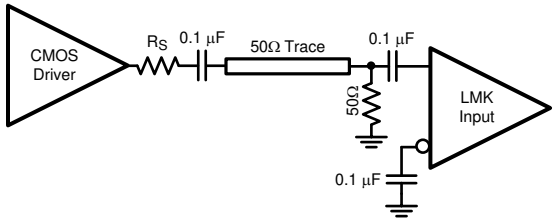


Figure 9-2. Single-Ended LVCMOS Input, AC Coupling

A single-ended clock can also be DC coupled to CLKinX as shown in Figure 9-3. Place a 50Ω load resistor near the CLKinX input for signal attenuation and line termination. Half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKinX, therefore CLKinX* must be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage must be within the specified input common-mode voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This verifies that the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

If the LVCMOS driver cannot achieve sufficient swing with a DC-terminated, 50Ω load at the CLKinX input as shown in Figure 9-3, then consider connecting the 50Ω load termination to ground through a capacitor (C_{AC}). This AC termination blocks the DC load current on the driver, so the voltage swing at the input is determined by the voltage divider formed by the source (Ro+Rs) and 50Ω load resistors. The value for C_{AC} depends on the trace delay, Td, of the 50Ω transmission line;

$$CAC \geq 3 \times Td / 50\Omega \quad (1)$$

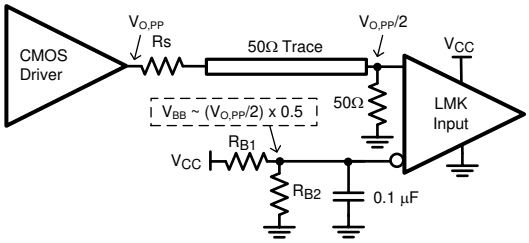


Figure 9-3. Single-Ended LVCMOS Input, DC Coupling With Common-Mode Biasing

If the crystal oscillator circuit is not used, driving the OSCin input with an single-ended external clock as shown in Figure 9-4 is possible. The input clock must be AC coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin must be left floating. While OSCin provides an alternative input to multiplex an external clock, TI recommends to use either universal input (CLKinX) because the inputs offer higher operating frequency, better common-mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

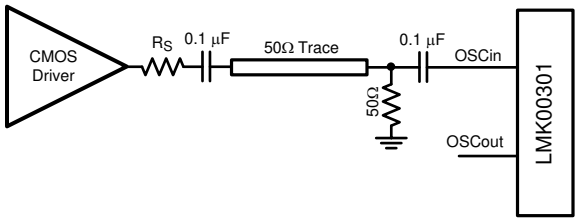


Figure 9-4. Driving OSCin With a Single-Ended Input

9.2.1.2 Crystal Interface

The LMK00301 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. Figure 9-5 shows the crystal interface.

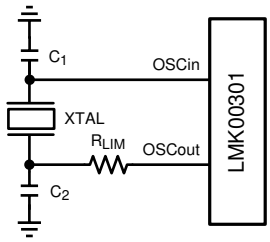


Figure 9-5. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but typically on the order of 18pF to 20pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 4pF typical) of the device and PCB stray capacitance (C_{STRAY} approximately 1pF to 3pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (2)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 2 can be rewritten in terms of C_1 only:

$$C_L = C_1{}^2 / (2 \times C_1) + C_{IN} + C_{STRAY} \quad (3)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY}) \times 2 \quad (4)$$

Electrical Characteristics provides crystal interface specifications with conditions that verify start-up of the crystal, but the electrical characteristics do not specify crystal power dissipation. The designer needs to verify the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level must be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}{}^2 \times R_{ESR} \times (1 + C_0/C_L)^2 \quad (5)$$

where

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the maximum equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the minimum shunt capacitance specified for the crystal

I_{RMS} can be measured using a current probe (for example, Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in Figure 9-5, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5kΩ.

9.2.2 Detailed Design Procedure

9.2.2.1 Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory must be followed for good impedance matching to prevent reflections.
- Clock drivers must be presented with the proper loads.
  - LVDS outputs are current drivers and require a closed current loop.
  - HCSL drivers are switched current outputs and require a DC path to ground through 50Ω termination.
  - LVPECL outputs are open emitter and require a DC path to ground.
- Receivers must be presented with a signal biased to the specified DC bias level (common-mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal must normally be AC coupled.

Driving a non-LVPECL or non-LVDS receiver with a LVDS or LVPECL driver is possible as long as the above guidelines are followed. Check the data sheet of the receiver or input being driven to determine the best termination and coupling method to verify that the receiver is biased at the optimum DC voltage (common-mode voltage).

9.2.2.1.1 Termination for DC Coupled Differential Operation

For DC coupled operation of an LVDS driver, terminate with 100Ω as close as possible to the LVDS receiver as shown in Figure 9-6.

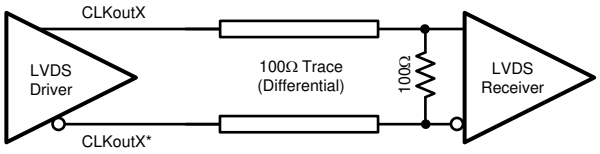


Figure 9-6. Differential LVDS Operation, DC Coupling, No Biasing by the Receiver

For DC coupled operation of an HCSL driver, terminate with 50Ω to ground near the driver output as shown in Figure 9-7. Series resistors, Rs, can be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50Ω termination resistors.

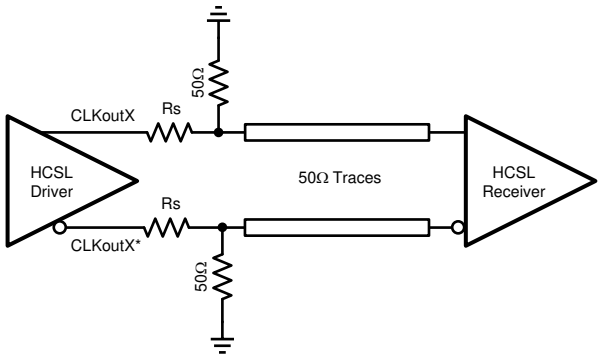


Figure 9-7. HCSL Operation, DC Coupling

For DC coupled operation of an LVPECL driver, terminate with 50Ω to Vcco - 2V as shown in Figure 9-8. Alternatively terminate with a Thevenin equivalent circuit as shown in Figure 9-9 for Vcco (output driver supply voltage) = 3.3V and 2.5V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to Vcco - 2V.

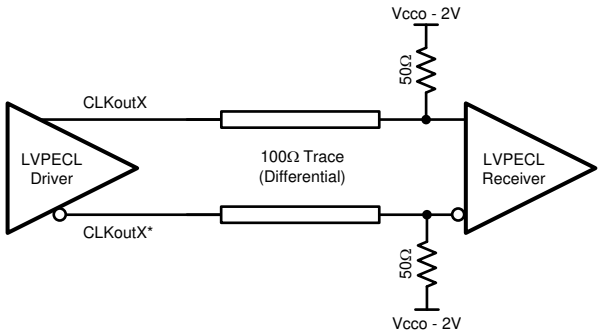
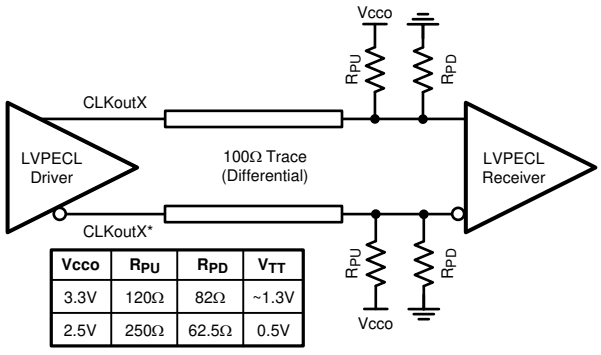


Figure 9-8. Differential LVPECL Operation, DC Coupling



Vcco	R_{PU}	R_{PD}	V_{TT}
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

Figure 9-9. Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

9.2.2.1.2 Termination for AC Coupled Differential Operation

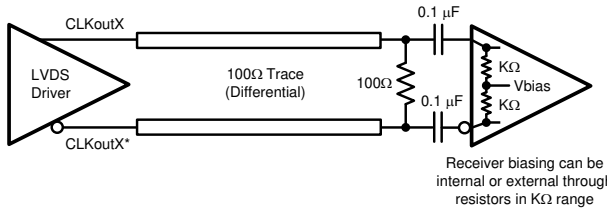
AC coupling allows for shifting the DC bias level (common-mode voltage) when driving different receiver standards. Since AC coupling prevents the driver from providing a DC bias voltage at the receiver, verify that the receiver is biased to the ideal DC level.

When driving differential receivers with an LVDS driver, the signal can be AC coupled by adding DC blocking capacitors; however the proper DC bias point needs to be established at both the driver side and the receiver side. The recommended termination scheme depends on whether the differential receiver has integrated termination resistors or not.

When driving a differential receiver without internal 100Ω differential termination, the AC coupling capacitors must be placed between the load termination resistor and the receiver to allow a DC path for proper biasing of the LVDS driver. This is shown in Figure 9-10. The load termination resistor and AC coupling capacitors must be placed as close as possible to the receiver inputs to minimize stub length. The receiver can be biased internally or externally to a reference voltage within the receiver's common mode input range through resistors in the kilo-ohm range.

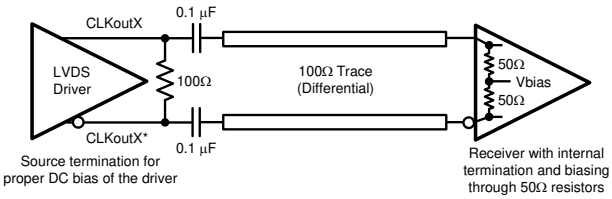
When driving a differential receiver with internal 100Ω differential termination, a source termination resistor must be placed before the AC coupling capacitors for proper DC biasing of the driver as shown in Figure 9-11. However, with a 100Ω resistor at the source and the load (that is, double terminated), the equivalent resistance seen by the LVDS driver is 50Ω which causes the effective signal swing at the input to be reduced by half. If a self-terminated receiver requires input swing greater than 250mVpp (differential) as well as AC coupling to the inputs, then the LVDS driver with the double-terminated arrangement in Figure 9-11 cannot always meet the minimum input swing requirement; alternatively, the LVPECL or HCSL output driver format with AC coupling is recommended to meet the minimum input swing required by the self-terminated receiver.

When using AC coupling with LVDS outputs, there can be a start-up delay observed in the clock output due to capacitor charging. The examples in Figure 9-10 and Figure 9-11 use 0.1µF capacitors, but this value can be adjusted to meet the start-up requirements for the particular application.



(a) LVDS DC termination with AC coupling at load

Figure 9-10. Differential LVDS Operation With AC Coupling to Receivers (a.) Without Internal 100Ω Termination



(b) LVDS DC termination with AC coupling at source and internal termination at load. Double termination at source and load will reduce swing by half.

Figure 9-11. Differential LVDS Operation With AC Coupling to Receivers (b.) With Internal 100Ω Termination

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 160Ω emitter resistors (or 91Ω for Vcco = 2.5V) close to the LVPECL driver to provide a DC path to ground as shown in Figure 9-15. For proper receiver operation, the signal must be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage (common mode voltage) for LVPECL receivers is 2V. Alternatively, a Thevenin equivalent circuit forms a valid termination as shown in Figure 9-12 for Vcco = 3.3V and 2.5V. Note: this Thevenin circuit is different from the DC coupled example in Figure 9-9, since the voltage divider is setting the input common-mode voltage of the receiver.

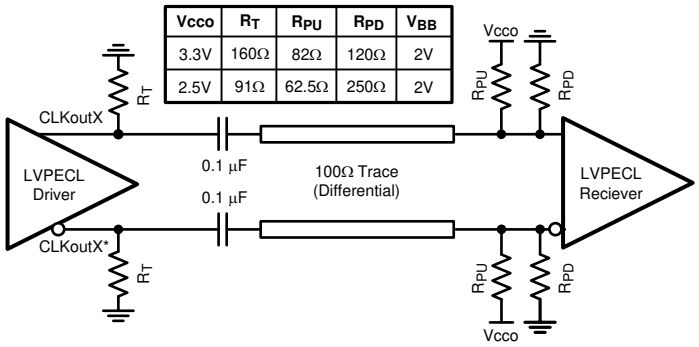


Figure 9-12. Differential LVPECL Operation, AC Coupling, Thevenin Equivalent

9.2.2.1.3 Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

Use an LVPECL driver as one or two separate 800mV p-p signals. When DC coupling one of the LMK00301 LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminate the unused driver. When DC coupling on of the LMK00301 LVPECL drivers, the termination must be 50Ω to Vcco - 2V as shown in Figure 9-13. The Thevenin equivalent circuit is also a valid termination as shown in Figure 9-14 for Vcco = 3.3V.

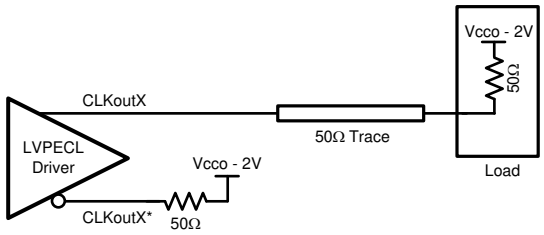


Figure 9-13. Single-Ended LVPECL Operation, DC Coupling

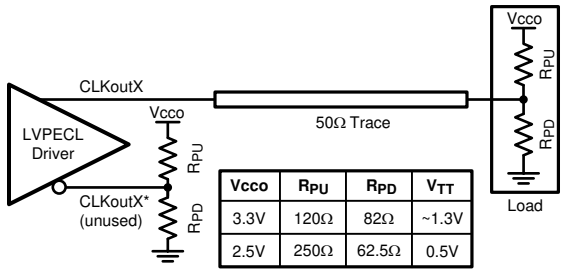


Figure 9-14. Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

When AC coupling an LVPECL driver use a 160Ω emitter resistor (or 91Ω for Vcco = 2.5V) to provide a DC path to ground and provide a 50Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL receivers is 2V. If the companion driver is not used, the companion driver must be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0VDC) is required for safe and proper operation. The internal 50Ω termination the test equipment correctly terminates the LVPECL driver being measured as shown in Figure 9-15. When using only one LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminated the unused driver.

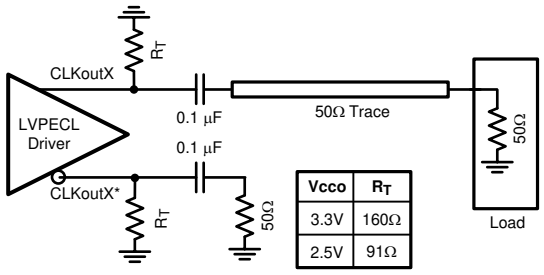


Figure 9-15. Single-Ended LVPECL Operation, AC Coupling

9.2.3 Application Curves

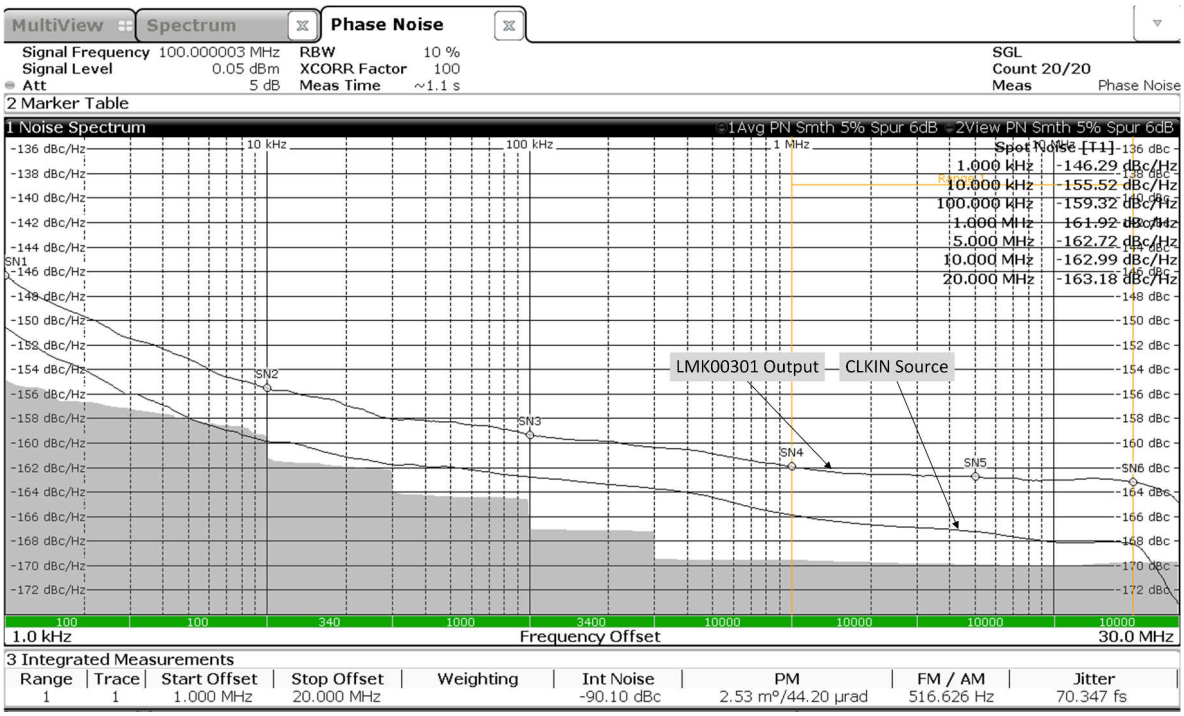


Figure 9-16. HCSL Phase Noise at 100MHz

9.3 Power Supply Recommendations

9.3.1 Power Supply Sequencing

For the LMK00301, when powering the V_{CC} and V_{CCO} pins from separate supply rails, the supplies are recommended by TI to reach the regulation point at approximately the same time while ramping up, or reach ground potential at the same time while ramping down. Using simultaneous or ratiometric power supply sequencing prevents internal current flow from V_{CC} to V_{CCO} pins that can occur when V_{CC} is powered before V_{CCO}.

For the LMK00301A, there is no power supply sequencing requirement between V_{CC} and V_{CCO}.

9.3.2 Current Consumption and Power Dissipation Calculations

The current consumption values specified in *Electrical Characteristics* can be used to calculate the total power dissipation and IC power dissipation for any device configuration. Use Equation 6 to calculate the total V_{CC} core supply current (I_{CC_TOTAL}):

$$I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANK\_A} + I_{CC\_BANK\_B} + I_{CC\_CMOS} \quad (6)$$

where

- I_{CC_CORE} is the current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- $I_{CC\_BANK\_A}$ is the current for Bank A and depends on output type (I_{CC_PECL}, I_{CC_LVDS}, I_{CC_HCSL}, or 0mA if disabled).
- $I_{CC\_BANK\_B}$ is the current for Bank B and depends on output type (I_{CC_PECL}, I_{CC_LVDS}, I_{CC_HCSL}, or 0mA if disabled).
- I_{CC_CMOS} is the current for the LVCMOS output (or 0mA if REFout is disabled).

Since the output supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) can be powered from 3 independent voltages, the respective output supply currents ($I_{CCO\_BANK\_A}$, $I_{CCO\_BANK\_B}$, I_{CCO_CMOS}) must be calculated separately.

I_{CCO_BANK} for either Bank A or B can be directly taken from the corresponding output supply current specification (I_{CCO_PECL}, I_{CCO_LVDS}, or I_{CCO_HCSL}) **provided the output loading matches the specified conditions**. Otherwise, I_{CCO_BANK} must be calculated as follows:

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N \times I_{OUT\_LOAD}) \quad (7)$$

where

- I_{BANK_BIAS} is the output bank bias current (fixed value).
- I_{OUT_LOAD} is the DC load current per loaded output pair.
- N is the number of loaded output pairs in the bank (N = 0 to 5).

Table 9-1 shows the typical I_{BANK_BIAS} values and I_{OUT_LOAD} expressions for the three differential output types.

For LVPECL, using a larger termination resistor (R_T) to ground instead of terminating with 50Ω to $V_{TT} = V_{CCO} – 2V$ is possible; this technique is commonly used to eliminate the extra termination voltage supply (V_{TT}) and potentially reduce device power dissipation at the expense of lower output swing. For example, when V_{CCO} is 3.3V, a R_T value of 160Ω to ground eliminates the 1.3V termination supply without sacrificing much output swing. In this case, the typical I_{OUT_LOAD} is 25mA, so I_{CCO_PECL} for a fully-loaded bank reduces to 158mA (versus 165mA with 50Ω resistors to $V_{CCO} – 2V$).

Table 9-1. Typical Output Bank Bias and Load Currents

CURRENT PARAMETER	LVPECL	LVDS	HCSL
I_{BANK_BIAS}	33mA	34mA	6mA
I_{OUT_LOAD}	$(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T$	0mA (No DC load current)	V_{OH}/R_T

When the current consumption is calculated or known for each supply, the total power dissipation (P_{TOTAL}) can be calculated as:

$$P_{TOTAL} = (V_{CC} \times I_{CC\_TOTAL}) + (V_{CCOA} \times I_{CCO\_BANK\_A}) + (V_{CCOB} \times I_{CCO\_BANK\_B}) + (V_{CCOC} \times I_{CCO\_CMOS}) \quad (8)$$

If the device configuration has LVPECL or HCSL outputs, then calculating the power dissipated in any termination resistors (P_{RT_PECL} and P_{RT_HCSL}) and in any termination voltages (P_{VTT}) is also necessary. The external power dissipation values can be calculated as follows:

$$P_{RT\_PECL} \text{ (per LVPECL pair)} = (V_{OH} - V_{TT})^2/R_T + (V_{OL} - V_{TT})^2/R_T \quad (9)$$

$$P_{VTT\_PECL} \text{ (per LVPECL pair)} = V_{TT} * [(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T] \quad (10)$$

$$P_{RT\_HCSL} \text{ (per HCSL pair)} = V_{OH}{}^2 / R_T \quad (11)$$

Finally, the IC power dissipation (P_{DEVICE}) can be computed by subtracting the external power dissipation values from P_{TOTAL} as follows:

$$P_{DEVICE} = P_{TOTAL} – N_1 \times (P_{RT\_PECL} + P_{VTT\_PECL}) – N_2 \times P_{RT\_HCSL} \quad (12)$$

where

- N_1 is the number of LVPECL output pairs with termination resistors to V_{TT} (typically Vcco - 2V or GND).
- N_2 is the number of HCSL output pairs with termination resistors to GND.

9.3.2.1 Power Dissipation Example #1: Separate V_{CC} and V_{CCO} Supplies with Unused Outputs

This example shows how to calculate IC power dissipation for a configuration with separate V_{CC} and V_{CCO} supplies and unused outputs. Because some outputs are not used, the I_{CCO_PECL} value specified in *Electrical Characteristics* cannot be used directly, and output bank current (I_{CCO_BANK}) must be calculated to accurately estimate the IC power dissipation.

- V_{CC} = 3.3V, V_{CCOA} = 3.3V, V_{CCOB} = 2.5V. Typical I_{CC} and I_{CCO} values.
- CLKin0/CLKin0* input is selected.
- Bank A is configured for LVPECL: 4 pairs used with R_T = 50Ω to $V_T = V_{CCO} – 2V$ (1 pair unused).
- Bank B is configured for LVDS: 3 pairs used with R_L = 100Ω differential (2 pairs unused).
- REFout is disabled.
- T_A = 85°C

Using the current and power calculations from the previous section, we can compute P_{TOTAL} and P_{DEVICE}.

- From Equation 6: I_{CC_TOTAL} = 8.5mA + 20mA + 26mA + 0mA = 54.5mA
- From Table 9-1: I_{OUT_LOAD} (LVPECL) = (1.6V – 0.5V) 50Ω + (0.75V – 0.5V)/50Ω = 27mA
- From Equation 7: $I_{CCO\_BANK\_A}$ = 33mA + (4 × 27mA) = 141mA
- From Equation 8: P_{TOTAL} = (3.3V × 54.5mA) + (3.3V × 141mA) + (2.5V × 34mA)] = 730mW
- From Equation 9: $P_{RT\_PECL} = ((2.4V – 1.3V)^2/50\ Ω) + ((1.55V – 1.3V)^2/50\ Ω)$ = 25.5mW (per output pair)
- From Equation 10: P_{VTT_PECL} = 0.5V × [((2.4V – 1.3V) / 50Ω) + ((1.55V – 1.3V) / 50Ω)] = 13.5mW (per output pair)
- From Equation 11: P_{RT_HCSL} = 0mW (no HCSL outputs)
- From Equation 12: P_{DEVICE} = 730mW – (4 × (25.5mW + 13.5mW)) – 0mW = 574mW

In this example, the IC device dissipates about 574mW or 79% of the total power (730mW), while the remaining 21% is dissipated in the emitter resistors (102mW for 4 pairs) and termination voltage (54mW into $V_{CCO} – 2V$).

Based on the thermal resistance junction-to-case ($R_{θJA}$) of 28.5°C/W, the estimated die junction temperature is approximately 16.4°C above ambient, or 101.4°C when T_A = 85°C.

9.3.2.2 Power Dissipation Example #2: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate **worst-case power dissipation**. In this case, the maximum supply voltage and supply current values specified in *Electrical Characteristics* are used.

- Maximum $V_{CC} = V_{CCO}$ = 3.465V. Maximum I_{CC} and I_{CCO} values
- CLKin0/CLKin0* input is selected
- Banks A and B are configured for LVPECL: all outputs terminated with 50Ω to $V_T = V_{CCO} – 2V$
- REFout is enabled with 5pF load
- T_A = 85°C

Using the *maximum* supply current and power calculations from the previous section, we can compute P_{TOTAL} and P_{DEVICE}.

- From Equation 6: I_{CC_TOTAL} = 10.5mA + 27mA + 27mA + 5.5mA = 70mA
- From I_{CCO_PECL} max spec: $I_{CCO\_BANK\_A} = I_{CCO\_BANK\_B}$ = 197mA
- From Equation 8: P_{TOTAL} = 3.465V × (70mA + 197mA + 197mA + 10mA) = 1642.4mW
- From Equation 9: $P_{RT\_PECL} = ((2.57V – 1.47V)^2/50Ω) + ((1.72V – 1.47V)^2/50\ Ω)$ = 25.5mW (per output pair)
- From Equation 10: P_{VTT_PECL} = 1.47V × [((2.57V – 1.47V) / 50Ω) + ((1.72V – 1.47V) / 50Ω)] = 39.5mW (per output pair)
- From Equation 11: P_{RT_HCSL} = 0mW (no HCSL outputs)

- From Equation 12: P_{DEVICE} = 1642.4mW – (10 × (25.5mW + 39.5mW)) – 0mW = 992.4mW

In this worst-case example, the IC device dissipates approximately 992.4mW or 60% of the total power (1642.4mW), while the remaining 40% dissipates in the LVPECL emitter resistors (255mW for 10 pairs) and termination voltage (395mW into V_{CCO} – 2V).

Based on θ_{JA} of 28.5°C/W, the estimated die junction temperature is about 28.3°C above ambient, or 113.3°C when T_A = 85°C.

9.3.3 Power Supply Bypassing

The V_{CC} and V_{CCO} power supplies must have a high-frequency bypass capacitor, such as 0.1µF or 0.01µF, placed very close to each supply pin. Place 1µF to 10µF decoupling capacitors nearby the device between the supply and ground planes. All bypass and decoupling capacitors must have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

9.3.3.1 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, and so forth. While power supply bypassing can help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00301, the signal can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00301, power supply ripple rejection, or PSRR, is measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal is injected onto the V_{CCO} supply. Figure 9-17 shows the PSRR test setup.

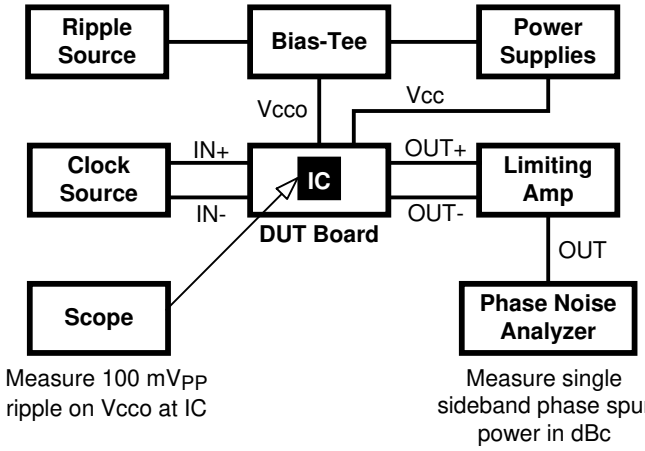


Figure 9-17. PSRR Test Setup

A signal generator is used to inject a sinusoidal signal onto the V_{CCO} supply of the DUT board, and the peak-to-peak ripple amplitude is measured at the V_{CCO} pins of the device. A limiting amplifier is used to remove amplitude modulation on the differential output clock and convert the amplitude modulation to a single-ended signal for the phase noise analyzer. The phase spur level measurements are taken for clock frequencies of 156.25MHz and 312.5MHz under the following power supply ripple conditions:

- Ripple amplitude: 100mVpp on V_{CCO} = 2.5V
- Ripple frequencies: 100kHz, 1MHz, and 10MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ\ (ps\ pk\text{-}pk) = [(2\times10^{(PSRR\ /\ 20)}) / (\pi\times f_{CLK})] \times 10^{12} \quad (13)$$

The *PSRR vs. Ripple Frequency* plots in *Typical Characteristics* show the ripple-induced phase spur levels for the differential output types at 156.25MHz and 312.5MHz . The LMK00301 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range for all differential output types. The phase spur levels for LVPECL are below –64dBc at 156.25MHz and below –62dBc at 312.5MHz. Using Equation 13, these phase spur levels translate to Deterministic Jitter values of 2.57ps pk-pk at 156.25MHz and 1.62ps pk-pk at 312.5MHz.

Testing has shown that the PSRR performance of the device improves for V_{CCO} = 3.3V under the same ripple amplitude and frequency conditions.

9.3.4 Thermal Management

Power dissipation in the LMK00301 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature must be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power dissipation times $R_{\theta JA}$ must not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to provide adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 9-18. More information on soldering WQFN packages can be obtained at: http://www.ti.com/packaging.

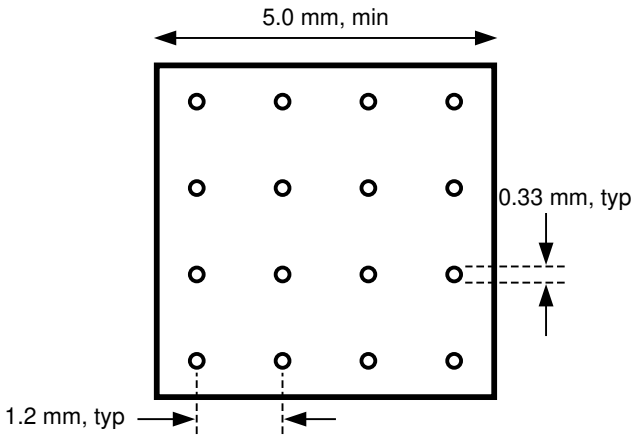


Figure 9-18. Recommended Land and Via Pattern

To minimize junction temperature, use a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area can be plated or solder coated to prevent corrosion but must not have conformal coating (if possible), which can provide thermal insulation. The vias shown in Figure 9-18 must connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where heat can be more effectively dissipated.

9.4 Layout

9.4.1 Layout Guidelines

Consider the following guidelines for this device:

- Keep the connections between the bypass capacitors and the power supply on the device as short as possible.
- Ground the other side of the capacitor using a low impedance connection to the ground plane.
- If the capacitors are mounted on the back side, 0402 components can be employed. However, soldering to the Thermal Dissipation Pad can be difficult
- For component side mounting, use 0201 body size capacitors to facilitate signal routing.

9.4.2 Layout Example

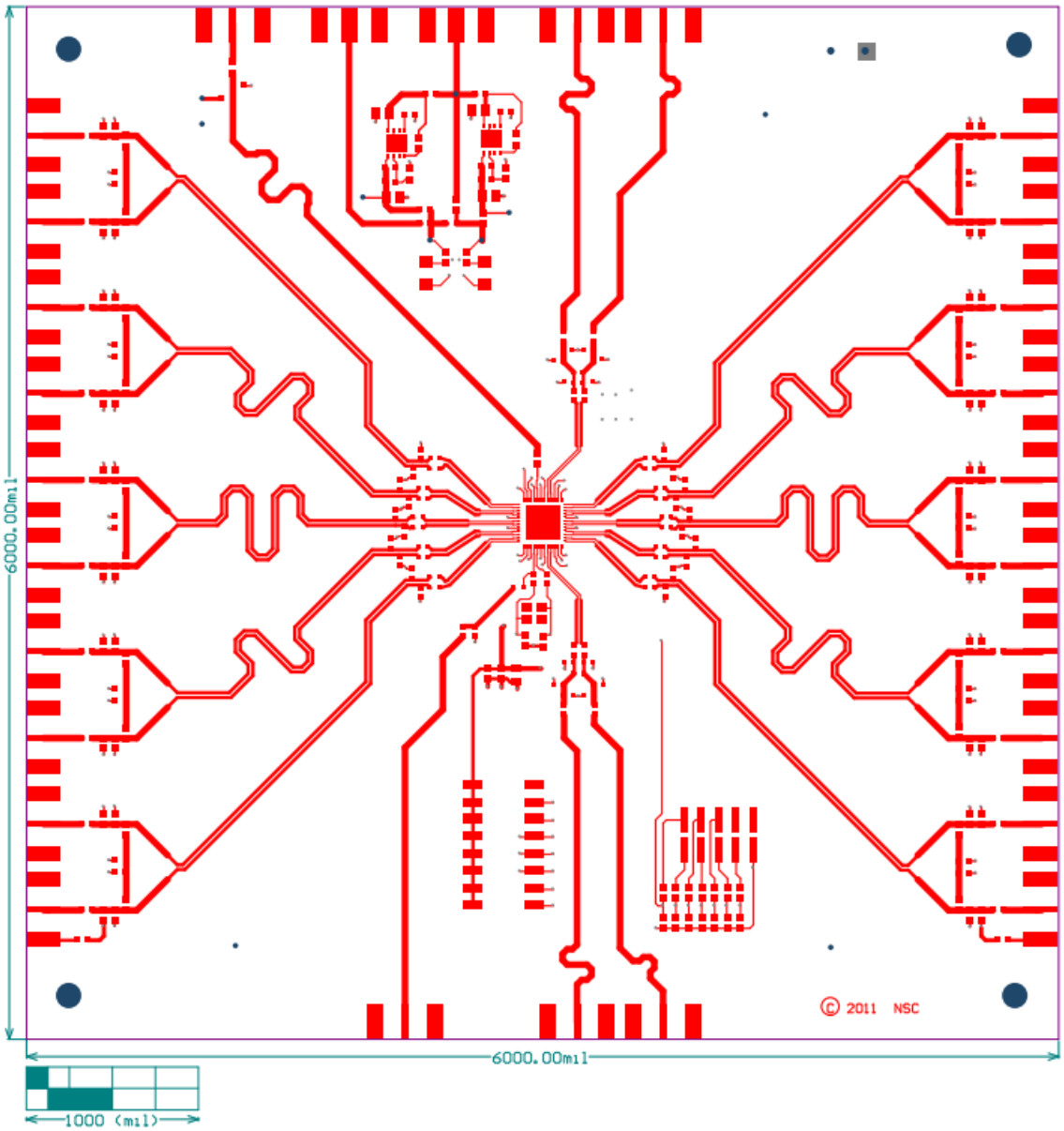


Figure 9-19. LMK00301 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Common Data Transmission Parameters and their Definitions*, application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (May 2023) to Revision K (October 2025)	Page
• Updated the *Features* and *Applications* sections to include PCIe Gen 7.0 specifications	1
• Updated throughout the *Specifications* section to include PCIe Gen 7.0 specifications	6

Changes from Revision I (December 2017) to Revision J (May 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Device Functional Modes*, *Application Information*, *Typical Application*, and *Layout* sections	1
• Added Frequency Range for LVPECL, LVDS, HCSL and LVCMOS in *Features* section	1
• Added PCIe 5.0 and 6.0 to *Applications*	1
• Added LMK00301A in *Package Information* Table	1
• Added PCIe 5.0 and PCIe 6.0 additive jitter specifications in *Electrical Characteristics*	7
• Changed HCSL *Maximum Output Frequency Range* to 800MHz *Electrical Characteristics*	7
• Added test conditions for HCSL *Duty Cycle* and ΔV_{CROSS} in *Electrical Characteristics*	7
• Updated typical plots for *HCSL, LVDS and LVPECL Phase Noise at 100MHz* in *Typical Characteristics* section.	14
• Added typical plots for *HCSL Output Swing (V_{OD}) vs Frequency* in *Typical Characteristics* section	14

- Moved *Clock Input* and *Clock Outputs* to *Device Functional Modes* section
- Added application use case in *Application Information*
- Added PCI Express Application example in *Typical Application* section
- Added *Driving the Clock Input* and *Crystal Interface* topics in *Design Requirement* section
- Moved *Termination and Use of Clock Drivers* in *Detailed Design Procedure* section
- Added *HCSL Phase Noise plot* in *Application Performance Plots* section
- Added layout guidelines in *Layout Guidelines* section
- Added PCB layout example for LMK00301 in *Layout Example* section

Changes from Revision H (March 2016) to Revision I (December 2017) **Page**

- Added and updated info to the following sections: *Applications; Description; Electrical Characteristics: Current Consumption; Electrical Characteristics: HCSL Outputs; and Power Supply Sequencing*
- Added LMK00301A orderable
- Added PCIe 4.0 to *Applications*
- Included difference between LMK00301 and LMK00301A to *Description*
- Added *Device Comparison Table*
- Added data for Icc and Icco of LMK00301A LVDS Driver in *Electrical Characteristics: Current Consumption*
- Added PCIe 4.0 Additive Jitter Spec in *Electrical Characteristics: HCSL Outputs*
- Added note about specs for LMK00301 and LMK00301A in footnote (2) of *Electrical Characteristics*
- Added short paragraph about LMK00301A in *Power Supply Sequencing*

Changes from Revision G (May 2013) to Revision H (March 2016) **Page**

- Added "Ultra-Low Additive Jitter" to document title
- Added, updated, or renamed the following sections: *Specifications*; *Detailed Description*; *Application and Implementation*; *Power Supply Recommendations*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information*
- Changed Cin (typ) from 1pF to 4pF (based on updated test method) in *Electrical Characteristics: Crystal Interface*.
- Added “Additive RMS Jitter, Integration Bandwidth 10kHz to 20MHz” parameter with 100MHz and 156.25MHz Test conditions, Typical values, Max values, and footnotes in Electrical Characteristics: LVPECL Outputs
- Added “Additive RMS Jitter, Integration Bandwidth 10kHz to 20MHz” parameter with 100MHz and 156.25MHz Test conditions, Typical values, Max values, and footnotes in Electrical Characteristics: LVDS Outputs
- Added footnote for V_{I_SE} parameter in the *Electrical Characteristics* table
- Added new paragraph at end of *Driving the Clock Inputs*
- Changed Cin = 4pF (typ, based on updated test method) in *Crystal Interface*
- Added POWER SUPPLY SEQUENCING

Changes from Revision F (February 2013) to Revision G (May 2013) **Page**

- Changed *Target Applications* by adding additional applications to the second and third bullets, and removing High-Speed and Serial Interfaces from first bullet.
- Changed V_{CM} text to condition for V_{IH} to V_{CM} parameters
- Deleted V_{IH} min value from Electrical Characteristics Table
- Deleted V_{IL} max value from Electrical Characteristics table
- Added V_{I_SE} parameter and spec limits with corresponding table note to Electrical Characteristics Table
- Changed third paragraph in *Driving the Clock Inputs* section to include CLKin* and LVCMOS text. Revised to better correspond with information in Electrical Characteristics Table.
- Changed bypass cap text to signal attenuation text of the fourth paragraph in *Driving the Clock Inputs* section

- Changed *Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing* image with revised graphic. 24
- Added text to second paragraph of *Termination for AC Coupled Differential Operation* to explain graphic update to *Differential LVDS Operation with AC Coupling to Receivers* 29
- Changed graphic for *Differential LVDS Operation, AC Coupling, No Biasing by the Receiver* and updated caption. 29

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK00301ARHSR	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301A
LMK00301ARHSR.A	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301A
LMK00301ARHST	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301A
LMK00301ARHST.A	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301A
LMK00301SQ/NOPB	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301
LMK00301SQ/NOPB.A	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301
LMK00301SQE/NOPB	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301
LMK00301SQE/NOPB.A	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301
LMK00301SQX/NOPB	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301
LMK00301SQX/NOPB.A	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LMK00301

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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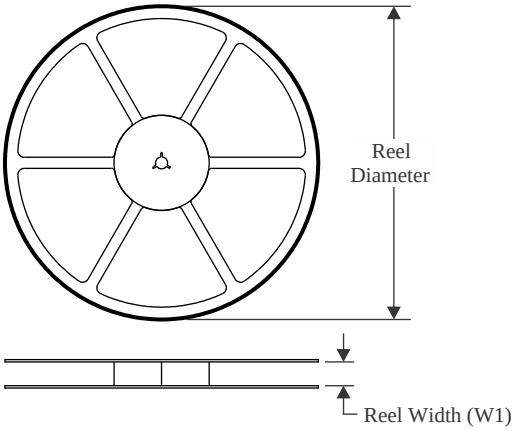
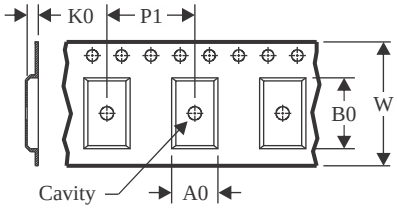
TAPE AND REEL INFORMATION

REEL DIMENSIONS

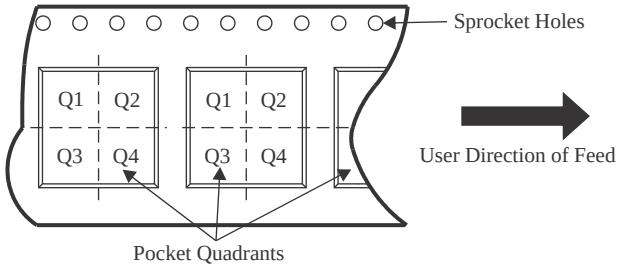


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

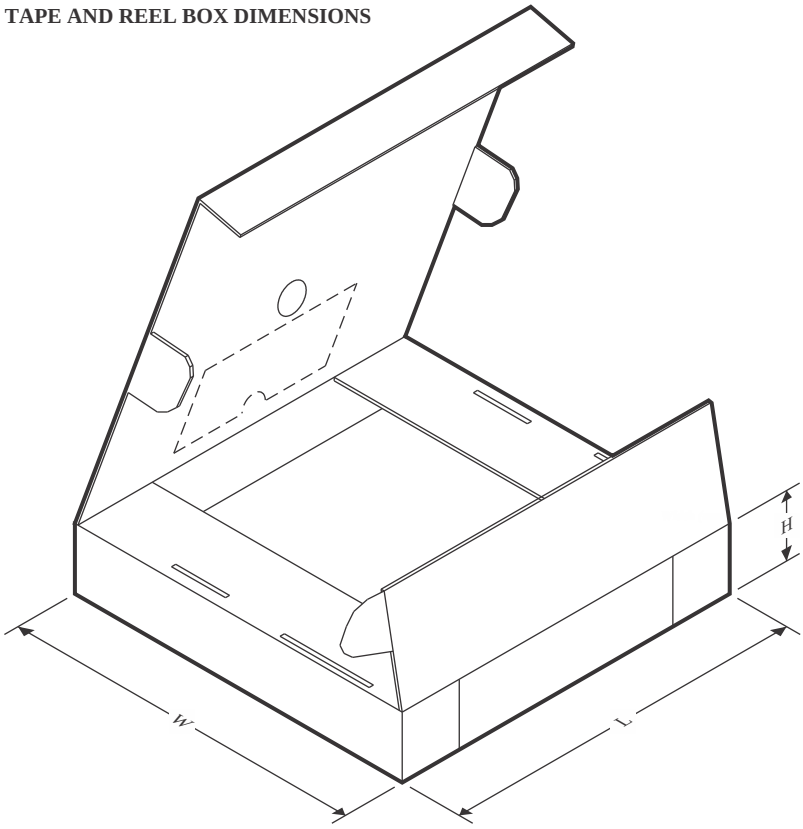
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00301ARHSR	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK00301ARHST	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK00301SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK00301SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK00301SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

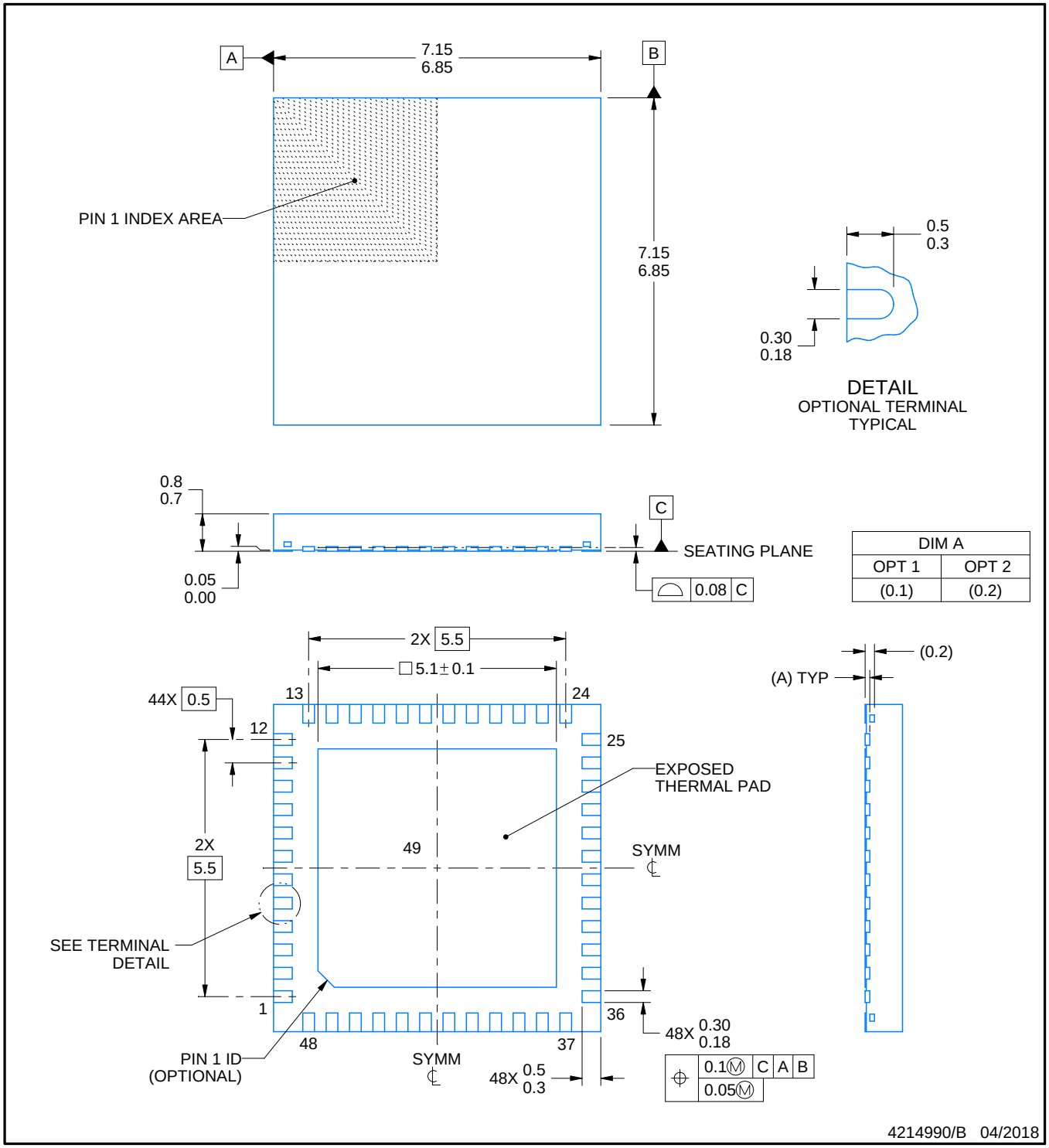
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00301ARHSR	WQFN	RHS	48	2500	356.0	356.0	36.0
LMK00301ARHST	WQFN	RHS	48	250	208.0	191.0	35.0
LMK00301SQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
LMK00301SQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
LMK00301SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RHS0048A

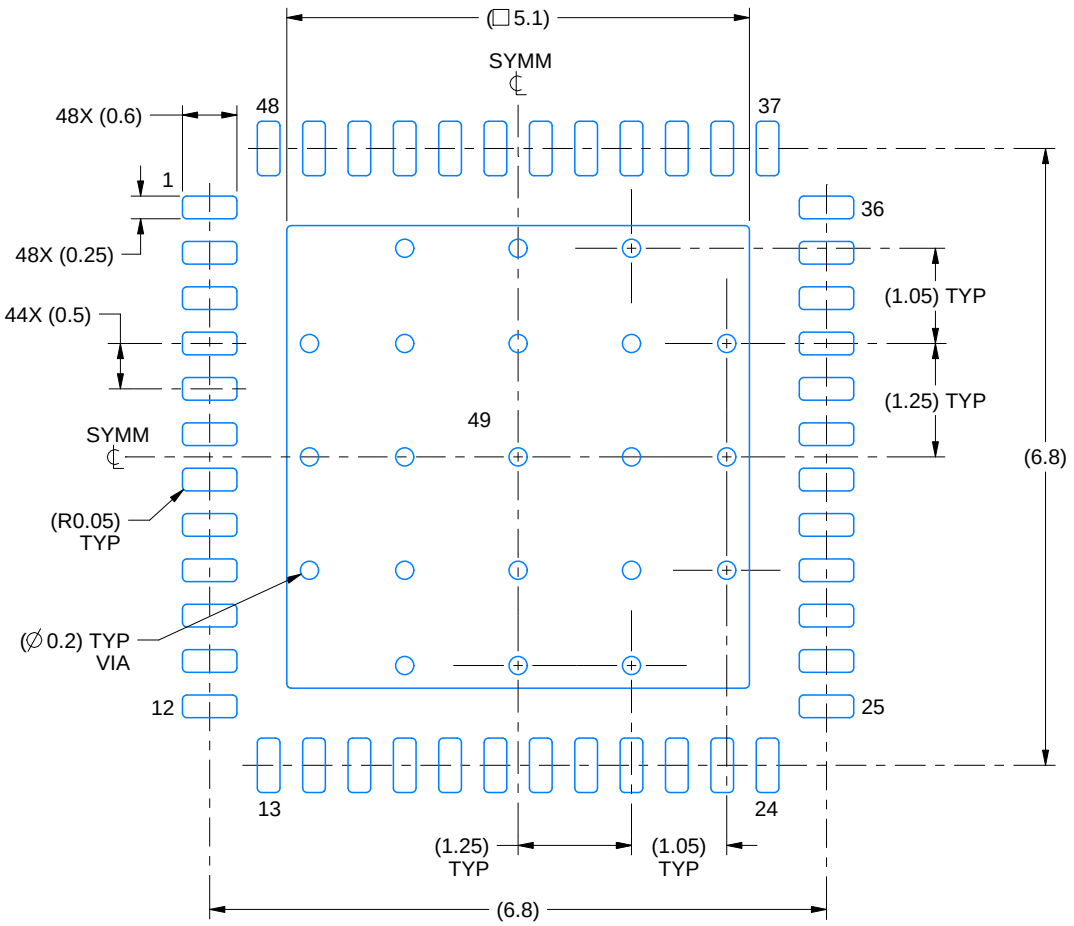
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

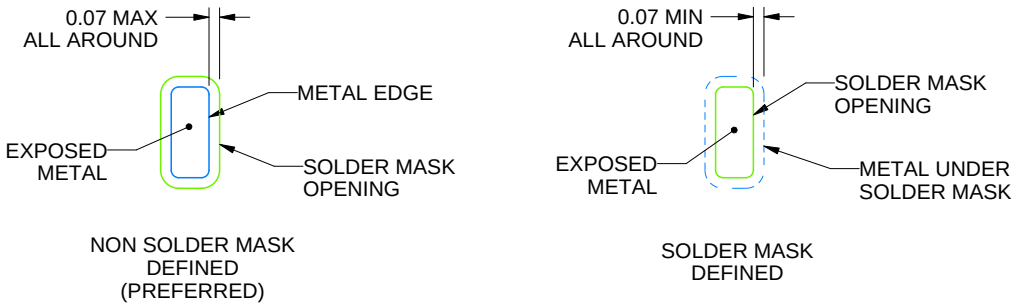


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

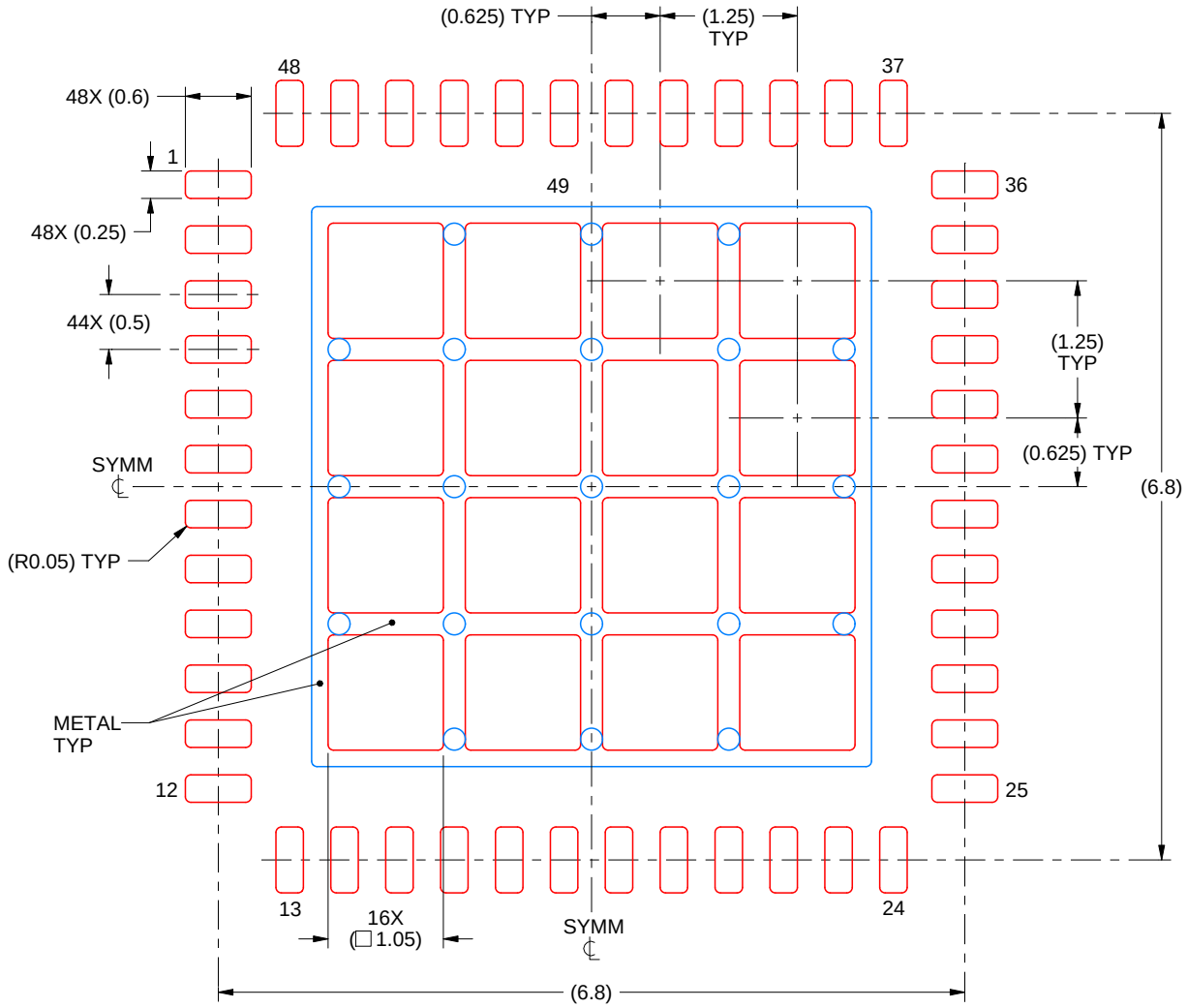


SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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