LP3971 Power Management Unit for Advanced Application Processors

Check for Samples: LP3971

FEATURES

- **Compatible with Advanced Applications Processors Requiring DVM (Dynamic Voltage Management)**
- **Three Buck Regulators for Powering High Current Processor Functions or I/O's**
- **6 LDO's for Powering RTC, Peripherals, and I/O's**
- **Backup Battery Charger with Automatic Switch for Lithium-Manganese Coin Cell Batteries and Super Capacitors**
- **I^2C Compatible High Speed Serial Interface**
- **Software Control of Regulator Functions and Settings**
- **Precision Internal Reference**
- **Thermal Overload Protection**
- **Current Overload Protection**
- **Tiny 40-pin 5x5 mm WQFN Package**

APPLICATIONS

- **PDA Phones**
- **Smart Phones**
- **Personal Media Players**
- **Digital Cameras**
- **Application Processors**
  - **Marvell PXA**
  - **Freescale**
  - **Samsung**

KEY SPECIFICATIONS

- **Buck Regulators**
  - **Programmable V_{OUT} from 0.725 to 3.3V**
  - **Up to 95% Efficiency**
  - **Up to 1.6A Output Current**
  - **±3% Output Voltage Accuracy**
- **LDO's**
  - **Programmable VOUT of 1.0V–3.3V**
  - **±3% output voltage accuracy**
  - **150/300/370 mA output currents**
    - **LDO RTC 30 mA**
    - **LDO 1 300 mA**
    - **LDO 2 150 mA**
    - **LDO 3 150 mA**
    - **LDO 4 150 mA**
    - **LDO 5 370 mA**
  - **100 mV (typ) dropout**

DESCRIPTION

The LP3971 is a multi-function, programmable Power Management Unit, designed especially for advanced application processors. The LP3971 is optimized for low power handheld applications and provides 6 low dropout, low noise linear regulators, three DC/DC magnetic buck regulators, a back-up battery charger and two GPIO's. A high speed serial interface is included to program individual regulator output voltages as well as on/off control.

Simplified Application Circuit

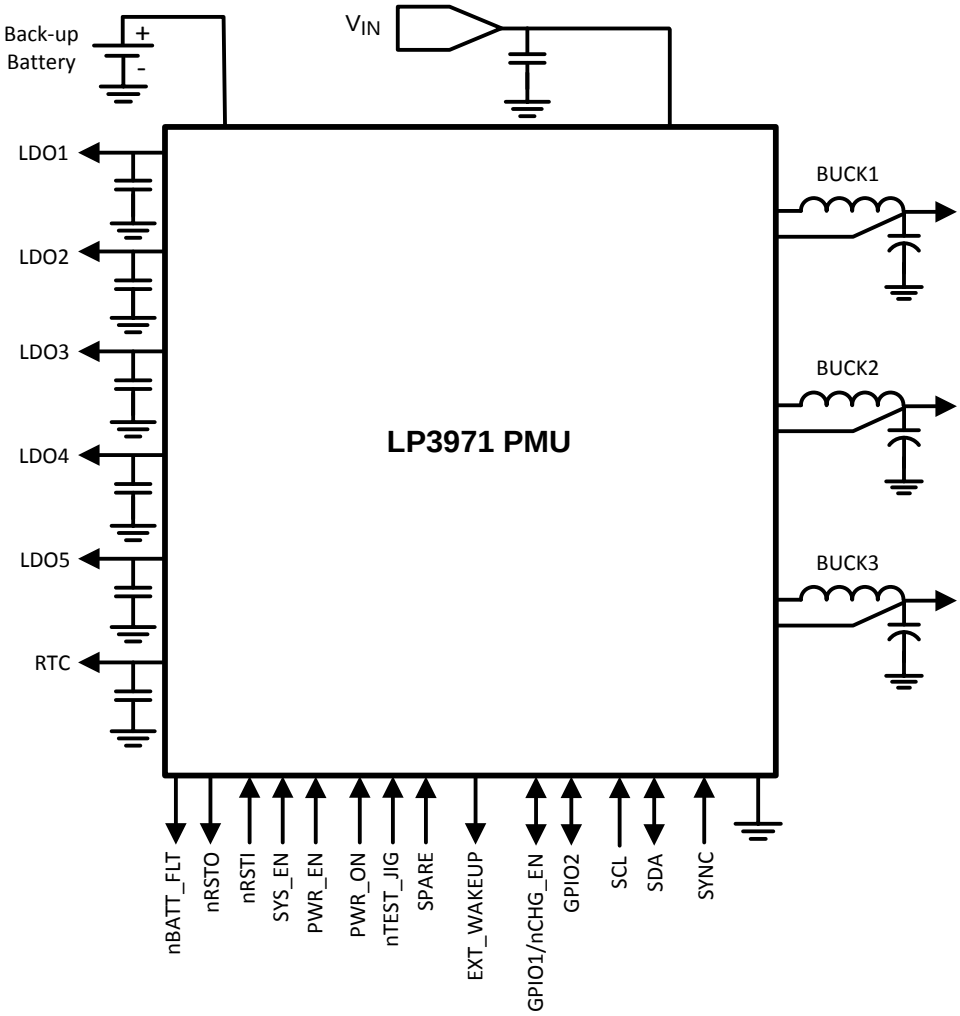
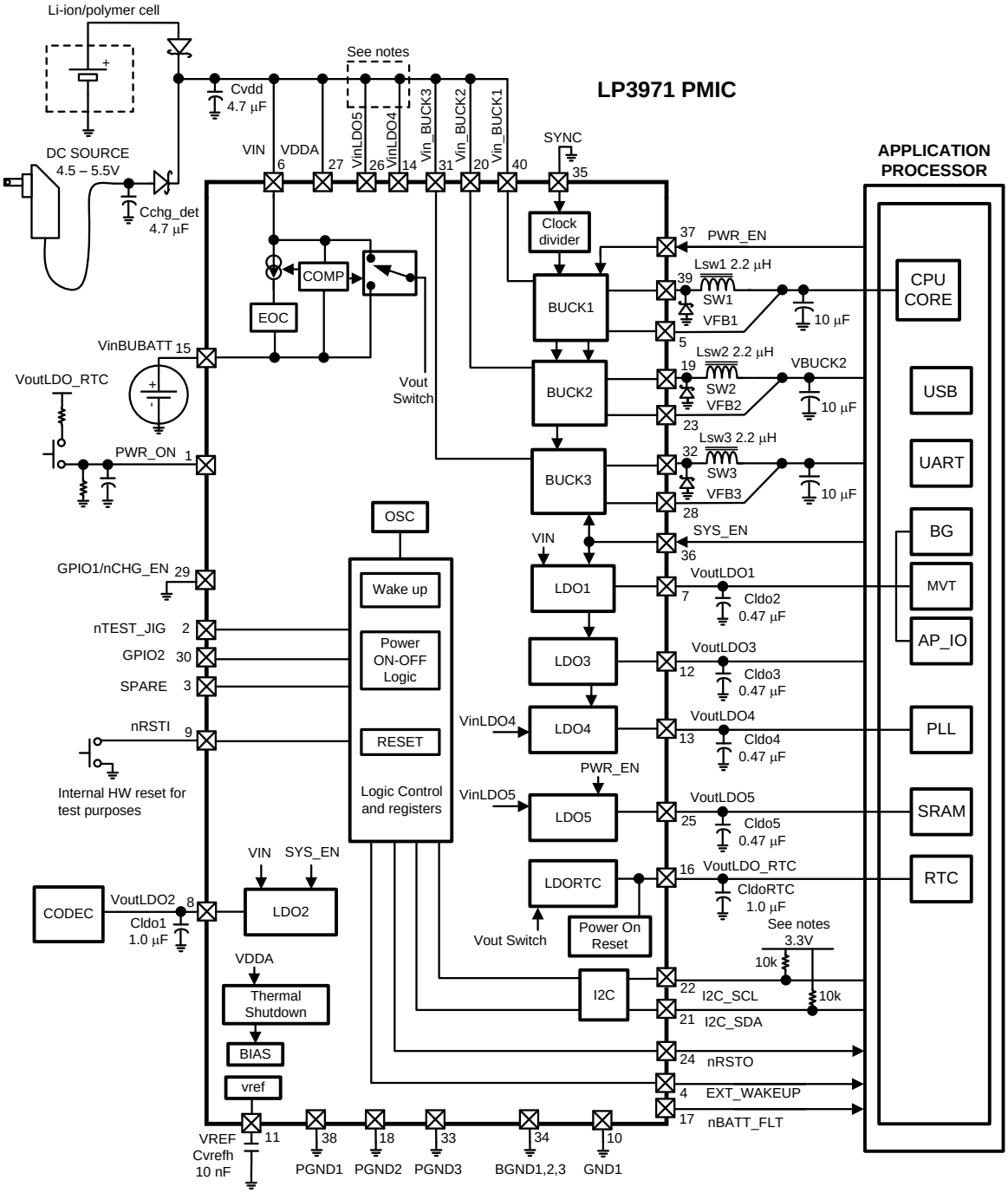


Figure 1.

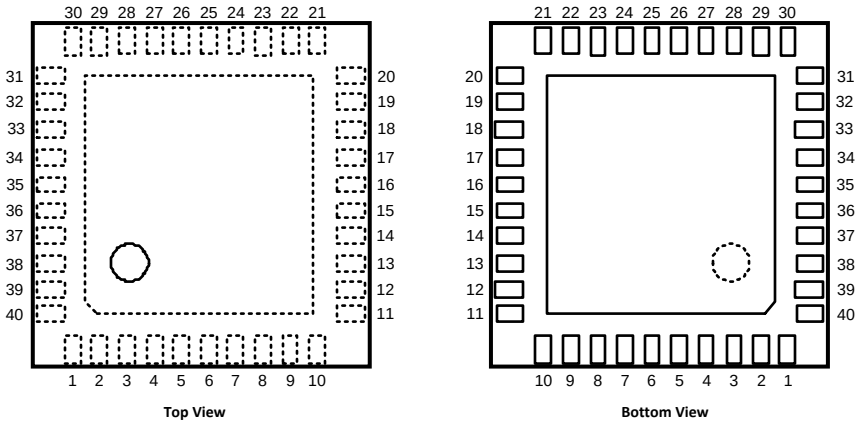


- The I^2C lines are pulled up via a I/O source
- V_{IN}LDO4, 5 can either be powered from main battery source, or by a buck regulator or V_{IN}.

Figure 2.

Connection Diagrams

Figure 3. 40-Pin WQFN
Package Number RSB0040A



Note: Circle marks Pin 1 position.

Table 1. Default V_{OUT} Coding

Z	Default V_{OUT}
0	1.3
1	1.8
2	2.5
3	2.8
4	3.0
5	3.3
6	1.0
7	1.4
8	1.2
9	1.25
A	1.35
Y	Default Enable Option: SYS_EN or PWR_EN

Pin Descriptions(1)

Pin #	Name	I/O	Type	Description
1	PWR_ON	I	D	This is an active HI push button input which can be used to signal PWR_ON and PWR_OFF events to the CPU by controlling the ext_wakup [pin4] and select contents of register 8H'02
2	nTEST_JIG	I	D	This is an active LOW input signal used for detecting an external HW event. The response is seen in the ext_wakup [pin4] and select contents of register 8H'02
3	SPARE	I	D	This is an input signal used for detecting a external HW event. The response is seen in the ext_wakup [pin4] and select contents of register 8H'02. The polarity on this pin is assignable
4	EXT_WAKEUP	O	D	This pin generates a single 10mS pulse output to CPU in response to input from pin[s] 1, 2, and 3. Flags CPU to interrogate register 8H'02
5	FB1	I	A	Buck1 input feedback terminal
6	V_{IN}	I	PWR	Battery Input (Internal circuitry and LDO1-3 power input)
7	V_{OUT} LDO1	O	PWR	LDO1 output
8	V_{OUT} LDO2	O	PWR	LDO2 output

(1) A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin I: Input Pin I/O: Input/Output Pin O: Output Pin
Note: In this document active low logic items are prefixed with a lowercase “n”

Pin Descriptions[1] (continued)

Pin #	Name	I/O	Type	Description
9	nRSTI	I	D	Active low Reset pin. Signal used to reset the IC (by default is pulled high internally). Typically a push button reset.
10	GND1	G	G	Ground
11	VREF	O	A	Bypass Cap. for the high internal impedance reference.
12	V_{OUT} LDO3	O	PWR	LDO3 output
13	V_{OUT} LDO4	O	PWR	LDO4 output
14	V_{IN} LDO4	I	PWR	Power input to LDO4, this can be connected to either from a 1.8V supply to main Battery supply.
15	V_{IN} BUBATT	I	PWR	Back Up Battery input supply.
16	V_{OUT} LDO_RTC	O	PWR	LDO_RTC output supply to the RTC of the application processor.
17	nBATT_FLT	O	D	Main Battery fault output, indicates the main battery is low
				(discharged) or the dc source has been removed from the system. This gives the processor an indicator that the power will shut down. During this time the processor will operate from the back up coin cell.
18	PGND2	G	G	Buck2 NMOS Power Ground
19	SW2	O	PWR	Buck2 switcher output
20	V_{IN} Buck2	I	PWR	Battery input power to Buck2
21	SDA	I/O	D	I^2C Data (Bidirectional)
22	SCL	I	D	I^2C Clock
23	FB2	I	A	Buck2 input feedback terminal
24	nRSTO	O	D	Reset output from the PMIC to the processor
25	V_{OUT} LDO5	O	PWR	LDO5 output
26	V_{IN} LDO5	I	PWR	Power input to LDO5, this can be connected to V_{IN} or to a separate 1.8V supply.
27	VDDA	I	PWR	Analog Power for VREF, BIAS
28	FB3	I	A	Buck3 Feedback
29	GPIO1 / nCHG_EN	I/O	D	General Purpose I/O / Ext. backup battery charger enable pin. This pin enables the main battery / DC source power to charge the backup battery. This pin toggled via the application processor. By grounding this pin the DC source continuously charges the backup battery
30	GPIO2	I/O	D	General Purpose I/O
31	V_{IN} Buck3	I	PWR	Battery input power to Buck3
32	SW3	O	PWR	Buck3 switcher output
33	PGND3	G	G	Buck3 NMOS Power Ground
34	BGND1,2,3	G	G	Bucks 1, 2 and 3 analog Ground
35	SYNC	I	D	Frequency Synchronization: Connection to an external clock signal PLL to synchronize the PMIC internal oscillator.
36	SYS_EN	I	D	Input Digital enable pin for the high voltage power domain supplies. Output from the Monahans processor.
37	PWR_EN	I	D	Digital enable pin for the Low Voltage domain supplies. Output signal from the Monahans processor
38	PGND1	G	G	Buck1 NMOS Power Ground
39	SW1	O	PWR	Buck1 Switcher output
40	VIN Buck1	I	PWR	Battery input power to Buck1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

All Inputs	−0.3V to +6.5V
GND to GND SLUG	±0.3V
Junction Temperature ($T_{J\text{-}MAX}$)	150°C
Storage Temperature	−65°C to +150°C
Power Dissipation (T_A = 70°C) [3]	3.2W
Junction-to-Ambient Thermal Resistance θ_{JA} [3]	25°C/W
Maximum Lead Temp (Soldering)	260°C
ESD Rating [4]	
Human Body Model	2 kV
Machine Model	200V

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA-MAX = TJ-MAX-OP – (θ_{JA} x PD-MAX).
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Operating Ratings

V_{IN} LDO 4,5	2.7V to 5.5V
V_{EN}	1.74 to (V_{IN}
Junction Temperature (T_J)	−40°C to +125°C
Operating Temperature (T_A)	−40°C to +85°C
Maximum Power Dissipation (T_A = 70°C) [1] [2]	2.2W

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA-MAX = TJ-MAX-OP – (θ_{JA} x PD-MAX).
(2) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51–7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/1.8 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation* section of this datasheet.

General Electrical Characteristics[1]

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C.[2] [3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}, VDDA, V_{IN} Buck1, 2 and 3	Battery Voltage		**2.7**	3.6	**5.5**	V
V_{IN}LDO4, V_{IN}LDO5	Power Supply for LDO 4 and 5		**1.74**	3.6	**5.5**	V

(1) No input supply should be higher then VDDA
(2) All voltages are with respect to the potential at the GND pin.
(3) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

General Electrical Characteristics[1] (continued)

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C.[2] [3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SD}	Thermal Shutdown [4]	Temperature		160		°C
		Hysteresis		20		

(4) Specified by design.Not prodution tested.

Supply Specification[1][2]

Supply	V_{OUT} (Volts)		I_{MAX} Maximum Output
	Range (V)	Resolution (mV)	Current (mA) [3]
LDO_RTC	Tracking [4]	N/A	**30 or 10**
LDO1	1.8 to 3.3	100	**300**
LDO2	1.8 to 3.3	100	**150**
LDO3	1.8 to 3.3	100	**150**
LDO4	1.0 to 3.3	50-600	**150**
LDO5	1.0 to 3.3	50-600	**370**
BUCK 1	0.8 to 3.3	50-600	**1600**
BUCK 2	0.8 to 3.3	50-600	**1600**
BUCK 3	0.8 to 3.3	50-600	**1600**

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Specified by design. Not production tested. design.
(4) LDO_RTC voltage can track LDO1 voltage. LP3971 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO1 voltage within 200mV down to 2.8V when LDO1 is enabled

Default Voltage Options

Version	LP3971SQ-B410		LP3971SQ-D510		LP3971Q-F211		LP3971SQ-W416	
Enable	**Version B**		**Version C**		**Version A**		**Version SW**	
LDO_RTC	--	2.8	--	2.8	--	2.8	--	2.8
LDO1	SYS_EN	3.0 (w/ Trkg)	SYS_EN	3.3 (w/ Trkg)	SYS_EN	3.3	SYS_EN	3.0
LDO2	SYS_EN	3.0	SYS_EN	3.3	SYS_EN	3.3	SYS_EN	3.3
LDO3	SYS_EN	3.0	SYS_EN	3.3	SYS_EN	3.3	PWR_EN	2.5
LDO4	PWR_EN	1.3	PWR_EN	1.3	SYS_EN	1.8	SYS_EN	1.0
LDO5	PWR_EN	1.1	PWR_EN	1.1	PWR_EN	3.3	PWR_EN	1.0
BUCK1	PWR_EN	1.4	PWR_EN	1.4	PWR_EN	1.5	PWR_EN	1.2
BUCK2	SYS_EN	3.0	SYS_EN	3.3	SYS_EN	2.5	SYS_EN	3.0
BUCK3	SYS_EN	1.8	SYS_EN	1.8	SYS_EN	1.8	SYS_EN	1.8

Version	LP3971SQ-N510		LP3971SQ-P55A		LP3971SQ-B510		LP3971SQ-O509	
Enable							set to default 00 on system enable delay	
LDO_RTC	Track	2.8	No Track	2.8	Track	2.8	NoTrack	2.8
LDO1	SYS_EN	3.3	SYS_EN	3.3	SYS_EN	3.0	SYS_EN	3.3
LDO2	SYS_EN	3.0	SYS_EN	3.3	SYS_EN	3.0	SYS_EN	3.3
LDO3	SYS_EN	3.0	SYS_EN	3.3	SYS_EN	3.0	PWR_EN	3.3
LDO4	PWR_EN	1.3	SYS_EN	1.35	PWR_EN	1.3	SYS_EN	1.25
LDO5	PWR_EN	1.1	PWR_EN	1.8	PWR_EN	1.1	SYS_EN	1.25

BUCK1	PWR_EN	1.4	PWR_EN	1.35	PWR_EN	1.4	PWR_EN	3.3
BUCK2	SYS_EN	3.3	SYS_EN	3.3	SYS_EN	3.3	SYS_EN	3.3
BUCK3	SYS_EN	1.8	SYS_EN	3.3	SYS_EN	1.8	SYS_EN	1.3

Version	**LP3971SQ-G824**		**LP3971SQ-Q418**		**LP3971SQ-2G16**	
Enable						
LDO_RTC	No Track	2.8	No Track	2.8	No Track	2.8
LDO1	SYS_EN	2.5	SYS_EN	3.0	SYS_EN	3.3
LDO2	SYS_EN	2.5	SYS_EN	3.0	SYS_EN	3.3
LDO3	SYS_EN	3.3	PWR_EN	3.3	PWR_EN	3.3
LDO4	SYS_EN	3.0	SYS_EN	1.2	SYS_EN	1.0
LDO5	PWR_EN	2.5	PWR_EN	1.2	PWR_EN	1.0
BUCK1	PWR_EN	3.3	PWR_EN	1.35	PWR_EN	1.0
BUCK2	SYS_EN	1.2	SYS_EN	3.0	PWR_EN	1.1
BUCK3	SYS_EN	2.5	SYS_EN	1.8	SYS_EN	1.8

Version	**LP3971SQ-7848**	
Enable		
LDO_RTC	No Track	2.8
LDO1	SYS_EN	3.0
LDO2	SYS_EN	2.6
LDO3	SYS_EN	3.3
LDO4	SYS_EN	1.2
LDO5	SYS_EN	1.8
BUCK1	PWR_EN	1.2
BUCK2	PWR_EN	1.2
BUCK3	SYS_EN	3.0

Version	**LP3971SQ-8858**	
Enable		
LDO_RTC	No Track	2.8
LDO1	SYS_EN	3.3
LDO2	SYS_EN	3.3
LDO3	SYS_EN	3.3
LDO4	SYS_EN	1.2
LDO5	SYS_EN	1.8
BUCK1	PWR_EN	1.2
BUCK2	PWR_EN	1.2
BUCK3	SYS_EN	3.3

LDO RTC

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1)(2) (3) and (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage Accuracy	V_{IN} Connected, Load Current = 1 mA	**2.632**	2.8	**2.968**	V
ΔV_{OUT}	Line Regulation	V_{IN} = (V_{OUT} nom + 1.0V) to 5.5V (5) Load Current = 1 mA			**0.15**	%/V
	Load Regulation	From Main Battery Load Current = 1 mA to 30 mA			**0.05**	%/mA
		From Backup Battery V_{IN} = 3.0V Load Current = 1 mA to 10 mA			**0.5**	
I_{SC}	Short Circuit Current Limit	From Main Battery V_{IN} = V_{OUT} +0.3V to 5.5V		100		mA
		From Backup Battery		30		
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = 10 mA			**375**	mV
I_Q_Max	Maximum Quiescent Current	I_{OUT} = 0 mA		30		µA
TP1	RTC LDO Input Switched from Main Battery to Backup Battery	V_{IN} Falling		2.9		V
TP2	RTC LDO Input Switched from Backup Battery to Main Battery	V_{IN} Rising		3.0		V
C_O	Output Capacitor	Capacitance for Stability	**0.7**	1.0		µF
		ESR	**5**		**500**	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(4) LDO_RTC voltage can track LDO1 voltage. LP3971 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO1 voltage within 200mV down to 2.8V when LDO1 is enabled.
(5) V_{IN} minimum for line regulation values is 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.

LDO 1 to 5

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1)(2)(3)(4)(5)(6) and (7).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage Accuracy (Default V_{OUT})	Load Current = 1 mA	**−3**		**3**	%
ΔV_{OUT}	Line Regulation	V_{IN} =3.1V to 5.0V, (8) Load Current = 1 mA			**0.15**	%/V
	Load Regulation	V_{IN} = 3.6V, Load Current = 1 mA to I_{MAX}			**0.011**	%/mA
I_{SC}	Short Circuit Current Limit	LDO1–4, V_{OUT} = 0V		400		mA
		LDO5, V_{OUT} = 0V		500		
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = 50 mA (3)			**150**	mV
PSRR	Power Supply Ripple Rejection	f = 10 kHz, Load Current = I_{MAX}		45		dB
I_Q	Quiescent Current “On”	I_{OUT} = 0 mA		40		µA
	Quiescent Current “On”	I_{OUT} = I_{MAX}		60		
	Quiescent Current “Off”	EN is de-asserted		0.03		
T_{ON}	Turn On Time	Start up from Shut-down		300		µsec
C_{OUT}	Output Capacitor	Capacitance for Stability 0°C ≤ T_J ≤ 125°C	**0.33**	0.47		µF
		−40°C ≤ T_J ≤ 125°C	**0.68**	1.0		
		ESR	**5**		**500**	mΩ

(1) All voltages are with respect to the potential at the GND pin.
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(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(4) LDO_RTC voltage can track LDO1 voltage. LP3971 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO1 voltage within 200mV down to 2.8V when LDO1 is enabled.
(5) V_{IN} minimum for line regulation values is 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.
(6) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(7) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5.
(8) V_{IN} minimum for line regulation values is 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.

LDO Dropout Voltage vs. Load Current Collect Data For All LDO’s

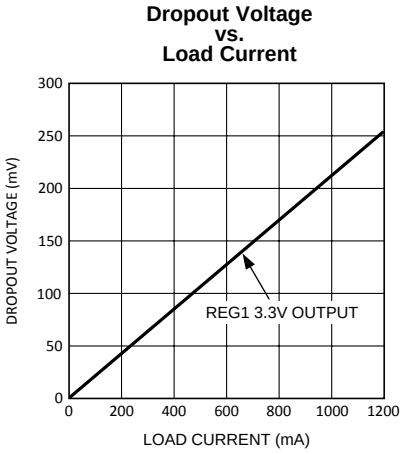


Figure 4.

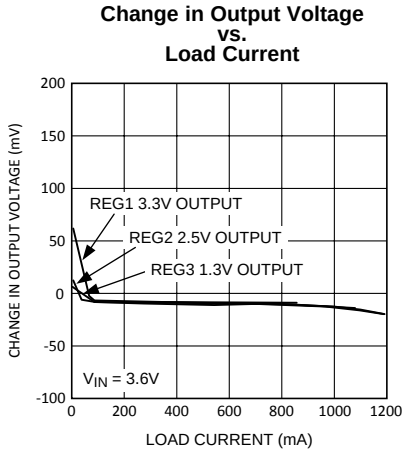


Figure 5.

LDO1 Line Regulation
V_{OUT} = 1.8 volts V_{IN} 3 to 4 volts Load = 100 mA

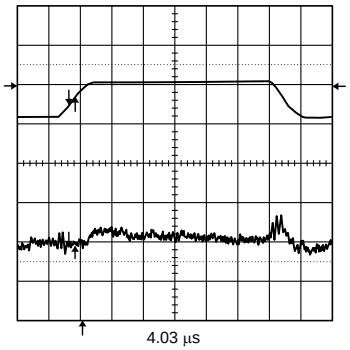


Figure 6.

LDO1 Load Transient
V_{IN} = 4.1 volts V_{OUT} = 1.8 volts no-load-100 mA

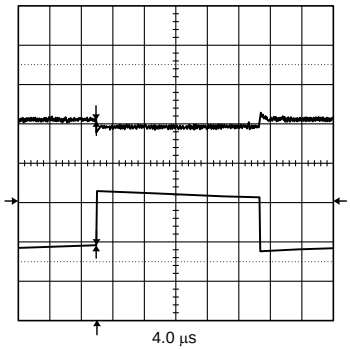


Figure 7.

Enable Start-up time (LDO1)
LDO1 channel 2 LDO4 Channel 1 Sys_enable from 0 volts Load = 100mA

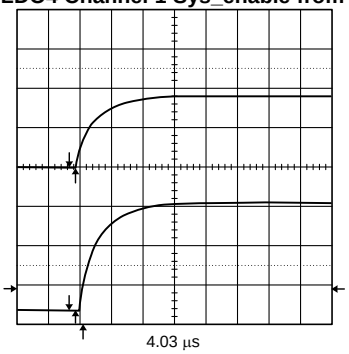


Figure 8.

Buck Converters SW1, SW2, SW3

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2 µH ceramic. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1)(2)(3) and (4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage Accuracy	Default V_{OUT}	−3		+3	%
Eff	Efficiency	Load Current = 500 mA		95		%
I_{SHDN}	Shutdown Supply Current	EN is de-asserted		0.1		µA
	Sync Mode Clock Frequency	Synchronized from 13 MHz System Clock	10.4	13	15.6	MHz
f_{OSC}	Internal Oscillator Frequency			2.0		MHz
I_{PEAK}	Peak Switching Current Limit			2.1	2.4	A
I_Q	Quiescent Current “On”	No Load PFM Mode		21		µA
		No Load PWM Mode		200		
R_{DSON} (P)	Pin-Pin Resistance PFET			240		mΩ
R_{DSON} (N)	Pin-Pin Resistance NFET			200		mΩ
T_{ON}	Turn On Time	Start up from Shut-down		500		µsec
C_{IN}	Input Capacitor	Capacitance for Stability	8			µF
C_O	Output Capacitor	Capacitance for Stability	8			µF

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) The input voltage range recommended for ideal applications performance for the specified output voltages is given below:V_{IN} = 2.7V to 5.5V for 0.80V < V_{OUT} < 1.8VV_{IN} = (V_{OUT}+ 1V) to 5.5V for 1.8V ≤ V_{OUT} ≤ 3.3V
(4) Test condition: for V_{OUT} less than 2.7V, V_{IN} = 3.6V; for V_{OUT} greater than or equal to 2.7V, V_{IN} = V_{OUT}+ 1V.

Buck 1 Output Efficiency vs. Load Current Varied from 1mA to 1.5 Amps

V_{IN} = 3, 3.5 volts V_{OUT} = 1.4 volts Forced PWM

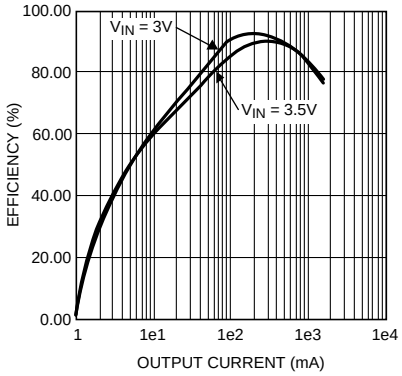


Figure 9.

V_{IN} = 4.0, 4.5 volts V_{OUT} = 1.4 volts Forced PWM

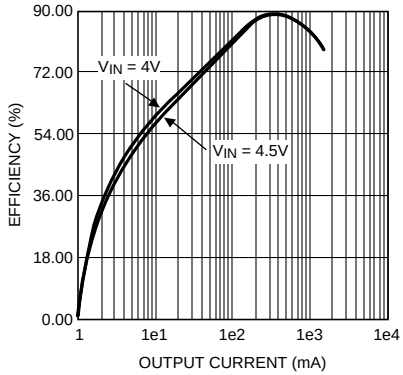


Figure 10.

V_{IN} = 3, 3.5 volts V_{OUT} = 1.4 volts Forced PWM

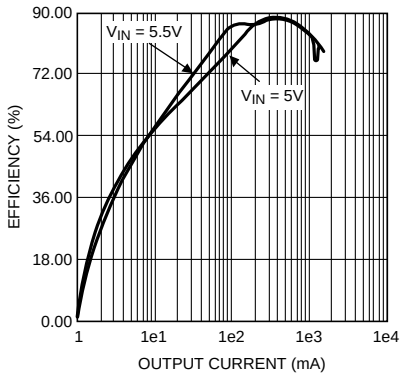


Figure 11.

Line Transient Response
V_{IN} = 3, 3.6 V, V_{OUT} = 1.2 V, 250 mA load

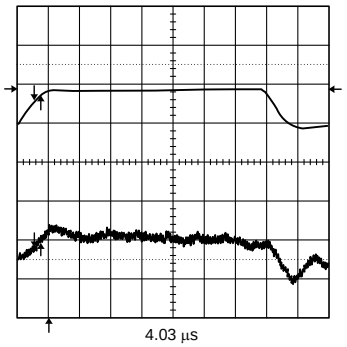


Figure 12.

Load Transient
3.6 V_{IN}, 3.3 V_{OUT}, 0 – 100 mA load

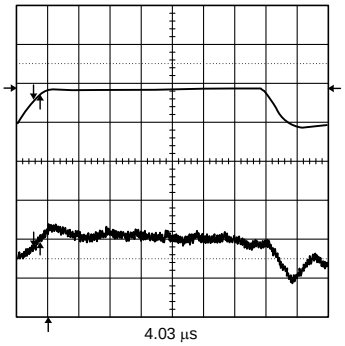


Figure 13.

Mode Change
Load transients 20 mA to 560 mA
V_{OUT} = 1.4 volts [PFM to PWM] V_{IN} = 4.1 volts

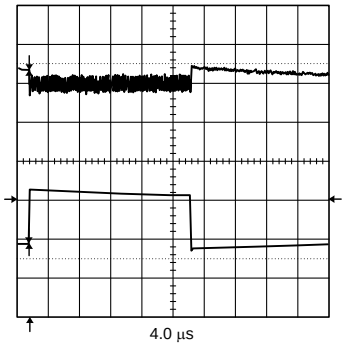


Figure 14.

Startup
Startup into PWM Mode 980 mA [channel 2]
V_{OUT} = 1.4 volts V_{IN} = 4.1 volts

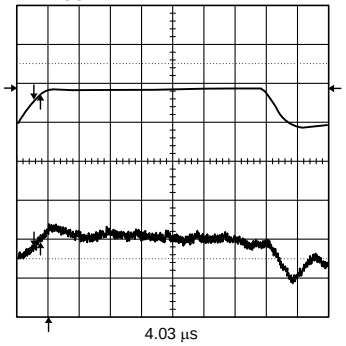


Figure 15.

Back-Up Charger Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1)(2) and (3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	Voltage at V_{IN}	**3.3**		**5.5**	V
I_{OUT}	Backup Battery Charging Current	V_{IN} = 3.6V, Backup_Bat = 2.5V, Backup Battery Charger Enabled (3)		190		µA
V_{OUT}	Charger Termination Voltage	V_{IN} = 5.0V Backup Battery Charger Enabled. Programmable	**2.91**	3.1		V
	Backup Battery Charger Short Circuit Current	Backup_Bat = 0V, Backup Battery Charger Enabled		9		mA
PSRR	Power Supply Ripple Rejection Ratio	$I_{OUT} \le 50$ µA, V_{OUT} = 3.15V $V_{OUT} + 0.4 \le V_{BATT} = V_{IN} \le 5.0V$ f < 10 kHz		15		dB
I_Q	Quiescent Current	$I_{OUT} < 50$ µA		25		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 100 µA		0.1		µF
	Output Capacitor ESR		**5**		**500**	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Back-up battery charge current is programmable via the I^2C compatible interface. Refer to the Application Section for more information.

LP3971 Battery Switch Operation

The LP3971 has provisions for two battery connections, the main battery Vbat and Backup Battery.

The function of the battery switch is to connect power to the RTC LDO from the appropriate battery, depending on conditions described below:

- If only the backup battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If only the main battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If both batteries are applied, and the main battery is sufficiently charged (Vbat > 3.1V), the switch will automatically connect the RTC LDO power to the main battery.
- As the main battery is discharged a separate circuit called nBATT_FLT will warn the system. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch will disconnect the input of the RTC_LDO from the main battery and connect to the backup battery.
- The main battery voltage at which the RTC LDO is switched over from main to backup battery is 2.8V typically.
- There is a hysteric voltage in this switch operation so; the RTC LDO will not be reconnected to main battery until main battery voltage is greater than 3.1V typically.
- The system designer may wish to disable the battery switch when only a main battery is used. This is accomplished by setting the “no back up battery bit” in the control register 8h’0B bit 7 NBUB. With this bit set to “1”, the above described switching will not occur, that is the RTC LDO will remain connected to the main battery even as it is discharged below the 2.9V threshold. The Backup battery input should also be connected to main battery.

Logic Inputs and Outputs DC Operating Conditions (1)

Logic Inputs (SYS_EN, PWR_EN, SYNC, nRSTI, PWR_ON, nTEST_JIG, SPARE and GPI's)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Low Level Input Voltage			**0.5**	V
V_{IH}	High Level Input Voltage		**V_{RTC} −0.5V**		V
I_{LEAK}	Input Leakage Current		**−1**	**+1**	µA

(1) All voltages are with respect to the potential at the GND pin.

Logic Outputs (nRSTO, EXT_WAKEUP and GPO's)

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output Low Level	Load = +0.2 mA = I_{OL} Max		**0.5**	V
V_{OH}	Output High Level	Load = −0.1 mA = I_{OL} Max	**V_{RTC} −0.5V**		V
I_{LEAK}	Output Leakage Current	V_{ON} = V_{IN}		**+5**	µA

Logic Output (nBATT_FLT)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	nBATT_FLT Threshold Voltage	Programmable via Serial Interface Default = 2.8V	**2.4**	2.8	**3.4**	V
V_{OL}	Output Low Level	Load = +0.4 mA = I_{OL} Max			**0.5**	V
V_{OH}	Output High Level	Load = −0.2 mA = I_{OH} Max	**V_{RTC} −0.5V**			V
I_{LEAK}	Input Leakage Current				**+5**	µA

I²C Compatible Serial Interface Electrical Specifications (SDA and SCL)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1)(2) and (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage	(4)	−0.5		0.3 V_{RTC}	V
V_{IH}	High Level Input Voltage	(4)	0.7 V_{RTC}		V_{RTC}	
V_{OL}	Low Level Output Voltage	(4)	0		0.2 V_{TRC}	
I_{OL}	Low Level Output Current	V_{OL} = 0.4V (4)	3.0			mA
F_{CLK}	Clock Frequency	(4)			400	kHz
t_{BF}	Bus-Free Time Between Start and Stop	(4)	1.3			µs
t_{HOLD}	Hold Time Repeated Start Condition	(4)	0.6			µs
t_{CLKLP}	CLK Low Period	(4)	1.3			µs
t_{CLKHP}	CLK High Period	(4)	0.6			µs
t_{SU}	Set Up Time Repeated Start Condition	(4)	0.6			µs
$t_{DATAHLD}$	Data Hold Time	(4)	0			µs
t_{CLKSU}	Data Set Up Time	(4)	100			ns
T_{SU}	Set Up Time for Start Condition	(4)	0.6			µs
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK Signals	(4)		50		ns

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are production tested, specified through statistical analysis or by design. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) The I²C signals behave like open-drain outputs and require an external pull-up resistor on the system module in the 2 kΩ to 20 kΩ range.
(4) Specified by design. Not production tested

BUCK CONVERTER OPERATION

DEVICE INFORMATION

The LP3971 includes three high efficiency step down DC-DC switching buck converters. Using a voltage mode architecture with synchronous rectification, the buck converters have the ability to deliver up to 1600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. The device operates in PWM mode at load currents of approximately 100 mA or higher, having voltage tolerance of ±3% with 95% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption. Shutdown mode turns off the device, offering the lowest current consumption ($I_{Q,\ SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.7V or higher.

CIRCUIT OPERATION

The buck converter operates as follows. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}–V_{OUT})/L$, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $–V_{OUT}/L$.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

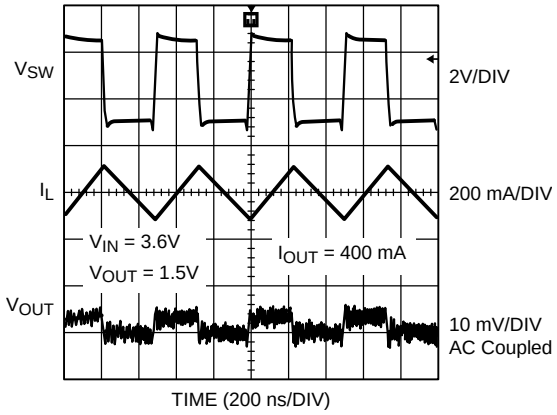


Figure 16. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the converters uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the converters to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 2.0 A (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A: The inductor current becomes discontinuous.

B: The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30 mA + V_{IN}/42Ω).

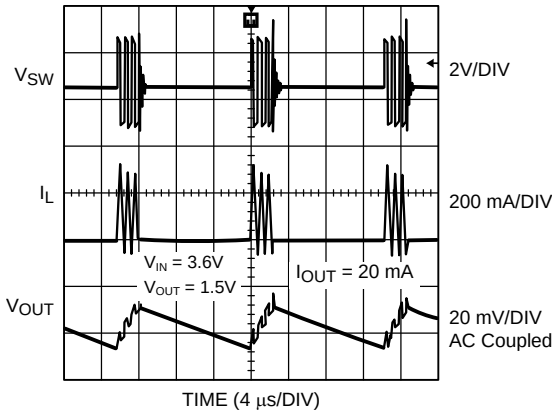


Figure 17. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between <0.6% and <1.7% above the nominal PWM output voltage. If the output voltage is below the “high” PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the ‘high’ PFM threshold or the peak current exceeds the IPFM level set for PFM mode. The typical peak current in PFM mode is: IPFM = 112 mA + V_{IN}/27Ω. Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the ‘high’ PFM comparator threshold (see Figure 18), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the ‘high’ PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this ‘sleep’ mode is 21 µA (typ), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the ‘low’ PFM threshold, the cycle repeats to restore the output voltage (average voltage in PFM mode) to <1.15% above the nominal PWM output voltage. If the load current should increase during PFM mode (see Figure 18) causing the output voltage to fall below the ‘low2’ PFM threshold, the part will automatically transition into fixed-frequency PWM mode. Typically when V_{IN} = 3.6V the part transitions from PWM to PFM mode at 100 mA output current .

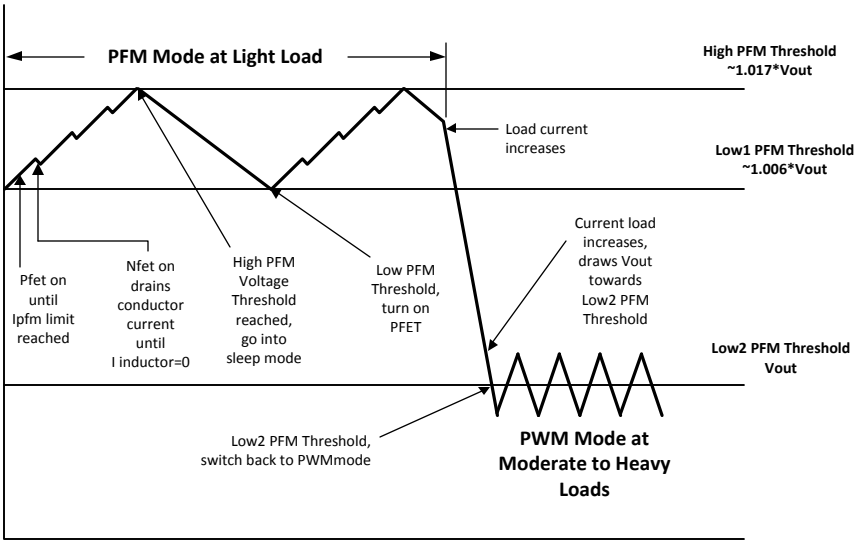


Figure 18. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch will be open in shutdown to discharge the output. When the converter is enabled, EN, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.7V.

SOFT START

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 213 mA, 425 mA, 850 mA and 1700 mA (typ. Switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 10 µF output capacitor and 1000 mA load current is 390 µs and with 1 mA load current is 295 µs.

LDO - LOW DROP OUT OPERATION

The LP3971 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} * (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT} \quad (1)$$

I_{LOAD}	Load Current
$R_{DSON,\ PFET}$	Drain to source resistance of PFET switch in the triode region
$R_{INDUCTOR}$	Inductor resistance

SPREAD SPECTRUM FEATURE

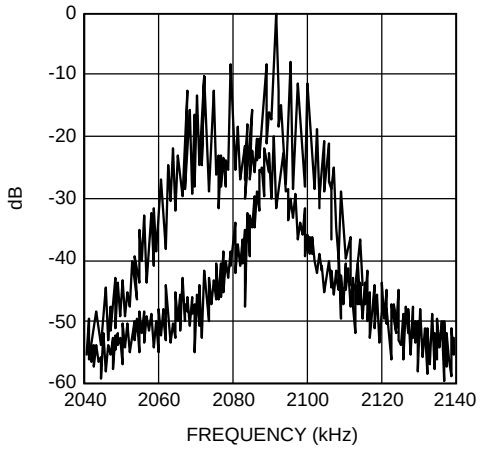
Periodic switching in the buck regulator is inherently a noisier function block compared to an LDO. It can be challenging in some critical applications to comply with stringent regulatory standards or simply to minimize interference to sensitive circuits in space limited portable systems. The regulator's switching frequency and harmonics can cause "noise" in the signal spectrum. The magnitude of this noise is measured by its power spectral density. The power spectral density of the switching frequency, F_C, is one parameter that system designers want to be as low as practical to reduce interference to the environment and subsystems within their products. The LP3971 has a user selectable function on chip, wherein a noise reduction technique known as "spread spectrum" can be employed to ease customer's design and production issues.

The principle behind spread spectrum is to modulate the switching frequency slightly and slowly, and spread the signal frequency over a broader bandwidth. Thus, its power spectral density becomes attenuated, and the associated interference electro-magnetic energy is reduced. The clock used to modulate the LP3971 buck regulator can be used as a spread spectrum clock via 2 I^2C control register (System Control Register 1 (SCR1) 8h'80) bits bk_ssen, and slomod. With this feature enabled, the intense energy of the clock frequency can be spread across a small band of frequencies in the neighborhood of the center frequency. This results in a reduction of the peak energy!

The LP3971 spread spectrum clock uses a triangular modulation profile with equal rise and fall slopes. The modulation has the following characteristics:

- The center frequency: F_C = 2 MHz, and
- The modulating frequency, f_M = 6.8 kHz or 12 kHz.
- Peak frequency deviation: Δ_f = ±100 kHz (or ±5%)
- Modulation index β = Δ_f/f_M = 14.7 or 8.3

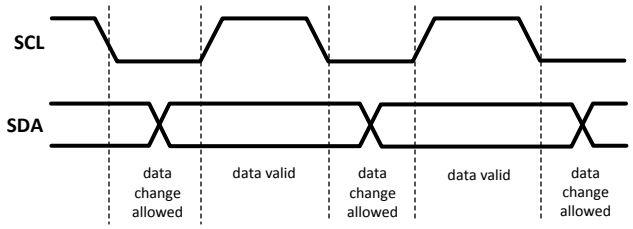
Figure 19. Switching Energy RBW = 300 Hz



I²C Compatible Interface

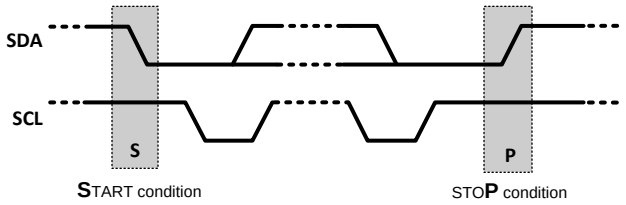
I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

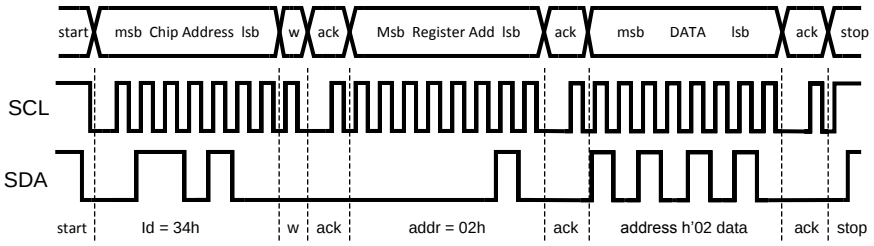
After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3971 address is 34h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C CHIP ADDRESS - 7h'34

MSB							
ADR6 Bit7	ADR5 Bit6	ADR4 Bit5	ADR3 Bit4	ADR2 Bit3	ADR1 Bit2	ADR0 Bit1	**R/W** Bit0
0	1	1	0	1	0	0	**R/W**

Write Cycle

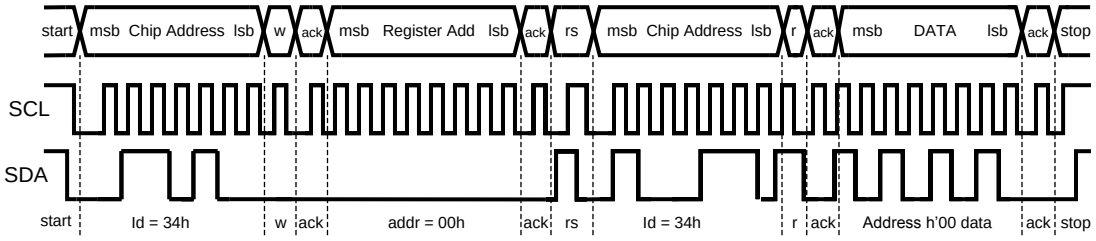
Figure 20. Write cycle



Read Cycle

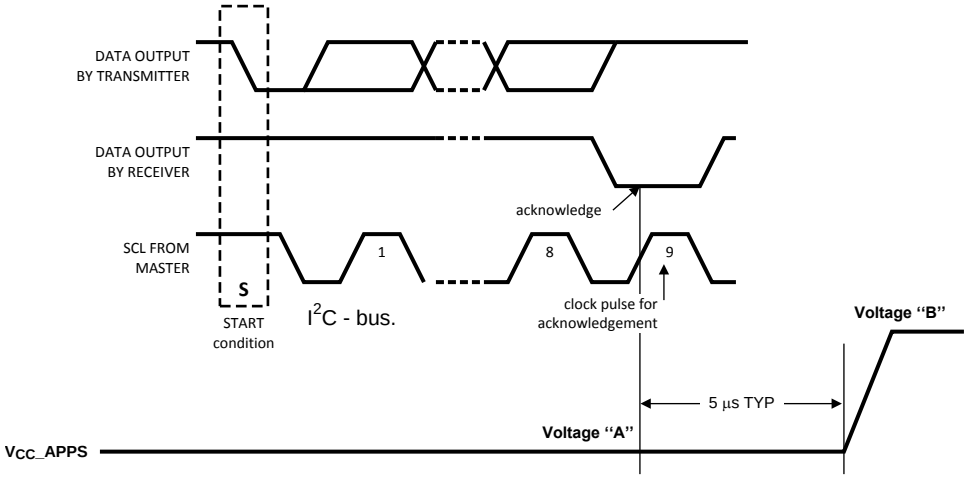
When a READ function is to be accomplished, a WRITE function must precede the READ function as follows.

Figure 21. Read Cycle



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 34h (Chip Address)

Figure 22. I^2C DVM Timing for V_{CC}_APPS (Buck1)



LP3971 I^2C Register Definitions

I^2C CONTROL REGISTERS

Register Address	Register Name	Read/ Write	Register Description
8h'02	ISR	R	Interrupt Status Register A
8h'07	SCR1	R/W	System Control Register 1

Register Address	Register Name	Read/ Write	Register Description
8h'0B	BBCC	R/W	Backup Battery Charger Control Register
8h'0E	SCR2	R/W	System Control Register 2
8h'10	BOVEN	R/W	Buck Output Voltage Enable Register
8h'11	BOVSR	R	Buck Output Voltage Status Register
8h'12	LDOEN	R/W	LDO Output Voltage Enable Register
8h'13	LDOVS	R	LDO Output Voltage Status Register
8h'20	$V_{CC}1$	R/W	Voltage Change Control Register 1
8h'23	B1TV1	R/W	Buck 1 Target Voltage 1 Register
8h'24	B1TV2	R/W	Buck 1 Target Voltage 2 Register
8h'25	B1RC	R/W	Buck 1 Ramp Control
8h'29	B2TV1	R/W	Buck 2 Target Voltage 1 Register
8h'2A	B2TV2	R/W	Buck 2 Target Voltage 2 Register
8h'2B	B2RC	R/W	Buck 2 Voltage Ramp Control
8h'32	B3TV1	R/W	Buck 3 Target Voltage 1 Register
8h'33	B3TV2	R/W	Buck 3 Target Voltage 2 Register
8h'34	B3RC	R/W	Buck 3 Voltage Ramp Control
8h'38	BFR	R/W	Buck Function Register
8h'39	L21VCR	R/W	LDO2 & 1 Voltage Control Registers
8h'3A	L43VCR	R/W	LDO4 & LDO3 Voltage Control Registers
8h'3B	L5VCR	R/W	LDO5 Voltage Control Registers

INTERRUPT STATUS REGISTER (ISR) 8H'02

Bit	7	6	5	4	3	2	1	0
Designation	T100	T125	GPI2	GPI1	WUP3	WUP2	WUPT	WUPS
Reset Value	0	0	0	0	0	0	0	0

INTERRUPT STATUS REGISTER (ISR) 8H'02 DEFINITIONS

Bit	Access	Name	Description
7	—	—	Reserved
6	R	T125	Status bit for thermal warming PMIC T>125°C 0 = PMIC Temp. <125°C 1 = PMIC Temp. >125°C
5	R	GPI2	Status bit for the input read in from GPIO 2 when set as Input 0 = GPI2 Logic Low 1 = GPI2 Logic High
4	R	GPI1	Status bit for the input read in from GPIO 1 when set as Input 0 = GPI1 Logic Low 1 = GPI1 Logic High
3	R	WUP3	PWR_ON Pin Long Pulse Wake Up Status 0 = 1 No wake up event 1 = Long pulse wake up event
2	R	WUP2	PWR_ON Pin Short Pulse Wake Up Status 0 = No wake up event 1 = Short pulse wake up event
1	R	WUPT	TEST_JIG Pin Wake Up Status 0 = No wake up event 1 = Wake up event
0	R	WUPS	SPARE Pin Wake Up Status 0 = No wake up event 1 = Wake up event

SYSTEM CONTROL REGISTER 1 (SCR1) 8H'07

Bit	7	6	5	4	3	2	1	0
Designation	BPSEN	Reserved	SENDL**		FPWM3	FPWM2	FPWM1	ECEN
Reset Value	0	1	1**	0**	0	0	0	0

SYSTEM CONTROL REGISTER 1 (SCR1) 8H'07 DEFINITIONS

Bit	Access	Name	Description		
7	R/W	BPSEN	Bypass System enable safety Lock. Prevents activation of PWR_EN when SYS_EN is low. 0 = PWR_EN "AND" with SYS_EN signal 1 = PWR_EN independent of SYS_EN		
6	—	—	Reserved		
5:4	R/W	SENDL	Delay time for High Voltage Power Domains LDO2, LDO3, LDO4, Buck2, and Buck3 after activation of SYS_EN. V_{CC}_LDO1 has no delay.		
			Data Code	**Delay mS**	**Notes**
			2h'0	0.0	
			2h'1	0.5	
			2h'2	**1.0**	Default
			2h'3	1.4	
3	R/W	FPWM3	Buck 3 PWM/PFM Mode Select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM		
2	R/W	FPWM2	Buck 2 PWM/PFM Mode Select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM		
1	R/W	FPWM1	Buck 1 PWM/PFM Mode Select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM		
0	R/W	ECEN	External Clock Select 0 = Internal Oscillator clock for Buck Converters 1 = External 13 MHz Oscillator clock for Buck Converters		

BACKUP BATTERY CHARGER CONTROL REGISTER (BBCC) 8H'0B

Bit	7	6	5	4	3	2	1	0
Designation	NBUB	CNBFL	nBFLT			BUCEN	IBUC	
Reset Value	0	0	0	1	0	0	0	1

BACKUP BATTERY CHARGER CONTROL REGISTER (BBCC) 8H'0B DEFINITIONS

Bit	Access	Name	Description		
7	R/W	NBUB	No back-up battery default setting. Logic will not allow switch over to back-up battery. 0 = Back up Battery Enabled 1 = Back up Battery Disabled		
6	---	---	Reserved		
5:3	R/W	BFLT	nBATT_FLT monitors the battery voltage and can be set to the De-assert voltages listed below.		
			Data Code	**Asserted**	**De-Asserted**
			3h'00	2.4	2.6
			3h'01	2.6	2.8
			3h'02	**2.8**	**3.0**
			3h'03	3.0	3.2
			3h'04	3.2	3.4
			3h'05	3.4	3.6

Bit	Access	Name	Description	
2	R/W	BUCEN	Enables backup battery charger 0 = Back up Battery Charger Disabled 1 = Back up Battery Charger Enabled	
1:0	R/W	IBUC	Charger current setting for back-up battery	
			Data Code	**BU Charger I (µA)**
			2h'00	260
			2h'01	**190**
			2h'02	325
			2h'03	390

SYSTEM CONTROL REGISTER (SCR2) 8H'0E

Bit	7	6	5	4	3	2	1	0
Designation	BBCS	SEB2	BPTR**	WUP3_ sense	GPIO2		GPIO1	
Reset Value	1	0	0**	1	0	0	0	0

SYSTEM CONTROL REGISTER (SCR2) 8H'0E DEFINITIONS

Bit	Access	Name	Description			
7	R/W	BBCS	Sets GPIO1 as control input for Back Up battery charger 0 = Back Up battery Charger GPIO Disabled 1 = Back Up battery Charger GPIO Pin Enabled			
6	R/W	SEB2	PWR_EN soft Low voltage Supply Enabled OR'ed with PWR_EN Pin 0 = Low voltage Supply Output Enabled 1 = Low voltage Supply Output Disabled			
5	R/W	BPTR	Bypass RTC_LDO Output Voltage to LDO1 Output Voltage Tracking 0 = RTC_LDO1 Tracking enabled 1 = RTC-LDO1 Tracking disabled			
4	R/W	WUP3_ sense	Spare Wakeup control input 0 = Active High 1 = Active Low			
3:2	R/W	GPIO2	Configure direction and output sense of GPIO2 Pin			
			Data Code	**GPIO2**		
			2h'00	Hi-Z		
			2h'01	Output Low		
			2h'02	Input		
			2h'03	Output high		
1:0	R/W	GPIO1	Configure direction and output sense of GPIO1 Pin			
			Data Code	**GPIO1**		
			2h'00	Hi-Z		
			2h'01	Output Low		
			2h'02	Input		
			2h'03	Output high		

BUCKS OUTPUT VOLTAGE ENABLE REGISTER (BOVEN) 8H'10

Bit	7	6	5	4	3	2	1	0
Designation	Reserved	B2ENC**	Reserved	B3EN	Reserved	B2EN	Reserved	B1EN
Reset Value	0	1**	0	1	0	1	0	1

BUCKS ENABLE REGISTER (BOVEN) 8H'10 DEFINITIONS

Bit	Access	Name	Description
7	—	—	Reserved
6	R/W	B2ENC	Connects Buck 2 enable to SYS_EN or PWR_EN Logic Control pin 0 = Buck 2 enable connected to PWR_EN 1 = Buck 2 enable connected to SYS_EN
5	—	—	Reserved
4	R/W	B3EN	V_{CC}_Buck3 Supply Output Enabled 0 = V_{CC}_Buck3 Supply Output Disabled 1 = V_{CC}_Buck3 Supply Output Enabled
3	—	—	Reserved
2	R/W	B2EN	V_{CC}_Buck2 Supply Output Enabled 0 = V_{CC}_Buck2 Supply Output Disabled 1 = V_{CC}_Buck2 Supply Output Enabled
1	—	—	Reserved
0	R/W	B1EN	V_{CC}_Buck1 Supply Output Enabled 0 = V_{CC}_Buck1 Supply Output Disabled 1 = V_{CC}_Buck1 Supply Output Enabled

BUCK STATUS REGISTER (BOVSR) 8H'11

Bit	7	6	5	4	3	2	1	0
Designation	BT_OK	Reserved	Reserved	B3_OK	Reserved	B2_OK		B1_OK
Reset Value	0	0	0	0	0	0	0	0

BUCK STATUS REGISTER (BOVSR) 8H'11 DEFINITIONS

Bit	Access	Name	Description
7	R	BT_OK	Buck 1–3 Supply Output Voltage Status 0 = (Buck 1–3) output voltage <90% Default value 1 = (Buck 1–3) output voltage >90% Default value
6:5	—	—	Reserved
4	R	B3_OK	Buck 3 Supply Output Voltage Status 0 = (Buck 3) output voltage <90% Default value 1 = (Buck 3) output voltage >90% Default value
3	—	—	Reserved
2	R	B2_OK	Buck 2 Supply Output Voltage Status 0 = (Buck 2) output voltage <90% Default value 1 = (Buck 2) output voltage >90% Default value
1	—	—	Reserved
0	R	B1_OK	Buck 1 Supply Output Voltage Status 0 = (Buck 1) output voltage <90% Default value 1 = (Buck 1) output voltage >90% Default value

LDO OUTPUT VOLTAGE ENABLE REGISTER (LDOEN) 8H'12

Bit	7	6	5	4	3	2	1	0
Designation	L5EC**	L4EC**	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN	Reserved
Reset Value	0**	0**	1	1	1	1	1	0

LDO OUTPUT VOLTAGE ENABLE REGISTER (LDOEN) 8H'12 DEFINITIONS

Bit	Access	Name	Description
7	R/W	L5EC	Connects LDO5 enable to SYS_EN or PWR_EN Logic Control pin 0 = LDO 5 enable connected to PWR_EN 1 = LDO 5 enable connected to SYS_EN

Bit	Access	Name	Description
6	R/W	L4EC	Connects LDO4 enable to SYS_EN or PWR_EN Logic Control pin 0 = LDO 4 enable connected to PWR_EN 1 = LDO 4 enable connected to SYS_EN
5	R/W	LDO5_EN	LDO_5 Output Voltage Enable 0 = LDO5 Supply Output Disabled 1 = LDO5 Supply Output Enabled
4	R/W	LDO4_EN	LDO_4 Output Voltage Enable 0 = LDO4 Supply Output Disabled 1 = LDO4 Supply Output Enabled
3	R/W	LDO3_EN	LDO_3 Output Voltage Enable 0 = LDO3 Supply Output Disabled 1 = LDO3 Supply Output Enabled
2	R/W	LDO2_EN	LDO_2 Output Voltage Enable 0 = LDO2 Supply Output Disabled 1 = LDO2 Supply Output Enabled
1	R/W	LDO1_EN	LDO_1 Output Voltage Enable 0 = LDO1 Supply Output Disabled 1 = LDO1 Supply Output Enabled
0	—	—	Reserved

LDO OUTPUT VOLTAGE STATUS REGISTER (LDOVS) 8H'13

Bit	7	6	5	4	3	2	1	0
Designation	LDOS_OK	N/A	LDO5_0K	LDO4_OK	LDO3_OK	LDO2_OK	LDO1_OK	N/A
Reset Value	0	0	0	0	0	0	0	0

LDO OUTPUT VOLTAGE STATUS REGISTER (LDOVS) 8H'13 DEFINITIONS

Bit	Access	Name	Description
7	R	LDO_OK	LDO 1–5 Supply Output Voltage Status 0 = (LDO 1–5) output voltage <90% of selected value 1 = (LDO 1–5) output voltage >90% of selected value
6	—	—	Reserved
5	R	LDO5_OK	LDO_5 Output Voltage Status 0 = (V_{CC}_LDO5) output voltage <90% of selected value 1 = (V_{CC}_LDO5) output voltage >90% of selected value
4	R	LDO4_OK	LDO_4 Output Voltage Status 0 = (V_{CC}_LDO4) output voltage <90% of selected value 1 = (V_{CC}_LDO4) output voltage >90% of selected value
3	R	LDO3_OK	LDO_3 Output Voltage Status 0 = (V_{CC}_LDO3) output voltage <90% of selected value 1 = (V_{CC}_LDO3) output voltage >90% of selected value
2	R	LDO2_OK	LDO_2 Output Voltage Status 0 = (V_{CC}_LDO2) output voltage <90% of selected value 1 = (V_{CC}_LDO2) output voltage >90% of selected value
1	R	LDO1_OK	LDO_1 Output Voltage Status 0 = (V_{CC}_LDO1) output voltage <90% of selected value 1 = (V_{CC}_LDO1) output voltage >90% of selected value
0	—	—	Reserved

VOLTAGE CHANGE CONTROL REGISTER 1 (V_{CC}1) 8H'20

Bit	7	6	5	4	3	2	1	0
Designation	B3VS	B3GO	B2VS	B2GO	Reserved		B2VS	B2GO
Reset Value	0	0	0	0	0	0	0	0

VOLTAGE CHANGE CONTROL REGISTER 1 (V_{CC}1) 8H'20 DEFINITIONS

Bit	Access	Name	Description
7	R/W	B3VS	Buck 3 Target Voltage Select 0 = Buck 3 Output Voltage to B3TV1 1 = Buck 3 Output Voltage to B3TV2
6	R/W	B3GO	Start Buck 3 Voltage Change 0 = Hold Buck 3 Output Voltage at current level 1 = Ramp Buck 3 Output Voltage as selected by B3VS
5	R/W	B2VS	Buck 2 Target Voltage Select 0 = Buck 2 Output Voltage to B2TV1 1 = Buck 2 Output Voltage to B2TV2
4	R/W	B2GO	Start Buck 2 Voltage Change 0 = Hold Buck 2 Output Voltage at current level 1 = Ramp Buck 2 Output Voltage as selected by B2VS
3:2	—	—	Reserved
1	R/W	B1VS	Buck 1 Target Voltage Select 0 = Buck 1 Output Voltage to B1TV1 1 = Buck 1 Output Voltage to B1TV2
0	R/W	B1GO	Start Buck 1 Voltage Change 0 = Hold Buck 1 Output Voltage at current level 1 = Ramp Buck 1 Output Voltage as selected by B1VS

BUCK1 TARGET VOLTAGE 1 REGISTER (B1TV1) 8H'23

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 1 Output Voltage (B1OV)**				
Reset Value	0	0	0**	0**	1**	1**	0**	1**

BUCK1 TARGET VOLTAGE 1 REGISTER (B1TV1) 8H'23 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	**5h'0D**	**1.40**
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	5h'14	1.80
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	5h'18	3.00
			5h'0C	1.35	5h'19	3.30

BUCK1 TARGET VOLTAGE 2 REGISTER (B1TV2) 8H'24

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 1 Output Voltage (B1OV)**				
Reset Value	0	0	0	0**	1**	1**	0**	1**

BUCK1 TARGET VOLTAGE 2 REGISTER (B1TV2) 8H'24 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	**5h'0D**	**1.40**
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	5h'14	1.80
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	5h'18	3.00
			5h'0C	1.35	5h'19	3.30

BUCK 1 VOLTAGE RAMP CONTROL REGISTER (B1RC) 8H'25

Bit	7	6	5	4	3	2	1	0
Designation	Reserved				Ramp Rate			
Reset Value	0	0	0	0	1	0	1	0

BUCK 1 VOLTAGE RAMP CONTROL REGISTER (B1RC) 8H'25 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1RS	DVM Ramp Speed			
			Data Code	**Ramp Rate (mV/µs)**		
			4h'0	Instant		
			4h'1	1		
			4h'2	2		
			4h'3	3		
			4h'4	4		
			4h'5	5		
			4h'6	6		
			4h'7	7		
			4h'8	8		
			4h'9	9		
			4h'A	**10**		

BUCK 2 TARGET VOLTAGE 1 REGISTER (B2TV1) 8H'29

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 2 Output Voltage (B2OV)**				
Reset Value	0	0	0	1**	1**	0**	0**	0**

BUCK 2 TARGET VOLTAGE 1 REGISTER (B2TV1) 8H'29 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B2OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	5h'14	1.80
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	**5h'18**	**3.00**
			5h'0C	1.35	5h'19	3.30

BUCK 2 TARGET VOLTAGE 2 REGISTER (B2TV2) 8H'2A

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 2 Output Voltage (B2OV)**				
Reset Value	0	0	0	1**	1**	0**	0**	0**

BUCK 2 TARGET VOLTAGE 2 REGISTER (B2TV2) 8H'2A DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B2OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	5h'14	1.80
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	**5h'18**	**3.00**
			5h'0C	1.35	5h'19	3.30

BUCK 2 VOLTAGE RAMP CONTROL REGISTER (B2RC) 8H'2B

Bit	7	6	5	4	3	2	1	0
Designation	Reserved				Ramp Rate			
Reset Value	0	0	0	0	1	0	1	0

BUCK 2 VOLTAGE RAMP CONTROL REGISTER (B2RC) 8H'2B DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B2RS	DVM Ramp Speed			
			Data Code	**Ramp Rate (mV/µs)**		
			4h'0	Instant		
			4h'1	1		
			4h'2	2		
			4h'3	3		
			4h'4	4		
			4h'5	5		
			4h'6	6		
			4h'7	7		
			4h'8	8		
			4h'9	9		
			4h'A	**10**		

BUCK 3 TARGET VOLTAGE 1 REGISTER (B3TV1) 8H'32

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 3 Output Voltage (B3OV)**				
Reset Value	0	0	0	1**	0**	1**	0**	0**

BUCK 3 TARGET VOLTAGE 1 REGISTER (B3TV1) 8H'32 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B3OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	**5h'14**	**1.80**
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	5h'18	3.00
			5h'0C	1.35	5h'19	3.30

BUCK 3 TARGET VOLTAGE 2 REGISTER (B3TV2) 8H'33

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 2 Output Voltage (B2OV)**				
Reset Value	0	0	0	1**	0**	1**	0**	0**

BUCK 3 TARGET VOLTAGE 2 REGISTER (B3TV2) 8H'33 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B2OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'11	1.60
			5h'05	1.00	5h'12	1.65
			5h'06	1.05	5h'13	1.70
			5h'07	1.10	5h'14	1.80
			5h'08	1.15	5h'15	1.90
			5h'09	1.20	5h'16	2.50
			5h'0A	1.25	5h'17	2.80
			5h'0B	1.30	5h'18	3.00
			5h'0C	1.35	5h'19	3.30

BUCK 3 VOLTAGE RAMP CONTROL REGISTER (B3RC) 8H'34

Bit	7	6	5	4	3	2	1	0
Designation	Reserved				Ramp Rate			
Reset Value	0	0	0	0	1	0	1	0

BUCK 3 VOLTAGE RAMP CONTROL REGISTER (B3RC) 8H'34 DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B3RC	DVM Ramp Speed			
			Data Code	**Ramp Rate (mV/µs)**		
			4h'0	Instant		
			4h'1	1		
			4h'2	2		
			4h'3	3		
			4h'4	4		
			4h'5	5		
			4h'6	6		
			4h'7	7		
			4h'8	8		
			4h'9	9		
			4h'A	**10**		

BUCK FUNCTION REGISTER (BFR) 8H'38

Bit	7	6	5	4	3	2	1	0
Designation	Reserved					SHBU	BK_SLOMOD	BK_SSEN
Reset Value	0	0	0	0	0	0	1	0

BUCK FUNCTION REGISTER (BFR) 8H'38 DEFINITIONS

Bit	Access	Name	Description
7:3	—	—	Reserved
		SHBU	Shut down Back up battery to prevent battery drain during shipping 0 = Back up Battery Enabled 1 = Back up Battery Disabled
1	R	BK_SLOMOD	Buck Spread Spectrum Modulation Buck 1–3 0 = 10 kHz triangular wave spread spectrum modulation 1 = 2 kHz triangular wave spread spectrum modulation
0	R	BK_SSEN	Spread spectrum function Buck 1–3 0 = SS Output Disabled 1 = SS Output Enabled

LDO2–LDO1 VOLTAGE CONTROL REGISTER (L21VCR) 8H'39

Bit	7	6	5	4	3	2	1	0
Designation	LDO 2 Output Voltage (L20V)**				LDO 1 Output Voltage (L1OV)**			
Reset Value	1**	1**	0**	0**	1**	1**	0**	0**

LDO2–LDO1 VOLTAGE CONTROL REGISTER (L21VCR) 8H'39 DEFINITIONS

Bit	Access	Name	Description			
7:4	R/W	L2OV	**Data Code**	**Output Voltage**		
			4h'0	1.8		
			4h'1	1.9		
			4h'2	2.0		
			4h'3	2.1		
			4h'4	2.2		
			4h'5	2.3		
			4h'6	2.4		
			4h'7	2.5		
			4h'8	2.6		
			4h'9	2.7		
			4h'A	2.8		
			4h'B	2.9		
			4h'C	**3.0**		
			4h'D	3.1		
			4h'E	3.2		
			4h'F	3.3		

Bit	Access	Name	Description			
3:0	R/W	L1OV	4h'0	1.8		
			4h'1	1.9		
			4h'2	2.0		
			4h'3	2.1		
			4h'4	2.2		
			4h'5	2.3		
			4h'6	2.4		
			4h'7	2.5		
			4h'8	2.6		
			4h'9	2.7		
			4h'A	2.8		
			4h'B	2.9		
			4h'C	**3.0**		
			4h'D	3.1		
			4h'E	3.2		
			4h'F	3.3		

LDO4–LDO3 VOLTAGE CONTROL REGISTER (L43VCR) 8H'3A

Bit	7	6	5	4	3	2	1	0
Designation	LDO 4 Output Voltage (L4OV)**				LDO 3 Output Voltage (L3OV)**			
Reset Value	0**	1**	1**	0**	1**	1**	0**	0**

LDO4–LDO3 VOLTAGE CONTROL REGISTER (L43VCR) 8H'3A DEFINITIONS

Bit	Access	Name	Description			
7:4	R/W	L4OV	**Data Code**	**Output Voltage**		
			4h'0	1.00		
			4h'1	1.05		
			4h'2	1.10		
			4h'3	1.15		
			4h'4	1.20		
			4h'5	1.25		
			4h'6	**1.30**		
			4h'7	1.35		
			4h'8	1.40		
			4h'9	1.50		
			4h'A	1.80		
			4h'B	1.90		
			4h'C	2.50		
			4h'D	2.80		
			4h'E	3.00		
			4h'F	**3.30**		

Bit	Access	Name	Description			
3:0	R/W	L3OV	4h'0	1.8		
			4h'1	1.9		
			4h'2	2.0		
			4h'3	2.1		
			4h'4	2.2		
			4h'5	2.3		
			4h'6	2.4		
			4h'7	2.5		
			4h'8	2.6		
			4h'9	2.7		
			4h'A	2.8		
			4h'B	2.9		
			4h'C	**3.0**		
			4h'D	3.1		
			4h'E	3.2		
			4h'F	3.3		

V_{CC}_LDO5 VOLTAGE CONTROL REGISTER (L5VCR) 8H'3B

Bit	7	6	5	4	3	2	1	0
Designation	Reserved				LDO 5 Output Voltage (L5OV)**			
Reset Value	0	0	0	0	0**	0**	1**	0**

V_{CC}_LDO5 VOLTAGE CONTROL REGISTER (L5VCR) 8H'3B DEFINITIONS

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV	**Data Code**	**Output Voltage**		
			4h'0	1.00		
			4h'1	1.05		
			4h'2	**1.10**		
			4h'3	1.15		
			4h'4	1.20		
			4h'5	1.25		
			4h'6	1.30		
			4h'7	1.35		
			4h'8	1.40		
			4h'9	1.50		
			4h'A	1.80		
			4h'B	1.90		
			4h'C	2.50		
			4h'D	2.80		
			4h'E	3.00		
			4h'F	3.30		

Register Programming Examples

Example 1. Setting register 8h'12 value to 8h'3E' will enable LDOs 1–5.

Example 2. Setting register 8h'39 to 8h'CC' will set LDOs 1 and 2 to 3.0V. These voltages will appear at the LDO outputs if the corresponding LDO has been enabled. Programming a voltage value to a LDO, which is off, will affect the LDO output voltage after the LDO is enabled. Enabling and programming the output voltage are separate operations.

DIGITAL INTERFACE CONTROL SIGNALS

Signal	Definition	Active State	Signal Direction
SYS_EN	High Voltage Power Enable	High	Input
PWR_EN	Low Voltage Power Enable	High	Input
SCL	Serial Bus Clock Line	Clock	Input
SDA	Serial Bus Data Line		Bidirectional
nRSTI	Forces an Unconditional Hardware Reset	Low	Input
nRSTO	Forces an Unconditional Hardware Reset	Low	Output
nBATT_FLT	Main Battery Removed or Discharged Indicator	Low	Output
PWR_ON	Wakeup Input to CPU	High	Input
nTEST_JIG	Wakeup Input to CPU	Low	Input
SPARE	Wakeup Input to CPU	High/Low*	Input
EXT_WAKEUP	Wake-Up Output for Application Processor	High	Output
GPIO1/nCHG_EN	General Purpose I/O/External Back-Up Battery Charger	-/Low	Bidirectional/Input
GPIO2	General Purpose I/O	-	Bidirectional

POWER DOMAIN ENABLES

PMU Output	HW Enable	SW Enable
LDO_RTC	-	-
LDO1	SYS_EN	LDO1_EN
LDO2	SYS_EN	LDO2_EN
LDO3	SYS_EN	LDO3_EN
LDO4	PWR_EN/SYS_EN	LDO4_EN
LDO5	PWR_EN/SYS_EN	LDO5_EN
BUCK1	PWR_EN	B1_EN
BUCK2	SYS_EN/PWR_EN	B2_EN
BUCK3	SYS_EN	B3_EN

LDO_RTC TRACKING (nIO_TRACK)

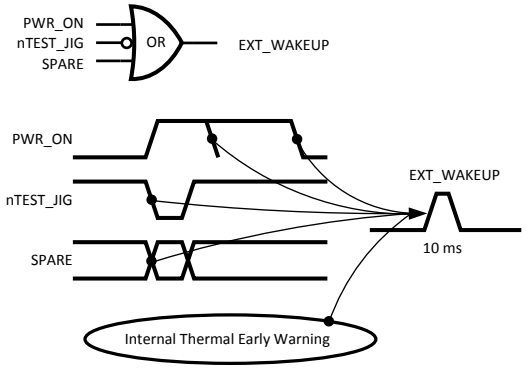
LP3971 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO1 voltage within 200 mV down to 2.8V when LDO1 is enabled. This function can be switched on/off by BPTR (8h'0E) register bit.

LDO4, LDO5 AND BUCK 2 ENABLE SELECTION (LDO4_ESEL, LDO5_ESEL AND BUCK2_ESEL)

LDO4, 5 and BUCK2 power domain enable is possible to change between SYS_EN and PWR_EN by register bits.

WAKE-UP FUNCTIONALITY (PWR_ON, nTEST_JIG, SPARE AND EXT_WAKEUP)

Three input pins can be used to assert wakeup output for 10 ms for application processor notification to wakeup. SPARE Input can be programmed through I^2C compatible interface to be active low or high (SPARE bit, Default is active low '1'). A reason for wakeup event can be read through I^2C compatible interface also. Additionally wakeup inputs have 30 ms de-bounce filtering. Furthermore PWR_ON have distinguishing between short and long (~1s) pulses (push button input). LP3971 also has an internal Thermal Shutdown early warning that generates a wakeup to the system also. This is generated usually at 125°C.



WAKEUP register bits	Reason for WAKEUP
WUP0	SPARE
WUP1	TEST_JIG
WUP2	PWR_ON short pulse
WUP3	PWR_ON long pulse
TSD_EW	TSD Early Warning

INTERNAL THERMAL SHUTDOWN PROCEDURE

Thermal shutdown is build to generate early warning (typ. 125°C) which triggers the EXT_WAKEUP for the processor acknowledge. When a thermal shutdown triggers (typ. 160°C) the PMU will reset the system until the device cools down.

BATTERY SWITCH AND BACK UP BATTERY CHARGER

When Back-Up battery is connected but the main battery has been removed or its supply voltage too low, LP3971 uses Back-Up Battery for generating LDO_RTC voltage. When Main Battery is available the battery fet switches over to the main battery for LDO_RTC voltage. When Main battery voltage is too low or removed nBATT_FLT is asserted. If no back up battery exists, the battery switch to back up can be switched off by nBU_BAT_EN bit. User can set the battery fault determination voltage and battery charger current via I^2C compatible interface. Enabling of back up battery charger can be done via serial interface (nBAT_CHG_EN) or external charger enable pin (nCHG_EN). Pin 29 is set as external charger enable input by default. A SHUTBKUPBAT register bit can be used to avoid discharging back up battery during storage etc. By setting this bit before removing main battery the back up battery connection will not draw any current and stays like this until the bit is set to default or the system is reset.

GENERAL PURPOSE I/O FUNCTIONALITY (GPIO1 AND GPIO2)

LP3971 has 2 general purpose I/Os for system control. I^2C compatible interface will be used for setting any of the pins to input, output or hi-Z mode. Inputs value can be read via serial interface (GPI1,2 bits). The pin 29 functionality needs to be set to GPIO by serial interface register bit nEXTCHGEN. (GPIO/CHG)

Controls				Port Function	Reg	batmonchg
GPIO<1>	GPIO<1>	Nextchgen_sel	bucen	GPIO1	Gpin 1	Function
X	X	1	0	Input = 0	0	Enabled
X	X	1	0	Input = 1	0	Not Enabled
1	0	1	X	X	0	

Controls				Port Function	Reg	batmonchg
GPIO<1>	GPIO<1>	Nextchgen_sel	bucen	GPIO1	Gpin 1	Function
X	X	X	1	X		Enabled
0	0	0	X	HiZ		
1	0	0	X	Input (dig)->	Input	
0	1	0	X	Output = 0	0	
1	1	0	X	Output = 1	0	

GPIO<1>	GPIO<1>	Factory fm disabled	GPIO_tstiob	GPIO2	gpin2
0	0		1	HiZ	0
1	0		1	Input (dig)->	input
0	1		1	Output = 0	0
1	1		1	Output = 1	0

The LP3971 has provision for two battery connections, the main battery Vbat and Backup Battery (See Applications Schematic Diagrams Figure 1 and Figure 2).

The function of the battery switch is to connect power to the RTC LDO from the appropriate battery, depending on conditions described below:

- If only the backup battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If only the main battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If both batteries are applied, and the main battery is sufficiently charged (V_{BAT} > 3.1V), the switch will automatically connect the RTC LDO power to the main battery.
- As the main battery is discharged by use, the user will be warned by a separate circuit called nBATT_FLT. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch will protect the RTC LDO by disconnecting from the main battery and connecting to the backup battery.
  - The main battery voltage at which the RTC LDO is switched from main to backup battery is 2.9V typically.
  - There is a hysterisis voltage in this switch operation so, the RTC LDO will not be reconnected to main battery until main battery voltage is greater than 3.1V typically.
- Additionally, the user may wish to disable the battery switch, such as, in the case when only a main battery is used. This is accomplished by setting the “no back up battery bit” in the control register 8h’89 bit 7 NBUB. With this bit set to “1”, the above described switching will not occur, that is the RTC LDO will remain connected to the main battery even as it is discharged below the 2.9 Volt threshold.

REGULATED VOLTAGES OK

All the power domains have own register bit (X_OK) that processor can read via serial interface to be sure that enabled powers are OK (regulating). Note that these read only bits are only valid when regulators are settled (avoid reading these bits during voltage change or power up).

THERMAL MANAGEMENT

Application: There is a mode wherein all 6 comparators (flags) can be turned on via the “enallflags” control register bit. This mode allows the user to interrogate the device or system temperature under the set operating conditions. Thus, the rate of temperature change can also be estimated. The system may then negotiate for speed and power trade off, or deploy cooling maneuvers to optimize system performance. The “enallflags” bit needs enabled only when the “bct<2:0> bits are read to conserve power.

Note: The thermal management flags have been verified functional. Presently these registers are accessible by factory only. If there is a demand for this function, the relevant register controls may be shifted into the user programmable bank; the temperature range and resolution of these flags, might also be refined/redefined.

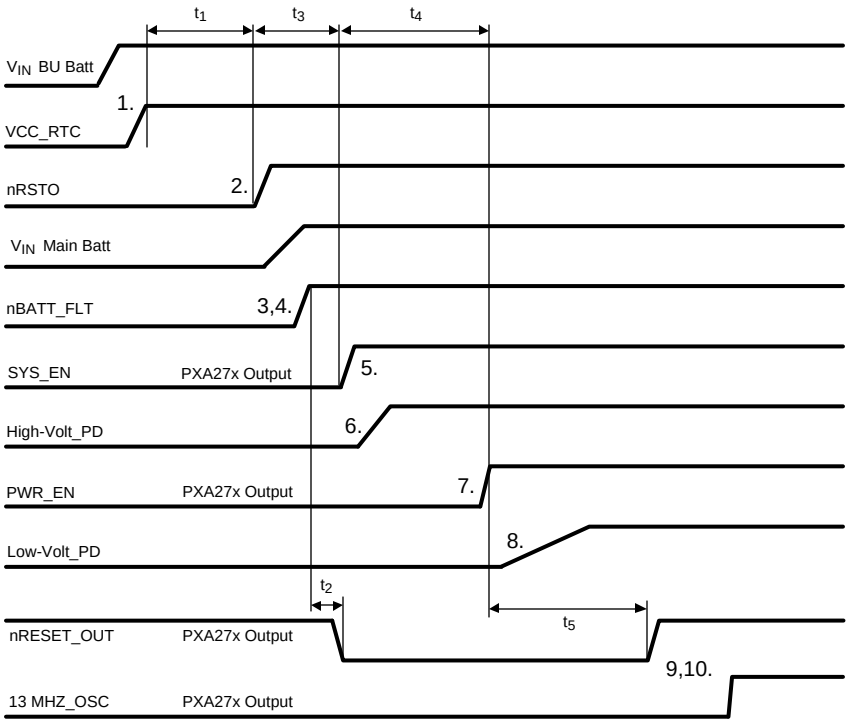
Application Note - LP3971 Reset Sequence

INITIAL COLD START POWER ON SEQUENCE

1. The Back up battery is connected to the PMU, power is applied to the back-up battery pin, the RTC_LDO

turns on and supplies a stable output voltage to the V_{CC}_BATT pin of the Applications processor (initiating the power-on reset event) with nRSTO asserted from the LP3971 to the processor.

2. nRSTO de-asserts after a minimum of 50 mS.
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is applied, the LP3971 de-asserts nBATT_FLT. Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other.
5. The Applications processor asserts SYS_EN, the LP3971 enables the system high-voltage power supplies. The Applications processor starts its countdown timer set to 125 mS.
6. The LP3971 enables the high-voltage power supplies.
   – LDO1 power for V_{CC}_MVT (Power for internal logic and I/O Blocks), BG (Bandgap reference voltage), OSC13M (13 MHz oscillator voltage) and PLL enabled first, followed by others if delay is on.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 mS period.
8. The Applications processor asserts PWR_EN (ext. pin or I^2C), the LP3971 enables the low-voltage regulators.
9. Countdown timer expires; If enabled power domains are OK (I^2C read) the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.



Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other and can occur is either order.

POWER-ON TIMING

Symbol	Description	Min	Typ	Max	Units
t1	Delay from V_{CC}_RTC assertion to nRSTO de-assertion	50			mS
t2	Delay from nBATT_FLT de-assertion to nRSTI assertion		100		µS

Symbol	Description	Min	Typ	Max	Units
t3	Delay from nRST de-assertion to SYS_EN assertion		10		mS
t4	Delay from SYS_EN assertion to PWR_EN assertion		125		mS
t5	Delay from PWR_EN assertion to nRSTO de-assertion		125		mS

HARDWARE RESET SEQUENCE

Hardware reset initiates when the nRSTI signal is asserted (low). Upon assertion of nRST the processor enters hardware reset state. The LP3971 holds the nRST low long enough (50 ms typ.) to allow the processor time to initiate the reset state.

RESET SEQUENCE

1. nRSTI is asserted.
2. nRSTO is asserted and will de-asserts after a minimum of 50 mS
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is turned on, the LP3971 de-asserts nBATT_FLT.
5. The Applications processor asserts SYS_EN, the LP3971 enables the system high-voltage power supplies. The Applications processor starts its countdown timer.
6. The LP3971 enables the high-voltage power supplies.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer.
8. The Applications processor asserts PWR_EN, the LP3971 enables the low-voltage regulators.
9. Countdown timer expires; If enabled power domains are OK (I^2C read) the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.

APPLICATION HINTS

LDO CONSIDERATIONS

External Capacitors

The LP3971's regulators require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability. It is recommended that a 1.0 µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 µF over the entire operating temperature range.

Output Capacitor

The LDO's are designed specifically to work with very small ceramic output capacitors. A 1.0 µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

No-Load Stability

The LDO's will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

Capacitor Characteristics

The LDO's are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDO's.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type. In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 23 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result

in the capacitance value falling below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

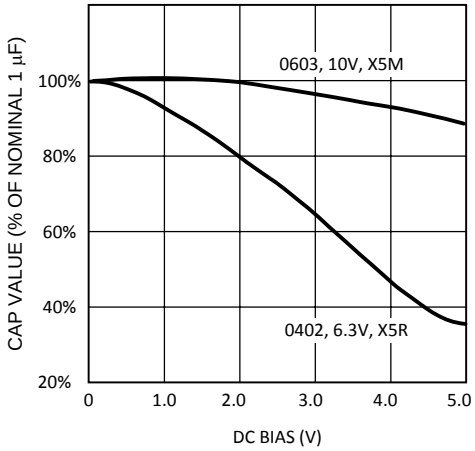


Figure 23. Graph Showing a Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

BUCK CONSIDERATIONS

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings at max ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (2)$$

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current (1500 mA)
- V_{IN}: Maximum input voltage in application
- L: Min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: Minimum switching frequency (1.6 MHz)
- V_{OUT}: Output voltage

Method 2

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of TBD mA.

A 2.2 µH inductor with a saturation current rating of at least TBD mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for a good efficiency. Table 2 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$\text{where } r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}} \tag{3}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$

Table 2. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (Typ)
FDSE0312-2R2M	Toko	3.0 x 3.0 x 1.2	160 mΩ
DO1608C-222	Coilcraft	6.6 x 4.5 x 1.8	80 mΩ

Output Capacitor Selection

Use a 10 µF, 6.3V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as:

$$V_{PP-C} = \frac{I_{RIPPLE}}{4 * f * C} \tag{4}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR} \quad (5)$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2} \quad (6)$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

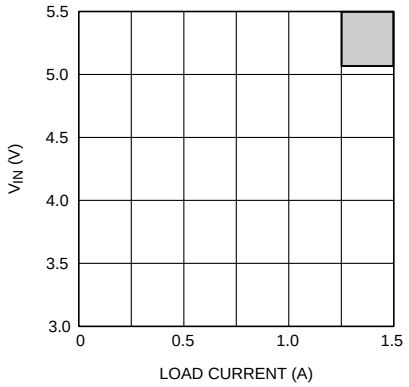
Table 3. Suggested Capacitor and Their Suppliers

Model	Type	Vendor	Voltage	Case Size Inch (mm)
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)

Buck Output Ripple Management

If V_{IN} and I_{LOAD} increase, the output ripple associated with the Buck Regulators also increases. The figure below shows the safe operating area. To ensure operation in the area of concern it is recommended that the system designer circumvents the output ripple issues to install schottky diodes on the Bucks(s) that are expected to perform under these extreme corner conditions.

(Schottky diodes are recommended to reduce the output ripple, if system requirements include this shaded area of operation. V_{IN} > 5.1V and I_{LOAD} > 1.24)



Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the converters can be implemented by following a few simple design rules.

1. Place the converters, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the converter and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the converter by the inductor to the output filter capacitor and then back through

ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.

3. Connect the ground pins of the converter and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the converter by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the converter circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. Place noise sensitive circuitry, such as radio RF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

REVISION HISTORY

Changes from Revision U (May 2013) to Revision V	Page
• Changed layout of National Data Sheet to TI format	45

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3971SQ-2G16/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	71-2G16
LP3971SQ-2G16/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	71-2G16
LP3971SQ-B410/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	71-B410
LP3971SQ-B410/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	71-B410
LP3971SQ-D510/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	71-D510
LP3971SQ-D510/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	71-D510
LP3971SQ-N510/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	71-N510
LP3971SQ-N510/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	71-N510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

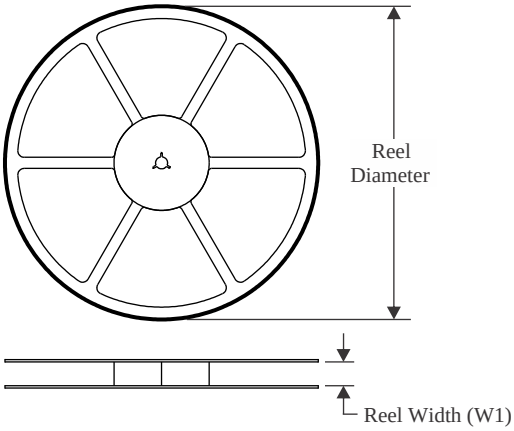
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

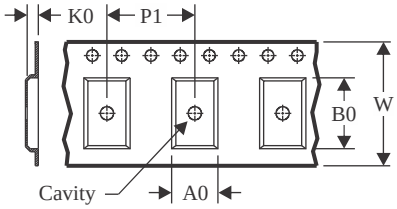
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

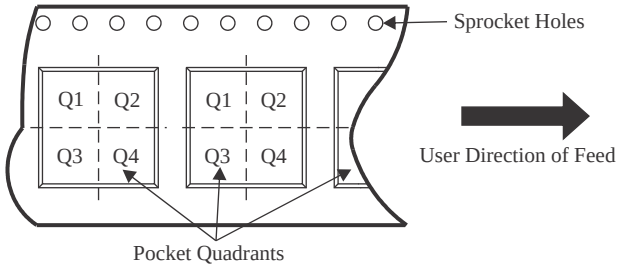


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

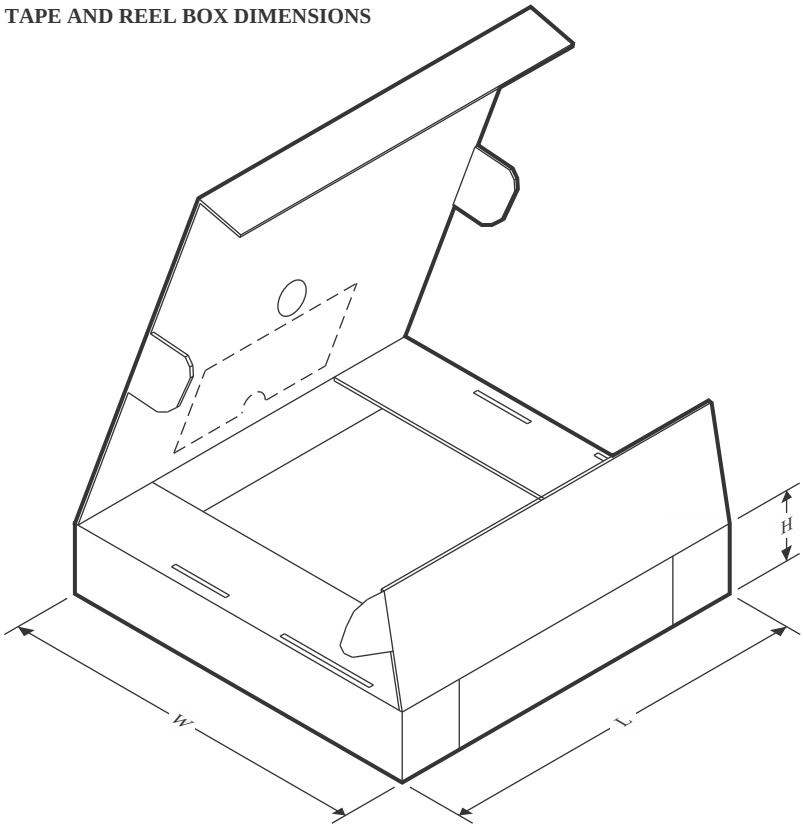
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3971SQ-2G16/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3971SQ-B410/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3971SQ-D510/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3971SQ-N510/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

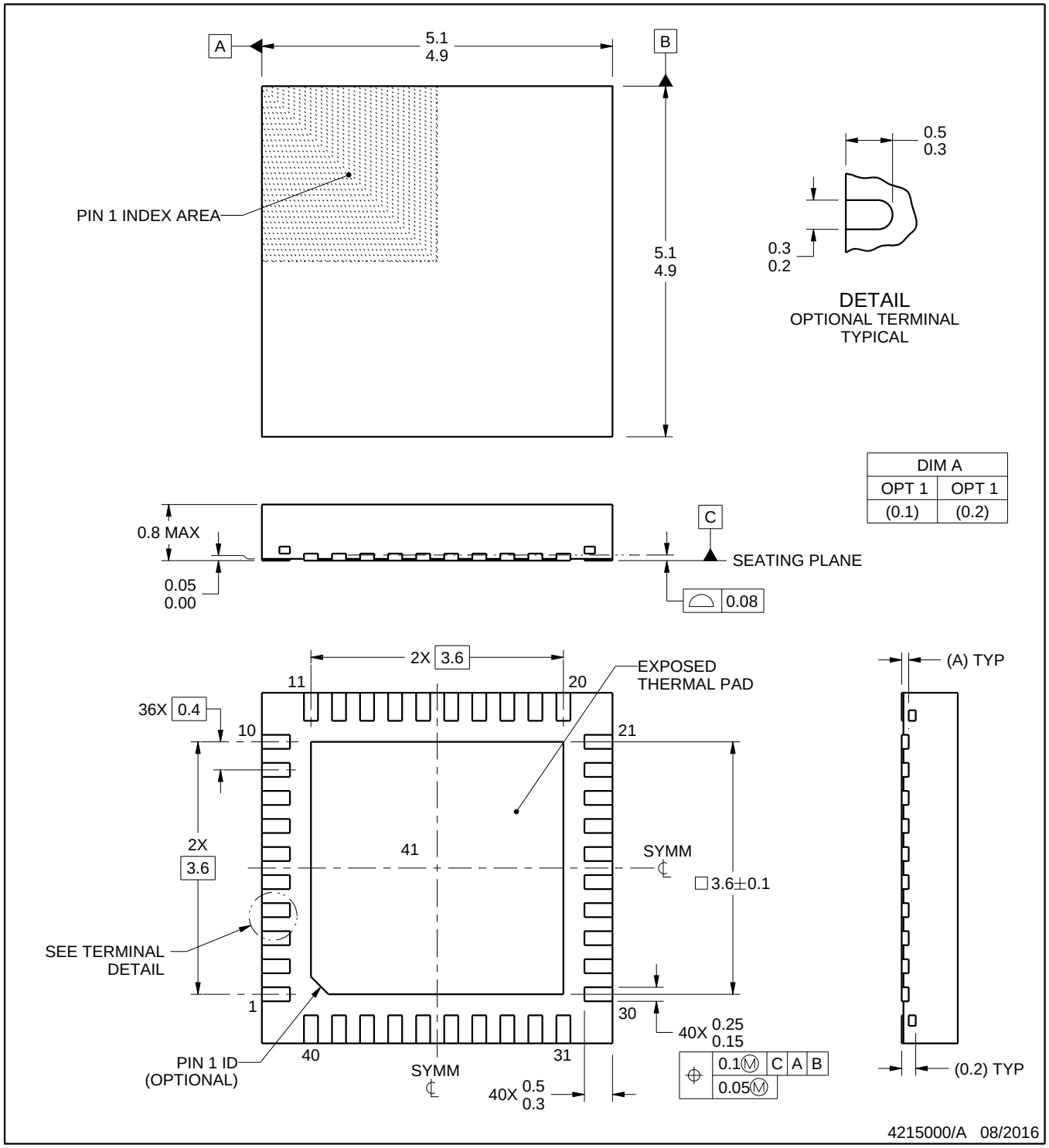
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3971SQ-2G16/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3971SQ-B410/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3971SQ-D510/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3971SQ-N510/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0

PACKAGE OUTLINE

RSB0040A

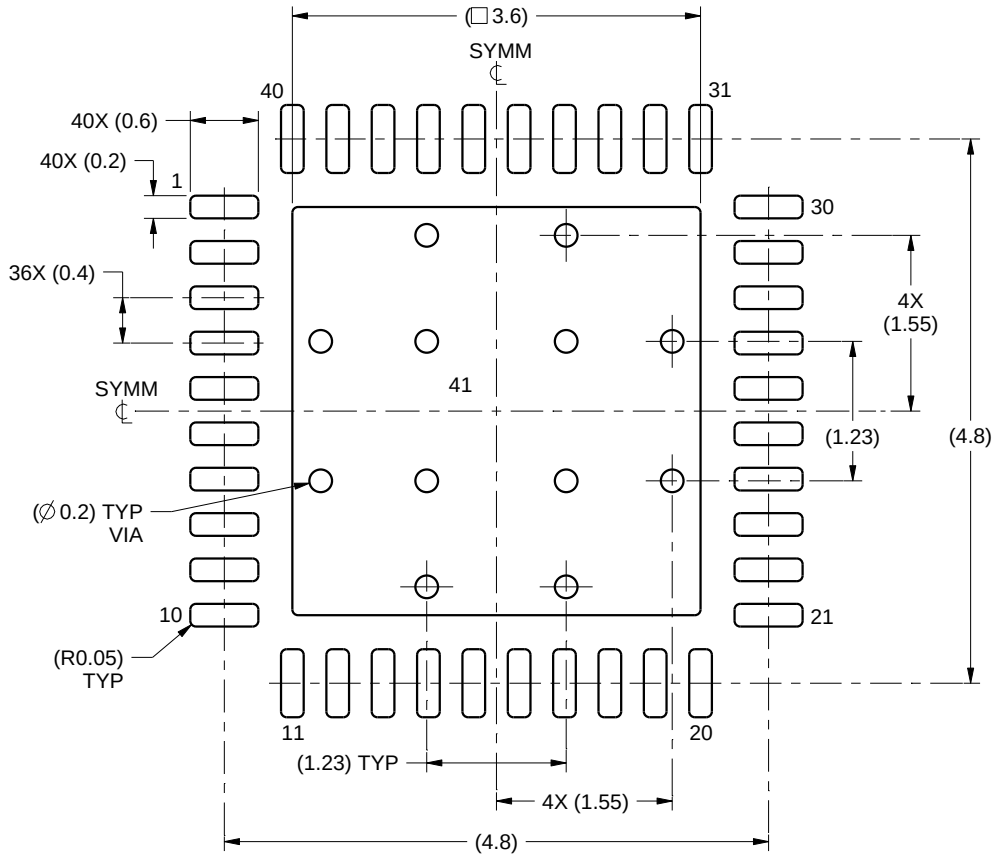
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

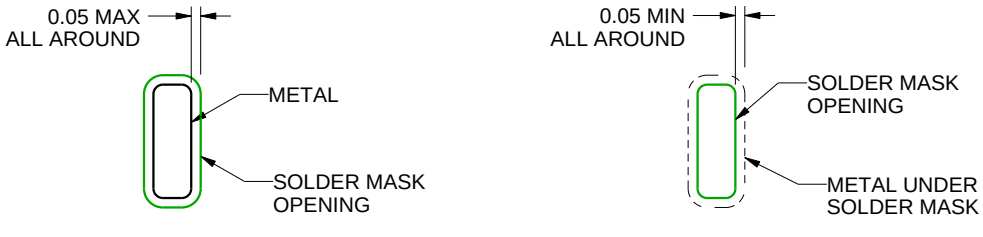


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

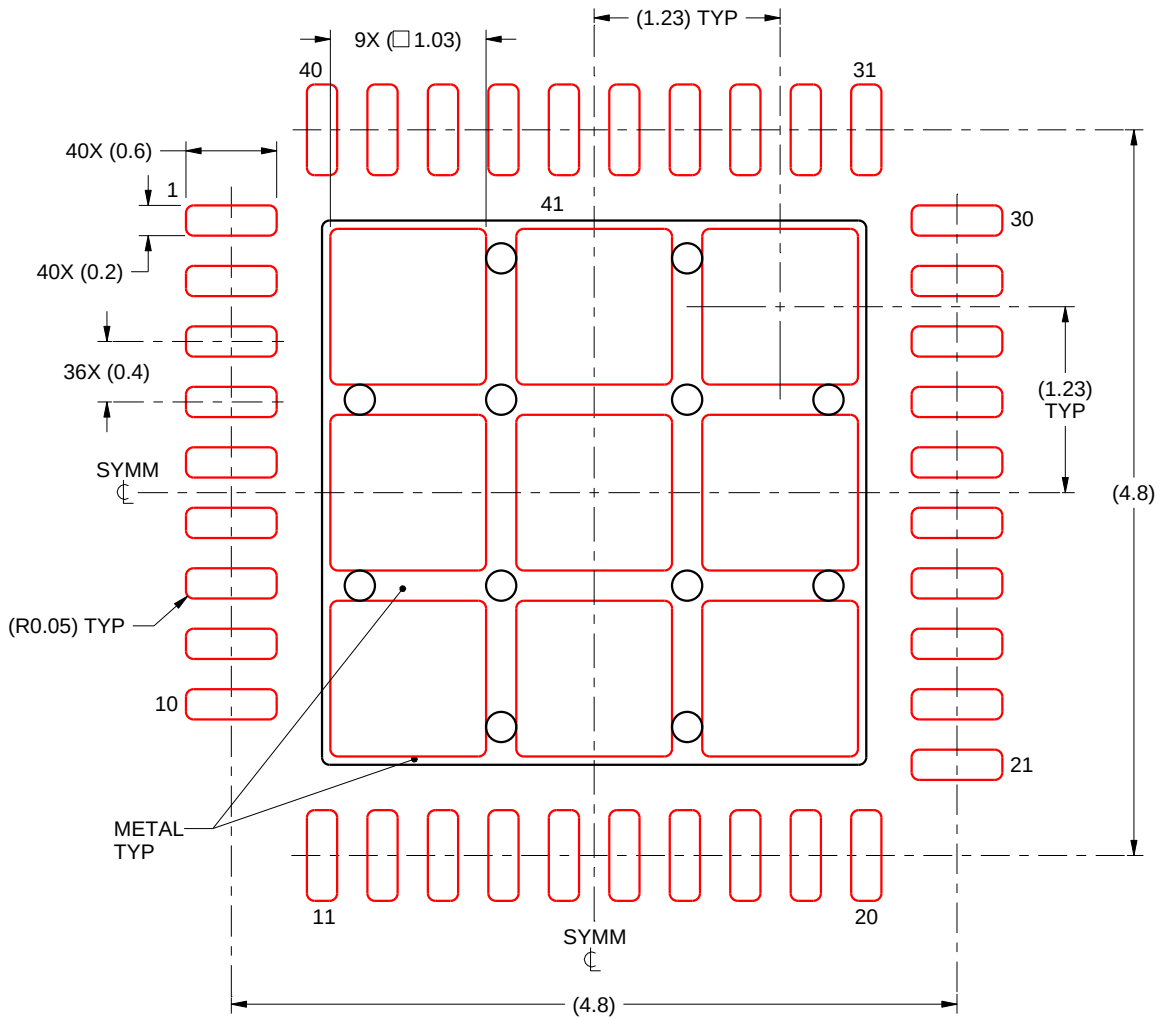


SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

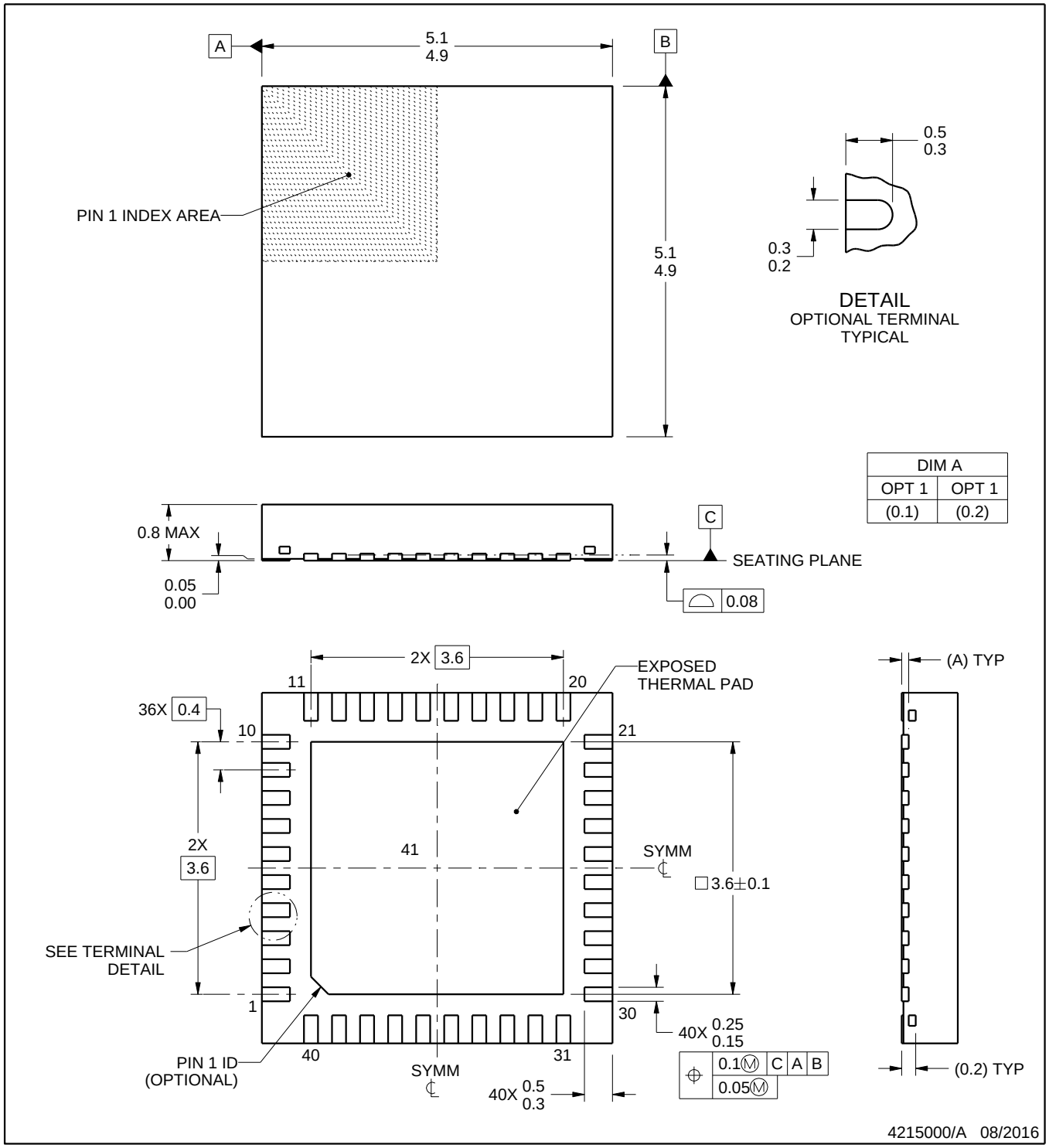
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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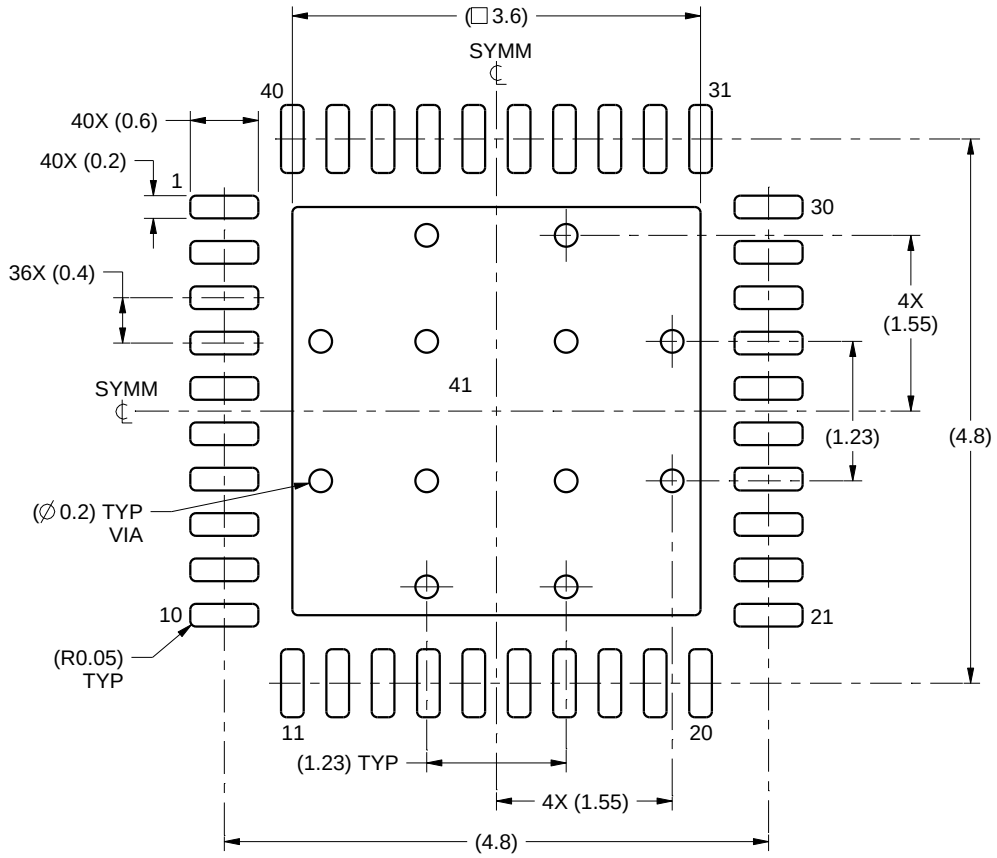
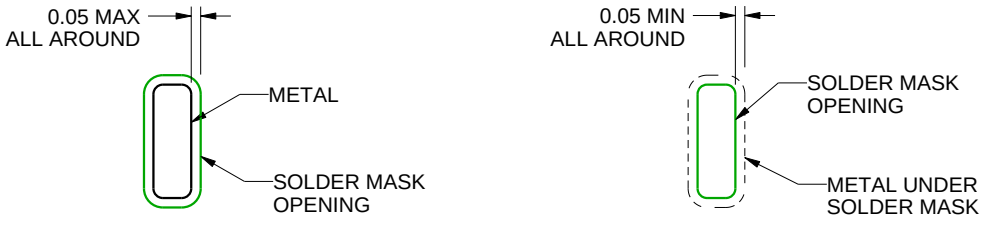


LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

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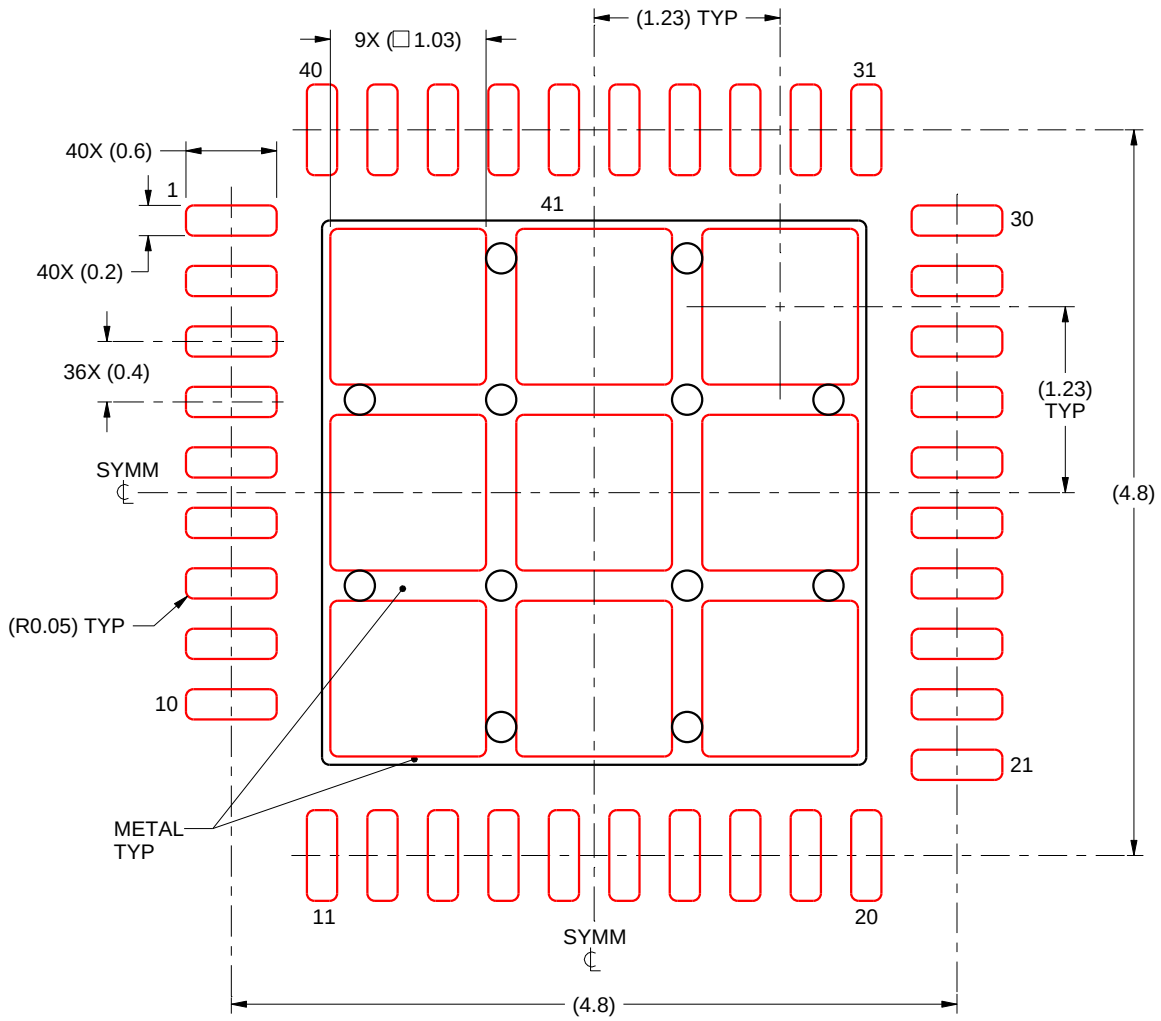

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

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