LP3972 Power Management Unit for Advanced Application Processors

1 Features

- Compatible With Advanced Applications Processors Requiring Dynamic Voltage Management (DVM)
- Backup Battery Charger With Automatic Switch for Lithium-Manganese Coin-Cell Batteries and Super Capacitors
- I^2C-Compatible High-Speed Serial Interface
- Software Control of Regulator Functions and Settings
- Thermal and Current Overload Protections
- Three Buck Regulators for Powering High-Current Processor Functions or I/Os
  - Programmable V_{OUT} from 0.725 V to 3.3 V
  - Up to 95% Efficiency and 1.6-A Output Current
  - ±3% Output Voltage Accuracy
- Six LDOs for Powering RTC, Peripherals, and I/Os
  - Programmable V_{OUT} of 1 V to 3.3 V
  - ±3% Output Voltage Accuracy
    - LDO_RTC 30 mA
    - LDO1 300 mA
    - LDO2 150 mA
    - LDO3 150 mA
    - LDO4 150 mA
    - LDO5 400 mA

2 Applications

- Smart Phones
- Personal Media Players
- Digital Cameras
- Application Processors
  - Marvell PXA
  - Freescale
  - Samsung

3 Description

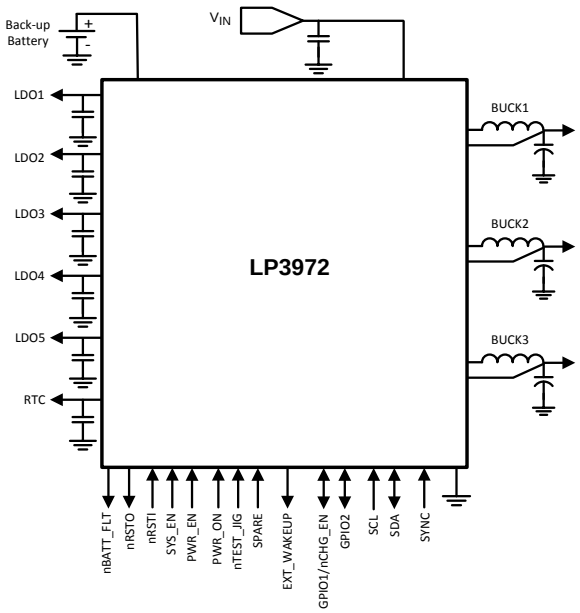
The LP3972 is a multi-function programmable power management unit (PMU) designed especially for advanced application processors. The LP3972 is optimized for low-power handheld applications and provides six low-dropout low-noise linear regulators, three DC-DC magnetic buck regulators, a backup battery charger, and two GPIOs. A high-speed serial interface is included to program individual regulator output voltages as well as on and off control.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3972	WQFN (40)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (May 2013) to Revision L — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision J (May 2013) to Revision K — **Page**

- Changed layout of National Data Sheet to TI format ... 55

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5 Device Comparison Tables

Table 1. Supply Specifications

SUPPLY	V_{OUT} (V)(1)(2)		I_{MAX}: MAXIMUM CURRENT
	RANGE	RESOLUTION	CURRENT (mA)
	(V)	(mV)	
LDO_RTC	2.8	N/A	30-mA DC source 10-mA backup source
LDO1 (V_{CC}_MVT)	1.7 to 2	25	300
LDO2	1.8 to 3.3	100	150
LDO3	1.8 to 3.3	100	150
LDO4	1.0 to 3.3	50 - 600	150
LDO5 (V_{CC}_SRAM)	0.850 to 1.5	25	400
BUCK1 (V_{CC}_APPS)	0.725 to 1.5	25	1600
BUCK2	0.8 to 3.3	50 - 600	1600
BUCK3	0.8 to 3.3	50 - 600	1600

(1) All voltages are with respect to the potential at the GND pin.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200-pF capacitor discharged directly into each pin. (EAIJ).

Table 2. Default Voltage Options(1)(2)(3)

VERSION	LP3972SQ-A514		LP3972SQ-A413	
Enable	Version A		Version A	
LDO_RTC	—	2.8 V	—	2.8 V
LDO1	SYS_EN	1.8 V	SYS_EN	1.8 V
LDO2	SYS_EN	1.8 V (D)	SYS_EN	1.8 V (D)
LDO3	SYS_EN	3 V (D)	SYS_EN	3 V (D)
LDO4	SYS_EN	3 V (D)	SYS_EN	2.8 V (D)
LDO5	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK1	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK2	SYS_EN	3.3 V	SYS_EN	3 V
BUCK3	SYS_EN	1.8 V	SYS_EN	1.8 V
VERSION	**P3972SQ-E514**		**LP3972SQ-I514**	
Enable	Version E		Version I	
LDO_RTC	—	2.8 V	—	2.8 V
LDO1	SYS_EN	1.8 V	SYS_EN	1.8 V
LDO2	SYS_EN	1.8 V (E)	SYS_EN	1.8 V (E)
LDO3	SYS_EN	3 V (D)	SYS_EN	3 V (E)
LDO4	SYS_EN	3 V (D)	SYS_EN	3 V (E)
LDO5	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK1	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK2	SYS_EN	3.3 V	SYS_EN	3.3 V
BUCK3	SYS_EN	1.8 V	SYS_EN	1.8 V

(1) All voltages are with respect to the potential at the GND pin
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200-pF capacitor discharged directly into each pin. (EAIJ).
(3) E = Regulator is ENABLED during start-up. D = Regulator is DISABLED during start-up.

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Table 2. Default Voltage Options(1)(2)(3) (continued)

VERSION	LP3972SQ-I414		LP3972SQ-0514	
Enable	Version I		Version 0	
LDO_RTC	—	2.8 V	Tracking enabled	3.3 V w/ tracking
LDO1	SYS_EN	1.8 V	SYS_EN	1.8 V
LDO2	SYS_EN	1.8 V (E)	SYS_EN	1.8 V (E)
LDO3	SYS_EN	3 V (E)	SYS_EN	3.3 V (E)
LDO4	SYS_EN	3 V (E)	SYS_EN	3 V (E)
LDO5	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK1	PWR_EN	1.4 V	PWR_EN	1.4 V
BUCK2	SYS_EN	3 V	SYS_EN	3.3 V
BUCK3	SYS_EN	1.8 V	SY_EN	1.8 V
VERSION	**LP3972SQ-5810**			
Enable	Version 5			
LDO_RTC	—	2.8 V		
LDO1	SYS_EN	1.8 V		
LDO2	SYS_EN	1.8 V (E)		
LDO3	SYS_EN	2.5 V (E)		
LDO4	PWR_EN	1.3 V (E)		
LDO5	PWR_EN	1.1 V		
BUCK1	PWR_EN	1.35 V		
BUCK2	SYS_EN	1.2 V		
BUCK3	SYS_EN	1.8 V		

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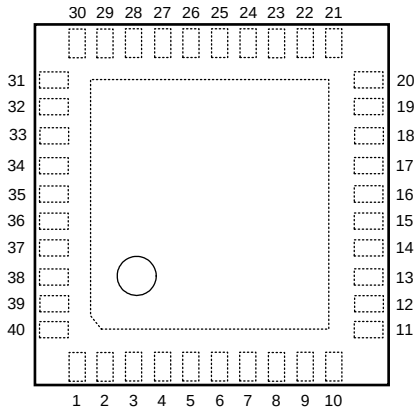
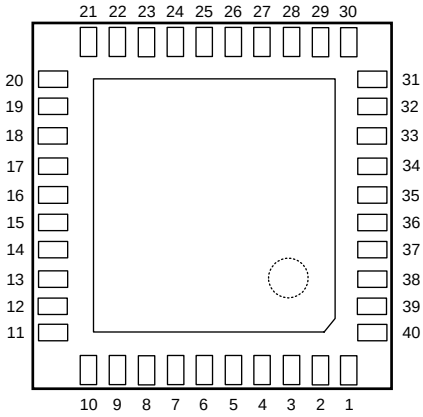
6 Pin Configuration and Functions

RSB Package
40-Pin WQFN
Top View



RSB Package
40-Pin WQFN
Bottom View



Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NUMBER	NAME(2)			
1	PWR_ON	I	D	This is an active HI push button input which can be used to signal PWR_ON and PWR_OFF events to the CPU by controlling the EXT_WAKEUP [pin4] and select contents of register 8H'88.
2	nTEST_JIG	I	D	This is an active LOW input signal used for detecting an external HW event. The response is seen in the EXT_WAKEUP [pin4] and select contents of register 8H'88.
3	SPARE	I	D	This is an input signal used for detecting a external HW event. The response is seen in the EXT_WAKEUP [pin4] and select contents of register 8H'88. The polarity on this pin is assignable.
4	EXT_WAKEUP	O	D	This pin generates a single 10-ms pulse output to CPU in response to input from pins 1, 2, and 3. Flags CPU to interrogate register 8H'88.
5	FB1	I	A	Buck1 input feedback pin.
6	V_{IN}	I	PWR	Battery input (internal circuitry and LDO1-3 power input)
7	VOUT LDO1	O	PWR	LDO1 output
8	VOUT LDO2	O	PWR	LDO2 output
9	nRSTI	I	D	Active low reset pin. Signal used to reset the device (by default is pulled high internally). Typically a push button reset.
10	GND1	G	G	Ground
11	VREF	O	A	Bypass capacitor for the high internal impedance reference.
12	VOUT LDO3	O	PWR	LDO3 output
13	VOUT LDO4	O	PWR	LDO4 output
14	VIN LDO4	I	PWR	Power input to LDO4 — this can be connected to either from a 1.8-V supply to main battery supply.
15	VIN BUBATT	I	PWR	Backup battery input supply.
16	VOUT LDO_RTC	O	PWR	LDO_RTC output supply to the RTC of the application processor.
17	nBATT_FLT	O	D	Main battery fault output, indicates the main battery is low (discharged) or the DC source has been removed from the system. This gives the processor an indicator that the power will shut down. During this time the processor will operate from the backup coin cell.
18	PGND2	G	G	Buck2 NMOS power ground
19	SW2	O	PWR	Buck2 switcher output

(1) A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin I: Input Pin I/O: Input/Output Pin O: Output Pin
(2) In this document, active-low logic items are prefixed with a lowercase "n".

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Pin Functions (continued)

PIN		I/O	TYPE(1)	DESCRIPTION
NUMBER	NAME(2)			
20	VIN BUCK2	I	PWR	Battery input power to Buck2
21	SDA	I/O	D	I^2C Data (Bidirectional)
22	SCL	I	D	I^2C Clock
23	FB2	I	A	Buck2 input feedback pin
24	nRSTO	O	D	Reset output from the PMIC to the processor
25	VOUT LDO5	O	PWR	LDO5 output
26	VIN LDO5	I	PWR	Power input to LDO5, this can be connected to V_{IN} or to a separate 1.8-V supply.
27	VDDA	I	PWR	Analog Power for VREF, BIAS
28	FB3	I	A	Buck3 Feedback
29	GPIO1 / nCHG_EN	I/O	D	General purpose I/O / Ext. backup battery charger enable pin. This pin enables the main battery or DC source power to charge the backup battery. This pin toggled via the application processor. By grounding this pin the DC source continuously charges the backup battery.
30	GPIO2	I/O	D	General purpose I/O
31	VIN BUCK3	I	PWR	Battery input power to Buck3
32	SW3	O	PWR	Buck3 switcher output
33	PGND3	G	G	Buck3 NMOS Power ground
34	BGND1,2,3	G	G	Bucks 1, 2 and 3 analog ground
35	SYNC	I	D	Frequency synchronization: Connection to an external clock signal PLL to synchronize the PMIC internal oscillator.
36	SYS_EN	I	D	Input digital enable pin for the high voltage power domain supplies. Output from the Monahans processor.
37	PWR_EN	I	D	Digital enable pin for the low-voltage domain supplies. Output signal from the Monahans processor
38	PGND1	G	G	Buck1 NMOS power ground
39	SW1	O	PWR	Buck1 switcher output
40	VIN BUCK1	I	PWR	Battery input power to Buck1

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
All inputs	−0.3	6.5	V
GND-to-GND SLUG	−0.3	0.3	V
Junction temperature, $T_{J\text{-}MAX}$		150	°C
Power dissipation (T_A = 70°C)(3)		3.2	W
Maximum lead temperature (soldering)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	2.7		5.5	V
V_{IN}LDO4, 5	1.74		V_{IN}	V
Junction temperature, T_J	−40		125	°C
Operating temperature, T_A	−40		85	°C
Maximum power dissipation (T_A = 70°C)(1)(2)(3)			2.2	W

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.
(2) Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51–7. The test board is a 4-layer FR-4 board measuring 102 mm × 76 mm × 1.6 mm with a 2 × 1 array of thermal vias. The ground plane on the board is 50 mm × 50 mm. Thickness of copper layers are 36 µm/1.8 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The value of $R_{\theta JA}$ of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, see Texas Instruments Application Note *Leadless Leadframe Package (LLP)*(SNOA401).
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

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7.4 Thermal Information

THERMAL METRIC[1]		LP3972 RSB (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Typical values and limits apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C, unless otherwise specified. All voltages are with respect to the potential at the GND pin.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}, VDDA, V_{IN} bucks 1, 2 and 3	Battery voltage		2.7	3.6	5.5	V
V_{IN}LDO4, V_{IN}LDO5	Power supply for LDOs 4 and 5		1.74	3.6	V_{IN}	V
T_{SD}	Thermal shutdown[3]	Temperature		160		°C
		Hysteresis		20		

(1) All limits specified at room temperature and at temperature extremes. All room temperature limits are production tested, ensured through statistical analysis or ensured by design. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Input supply must not be higher then VDDA.
(3) This electrical specification is ensured by design.

7.6 Electrical Characteristics: LDO RTC

V_{IN} = 3.6 V, C_{IN} = 1 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1 µF ceramic (unless otherwise noted).
Typical values and limits apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C, unless otherwise specified. All voltages are with respect to the potential at the GND pin.[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} accuracy	Output voltage accuracy	V_{IN} connected, load current = 1 mA	2.632	2.8	2.968	V
ΔV_{OUT}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V[4] Load current = 1 mA			0.15	%/V
	Load regulation	From main battery Load current = 1 mA to 30 mA			0.05	%/mA
		From backup battery, V_{IN} = 3 V Load current = 1 mA to 10 mA			0.5	
I_{SC}	Short-circuit current limit	From main battery V_{IN} = V_{OUT} + 0.3 V to 5.5 V		100		mA
		From backup battery		30		
$V_{IN} - V_{OUT}$	Dropout voltage	Load current = 10 mA			375	mV
I_{Q_MAX}	Maximum quiescent current	I_{OUT} = 0 mA		30		µA
TP1	RTC LDO input switched from main battery to backup battery	V_{IN} falling		2.9		V
TP2	RTC LDO input switched from backup battery to main battery	V_{IN} rising		3		V
C_{OUT}	Output capacitor	Capacitance for stability	0.7	1		µF
		ESR	5		500	mΩ

(1) All limits specified at room temperature and at temperature extremes. All room temperature limits are production tested, ensured through statistical analysis or ensured by design. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(3) LDO_RTC voltage can track LDO3 voltage. LP3972 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage tracks LDO3 voltage within 200 mV down to 2.8 V when LDO3 is enabled.
(4) V_{IN} minimum for line regulation values is 2.7 V for LDOs 1–3 and 1.8 V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.

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7.7 Electrical Characteristics: LDOs 1 to 5

V_{IN} = 3.6 V, C_{IN} = 1 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic (unless otherwise noted). Typical values and limits apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C, unless otherwise specified. All voltages are with respect to the potential at the GND pin.(1)(2)(3)(4)(5)(6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} accuracy	Output voltage accuracy (default V_{OUT})	Load current = 1 mA	–3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = 3.1 V to 5 V(7), Load Current = 1 mA			0.15	%/V
	Load regulation	V_{IN} = 3.6 V, Load current = 1 mA to I_{MAX}			0.011	%/mA
I_{SC}	Short-circuit current limit	LDO1–4, V_{OUT} = 0 V		400		mA
		LDO5, V_{OUT} = 0 V		500		
$V_{IN} – V_{OUT}$	Dropout voltage	Load current = 50 mA(8)			150	mV
PSRR	Power Supply Ripple Rejection	f = 10 kHz, load current = I_{MAX}		45		dB
I_Q	Quiescent current *On*	I_{OUT} = 0 mA		40		µA
	Quiescent current *On*	I_{OUT} = I_{MAX}		60		
	Quiescent current *Off*	EN is de-asserted		0.03		
T_{ON}	Turnon time	Start-up from shutdown		300		µs
C_{OUT}	Output capacitor	Capacitance for stability 0°C ≤ T_J ≤ 125°C	0.33	0.47		µF
		−40°C ≤ T_J ≤ 125°C	0.68	1.0		
		ESR	5		500	mΩ

(1) All limits specified at room temperature and are production tested, ensured through statistical analysis or ensured by design. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(3) LDO_RTC voltage can track LDO3 voltage. LP3972 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage tracks LDO3 voltage within 200 mV down to 2.8 V when LDO3 is enabled.
(4) V_{IN} minimum for line regulation values is 2.7 V for LDOs 1–3 and 1.8 V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.
(5) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(6) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.7 V for LDOs 1 to 3 and 1.8 V for LDOs 4 and 5.
(7) V_{IN} minimum for line regulation values is 2.7 V for LDOs 1–3 and 1.8 V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.
(8) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.

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7.8 Electrical Characteristics: Buck Converters SW1, SW2, SW3

V_{IN} = 3.6 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2-µH ceramic (unless otherwise noted). Values and limits apply for T_J = 25°C. All voltages are with respect to the potential at the GND pin.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	Default V_{OUT}	−3%		3%	
Eff	Efficiency	Load current = 500 mA		95%		
I_{SHDN}	Shutdown supply current	EN is de-asserted		0.1		µA
	Sync mode clock frequency	Synchronized from 13-MHz system clock	10.4	13	15.6	MHz
f_{OSC}	Internal oscillator frequency			2		MHz
I_{PEAK}	Peak switching current limit			2.1	2.4	A
I_Q	Quiescent current *On*	No-load PFM mode		21		µA
		No-load PWM mode		20		
R_{DSON} (P)	Pin-pin resistance PFET			240		mΩ
R_{DSON} (N)	Pin-pin resistance NFET			200		mΩ
T_{ON}	Turnon time	Start-up from shutdown		500		µs
C_{IN}	Input capacitor	Capacitance for stability	8			µF
C_{OUT}	Output capacitor	Capacitance for stability	8			µF

(1) All limits specified at room temperature and at temperature extremes. All room temperature limits are production tested, ensured through statistical analysis or ensured by design. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) The input voltage range recommended for ideal applications performance for the specified output voltages is V_{IN} = 2.7 V to 5.5 V for 0.8 V < V_{OUT} < 1.7 V_{VIN} = (V_{OUT} + 1 V) to 5.5 V for 1.8 V ≤ V_{OUT} ≤ 3.3 V.
(3) Test condition for V_{OUT} < 2.7 V, V_{IN} = 3.6 V; for V_{OUT} ≥ to 2.7 V, V_{IN} = V_{OUT} + 1 V.

7.9 Electrical Characteristics: Backup Charger

V_{IN} = V_{BATT} = 3.6 V (unless otherwise noted). Typical values and limits apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C. All voltages are with respect to the potential at the GND pin.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operational voltage range	Voltage at V_{IN}	3.3		5.5	V
I_{OUT}	Backup battery charging current	V_{IN} = 3.6 V, Backup_Bat = 2.5 V backup battery charger enabled		190		µA
V_{OUT}	Charger termination voltage	V_{IN} = 5 V, backup battery charger enabled; programmable	2.91	3.1		V
	Backup battery charger short circuit current	Backup_Bat = 0 V, backup battery charger enabled		9		mA
PSRR	Power supply ripple rejection ratio	I_{OUT} ≤ 50 µA, V_{OUT} = 3.15 V V_{OUT} + 0.4 ≤ V_{BATT} = V_{IN} ≤ 5 V f < 10 kHz		15		dB
I_Q	Quiescent current	I_{OUT} < 50 µA		25		µA
C_{OUT}	Output capacitance	0 µA ≤ I_{OUT} ≤ 100 µA		0.1		µF
	Output capacitor ESR		5		500	mΩ

(1) All limits specified at room temperature and at temperature extremes. All room temperature limits are production tested, ensured through statistical analysis or ensured by design. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Backup battery charge current is programmable via the I^2C-compatible interface.

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7.10 Electrical Characteristics: I²C Compatible Serial Interface (SDA and SCL)

V_{IN} = 3.6 V (unless otherwise noted). Typical values and limits appearing in normal type apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C. All voltages are with respect to the potential at the GND pin.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage	See(3)	−0.5		0.3 V_{RTC}	V
V_{IH}	High level input voltage	See(3)	0.7 V_{RTC}		V_{RTC}	
V_{OL}	Low level output voltage	See(3)	0		0.2 V_{TRC}	
I_{OL}	Low level output current	V_{OL} = 0.4 V(3)	3			mA
F_{CLK}	Clock frequency	See(3)			400	kHz

(1) All limits specified at room temperature and are production tested, ensured through statistical analysis or ensured by design.
(2) The I²C signals behave like open-drain outputs and require an external pullup resistor on the system module in the 2-kΩ to 20-kΩ range.
(3) This electrical specification is ensured by design.

7.11 Logic Inputs and Outputs DC Operating Conditions

V_{IN} = V_{BATT} = 3.6 V (unless otherwise noted). Typical values and limits apply for T_J = 25°C; minimum and maximum limits apply over the entire junction temperature range for operation, −40°C to +125°C. All voltages are with respect to the potential at the GND pin.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SYS_EN, PWR_EN, SYNC, nRSTI, PWR_ON, nTEST_JIG, SPARE and GPIs)						
V_{IL}	Low-level input voltage				0.5	V
V_{IH}	High-level input voltage		V_{RTC} − 0.5 V			V
I_{LEAK}	Input leakage current		−1		1	µA
LOGIC OUTPUTS (nRSTO, EXT_WAKEUP and GPOs)						
V_{OL}	Output low level	Load = 0.2 mA = I_{OL} maximum			0.5	V
V_{OH}	Output high level	Load = −0.1 mA = I_{OL} maximum	V_{RTC} − 0.5 V			V
I_{LEAK}	Output leakage current	V_{ON} = V_{IN}			5	µA
LOGIC OUTPUT (nBATT_FLT)						
	nBATT_FLT threshold voltage	Programmable via serial interface Default = 2.8 V	2.4	2.8	3.4	V
V_{OL}	Output low level	Load = 0.4 mA = I_{OL} maximum			0.5	V
V_{OH}	Output high level	Load = −0.2 mA = I_{OH} maximum	V_{RTC} − 0.5 V			V
I_{LEAK}	Input leakage current				5	µA

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7.12 I²C Compatible Serial Interface Timing Requirements (SDA and SCL)

All voltages are with respect to the potential at the GND pin. See(1)(2)(3)

		MIN	NOM	MAX	UNIT
t_{BF}	Bus-free time between start and stop	1.3			µs
t_{HOLD}	Hold Time repeated start condition	0.6			µs
t_{CLKLP}	CLK low period	1.3			µs
t_{CLKHP}	CLK high period	0.6			µs
t_{SU}	Setup time repeated start condition	0.6			µs
$t_{DATAHLD}$	Data hold time	0			µs
t_{CLKSU}	Data set up time	100			ns
T_{SU}	Setup time for start condition	0.6			µs
T_{TRANS}	Maximum pulse width of spikes that must be suppressed by the input filter of both DATA and CLK signals		50		ns

(1) All limits specified at room temperature and are production tested, ensured through statistical analysis or ensured by design.
(2) The I²C signals behave like open-drain outputs and require an external pullup resistor on the system module in the 2-kΩ to 20-kΩ range.
(3) This electrical specification is ensured by design.

7.13 Power-On Timing Delays

See *Initial Cold Start Power-On Sequence*.

	DESCRIPTION	MIN	TYP	MAX	UNIT
t1	Delay from V_{CC}_RTC assertion to nRSTO de-assertion	50			ms
t2	Delay from nBATT_FLT de-assertion to nRSTI assertion		100		µs
t3	Delay from nRST de-assertion to SYS_EN assertion		10		ms
t4	Delay from SYS_EN assertion to PWR_EN assertion		125		ms
t5	Delay from PWR_EN assertion to nRSTO de-assertion		125		ms

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7.14 Typical Characteristics

7.14.1 LDO Dropout Voltage vs Load Current Collect Data for all LDOs

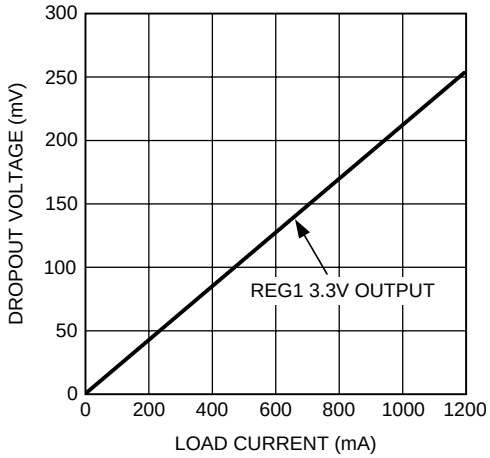


Figure 1. Dropout Voltage vs Load Current

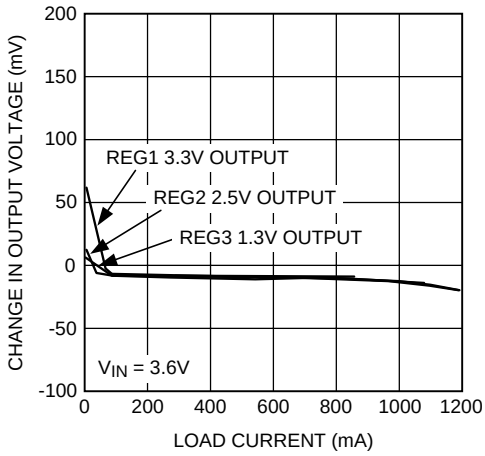
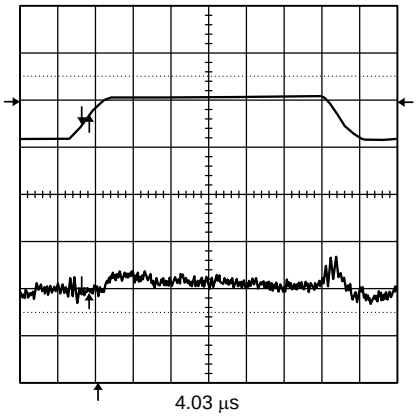
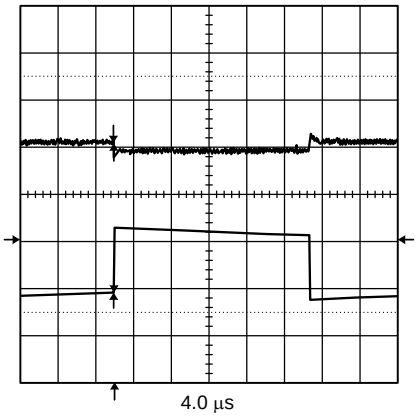


Figure 2. Change In Output Voltage vs Load Current



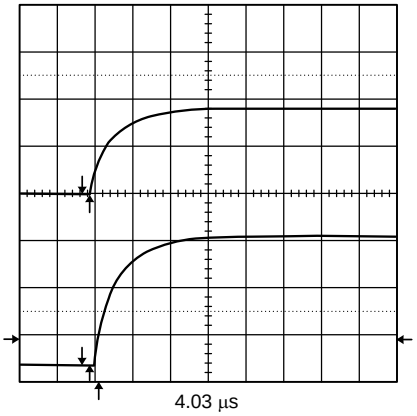
V_{IN} = 3 V to 4 V V_{OUT} = 1.8 V Load = 100 mA

Figure 3. LDO1 Line Regulation



V_{IN} = 4.1 V V_{OUT} = 1.8 V No-Load = 100 mA

Figure 4. LDO1 Load Transient



SYS_ENABLE from 0 Load (V) = 100 mA LDO1 Channel 2 LDO4 Channel 1

Figure 5. Enable Start-Up Time (LDO1)

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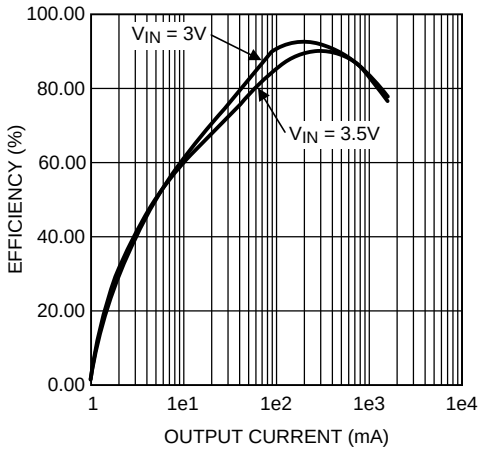
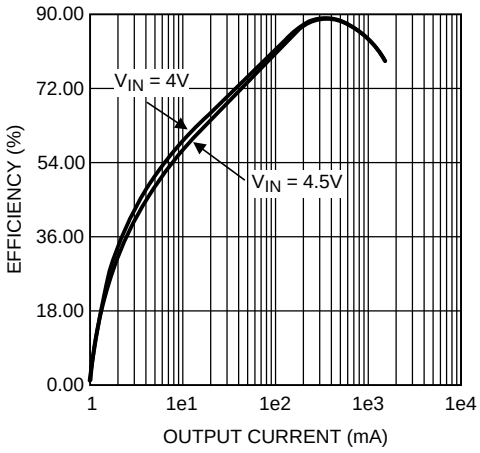
7.14.2 Buck1 Output Efficiency vs. Load Current Varied From 1 mA to 1.5 A



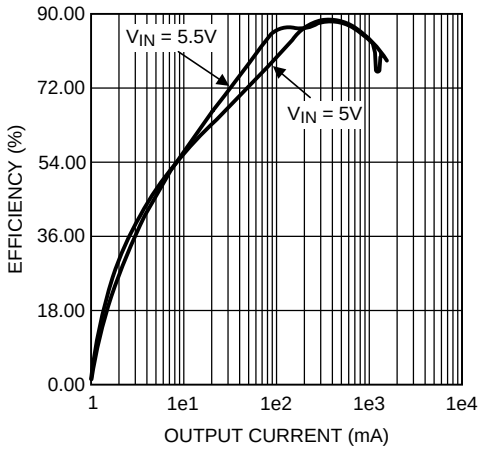
V_{IN} = 3 V, 3.5 V V_{OUT} = 1.4 V

Figure 6. Buck1 Efficiency



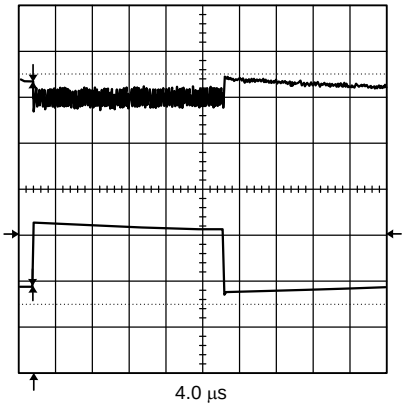
V_{IN} = 4 V to 4.5 V V_{OUT} = 1.4 V

Figure 7. Buck1 Efficiency



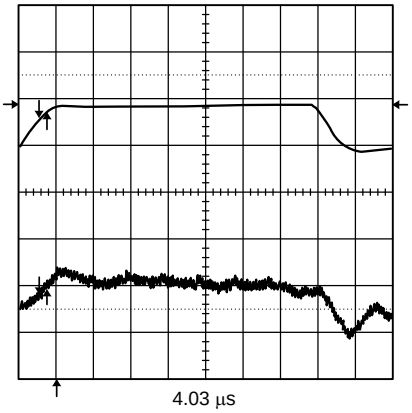
V_{IN} = 3 V, 3.5 V V_{OUT} = 1.4 V

Figure 8. Buck1 Efficiency



V_{IN} = 4.1 V V_{OUT} = 1.4 V (PFM to PWM)

Figure 9. Mode Change Load Transients 20 mA To 560 mA



V_{IN} = 4.1 V V_{OUT} = 1.4 V 980 mA [Channel 2]

Figure 10. Start-up into PWM Mode

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8 Detailed Description

8.1 Overview

The LP3972 includes three high-efficiency step-down DC-DC switching buck converters. Using a voltage mode architecture with synchronous rectification, the buck converters have the ability to deliver up to 1600 mA depending on the input voltage, output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required: PWM, PFM, and shutdown. The device operates in PWM mode at load currents of approximately 100 mA or higher, having voltage tolerance of ±3% with 95% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption. Shutdown mode turns off the device, offering the lowest current consumption ($I_{Q,\ SHUTDOWN}$ = 0.01 µA typical).

Additional features include soft-start, undervoltage protection, current-overload protection, and thermal-shutdown protection.

The part uses an internal reference voltage of 0.5 V. TI recommends that the device be kept in shutdown until the input voltage is 2.7 V or higher.

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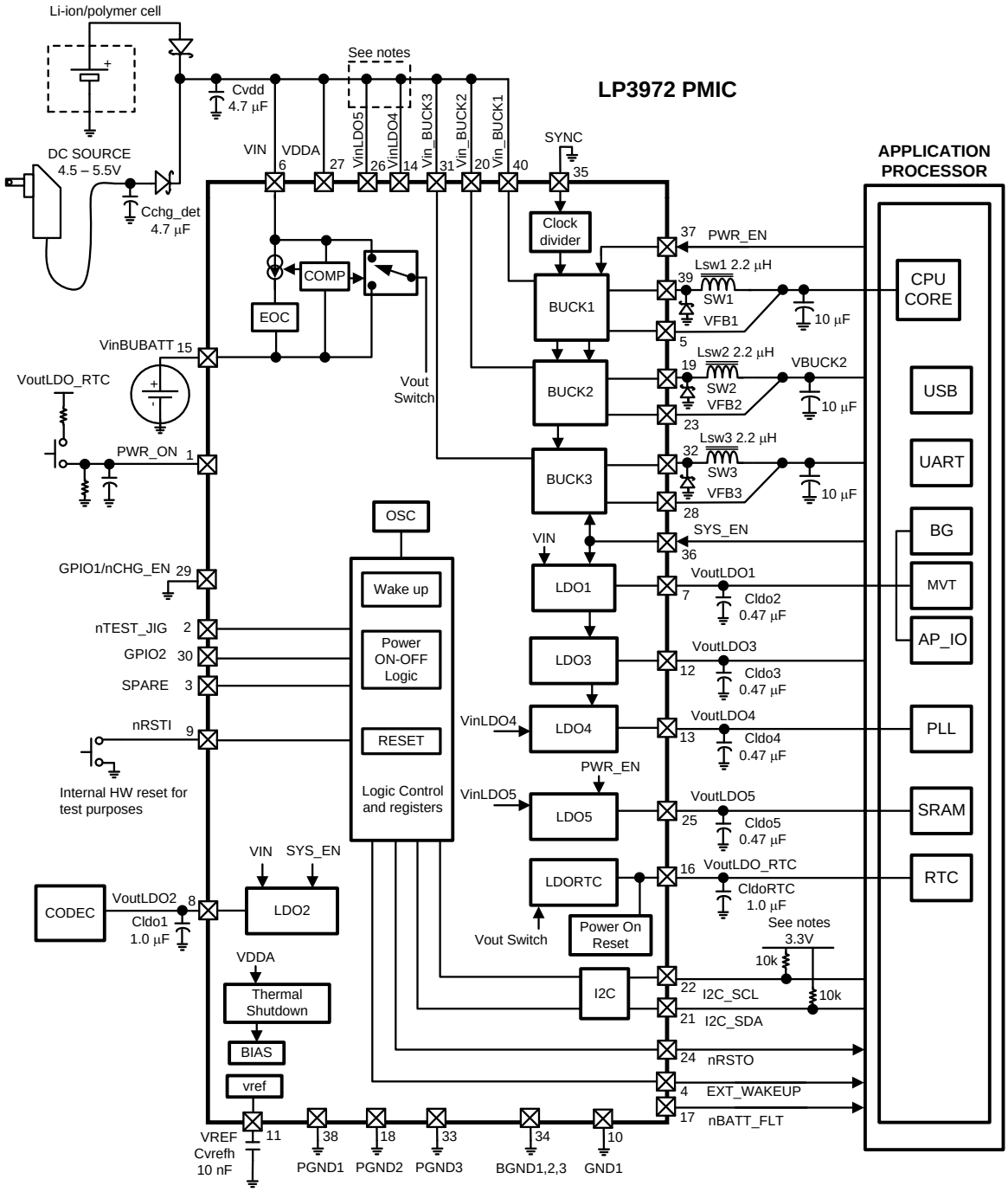
8.2 Functional Block Diagram



- The I^2C lines are pulled up via a I/O source.
- VINLDOs 4, 5 can either be powered from main battery source or by a buck regulator or V_{IN}.

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8.3 Feature Description

8.3.1 Buck Converter Operation

8.3.1.1 Circuit Operation

The buck converter operates as follows: during the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN} – V_{OUT})/L, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of –V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

8.3.1.2 PWM Operation

During pulse width modulation (PWM) operation the converter operates as a voltage mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

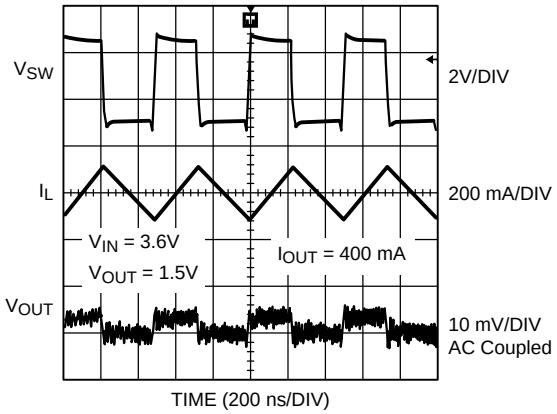

Figure 11. Typical PWM Operation

8.3.1.2.1 Internal Synchronous Rectification

While in PWM mode, the converters uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

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Feature Description (continued)

8.3.1.2.2 Current Limiting

A current limit feature allows the converters to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 2 A (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

8.3.1.3 PFM Operation

At very light loads, the converter enters pulse frequency modulation (PFM) mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous.
2. The peak PMOS switch current drops below the I_{MODE} level (typically I_{MODE} < 30 mA + V_{IN}/42 Ω).

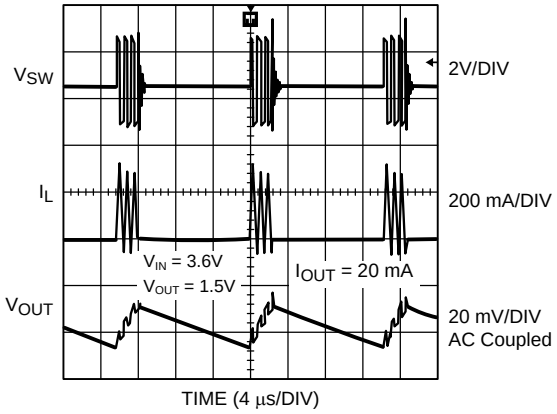

Figure 12. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between < 0.6% and <1.7% above the nominal PWM output voltage. If the output voltage is below the high PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the *high* PFM threshold or the peak current exceeds the IPFM level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + V_{IN}/27 Ω. Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the high PFM comparator threshold (see Figure 13), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this *sleep* mode is 21 µA (typical), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the low PFM threshold, the cycle repeats to restore the output voltage (average voltage in PFM mode) to < 1.15% above the nominal PWM output voltage. If the load current increases during PFM mode (see Figure 13) causing the output voltage to fall below the low2 PFM threshold, the device automatically transitions into fixed-frequency PWM mode. Typically when V_{IN} = 3.6 V the device transitions from PWM-to-PFM mode at 100-mA output current.

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Feature Description (continued)

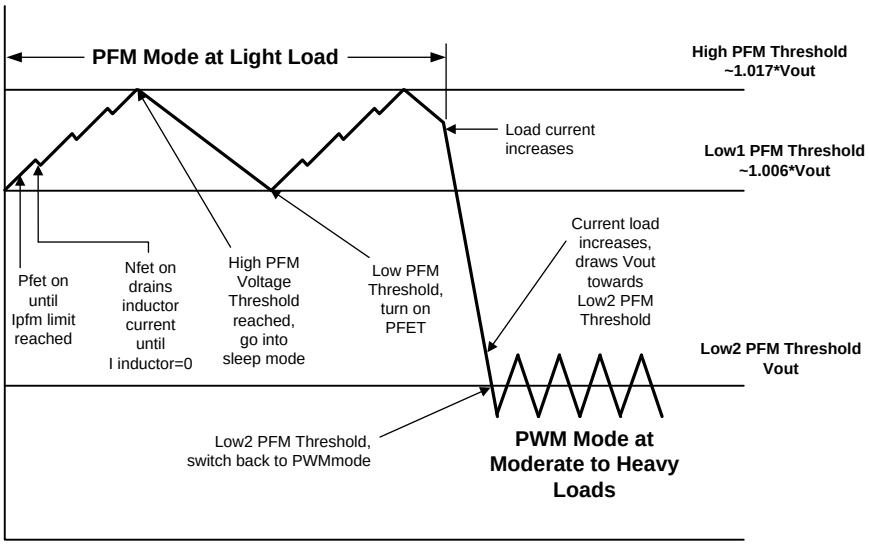

Figure 13. Operation in PFM Mode and Transfer to PWM Mode

8.3.1.4 Soft Start

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7 V. Soft start is implemented by increasing switch current limit in steps of 213 mA, 425 mA, 850 mA and 1700 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up time with a 10-µF output capacitor and 1000-mA load current is 390 µs and with a 1-mA load current, it is 295 µs.

8.3.1.5 Low Dropout (LDO) Operation

The LP3972 can operate at 100% duty cycle (no switching; PMOS switch completely on) for LDO support of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} \times (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT} \quad (1)$$

where

- I_{LOAD} = Load Current
- $R_{DSON,\ PFET}$ = drain-to-source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ = Inductor resistance

8.3.1.6 Spread-Spectrum Feature

Periodic switching in the buck regulator is inherently a noisier function block compared to an LDO. It can be challenging in some critical applications to comply with stringent regulatory standards or simply to minimize interference to sensitive circuits in space limited portable systems. The regulator's switching frequency and harmonics can cause *noise* in the signal spectrum. The magnitude of this noise is measured by its power spectral density. The power spectral density of the switching frequency, F_C, is one parameter that system designers want to be as low as practical to reduce interference to the environment and subsystems within their products. The LP3972 has a user selectable function on chip, wherein a noise reduction technique known as *spread spectrum* can be employed to ease customer's design and production issues.

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Feature Description (continued)

The principle behind spread spectrum is to modulate the switching frequency slightly and slowly, and spread the signal frequency over a broader bandwidth. Thus, its power spectral density becomes attenuated, and the associated interference electro-magnetic energy is reduced. The clock used to modulate the LP3972 buck regulator can be used as a spread spectrum clock via 2 I^2C control register (System Control Register 1 (SCR1) 8h'80) bits bk_ssen, and slomod. With this feature enabled, the intense energy of the clock frequency can be spread across a small band of frequencies in the neighborhood of the center frequency. *This results in a reduction of the peak energy.*

The LP3972 spread-spectrum clock uses a triangular modulation profile with equal rise and fall slopes. The modulation has the following characteristics:

- The center frequency: f_C = 2 MHz, and
- The modulating frequency, f_M = 6.8 kHz or 12 kHz.
- Peak frequency deviation: Δ_f = ±100 kHz (or ±5%)
- Modulation index $\beta = \Delta_f/f_M$ = 14.7 or 8.3

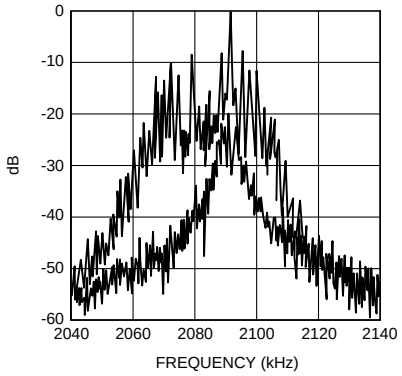

Figure 14. Switching Energy RBW = 300 Hz

8.3.2 LP3972 Battery Switch Operation

The LP3972 has provisions for two battery connections, the main battery V_{BAT} and the backup battery.

The function of the battery switch is to connect power to the LDO_RTC from the appropriate battery, depending on conditions described as follows:

- If only the backup battery is applied, the switch automatically connect sthe LDO_RTC power to this battery.
- If only the main battery is applied, the switch automatically connects the LDO_RTC power to this battery
- If both batteries are applied, and the main battery is sufficiently charged (V_{BAT} > 3.1 V), the switch automatically connects the LDO_RTC power to the main battery.
- As the main battery is discharged a separate circuit called nBATT_FLT warns the system. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch disconnects the input of the LDO_RTC from the main battery and connect to the backup battery.
- The main battery voltage at which the LDO_RTC is switched over from main to backup battery is 2.8 V typically.
- There is a hysteric voltage in this switch operation, thus the LDO_RTC is not reconnected to main battery until main battery voltage is greater than 3.1 V typically.
- The system designer may wish to disable the battery switch when only a main battery is used. This is accomplished by setting the *no backup battery bit* in the control register 8h'0B bit 7 NBUB. With this bit set to 1, the switching does not occur; that is, the LDO_RTC remains connected to the main battery even as it is discharged below the 2.9-V threshold. The backup battery input must also be connected to main battery.

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8.4 Device Functional Modes

8.4.1 Start-Up Mode

Start-up mode is entered once the battery backup supply is connected to LP3972. The RTC LDO is then turned on to power the VCC_BATT pin of the application processor. Start-up state exits once nRSTO de-asserts (after a minimum of 50 ms) and when nBATT_FLT de-asserts once system power is available.

8.4.2 Shutdown Mode

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch opens in shutdown to discharge the output. When the converter is enabled, EN, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.7V.

8.4.3 Standby Mode

Once NRSTO and nBATT_FLT are de-asserted the LP3972 waits for SYS_EN signal in standby mode. All high-voltage power domains are still disabled in this state.

8.4.4 Active Mode

Once SYS_EN goes high the device begins turning on the high-voltage power supplies. Once PWR_EN goes high the LP3972 enables the low-voltage power supplies. The Apps processor must monitor the “Power OK” status bits before beginning execution of code to make sure all supplies have been properly enabled.

8.5 Programming

8.5.1 LP3972 Reset Sequence

8.5.1.1 LP3972 Controls

8.5.1.1.1 Digital Interface Control Signals

SIGNAL	DEFINITION	ACTIVE STATE	SIGNAL DIRECTION
SYS_EN	High Voltage Power Enable	High	Input
PWR_EN	Low Voltage Power Enable	High	Input
SCL	Serial Bus Clock Line	Clock	Input
SDA	Serial Bus Data Line		Bidirectional
nRSTI	Forces an unconditional hardware reset	Low	Input
nRSTO	Forces an unconditional hardware reset	Low	Output
nBATT_FLT	Main Battery removed or discharged indicator	Low	Output
PWR_ON	Wake-up Input to CPU	High	Input
nTEST_JIG	Wake-up Input to CPU	Low	Input
SPARE	Wake-up Input to CPU	High/Low	Input
EXT_WAKEUP	Wake-up Output for application processor	High	Output
GPIO1 / nCHG_EN	General Purpose I/O /External backup Battery Charger enable	—	Bidirectional /Input
GPIO2	General Purpose I/O	—	Bidirectional

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8.5.1.1.2 Power Domain Enables

Table 3. Hardware and Software Enable Options for Each Supply

PMU OUTPUT	HW ENABLE	SW ENABLE
LDO_RTC	—	—
LDO1 (V_{CC_MVT})	SYS_EN	LDO1_EN
LDO2	SYS_EN	LDO2_EN
LDO3	SYS_EN	LDO3_EN
LDO4	SYS_EN	LDO4_EN
LDO5 (V_{CC_SRAM})	PWR_EN	S_EN
Buck1 (V_{CC_APPS})	PWR_EN	A_EN
BUCK2	SYS_EN	B2_EN
BUCK3	SYS_EN	B3_EN

8.5.1.1.3 Power Domains Sequencing (Delay)

By default SYS_EN must be on to have PWR_EN enable but this feature can be switched off by register bit BP_SYS.

By default always enables SYS_EN LDO1 and, after a typical 1-ms delay, others. Also when SYS_EN is set off the LDO1 goes off last. This function can be switched off or delay can be changed by DELAY bits via serial interface as seen in Table 4.

8h'80 Bit 5:4

Table 4. Programmable Supply Delay Options

DELAY (bits)	DELAY (ms)
00	0
01	0.5
10	1
11	1.5

8.5.1.1.4 Power Supply Enable

SYS_EN and PWR_EN can be changed by programmable register bits.

8.5.1.1.5 Wake-up Functionality (PWR_ON, NTEST_JIG, SPARE and EXT_WAKEUP)

Three input pins can be used to assert wake-up output for 10 ms for application processor notification to wake up. SPARE Input can be programmed through I^2C-compatible interface to be active low or high (SPARE bit, Default is active low 1). A reason for a wake-up event can be read through I^2C-compatible interface also. Additionally, wake-up inputs have 30 ms de-bounce filtering, and PWR_ON distinguishes between short and long (~1 s) pulses (push-button input). The LP3972 also has an internal thermal shutdown early warning that generates a wake-up to the system also. This is generated usually at 125°C.

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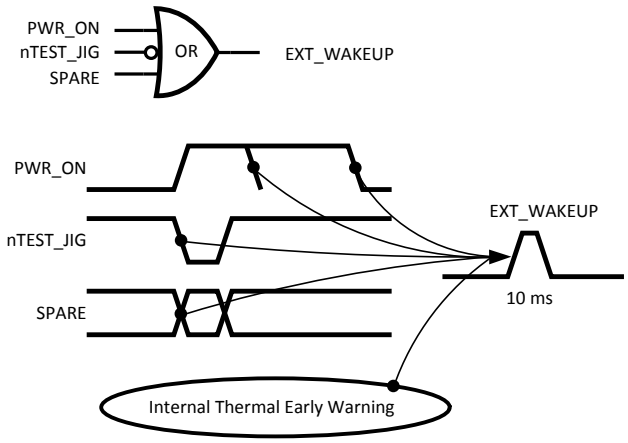

Figure 15. Wake-Up Functionality

Table 5. Wake-Up Functions

WAKE-UP REGISTER BITS	REASON FOR WAKE-UP
WUP0	SPARE
WUP1	TEST_JIG
WUP2	PWR_ON short pulse
WUP3	PWR_ON long pulse
TSD_EW	TSD Early Warning

8.5.1.1.6 Internal Thermal Shutdown Procedure

Thermal shutdown is build to generate early warning (typically 125°C) which triggers the EXT_WAKEUP for the processor acknowledge. When a thermal shutdown triggers (typical 160°C) the PMU resets the system until the device cools down.

8.5.1.1.7 Battery Switch and Backup Battery Charger

When backup battery is connected but the main battery has been removed or its supply voltage too low, the LP3972 uses the backup battery for generating LDO_RTC voltage. When Main Battery is available the battery FET switches over to the main battery for LDO_RTC voltage. When the main battery voltage is too low or removed nBATT_FLT is asserted. If no backup battery exists, the battery switch to backup can be switched off by nBU_BAT_EN bit. User can set the battery fault determination voltage and battery charger current via I^2C-compatible interface. Enabling of backup battery charger can be done via serial interface (nBAT_CHG_EN) or external charger enable pin (nCHG_EN). The GPIO1/nCHG_EN pin is set as an external charger enable input by default.

8.5.1.1.8 General Purpose I/O Functionality (GPIO1 And GPIO2)

The LP3972 has 2 general purpose I/Os for system control. I^2C-compatible interface is used for setting any of the pins to input, output or hi-Z mode. Inputs value can be read via serial interface (GPIO1,2 bits). The GPIO1/nCHG_EN pin functionality needs to be set to GPIO by serial interface register bit nEXTCHGEN (GPIO/CHG).

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Table 6. GPIO1 Configuration Options

CONTROLS				PORT FUNCTION	reg	batmonchg
GPIO<1>	GPIO<1>	Nextchgen_sel	bucen	GPIO1	Gpin 1	Function
X	X	1	0	Input = 0	0	Enabled
X	X	1	0	Input = 1	0	Not enabled
1	0	1	X	X	0	
X	X	X	1	X		Enabled
0	0	0	X	HiZ		
1	0	0	X	Input (dig)->	Input	
0	1	0	X	Output = 0	0	
1	1	0	X	Output = 1	0	

Table 7. GPIO2 Configuration Options

GPIO<1>	GPIO<1>	GPIO_tstiob	GPIO2	gpin2
0	0	1	HiZ	0
1	0	1	Input (dig)->	input
0	1	1	Output = 0	0
1	1	1	Output = 1	0

The LP3972 has provision for two battery connections, the main battery V_{BAT} and backup battery (see Figure 27).

The function of the battery switch is to connect power to the LDO_RTC from the appropriate battery, depending on conditions described as follows:

- If only the backup battery is applied, the switch automatically connects the LDO_RTC power to this battery.
- If only the main battery is applied, the switch automatically connects the LDO_RTC power to this battery.
- If both batteries are applied, and the main battery is sufficiently charged (V_{BAT} > 3.1 V), the switch automatically connects the RTC LDO power to the main battery.
- As the main battery is discharged by use, the user is warned by a separate circuit called nBATT_FLT. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch protects the LDO_RTC by disconnecting from the main battery and connecting to the backup battery.
  - The main battery voltage at which the LDO_RTC is switched from main to backup battery is 2.9 V typically.
  - There is a hysteresis voltage in this switch operation so, the LDO_RTC is not reconnected to main battery until main battery voltage is greater than 3.1 V typically.
- Additionally, the user may wish to disable the battery switch, such as, in the case when only a main battery is used. This is accomplished by setting the *no backup battery bit* in the control register 8h'89 bit 7 NBUB. With this bit set to 1, the switching does not occur; that is, the LDO_RTC remains connected to the main battery even as it is discharged below the 2.9-V threshold.

8.5.1.1.9 Regulated Voltages OK

All the power domains have own register bit (X_OK) that processor can read via serial interface to be sure that enabled powers are OK (regulating). Note that these read only bits are only valid when regulators are settled (avoid reading these bits during voltage change or power up).

8.5.1.1.10 Thermal Management

There is a mode wherein all 6 comparators (flags) can be turned on via the *enallflags* control register bit. This mode allows the user to interrogate the device or system temperature under the set operating conditions. Thus, the rate of temperature change can also be estimated. The system may then negotiate for speed and power trade off, or deploy cooling maneuvers to optimize system performance. The *enallflags* bit needs enabled only when the bct<2:0> bits are read to conserve power.

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NOTE

The thermal management flags have been verified functional. Presently these registers are accessible by factory only. If there is a demand for this function, the relevant register controls may be shifted into the user programmable bank; the temperature range and resolution of these flags, might also be refined or redefined.

8.5.1.1.11 Thermal Warning

Two of six low-power comparators, each consuming less than 1 µA, are always enabled to operate the *T = 125°C warning flag* with hysteresis. This allows continuous monitoring of a thermal-warning flag feature with very low power consumption.

8.5.1.1.12 LP3972 Thermal Flags Functional Diagram, Data from Initial Silicon

Figure 16 shows extra features from the thermal shutdown circuit:

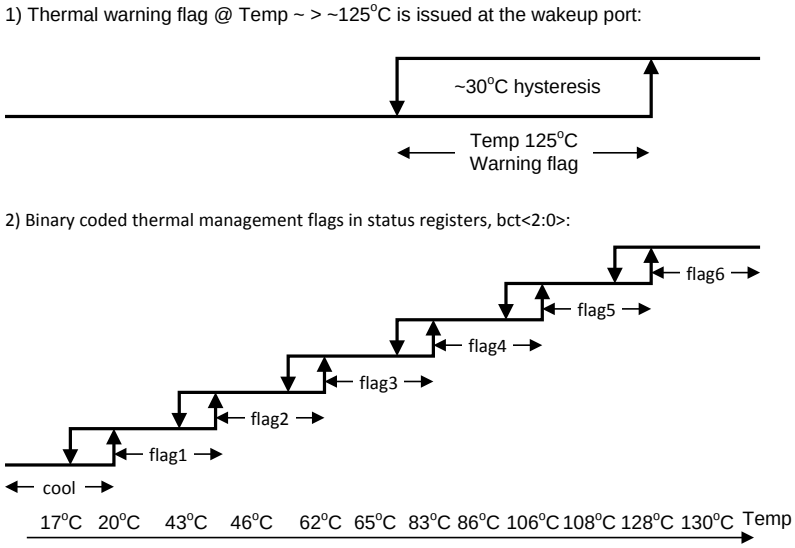

Figure 16. Thermal Shutdown Circuit Features

8.5.1.2 Initial Cold Start Power-On Sequence

1. The backup battery is connected to the PMU, power is applied to the backup battery pin, the LDO_RTC turns on and supplies a stable output voltage to the V_{CC}_BATT pin of the Applications processor (initiating the power-on reset event) with nRSTO asserted from the LP3972 to the processor.
2. nRSTO de-asserts after a minimum of 50 ms.
3. The applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is applied, the LP3972 de-asserts nBATT_FLT. Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other.
5. The Applications processor asserts SYS_EN, the LP3972 enables the system high-voltage power supplies. The applications processor starts its countdown timer set to 125 ms.
6. The LP3972 enables the high-voltage power supplies.
   – LDO1 power for V_{CC}_MVT (power for internal logic and I/O Blocks), BG (bandgap reference voltage), OSC13M (13-MHz oscillator voltage) and PLL enabled first, followed by others if delay is on.
7. Countdown timer expires; the applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 ms period.
8. The applications processor asserts PWR_EN (ext. pin or I^2C), the LP3972 enables the low-voltage regulators.

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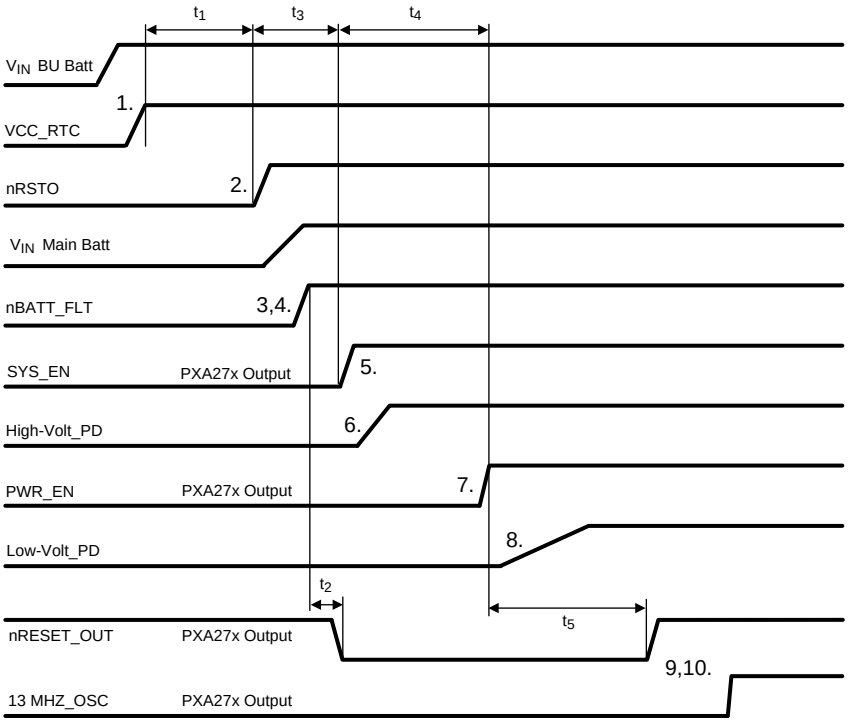
9. Countdown timer expires; if enabled power domains are OK (I^2C read) the power-up sequence continues by enabling the 13-MHz oscillator of the processor and PLLs.
10. The applications processor begins the execution of code.

See *Power-On Timing Delays* for more information.



* Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other and can occur is either order.

Figure 17. Cold Start Power-On Efficiency

8.5.1.3 Hardware Reset Sequence

Hardware reset initiates when the nRSTI signal is asserted (low). Upon assertion of nRST the processor enters hardware reset state. The LP3972 holds the nRST low long enough (50 ms typica) to allow the processor time to initiate the reset state.

8.5.1.4 Reset Sequence

1. nRSTI is asserted.
2. nRSTO is asserted and de-asserts after a minimum of 50 ms.
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is turned on, the LP3972 de-asserts nBATT_FLT.
5. The applications processor asserts SYS_EN, the LP3972 enables the system high-voltage power supplies. The applications processor starts its countdown timer set to 125 ms.
6. The LP3972 enables the high-voltage power supplies.
7. Countdown timer expires; the applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 ms.
8. The applications processor asserts PWR_EN, the LP3972 enables the low-voltage regulators.
9. Countdown timer expires; if enabled power domains are OK (I^2C read) the power-up sequence continues by enabling the 13-MHz oscillator of the processor and PLLs.
10. The applications processor begins the execution of code.

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8.5.2 I²C Compatible Interface

8.5.2.1 I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

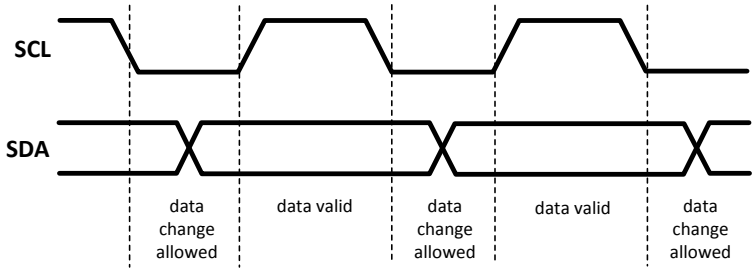

Figure 18. Data Validity

8.5.2.2 I²C Start And Stop Conditions

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

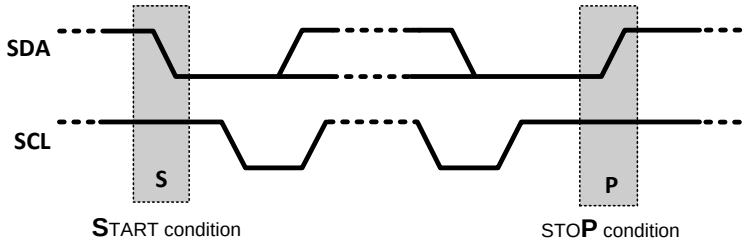

Figure 19. Stop and Start Conditions

8.5.2.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3972 address is 34h. For the eighth bit, a 0 indicates a WRITE and a1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

8.5.2.4 I²C Chip Address - 7h'34

Table 8. I²C Slave Address

MSB							
ADR6 Bit7	ADR5 Bit6	ADR4 Bit5	ADR3 Bit4	ADR2 Bit3	ADR1 Bit2	ADR0 Bit1	**R/W** Bit0
0	1	1	0	1	0	0	**R/W**

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8.5.2.4.1 Write Cycle

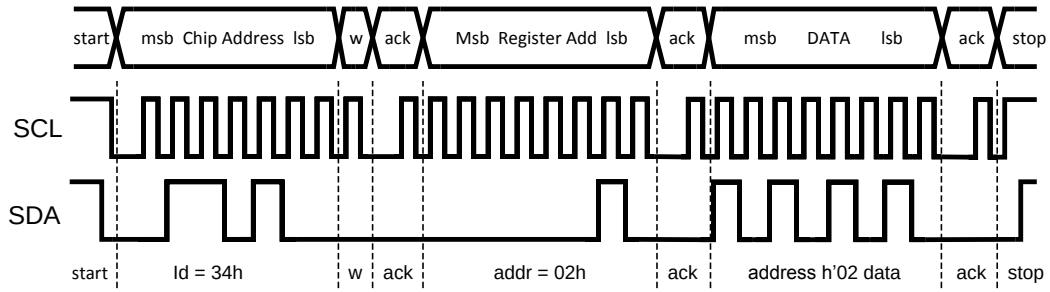
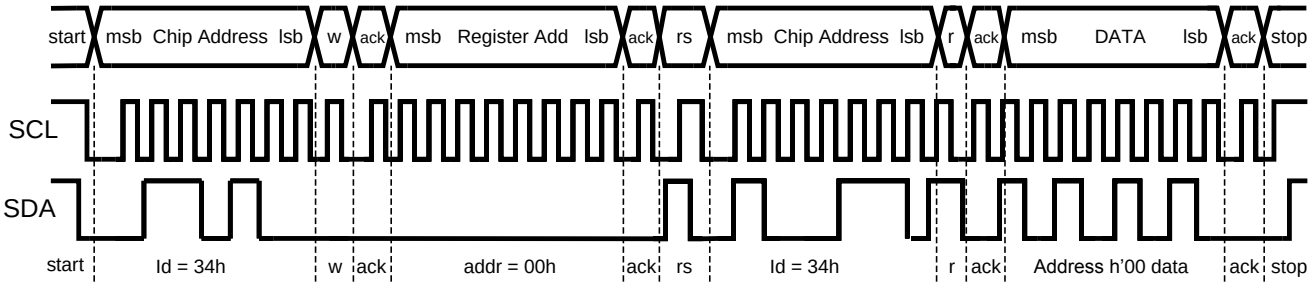


Figure 20. Write Cycle

8.5.2.4.2 Read Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function as follows.



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 34h (Chip Address)

Figure 21. Read Cycle

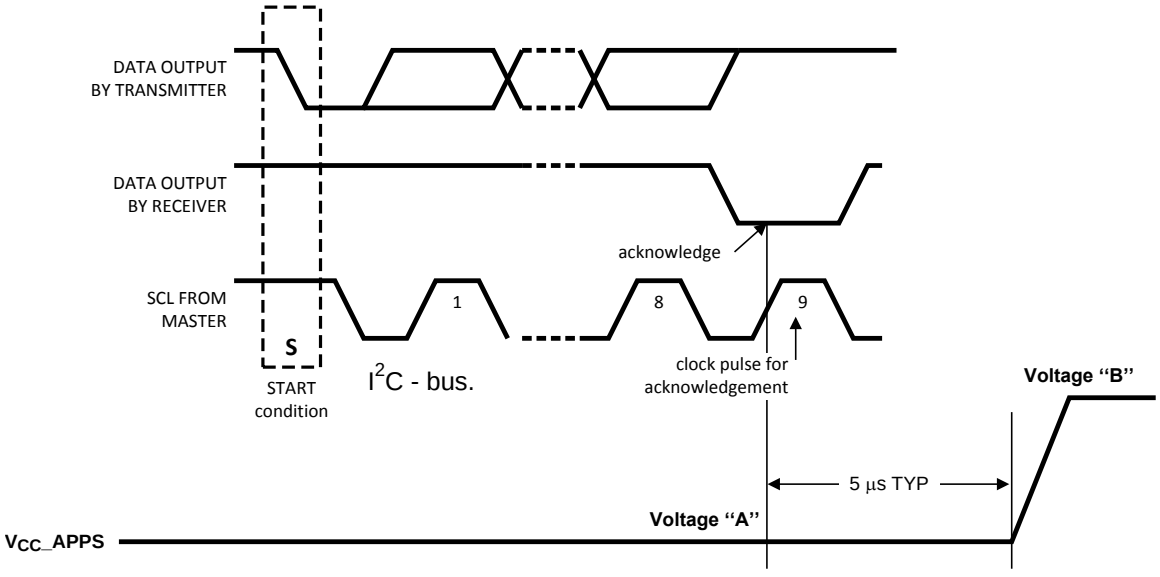


Figure 22. I^2C DVM Timing For V_{CC_APPS} (Buck1)

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8.5.2.5 Multi-Byte I²C Command Sequence

To correctly function with the Monahan's Power Management I²C the I²C serial interface of the device supports random register multi-byte command sequencing: During a multi-byte write the Master sends the start command followed by the device address, which is sent only once, followed by the 8-bit register address, then 8 bits of data. The I²C slave must then accept the next random register address followed by 8 bits of data and continue this process until the master sends a valid stop condition.

A typical multi-byte random register transfer is outlined in the following:

Device Address	Register A Address, Ach, Register A Data, Ach Register M Address, Ach, Register M Data, Ach Register X Address, Ach, Register X Data, Ach Register Z Address, Ach, Register Z Data, Ach, Stop

NOTE

The PMIC is not required to see the I²C device address for each transaction. A, M, X, and Z are Random numbers.

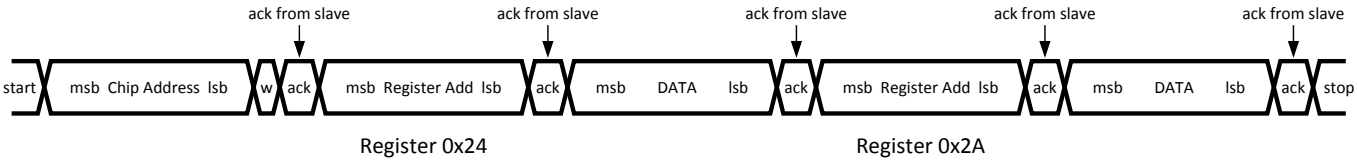

Figure 23. Multi-Byte I²C Command

8.5.2.6 Incremental Register I²C Command Sequence

The LP3972 supports address increment (burst mode). When there is a defined register address n data bytes can be sent, and the register address is incremented after each data byte has been sent. Address incrimination may be required for non XScale applications. User can define whether multi-byte (default) to random address or address incrimination will be used.

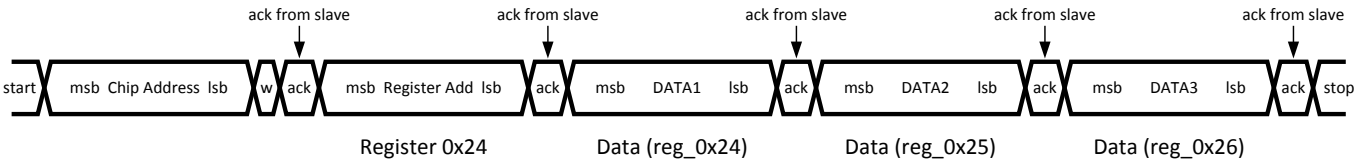

Figure 24. Incremental Register I²C Command

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8.6 Register Maps

Table 9. LP3972 Control Register

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
8h'07	SCR	R/W	System Control Register
8h'10	OVER1	R/W	Output Voltage Enable Register 1
8h'11	OVSR1	R	Output Voltage Status Register 1
8h'12	OVER2	R/W	Output Voltage Enable Register 2
8h'13	OVSR2	R	Output Voltage Status Register 2
8h'20	$V_{CC}1$	R/W	Voltage Change Control Register 1
8h'23	ADTV1	R/W	Buck1 Target Voltage 1 Register
8h'24	ADTV2	R/W	Buck1 DVM Target Voltage 2 Register
8h'25	AVRC	R/W	V_{CC_APPS} Voltage Ramp Control
8h'26	CDTC1	W	Dummy Register
8h'27	CDTC2	W	Dummy Register
8h'29	SDTV1	R/W	LDO5 Target Voltage 1
8h'2A	SDTV2	R/W	LDO5 Target Voltage 2
8h'32	MDTV1	R/W	LDO1 Target Voltage 1 Register
8h'33	MDTV2	R/W	LDO1 Voltage 2 Register
8h'39	L2VCR	R/W	LDO2 Voltage Control Registers
8h'3A	L34VCR	R/W	LDO3 & LDO4 Voltage Control Registers
8h'80	SCR1	R/W	System Control Register 1
8h'81	SCR2	R/W	System Control Register 2
8h'82	OEN3	R/W	Output Voltage Enable Register 3
8h'83	OSR3	R/W	Output Voltage Status Register 3
8h'84	LOER4	R/W	Output Voltage Enable Register 3
8h'85	B2TV	R/W	V_{CC_Buck2} Target Voltage
8h'86	B3TV	R/W	V_{CC_Buck3} Target Voltage
8h'87	B32RC	R/W	Buck 3:2 Voltage Ramp Control
8h'88	ISRA	R	Interrupt Status Register A
8h'89	BCCR	R/W	Backup Battery Charger Control Register
8h'8E	II1RR	R	Internal 1 Revision Register
8h'8F	II2RR	R	Internal 2 Revision Register

8.6.1 Serial Interface Register Selection Codes

8.6.1.1 System Control Status Register

Register is an 8-bit register which specifies the control bits for the PMIC clocks. This register works in conjunction with the SYNC pin where an external clock PLL buffer operating at 13 MHz is synchronized with the oscillators of the buck converters.

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8.6.1.1.1 System Control Register (SCR) 8h'07

Bit	7	6	5	4	3	2	1	0
Designation	Reserved							CLK_SCL
Reset Value	0	0	0	0	0	0	0	0

8.6.1.1.2 System Control Register (SCR) 8h'07 Definitions

Bit	Access	Name	Description
7-1	—	—	Reserved
0	R/W	CLK_SCL	External Clock Select 0 = Internal oscillator clock for buck converters 1 = External 13-MHz oscillator clock for buck converters

8.6.1.2 Output Voltage Enable Register 1

This register enables or disables the low voltage supplies LDO1 and Buck1. See details below.

8.6.1.2.1 Output Voltage Enable Register 1 (OVER1) 8h'10

Bit	7	6	5	4	3	2	1	0
Designation	Reserved					S_EN	Reserved	A_EN
Reset Value	0	0	0	0	0	1	0	1

8.6.1.2.2 Output Voltage Enable Register 1 (OVER1) 8h'10 Definitions

Bit	Access	Name	Description
7-3	—	—	Reserved
2	R/W	S_EN	V_{CC_SRAM} (LDO5) Supply Output Enabled 0 = V_{CC_SRAM} (LDO5) Supply Output Disabled 1 = V_{CC_SRAM} (LDO5) Supply Output Enabled
1	—	—	Reserved
0	R/W	A_EN	V_{CC_APPS} (Buck1) Supply Output Enabled 0 = V_{CC_APPS} (Buck1) Supply Output Disabled 1 = $V_{CC_APPS_}$ (Buck1) Supply Output Enabled

8.6.1.3 Output Voltage Status Register

This 8-bit register is used to indicate the status of the low-voltage supplies. By polling each of the specify supplies is within its specified operating range.

8.6.1.3.1 Output Voltage Status Register 1 (OVSR1) 8h'11

Bit	7	6	5	4	3	2	1	0
Designation	LP_OK	Reserved				S_OK	Reserved	A_OK
Reset Value	0	0	0	0	0	0	0	0

8.6.1.3.2 Output Voltage Status Register 1 (OVSR1) 8h'11 Definitions

Bit	Access	Name	Description
7	R	LP_OK	Low Voltage Supply Output Voltage Status 0 - V_{CC_APPS} (Buck1) and $V_{CC_}$SRAM (LDO5) output voltage < 90% of selected value 1 - V_{CC_APPS} (Buck1) and $V_{CC_}$SRAM (LDO5) output voltage > 90% of selected value
6:3	—	—	Reserved
2	R	S_OK	$V_{CC\text{-}SRAM}$ Supply Output Voltage Status 0 - V_{CC_SRAM} (LDO5) output voltage < 90% of selected value 1 - $V_{CC_}$SRAM (LDO5) output voltage > 90% of selected value

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Bit	Access	Name	Description
1	—	—	Reserved
0	R	A_OK	V_{CC_APPS} Supply output Voltage Status 0 - V_{CC_APPS} (Buck1) output voltage < 90% of selected value 1 - V_{CC_APPS} (Buck1) output voltage > 90% of selected value

8.6.1.4 Output Voltage Enable Register 2

This 8 bit output register enables and disables the output voltages on the LDOs 2,3,4 supplies.

8.6.1.4.1 Output Voltage Enable Register 2 (OVER2) 8h'12

Bit	7	6	5	4(1)	3(1)	2(1)	1	0
Designation	Reserved			LDO4_EN	LDO3_EN	LDO2_EN	Reserved	
Reset Value	0	0	0	0	0	0	0	0

(1) One-time factory programmable EPROM registers for default values

8.6.1.4.2 Output Voltage Enable Register 2 (OVER2) 8h'12 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7	—	—	Reserved
6	—	—	Reserved
5	—	—	Reserved
4	R/W	LDO4_EN	LDO4 Output Voltage Enable 0 = LDO4 Supply Output Disabled, Default 1 = LDO4 Supply Output Enabled
3	R/W	LDO3_EN	LDO3 Output Voltage Enable 0 = LDO3 Supply Output Disabled, Default 1 = LDO3 Supply Output Enabled
2	R/W	LDO2_EN	LDO2 Output Voltage Enable 0 = LDO2 Supply Output Disabled, Default 1 = LDO2 Supply Output Enabled
1	—	—	Reserved
0	—	—	Reserved

8.6.1.5 Output Voltage Status Register 2

8.6.1.5.1 Output Voltage Status Register 2 (OVSR2) 8h'13

BIT	7	6	5	4	3	2	1	0
Designation	LDO_OK	N/A	N/A	LDO4_OK	LDO3_OK	LDO2_OK	N/A	N/A
Reset Value	0	0	0	0	0	0	0	0

8.6.1.5.2 Output Voltage Status Register 2 (OVSR2) 8h'13 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7	R	LDO_OK	LDOs 2-4 Supply Output Voltage Status 0 - (LDOs 2-4) output voltage < 90% of selected value 1 - (LDOs 2-4) output voltage > 90% of selected value
6	—	—	Reserved
5	—	—	Reserved
4	R	LDO4_OK	LDO4 Output Voltage Status 0 - (V_{CC_LDO4}) output voltage < 90% of selected value 1 - (V_{CC}_LDO4) output voltage > 90% of selected value
3	R	LDO3_OK	LDO3 Output Voltage Status 0 - (V_{CC_LDO3}) output voltage < 90% of selected value 1 - (V_{CC_LDO3}) output voltage > 90% of selected value

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BIT	ACCESS	NAME	DESCRIPTION
2	R	LDO2_OK	LDO2 Output Voltage Status 0 - (V_{CC_LDO2}) output voltage < 90% of selected value 1 - (V_{CC_LDO2}) output voltage > 90% of selected value
1	—	—	Reserved
0	—	—	Reserved

8.6.1.6 DVM Voltage Change Control Register 1

8.6.1.6.1 DVM Voltage Change Control Register 1 (V_{CC}1) 8h'20

BIT	7	6	5	4	3	2	1	0
Designation	MVS	MGO	SVS	SGO	Reserved		AVS	AGO
Reset Value	0	0	0	0	0	0	0	0

8.6.1.6.2 DVM Voltage Change Control Register 1 (V_{CC}1) 8h'20 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7	R/W	MVS	V_{CC_MVT} (LDO1) Voltage Select 0 - Change V_{CC_MVT} Output Voltage to MDVT1 1 - Change V_{CC_MVT} Output Voltage to MDVT2
6	R/W	MGO	Start V_{CC_MVT} (LDO1) Voltage Change 0 - Hold V_{CC_MVT} Output Voltage at current Level 1 - Ramp V_{CC_MVT} Output Voltage as selected by MVS
5	R/W	SVS	V_{CC_SRAM} (LDO5) Voltage Select 0 - Change V_{CC_SRAM} Output Voltage to SDTV1 1 - Change V_{CC_SRAM} Output Voltage to SDTV2
4	R/W	SGO	Start V_{CC_SRAM} (LDO5) Voltage Change 0 - Hold V_{CC_SRAM} Output Voltage at current Level 1 - Change V_{CC_SRAM} Output Voltage as selected by SVS
3:2	—	—	Reserved
1	R/W	AVS	V_{CC_APPS} (Buck1) Voltage Select 0 - Ramp V_{CC_APPS} Output Voltage to ADVT1 1 - Ramp V_{CC_APPS} Output Voltage to ADVT2
0	R/W	AGO	Start V_{CC_APPS}(Buck1) Voltage Change 0 - Hold V_{CC_APPS} Output Voltage at current Level 1 - Ramp V_{CC_APPS} Output Voltage as selected by AVS

8.6.1.7 Buck1 (V_{CC_APPS}) Voltage 1

8.6.1.7.1 Buck1 (V_{CC}_APPS) Target Voltage 1 Register (ADTV1) 8h'23

BIT	7	6	5	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	Reserved			Buck1 Output Voltage (B1OV1)				
Reset Value	0	0	0	0	1	0	1	1

(1) One-time factory programmable

8.6.1.7.2 Buck1 (V_{CC}_apps) Target Voltage 1 Register (ADTV1) 8h'23 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7:5	—	—	Reserved

BIT	ACCESS	NAME	DESCRIPTION			
4:0	R/W	B1OV1	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	0.725	5h'10	1.125
			5h'1	0.750	5h'11	1.150
			5h'2	0.775	5h'12	1.175
			5h'3	0.800	5h'13	1.200
			5h'4	0.825	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B (default)	1.400 (default)
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

8.6.1.8 Buck1 (V_{CC}_APPS) Target Voltage 2 Register

8.6.1.8.1 Buck1 (V_{CC}_APPS) Target Voltage 2 Register (ADTV2) 8h'24

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			Buck1 Output Voltage (B1OV2)				
Reset Value	0	0	0	0	1	0	1	1

8.6.1.8.2 Buck1 (V_{CC}_APPS) Target Voltage 2 Register (ADTV2) 8h'24 Definitions

BIT	ACCESS	NAME	DESCRIPTION			
7:5	—	—	Reserved			
4:0	R/W	B1OV2	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	0.725	5h'10	1.125
			5h'1	0.750	5h'11	1.150
			5h'2	0.775	5h'12	1.175
			5h'3	0.800	5h'13	1.200
			5h'4	0.825	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B	1.400
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

8.6.1.9 Buck1 (V_{CC}_APPS) Voltage Ramp Control Register

8.6.1.9.1 Buck1 (V_{CC}_APPS) Voltage Ramp Control Register (AVRC) 8h'25

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			Ramp Rate (B1RR)				
Reset Value	0	0	0	0	1	0	1	0

8.6.1.9.2 Buck1 (V_{CC}_APPS) Voltage Ramp Control Register (AVRC) 8h'25 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7:5	—	—	Reserved

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BIT	ACCESS	NAME	DESCRIPTION	
4:0	R/W	B1RR	DVM Ramp Speed	
			Data Code	**Ramp Rate (mV/us)**
			5h'0	Instant
			5h'1	1
			5h'2	2
			5h'3	3
			5h'4	4
			5h'5	5
			5h'6	6
			5h'7	7
			5h'8	8
			5h'9	9
			5h'A	10 (default)
			4h'B-4h'1F	Reserved

8.6.1.10 V_{CC}_comm Target Voltage 1 Dummy Register (CDTV1)

8.6.1.10.1 V_{CC}_comm Target Voltage 1 Dummy Register (CDTV1) 8h'26 Write Only(1)

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage				
Reset Value	0	0	0	0	0	0	0	0

(1) CDTV1 must be writable by an I^2C controller. This is a dummy register

8.6.1.11 V_{CC}_COMM Target Voltage 2 Dummy Register (CDTV2)

8.6.1.11.1 V_{CC}_COMM Target Voltage 2 Dummy Register (CDTV2) 8h'27 Write Only(1)

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage				
Reset Value	0	0	0	0	0	0	0	0

(1) CDTV2 must be writable by an I^2C controller. This is a dummy register and cannot be read.

This is a variable voltage supply to the internal SRAM of the application processor.

8.6.1.12 LDO5 (V_{CC}_SRAM) Target Voltage 1 Register

8.6.1.12.1 LDO5 (V_{CC}_SRAM) Target Voltage 1 Register (SDTV1) 8h'29

BIT	7	6	5	4(1)	3(1)	2(1)	1*(1)	0(1)
Designation	Reserved			LDO 5 Output Voltage (L5OV)				
Reset Value	0	0	0	0	1	0	1	1

(1) One-time factory programmable EPROM registers for default values

8.6.1.12.2 LDO5 (V_{CC}_SRAM) Target Voltage 1 Register (SDTV1) 8h'29 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7:5	—	—	Reserved

BIT	ACCESS	NAME	DESCRIPTION			
4:0	R/W	B1OV	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	—	5h'10	1.125
			5h'1	—	5h'11	1.150
			5h'2	—	5h'12	1.175
			5h'3	—	5h'13	1.200
			5h'4	—	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B (default)	1.400 (default)
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

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8.6.1.13 LDO5 (V_{CC}_SRAM) Target Voltage 2 Register

8.6.1.13.1 LDO5 (V_{CC}_SRAM) Target Voltage 2 Register (SDTV2) 8h'2A

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			LDO 5 Output Voltage (L5OV)				
Reset Value	0	0	0	0	1	0	1	1

8.6.1.13.2 LDO5 (V_{CC}_SRAM) Target Voltage 2 Register (SDTV2) 8h'2A Definitions

BIT	ACCESS	NAME	DESCRIPTION			
7:5	—	—	Reserved			
4:0	R/W	B1OV	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	—	5h'10	1.125
			5h'1	—	5h'11	1.150
			5h'2	—	5h'12	1.175
			5h'3	—	5h'13	1.200
			5h'4	—	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B	1.400
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

V_{CC_MVT} is low tolerance regulated power supply for the application processor ring oscillator and logic for communicating to the LP3972. V_{CC_MVT} is enabled when SYS_EN is asserted and disabled when SYS_EN is deasserted.

8.6.1.14 LDO1 (V_{CC_MVT}) Target Voltage 1 Register (MDTV1)

8.6.1.14.1 LDO1 (V_{CC_MVT}) Target Voltage 1 Register (MDTV1) 8h'32

BIT	7	6	5	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	Reserved			Output Voltage (OV)				
Reset Value	0	0	0	0	0	1	0	0

(1) One-time factory programmable EPROM registers for default values.

8.6.1.14.2 LDO1 (V_{CC_MVT}) Target Voltage 1 Register (MDTV1) 8h'32 Definitions

BIT	ACCESS	NAME	DESCRIPTION		
7:5	—	—	Reserved		
4:0	R/W	L1OV	**Data Code**	**Output Voltage**	Notes:
			5h'0	1.700	
			5h'1	1.725	
			5h'2	1.750	
			5h'3	1.775	
			5h'4 (default)	1.800 (default)	
			5h'5	1.825	
			5h'6	1.850	
			5h'7	1.875	
			5h'8	1.900	
			5h'9	1.925	
			5h'A	1.950	
			5h'B	1.975	
			5h'C	2.000	
			5h'D-5h'F	Reserved	

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8.6.1.15 LDO1 (V_{CC_MVT}) Target Voltage 2 Register

8.6.1.15.1 LDO1 (V_{CC_MVT}) Target Voltage 2 Register (MDTV2) 8h'33

BIT	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage (OV)				
Reset Value	0	0	0	0	1	0	1	1

8.6.1.15.2 LDO1 (V_{CC_MVT}) Target Voltage 2 Register (MDTV2) 8h'33 Definitions

BIT	ACCESS	NAME	DESCRIPTION		
7:5	—	—	Reserved		
4:0	R/W	L1OV	**Data Code** 5h'0 5h'1 5h'2 5h'3 5h'4 (default) 5h'5 5h'6 5h'7 5h'8 5h'9 5h'A 5h'B 5h'C 5h'D-5h'F	**Output Voltage** 1.700 1.725 1.750 1.775 1.800 (default) 1.825 1.850 1.875 1.900 1.925 1.950 1.975 2.000 Reserved	Notes:

8.6.1.16 LDO2 Voltage Control Register (L12VCR)

8.6.1.16.1 LDO2 Voltage Control Register (L12VCR) 8h'39

BIT	7(1)	6(1)	5(1)	4(1)	3	2	1	0
Designation	LDO2 Output Voltage (L2OV)				Reserved			
Reset Value	0	0	0	0	0	0	0	0

(1) One-time factory programmable EPROM registers for default values.

8.6.1.16.2 LDO2 Voltage Control Register (L12VCR) 8h'39 Definitions

BIT	ACCESS	NAME	DESCRIPTION	
7:4	R/W	L2OV	**Data Code** 4h'0 (default) 4h'1 4h'2 4h'3 4h'4 4h'5 4h'6 4h'7 4h'8 4h'9 4h'A 4h'B 4h'C 4h'D 4h'E 4h'F	**Output Voltage** 1.8 (Default) 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3
3:0	—	—	Reserved	

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8.6.1.17 LDO4 – LDO3 Voltage Control Register (L34VCR)

8.6.1.17.1 LDO4 – LDO3 Voltage Control Register (L34VCR) 8h'3A

BIT	7(1)	6(1)	5(1)	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	LDO4 Output Voltage (L4OV)				LDO3 Output Voltage (L3OV)			
Reset Value	0	0	0	0	0	0	0	0

(1) One-time factory programmable EPROM registers for default values.

8.6.1.17.2 LDO4 – LDO3 Voltage Control Register (L34VCR) 8h'3A Definitions

BIT	ACCESS	NAME	DESCRIPTION	
7:4	R/W	L4OV	**Data Code**	**Output Voltage**
			4h'0	1.00
			4h'1	1.05
			4h'2	1.10
			4h'3	1.15
			4h'4	1.20
			4h'5	1.25
			4h'6	1.30
			4h'7	1.35
			4h'8	1.40
			4h'9	1.50
			4h'A	1.80
			4h'B	1.90
			4h'C	2.50
			4h'D	2.80
			4h'E (default0	3.00 (default) (Default)
			4h'F	3.30
3:0	R/W	L3OV	**Data Code**	**Output Voltage**
			4h'0	1.8
			4h'1	1.9
			4h'2	2.0
			4h'3	2.1
			4h'4	2.2
			4h'5	2.3
			4h'6	2.4
			4h'7	2.5
			4h'8	2.6
			4h'9	2.7
			4h'A	2.8
			4h'B	2.9
			4h'C (default)	3.0 (Default)
			4h'D	3.1
			4h'E	3.2
			4h'F	3.3

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8.6.2 TI-Defined Control and Status Registers

8.6.2.1 System Control Register 1 (SCR1)

8.6.2.1.1 System Control Register 1 (SCR1) 8h'80

BIT	7 (1)	6 (1)	5 (1)	4	3	2	1	0
Designation	BPSEN	SENDL		FPWM3	FPWM2	FPWM1	BK_SLOMOD	BK_SSEN
Reset Value	0	1	0	0	0	0	0	0

(1) One-time factory programmable EPROM registers for default values.

8.6.2.1.2 System Control Register 1 (SCR1) 8h'80 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7	R/W	BPSEN	Bypass System enable safety Lock. Prevents activation of PWR_EN when SYS_EN is low. 0 = PWR_EN "AND" with SYS_EN signal, Default 1 = PWR_EN independent of SYS_EN
6:5	R/W	SENDL	Delay time for High Voltage Power Domains LDO2, LDO3, LDO4, Buck2, and Buck3 after activation of SYS_EN. V_{CC}_LDO1 has no delay. **Data Code** / **Delay (ms)** 2h'0 / 0.0 2h'1 / 0.5 **2h'2** / **1** (Default) 2h'3 / 1.4
4	R/W	FPWM3	Buck3 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only does not switch to PFM
3	R/W	FPWM2	Buck2 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only does not switch to PFM
2	R/W	FPWM1	Buck1 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only does not switch to PFM
1	R	BK_SLOMOD	Buck Spread Spectrum Modulation Bucks 1-3 0 = 10 kHz triangular wave spread spectrum modulation 1 = 2 kHz triangular wave spread spectrum modulation
0	R	BK_SSEN	Spread spectrum function Bucks 1-3 0 = SS Output Disabled 1 = SS Output Enabled

8.6.2.2 System Control Register 2 (SCR2)

8.6.2.2.1 System Control Register 2 (SCR2) 8h'81

BIT	7	6	5 (1)	4	3	2	1	0
Designation	BBCS	SHBU	BPTR	WUP3	GPIO2		GPIO1	
	1	0	1	1	0	0	1	0

(1) One time factory programmable EPROM registers for default values.

8.6.2.2.2 System Control Register 2 (SCR2) 8h'81 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7	R/W	BBCS	Sets GPIO1 as control input for backup battery charger 0 - Backup battery Charger GPIO Disabled 1 - Backup battery Charger GPIO Pin Enabled
6	R/W	SHBU	Shut down backup battery to prevent battery drain during shipping 0 = Backup Battery Enabled 1 = Backup battery Disabled

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BIT	ACCESS	NAME	DESCRIPTION
5	R/W	BPTR	Bypass LDO_RTC Output Voltage to LDO3 Output Voltage Tracking 0 - LDO_RTC3 Tracking enabled 1 - LDO_RTC3 Tracking disabled, Default
4	R/W	WUP3	Spare Wake-up control input 0 - Active High 1 - Active Low
3:2	R/W	GPIO2	Configure direction and output sense of GPIO2 Pin
			Data Code / **GPIO2** 2h'00 / Hi-Z 2h'01 / Output Low 2h'02 / Input 2h'03 / Output high
1:0	R/W	GPIO1	Configure direction and output sense of GPIO1 Pin
			Data Code / **GPIO1** 2h'00 / Hi-Z 2h'01 / Output Low 2h'02 / Input 2h'03 / Output high

8.6.2.3 Output Enable 3 Register (OEN3) 8h'82

BIT	7	6	5	4(1)	3	2(1)	1	0(1)
Designation	Reserved			B3EN	ENFLAG	B2EN	Reserved	L1EN
Reset Value	0	0	0	1	0	1	0	1

(1) One time factory programmable EPROM registers for default values.

8.6.2.4 Output Enable 3 Register (OEN3) 8h'82 Definitions

BIT	ACCESS	NAME	DESCRIPTION
7:5	—	—	Reserved
4	R/W	B3EN	V_{CC_Buck3} Supply Output Enabled 0 = V_{CC_Buck3} Supply Output Disabled 1 = $V_{CC_}$Buck3 Supply Output Enabled, Default
3	R/W	ENFLAG	Enable for Temperature Flags (BCT) 0 = Temperature Flag Disabled 1 = Temperature Flag Enabled
2	R/W	B2EN	V_{CC_Buck2} Supply Output Enabled 0 = V_{CC_Buck2} Supply Output Disabled 1 = V_{CC_Buck2} Supply Output Enabled, Default
1	—	—	Reserved
0	R/W	L1EN	LDO1 (MVT)Output Voltage Enable 0 = LDO1 Supply Output Disabled 1 = LDO1 Supply Output Enabled, Default

8.6.2.5 Status Register 3 (OSR3) 8h'83

BIT	7	6	5	4	3	2	1	0
Designation	BT_OK	B3_OK	B2_OK	LDO1_OK	Reserved	BCT2	BCT1	BCT0
Reset Value	0	0	0	0	0	0	0	0

8.6.2.6 Status Register 3 (OSR3) Definitions 8h'83

BIT	ACCESS	NAME	DESCRIPTION
7	R	BT_OK	Bucks 2-3 Supply Output Voltage Status 0 - (Bucks 1-3) output voltage < 90% Default value 1 - (Bucsk 1-3) output voltage > 90% Default value

BIT	ACCESS	NAME	DESCRIPTION
6	R	B3_OK	Buck3 Supply Output Voltage Status 0 - (Buck3) output voltage < 90% Default value 1 - (Buck3) output voltage > 90% Default value
5	R	B2_OK	Buck2 Supply Output Voltage Status 0 - (Buck2) output voltage < 90% Default value 1 - (Buck2) output voltage > 90% Default value
4	R	LDO1_OK	LDO1 Output Voltage Status 0 - (V_{CC}_LDO1) output voltage < 90% of selected value 1 - (V_{CC}_LDO1) output voltage > 90% of selected value
3	—	—	Reserved
2:0	R	BCT	Binary coded thermal management flag status register

Data Code	Temperature Ascending °C
000	40
001	60
010	80
011	100
100	120
101	140
110	160
111	Reserved

8.6.2.7 Logic Output Enable Register (LOER) 8h'84

BIT	7	6(1)	5(1)	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	Reserved	B3ENC	B2ENC	B1ENC	L5EC	L4EC	L3EC	L2EC
Reset Value	0	1	1	0	0	1	1	1

(1) One time factory programmable EPROM registers for default values.

8.6.2.8 Logic Output Enable Register (LOER) Definitions 8h'84

BIT	ACCESS	NAME	DESCRIPTION
7	—	—	Reserved
6	R/W	B3ENC	Connects Buck3 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck3 enable connected to PWR_EN 1 - Buck3 enable connected to SYS_EN, Default
5	R/W	B2ENC	Connects Buck2 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck2 enable connected to PWR_EN 1 - Buck2 enable connected to SYS_EN, Default
4	R/W	B1ENC	Connects Buck1 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck1 enable connected to PWR_EN, Default 1 - Buck1 enable connected to SYS_EN
3	R/W	L5EC	Connects LDO5 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO5 enable connected to PWR_EN, Default 1 - LDO5 enable connected to SYS_EN
2	R/W	L4EC	Connects LDO4 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO4 enable connected to PWR_EN 1 - LDO4 enable connected to SYS_EN, Default
1	R/W	L3EC	Connects LDO3 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO3 enable connected to PWR_EN 1 - LDO3 enable connected to SYS_EN, Default
0	R/W	L2EC	Connects LDO2 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO2 enable connected to PWR_EN 1 - LDO2 enable connected to SYS_EN, Default

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8.6.2.9 V_{CC}_BUCK2 Target Voltage Register (B2TV) 8h'85

Bit	7	6	5	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	Reserved			Buck2 Output Voltage (B2OV)				
Reset Value	0	0	0	1	1	0	0	1

(1) One time factory programmable EPROM registers for default values.

8.6.2.10 V_{CC}_BUCK2 Target Voltage Register (B2TV) 8h'85 Definitions

Bit	Access	Name	Description			
7:5	—		Reserved			
4:0	R/W	B2OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'10	1.55
			5h'05	1.00	5h'11	1.60
			5h'06	1.05	5h'12	1.65
			5h'07	1.10	5h'13	1.70
			5h'08	1.15	5h'14	1.80
			5h'09	1.20	5h'15	1.90
			5h'0A	1.25	5h'16	2.50
			5h'0B	1.30	5h'17	2.80
			5h'0C	1.35	5h'18	3.00
					5h'19 (default)	3.30 (default)

8.6.2.11 BUCK3 Target Voltage Register (B3TV) 8h'86

Bit	7	6	5	4(1)	3(1)	2(1)	1(1)	0(1)
Designation	Reserved			Buck3 Output Voltage (B3OV)				
Reset Value	0	0	0	1	0	1	0	0

(1) One time factory programmable EPROM registers for default values.

8.6.2.12 BUCK3 Target Voltage Register (B3TV) 8h'86 Definitions

Bit	Access	Name	Description				
7:5	—		Reserved				
4:0	R/W	B3OV	Output Voltage				
			Data Code	**(V)**	**Data Code**	**(V)**	
			5h'01	0.80	5h'0D	1.40	Default
			5h'02	0.85	5h'0E	1.45	
			5h'03	0.90	5h'0F	1.50	
			5h'04	0.95	5h'11	1.60	
			5h'05	1.00	5h'12	1.65	
			5h'06	1.05	5h'13	1.70	
			5h'07	1.10	5h'14 (default)	1.80 (default)	
			5h'08	1.15	5h'15	1.90	
			5h'09	1.20	5h'16	2.50	
			5h'0A	1.25	5h'17	2.80	
			5h'0B	1.30	5h'18	3.00	
			5h'0C	1.35	5h'19	3.30	

8.6.2.13 V_{CC}_BUCK3:2 Voltage Ramp Control Register (B32RC)

8.6.2.13.1 V_{cc}_BUCK3:2 Voltage Ramp Control Register (B32RC) 8h'87

Bit	7	6	5	4	3	2	1	0
Designation	Ramp Rate (B3RR)				Ramp Rate (B2RR)			
Reset Value	1	0	1	0	1	0	1	0

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8.6.2.13.2 Buck3:2 Voltage Ramp Control Register (B3RC) 8h'87 Definitions

Bit	Access	Name	Description	
7:4	R/W	B3RR	**Data Code** 4h'0 4h'1 4h'2 4h'3 4h'4 4h'5 4h'6 4h'7 4h'8 4h'9 **4h'A**	**Ramp Rate mV/µS** Instant 1 2 3 4 5 6 7 8 9 **10**
3:0	R/W	B2RR	**Data Code** 4h'0 4h'1 4h'2 4h'3 4h'4 4h'5 4h'6 4h'7 4h'8 4h'9 4h'A (default)	**Ramp Rate mV/µS** Instant 1 2 3 4 5 6 7 8 9 10 (default)

8.6.2.14 Interrupt Status Register ISRA

This register specifies the status bits for the interrupts generated by the LP3972 device.

8.6.2.14.1 Interrupt Status Register ISRA 8h'88

Bit	7	6	5	4	3	2	1	0
Designation	Reserved	T125	GPI2	GPI1	WUP3	WUP2	WUPT	WUPS
Reset Value	0	0	0	0	0	0	0	0

8.6.2.14.2 Interrupt Status Register ISRA 8h'88 Definitions

Bit	Access	Name	Description
7	—	—	Reserved
6	R	T125	Status bit for thermal warning PMIC T>125°C 0 = PMIC Temp. < 125°C 1 = PMIC Temp. > 125°C
5	R	GPI2	Status bit for the input read in from GPIO 2 when set as Input 0 = GPI2 Logic Low 1 = GPI2 Logic High
4	R	GPI1	Status bit for the input read in from GPIO 1 when set as Input 0 = GPI1 Logic Low 1 = GPI1 Logic High
3	R	WUP3	PWR_ON Pin long pulse wake-up status 0 = No wake-up event 1 = Long pulse wake-up event
2	R	WUP2	PWR_ON Pin Short pulse wake-up Status 0 = No wake-up event 1 = Short pulse wake-up event
1	R	WUPT	TEST_JIG Pin wake-up Status 0 = No wake-up event 1 = Wake-up event
0	R	WUPS	SPARE pin wake-up status 0 = No wake-up event 1 = Wake-up event

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8.6.2.15 Backup Battery Charger Control Register (BCCR)

This register specifies the status of the main battery supply (NBUB bit).

8.6.2.15.1 Backup Battery Charger Control Register (BCCR) 8h'89

Bit	7(1)	6	5(1)	4(1)	3(1)	2	1	0
Designation	NBUB	CNBFL	nBFLT			BUCEN	IBUC	
Reset Value	0	0	0	1	0	0	0	1

(1) One-time factory programmable EPROM registers for default values.

8.6.2.15.2 Backup Battery Charger Control Register (BCCR) 8h'89 Definitions

Bit	Access	Name	Description
7	R/W	NBUB	No backup battery default setting. Logic does not allow switch-over to backup battery. 0 = Backup Battery Enabled, Default 1 = Backup Battery Disabled
6	R/W	CNBFL	Control for nBATT_FLT output signal 0 = nBATT_FLT Enabled 1 = nBATT_FLT Disabled
5:3	R/W	BFLT	nBATT_FLT monitors the battery voltage and can be set to the Assert voltages listed below.

Data Code	Asserted	De-Asserted
3h'01	2.6	2.8
3h'02	2.8 (default)	3.0 (Default)
3h'03	3.0	3.2
3h'04	3.2	3.4
3h'05	3.4	3.6

Bit	Access	Name	Description
2	R/W	BUCEN	Enables backup battery charger 0 = Backup Battery Charger Disabled 1 = Backup Battery Charger Enabled
1:0	R/W	IBUC	Charger current setting for backup battery

Data Code	BU Charger I (µA)
2h'00	260
2h'01 (default)	190 (Default)
2h'02	325
2h'03	390

8.6.2.16 Marvell PXA Internal 1 Revision Register (II1RR) 8h'8E

Bit	7	6	5	4	3	2	1	0
Designation	II1RR							
Reset Value	0	0	0	0	0	0	0	0

8.6.2.17 Marvell PXA Internal 1 Revision Register (II1RR) (Ii1rr) 8h'8E Definitions

Bit	Access	Name	Description
7:0	R	II1RR	Intel internal usage register for revision information.

8.6.2.18 Marvell PXA Internal 2 Revision Register (II1RR) 8h'8F

Bit	7	6	5	4	3	2	1	0
Designation	II2RR							
Reset Value	0	0	0	0	0	0	0	0

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8.6.2.19 Marvell PXA Internal 2 Revision Register (II1RR) 8h'8F Definitions

Bit	Access	Name	Description
7:0	R	II2RR	Intel internal usage register for revision information.

8.6.2.20 Register Programming Examples

8.6.2.20.1 Example 1: Start-of-Day (SOD) Sequence

PMIC Register Address	PMIC Register Name	Register Data	Description
8h'23	ADTVI	00011011	Sets the SOD V_{CC_APPS} voltage
8h'29	SDTV1	00011011	Sets the SOD V_{CC_SRAM} voltage
8h'10	OVER1	00000111	Enables V_{CC_SRAM} and V_{CC_APPS} to their programmed values.

SODl multi-byte random register transfer is shown in Figure 25:

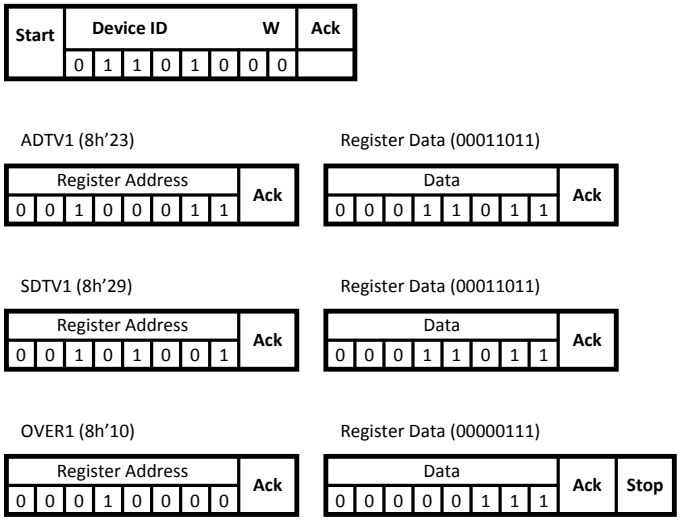

Figure 25. SOD Multi-Byte Random Register Transfer

Device Address	Register A Address, Ach, Register A Data, Ach Register M Address, Ach, Register M Data, Ach Register X Address, Ach, Register X Data, Ach Register Z Address, Ach, Register Z Data, Ach, Stop

8.6.2.20.2 Example 2: Voltage Change Sequence

PMIC Register Address	PMIC Register Name	Register Data	Description
8h'24	ADTV2	00010111	Sets the $V_{CCAPPS_}$ target voltage 2 to 1.3 V.
8h'2A	SDTV2	00001111	Sets the $V_{CC_}$SRAM target voltage 2 to 1.1 V.
8h'20	V_{CC}1	00110011	Enables V_{CC_SRAM} and V_{CC_APPS} to change to their programmed target values.

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8.6.2.20.3 I²C Data Exchange Between Master and Slave Device

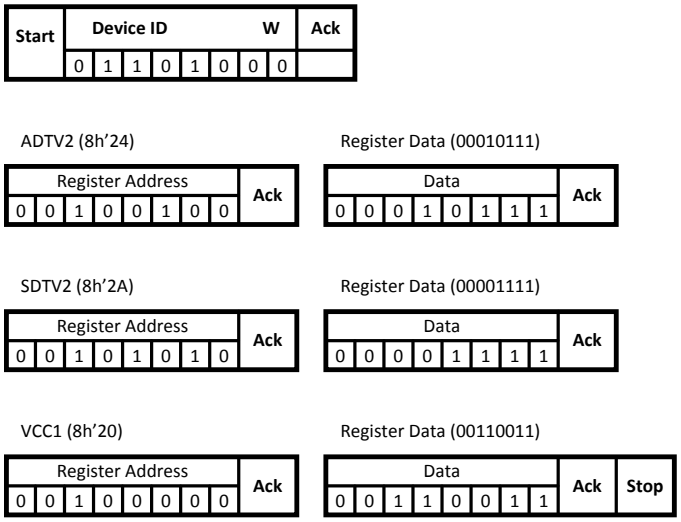

Figure 26. Master and Slave Data Exchange

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3972 is designed for powering systems that use advanced application processors. The device is specifically optimized for lower power handheld applications using Lithium-Ion main battery, DC chargers, and battery backup. The device is internally powered from the VIN and VDDA pins, and voltage must be in 2.7-V to 5.5-V range. The device has flexible configurability; output supply voltages and start-up delays for the buck converters and LDOs are configured via I^2C registers.

9.2 Typical Application

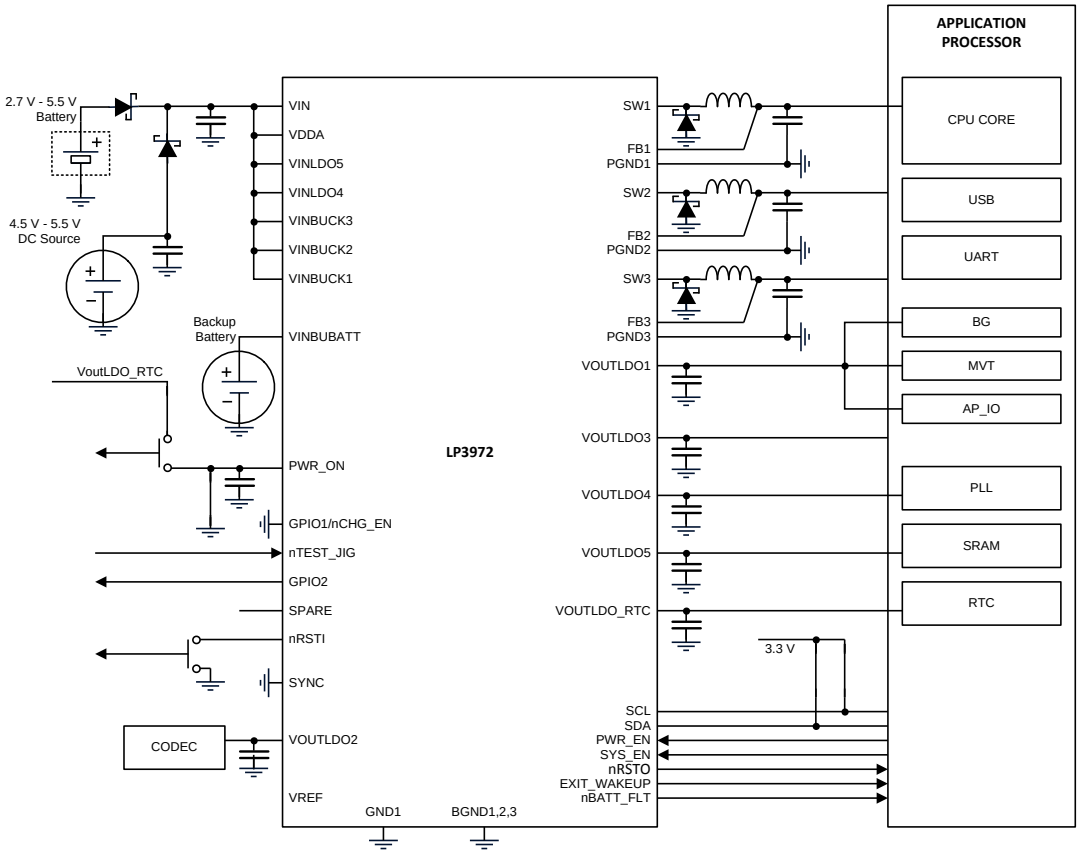

Figure 27. LP3972 Typical Application

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Typical Application (continued)

9.2.1 Design Requirements

For typical PMU advanced application processor applications, use the parameters listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7
Maximum input voltage	5.5
External SYNC clock used	No
LDO RTC output voltage	2.8 V
LDO1 output voltage	1.8 V
LDO2 output voltage	1.8 V
LDO3 output voltage	3 V
LDO4output voltage	3 V
LDO5 output voltage	1.4 V
BUCK1 output voltage	1.4 V
BUCK2 output voltage	3.3 V
BUCK3 output voltage	1.8 V
Low voltage designated rails	LDO5, BUCK1
High voltage designated rails	LDO1, LDO2, LDO3, LDO4, BUCK2, BUCK3

9.2.2 Detailed Design Procedure

9.2.2.1 LDO Considerations

9.2.2.1.1 External Capacitors

Regulators of the LP3972require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.1.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains approximately 1 µF over the entire operating temperature range.

9.2.2.1.3 Output Capacitor

The LDOs are designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit.

For this device the output capacitor must be connected between the V_{OUT} pin and ground.

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It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

9.2.2.1.4 No-Load Stability

The LDOs remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

9.2.2.1.5 Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type. In particular, the output capacitor selection must take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values may also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 28 shows a typical graph comparing different capacitor case sizes. As shown in Figure 28, increasing the DC bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

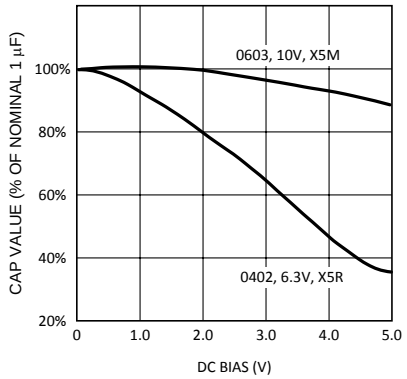

Figure 28. Typical Variation in Capacitance vs DC Bias

Capacitance of the ceramic capacitor can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, only varies the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

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9.2.2.2 Buck Considerations

9.2.2.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specificationss are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings at maximum ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

9.2.2.2.1.1 Method 1

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current (Equation 2):

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (2)$$

where

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current (1500 mA)
- V_{IN}: Maximum input voltage in application
- L: Minimum inductor value including worst case tolerances (30% drop can be considered for Method 1)
- f: Minimum switching frequency (1.6 MHz)
- V_{OUT}: Output voltage

9.2.2.2.1.2 Method 2

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit of 3 A.

A 2.2-µH inductor with a saturation current rating of at least 3 A is recommended for most applications. Resistance of the inductor must be less than 0.3 Ω for a good efficiency. Table 11 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

9.2.2.2.2 Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the VIN pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as in Equation 3:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$\text{where } r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}} \quad (3)$$

The worst case is when $V_{IN} = 2 \times V_{OUT}$.

Table 11. Suggested Inductors And Their Suppliers

MODEL	VENDOR	DIMENSIONS L × W × H (mm)	DCR (typical)
FDSE0312-2R2M	Toko	3 × 3 × 1.2	160 mΩ
DO1608C-222	Coilcraft	6.6 × 4.5 × 1.8	80 mΩ

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9.2.2.2.3 Output Capacitor Selection

Use a 10-µF, 6.3-V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 * f * C} \quad (4)$$

Voltage peak-to-peak ripple due to ESR can be expressed as in Equation 5:

$$V_{PP\text{-}ESR} = (2 \times I_{RIPPLE}) \times R_{ESR} \quad (5)$$

Because these two components are out of phase the RMS value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2} \quad (6)$$

Output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 12. Suggested Capacitor and Their Suppliers

MODEL	TYPE	VENDOR	VOLTAGE	CASE SIZE INCH (mm)
GRM21BR60J106K	Ceramic, X5R	Murata	6.3 V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3 V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3 V	0805 (2012)

9.2.2.2.4 Buck Output Ripple Management

If V_{IN} and I_{LOAD} increase, the output ripple associated with the buck regulators also increases. Figure 29 shows the safe operating area. To ensure operation in the area of concern, TI recommends that the system designer circumvents the output ripple issues to install Schottky diodes on the buck(s) that are expected to perform under these extreme corner conditions. Schottky diodes are recommended to reduce the output ripple, if system requirements include this shaded area of operation. V_{IN} > 1.5 V and I_{LOAD} > 1.24 A.

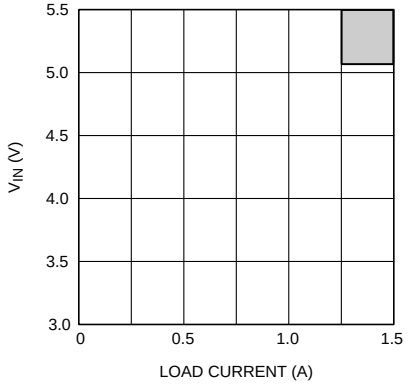
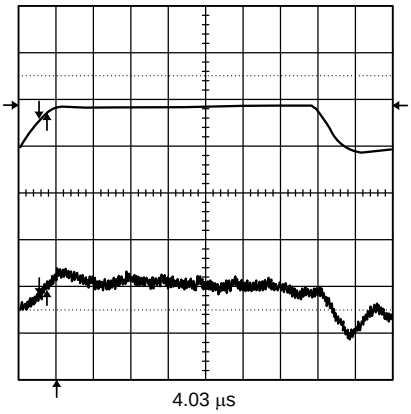


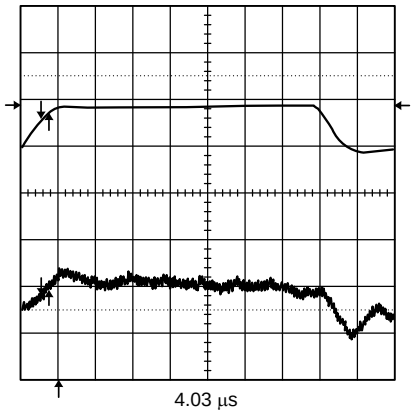
Figure 29. Application Conditions for Schottky Diodes

9.2.3 Application Curves



V_{IN} = 3 V to 3.6 V V_{OUT} = 1.2 V 250-mA Load

Figure 30. Line Transient Response



V_{IN} = 3.6 V V_{OUT} = 3.3 V 0 – 100 mA Load

Figure 31. Load Transient

10 Power Supply Recommendations

The LP3972 is designed to operate from a single-cell lithium-ion battery and a coin-cell backup battery. V_{IN} input must be between 2.7 V and 5.5 V. The RTC LDO input automatically switches between main and backup batteries at V_{IN} > 3 V, and device operational range is V_{IN} between 3.3 V and 5.5 V. Decoupling capacitance at VIN pin can be shared for all LDO and Buck inputs. It must be placed as close to device as possible.

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11 Layout

11.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability.

Good layout for the converters can be implemented by following a few simple design rules.

1. Place the converters, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the VIN and GND pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the converter and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the converter by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the converter and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the converter by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the converter circuit and must be direct but must be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. Place noise sensitive circuitry, such as radio RF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

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11.2 Layout Example

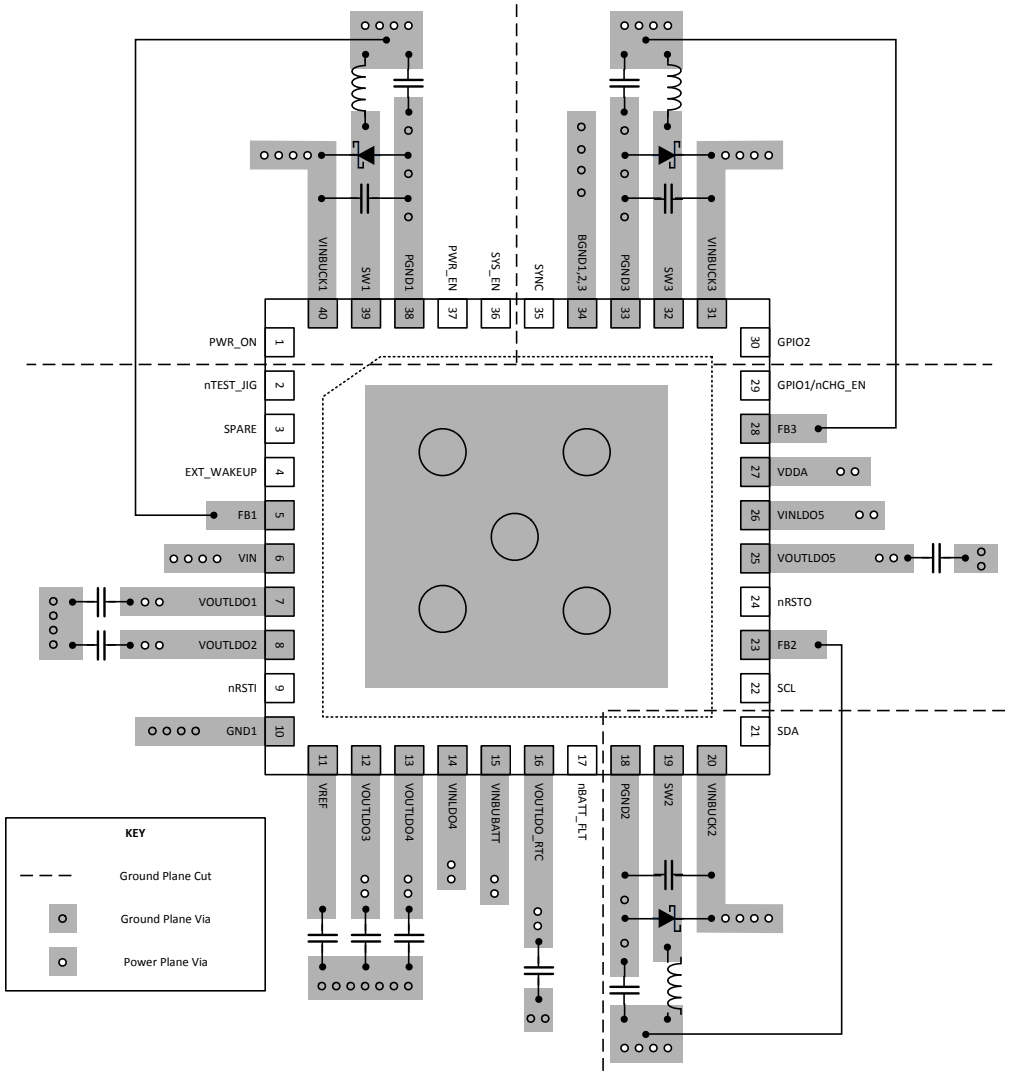

Figure 32. LP3972 Layout

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12 Device and Documentation Support

12.1 Device Support

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12.2 Related Documentation

For additional information, see the following:

TI Application Note *Leadless Leadframe Package (LLP)* (SNOA401)

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The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3972SQ-0514/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	72-0514
LP3972SQ-0514/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-0514
LP3972SQ-5810/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	72-5810
LP3972SQ-5810/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-5810
LP3972SQ-A413/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-A413
LP3972SQ-A413/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-A413
LP3972SQ-A514/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-A514
LP3972SQ-A514/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-A514
LP3972SQ-E514/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-E514
LP3972SQ-E514/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-E514
LP3972SQ-I414/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-I414
LP3972SQ-I414/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-I414
LP3972SQ-I514/NOPB	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-I514
LP3972SQ-I514/NOPB.A	NRND	Production	WQFN (RSB) | 40	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	72-I514

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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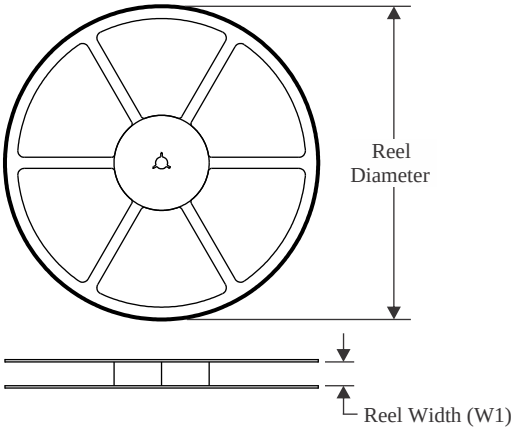
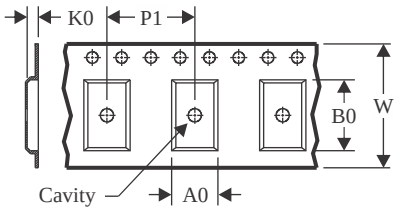
TAPE AND REEL INFORMATION

REEL DIMENSIONS

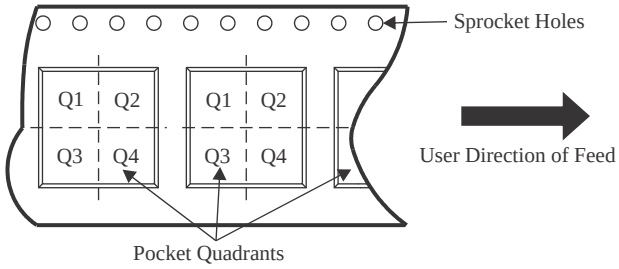


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

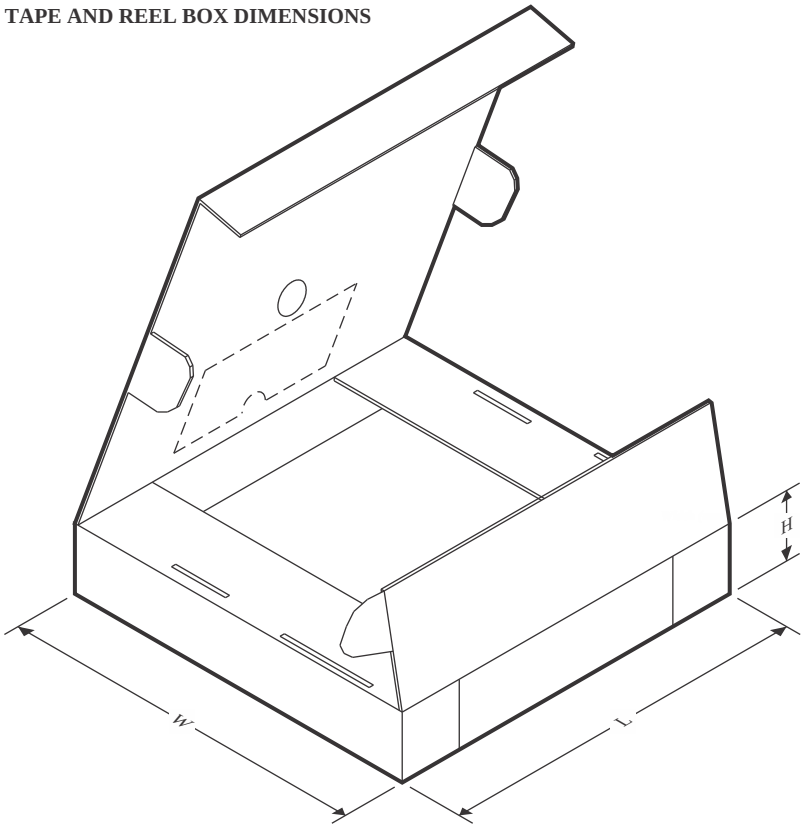
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3972SQ-0514/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-5810/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-A413/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-A514/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-E514/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-I414/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP3972SQ-I514/NOPB	WQFN	RSB	40	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

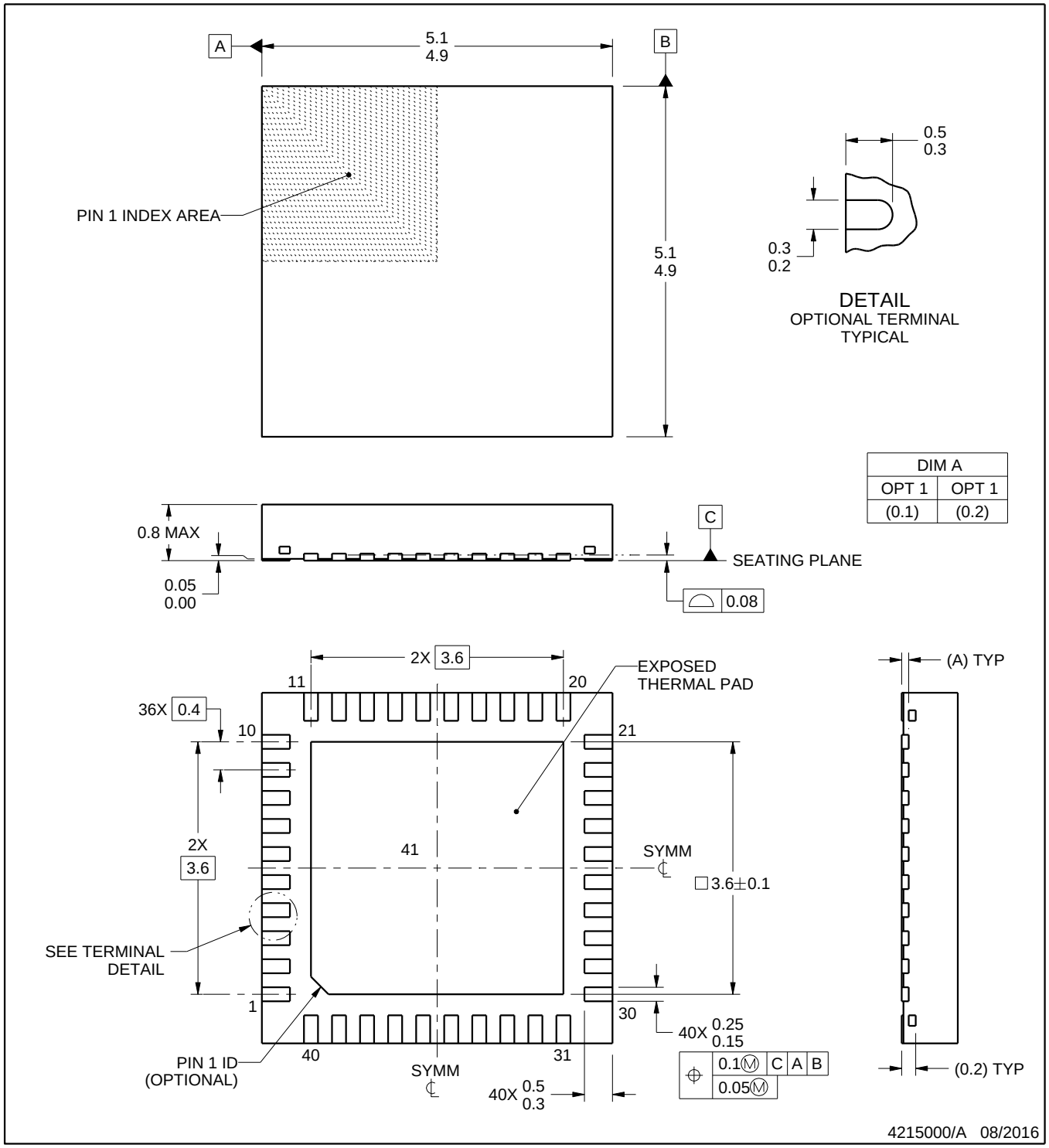
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3972SQ-0514/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-5810/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-A413/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-A514/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-E514/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-I414/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LP3972SQ-I514/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0

PACKAGE OUTLINE

RSB0040A

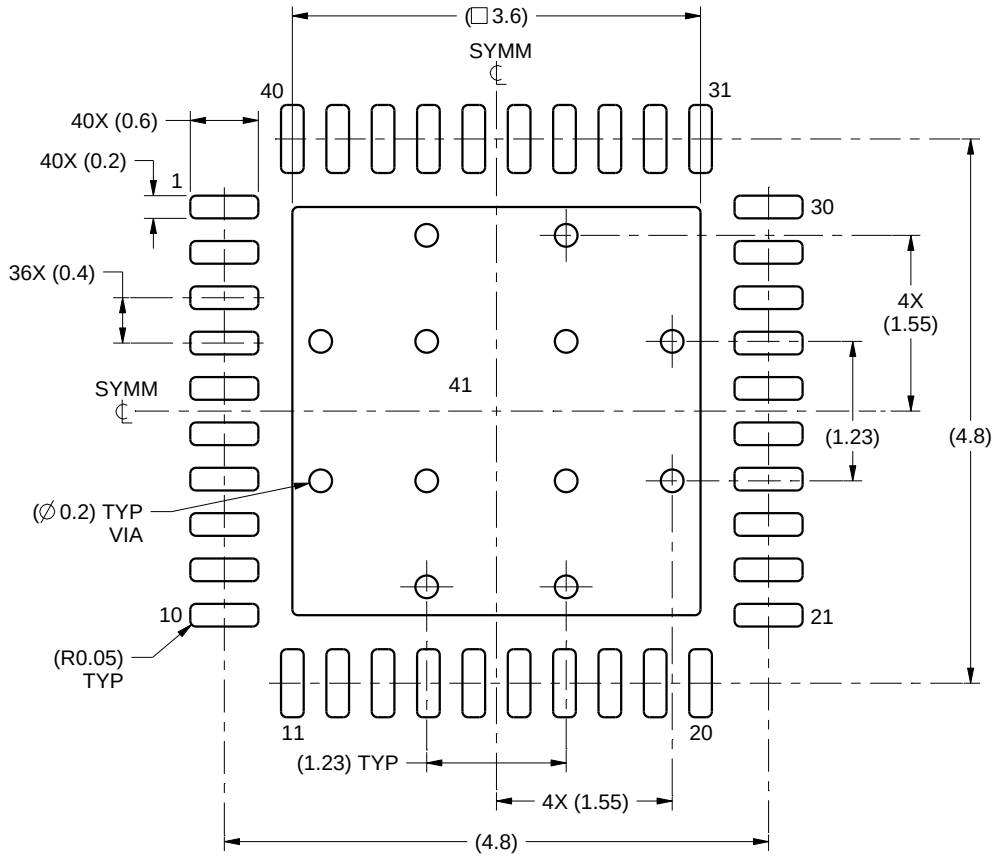
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



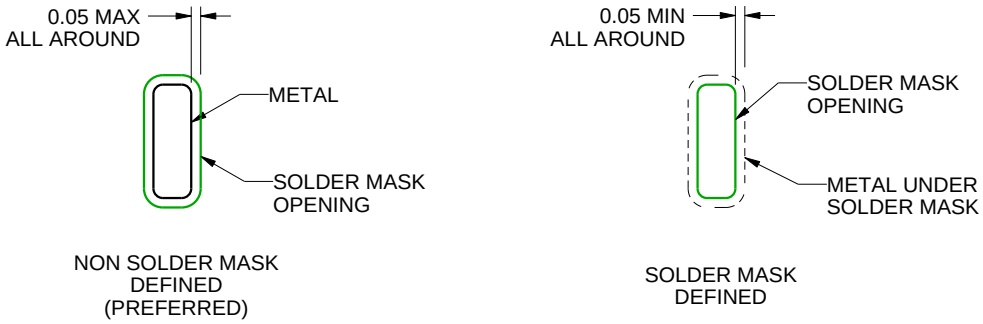
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE:15X

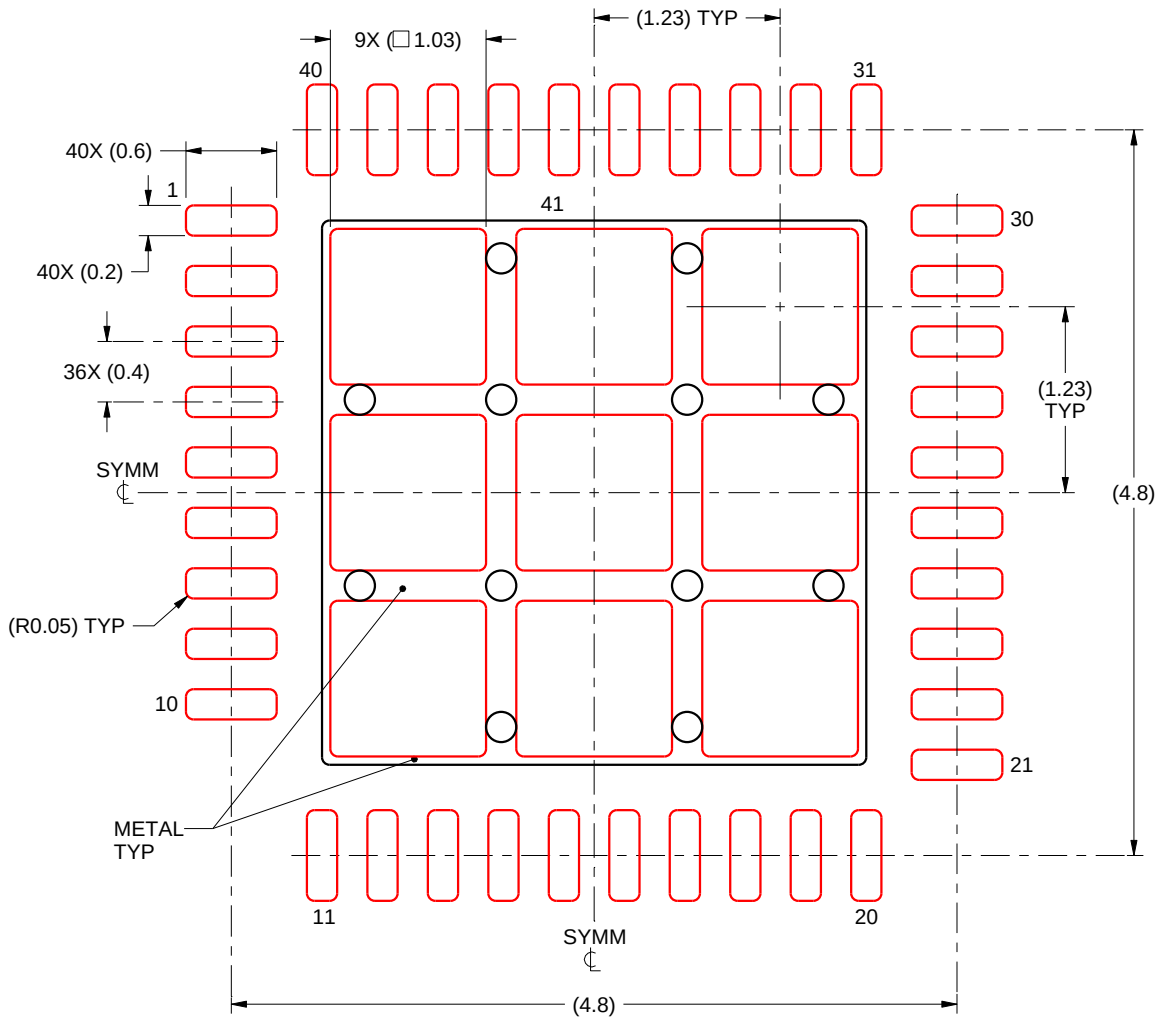


SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

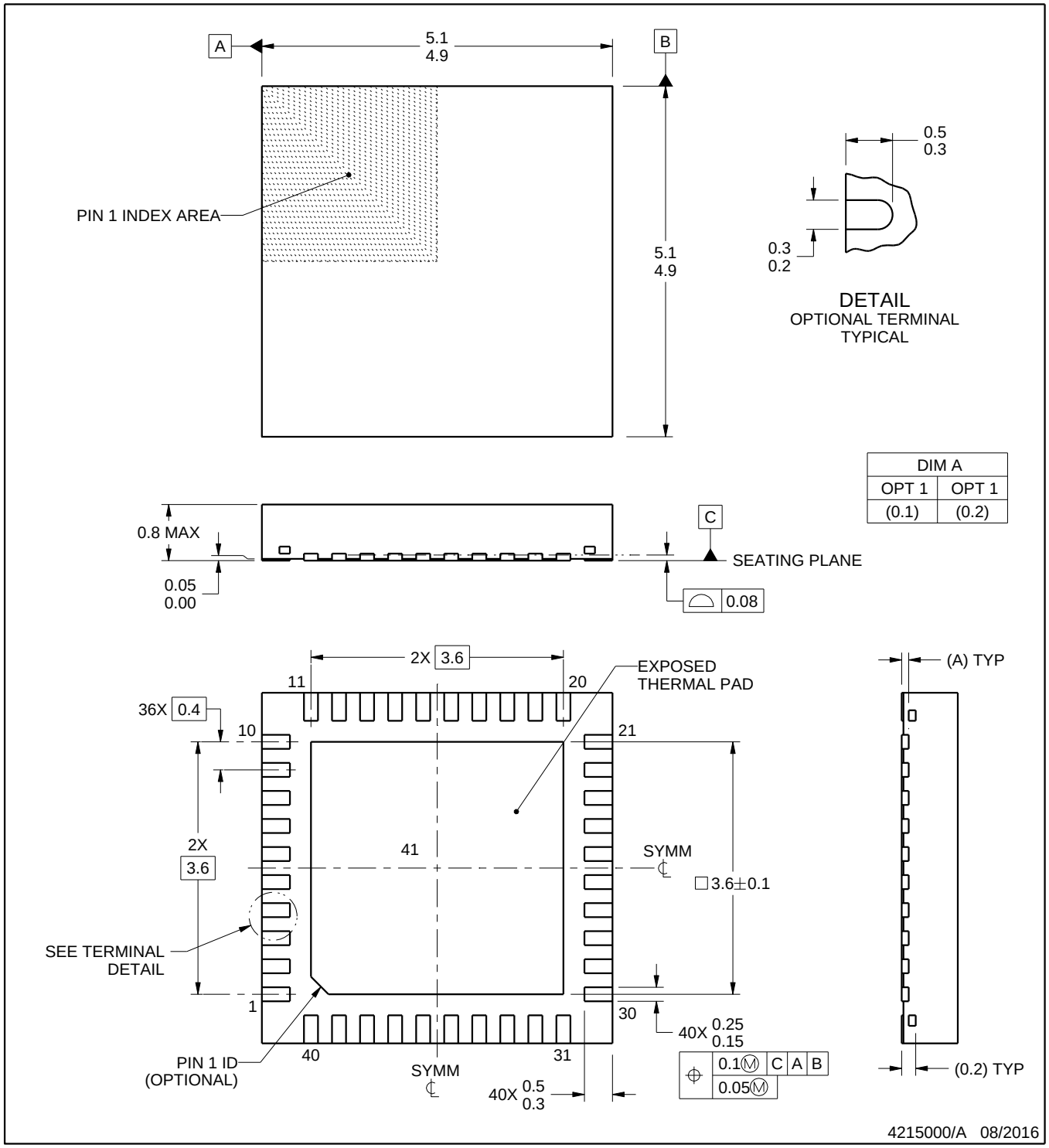
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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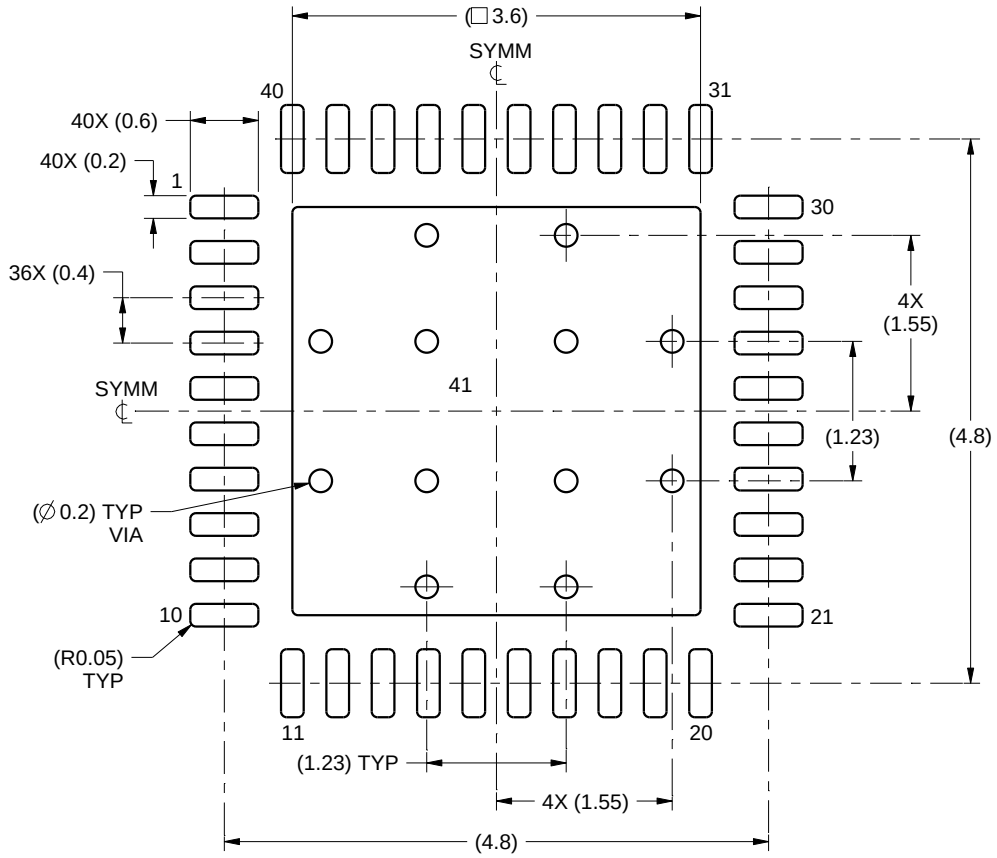
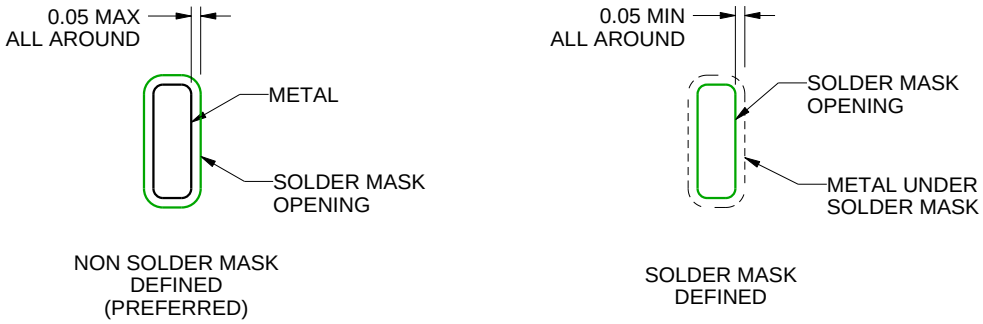
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE:15X



SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

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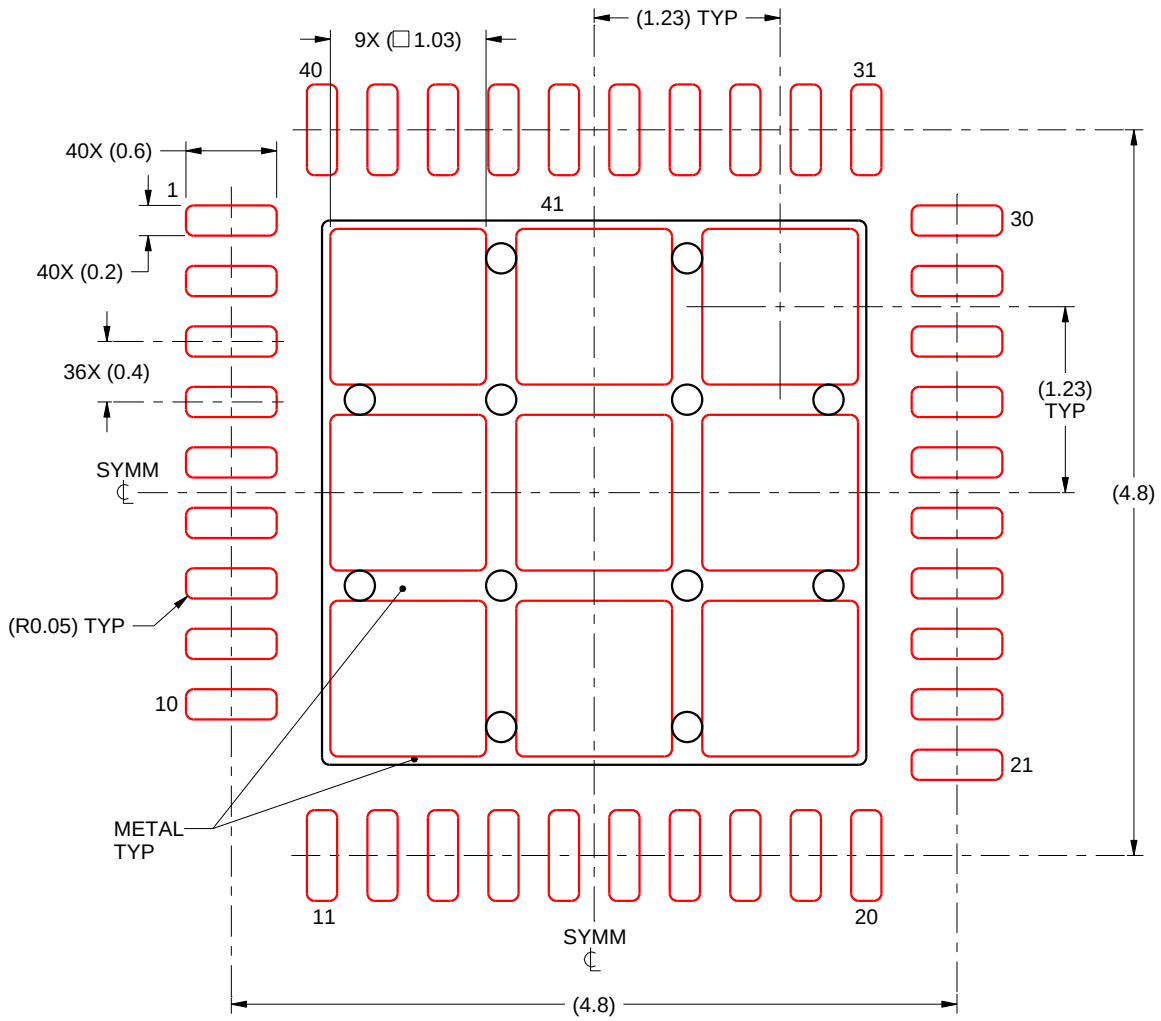
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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